Preliminary Data Sheet

VSC8132

2.488Gb/s 1:32 SONET/SDH Demux

Features

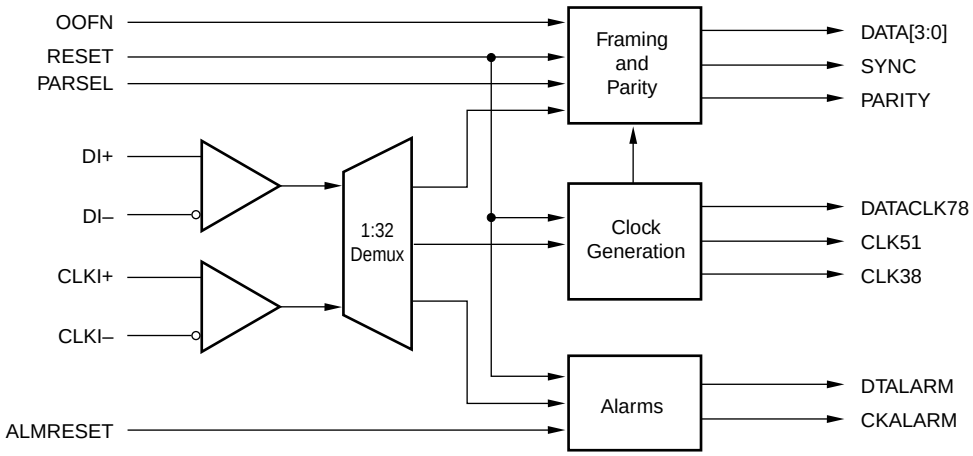
- 2.488Gb/s 1:32 Demultiplexer
- SONET STS-48/SDH STM-16
- HSPECL Differential Serial Data and Clock Inputs
- 32-Bit TTL Parallel Data Outputs with Odd/ Even Parity Check
- Frame Detect Synchronization
- 77.76, 51.84, and 38.88MHz TTL Clock Outputs
- Single 3.3V supply
- Loss of Clock Alarm
- Loss of Data Alarm
- 2.05W Max Power Dissipation
- 128-Pin PQFP Package

General Description

The VSC8132 demultiplexes a 2.488Gb/s HSPECL serial input datastream (DI±) to 32-bit wide, TTL 77.76Mb/s parallel data outputs D[31:0] for SONET/SDH applications. A 2.488GHz HSPECL input clock (CLKI±) is used to time the incoming data and 3 TTL clock outputs, at frequencies of 77.76MHz, 51.84MHz, and 38.88MHz, are generated for upstream devices (DATACLK78, CLK51, CLK38). Odd or even parity is performed on the incoming high-speed data via the TTL Parity Select input (PARSEL), and a TTL Parity output (PARITY) is provided to indicate parity of the input data. Frame Detect on the incoming data is controlled via the Frame Detect Inhibit (OOFN) and Reset (RESET) TTL inputs. A frame detect monitors the incoming data steam and screens for 2 bits in A1 byte out of the 8 bits and 2 bits of A2 byte out of the 8 bits. When a Frame Detect occurs, a synchronization TTL output (SYNC) will be set. Alarm indicators are used to monitor the activity of the clock and data with TTL compatible control inputs (ALMRESET) and outputs (DTALARM, CKALARM).

Only a single 3.3V power supply is required for device operation. The VSC8132 is packaged in a thermally-enhanced 128-pin, 14x20x2mm PQFP package.

VSC8132 Block Diagram



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Functional Description

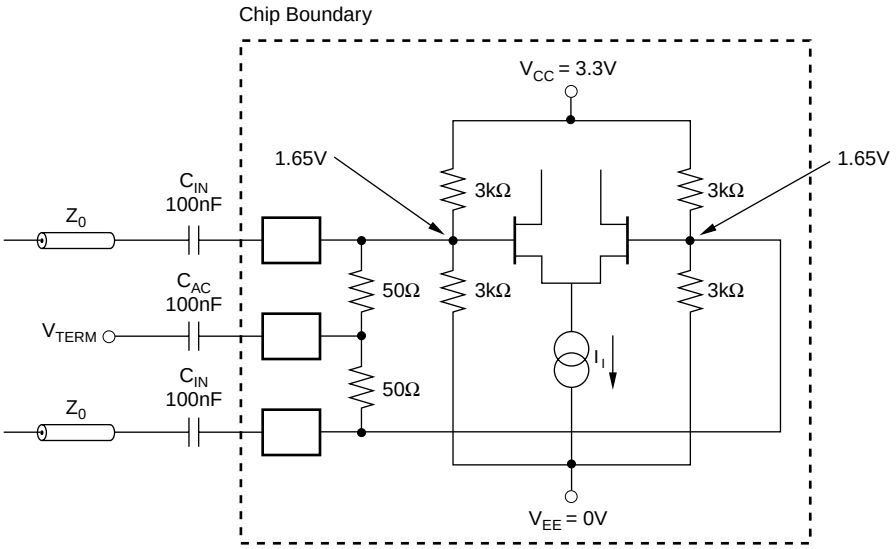
High-Speed Clock and Data Interface

The incoming high-speed data and high-speed clock are received by high-speed inputs DI± and CLKI±. The inputs are internally biased to accommodate AC-coupling.

The data and clock inputs are internally terminated by a center-tapped resistor network. For differential input DC-coupling, the network is terminated to the appropriate termination voltage, V_{TERM} providing a 50Ω to V_{TERM} termination for both true and complement inputs. For differential input AC-coupling, the network is terminated to V_{TERM} via a blocking capacitor.

In most situations, these inputs will have high transition density and little DC offset. However, in cases where this does not hold, direct DC connection is possible. All serial data and clock inputs have the same circuit topology as shown in Figure 1. The reference voltage is created by a resistor divider as shown. If the input signal is driven differentially and DC-coupled to the part, the mid-point of the input signal swing should be centered about this reference voltage and not exceed the maximum allowable amplitude. For single-ended, DC-coupling operations, it is recommended that the user provides an external reference voltage which has better temperature and power supply noise rejection than the on-chip resistor divider. The external reference should have a nominal value equivalent to the common mode switch point of the DC-coupled signal, and can be connected to either side of the differential gate.

Figure 1: High-Speed Clock and Data Inputs



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Low-Speed Data Interface

The 77.76Mb/s parallel data outputs D[31:0] are clocked out of the VSC8132 on the falling clock edge of the 77.76MHz output clock (DATA78CLK). The data and clock are TTL levels. The MSB (D31) bit is the first bit into the serial interface.

Parity Selection

The parity output bit (PARITY) is clocked out on the falling edge of the 77.76MHz clock (DATA78CLK). This bit indicates the parity of the 32 bits of data along with the frame sync bit. The parity of the output is determined by the parity select input (PARSEL). When the parity select input is LOW, the output parity is odd. When the parity select is HIGH, the output parity is even. The parity inputs and outputs are TTL levels. See Figure 2 for output timing relationship.

Framing Logic Interface

When a frame detect occurs and the frame detect inhibit input (OOFN) is set LOW, the frame detect output (SYNC) is set HIGH on the negative edge of the 77.76MHz clock and on the 3rd set of four A2 bytes at the 32-bit data output. The frame detect mechanism is inhibited when the frame detect inhibit (OOFN) input is set HIGH. The frame detect output and frame detect inhibit are TTL levels.

NOTE: The 77.76MHz clock misses one clock cycle during a frame detect. This missed cycle occurs one clock period before the Sync pulse is set HIGH (see Figure 4).

To use as a framer:

Step 1: Set OOFN LOW

Step 2:Wait for Sync pulse

Step 3:When Sync Pulse goes HIGH, set OOFN HIGH

Chip Reset

Chip reset (RESET) will reset the framing logic so that no frame detection barrel shifting is performed. Therefore, if the frame detect inhibit input is set high, the chip will act as a simple demux after reset. The reset should be set high for 16 clock cycles of the high speed clock input. The chip reset is a TTL level.

Alarm Logic Interface

The Loss of Clock (CKALARM) and Loss of Data (DTALARM) alarms monitor the activity of the clock and data. The Alarm Reset (ALMRESET) input controls the alarm activity. Polling of the alarms signals are initiated by toggling the Alarm Reset input HIGH and then LOW one time. To reset both alarm outputs, the Alarm Reset should be toggled HIGH to LOW two times. All alarm logic interface signals are TTL levels.

Supplies

The VSC8132 is specified as a HSPECL/TTL device with a single positive 3.3V supply. Normal operation is to have V_{CC} = +3.3V and V_{EE} = ground. Should the user desire to use the device in a ECL environment with a negative 3.3V supply, V_{CC} will be ground and V_{EE} will be -3.3V. If used with V_{EE} tied to -3.3V, the TTL output signals are still referenced to V_{EE}.

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Decoupling of the power supplies is a critical element in maintaining the proper operation of the part. It is recommended that the V_{CC} power supply be decoupled using a 0.1µF and 0.01µF capacitor placed in parallel on each V_{CC} power supply pin as close to the package as possible. If room permits, a 0.001µF capacitor should also be placed in parallel with the 0.1µF and 0.01µF capacitors mentioned above. Recommended capacitors are low-inductance ceramic SMT X7R devices. For the 0.1µF capacitor, a 0603 package should be used. The 0.01µF and 0.001µF capacitors can be either 0603 or 0402 packages.

For low frequency decoupling, 47µF tantalum, low-inductance SMT caps should be sprinkled over the board's main +3.3V power supply and placed close to the C-L-C pi filter.

If the device is being used in an ECL environment with a -3.3V supply, all references to decoupling V_{CC} must be changed to V_{EE}, and all references to decoupling 3.3V must be changed to -3.3V.

AC Characteristics

Figure 2: Output Timing

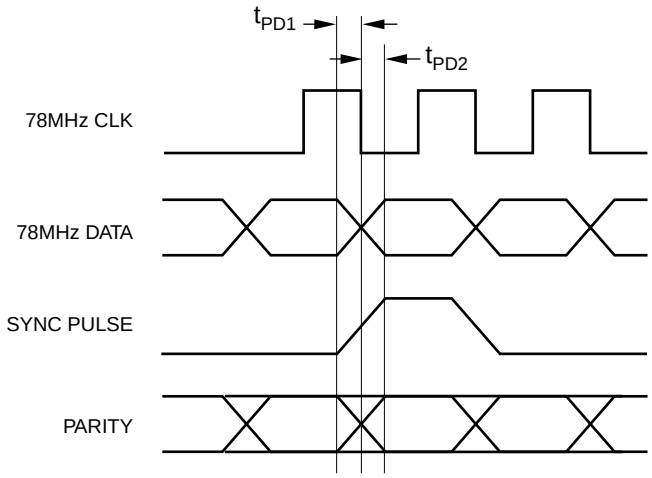
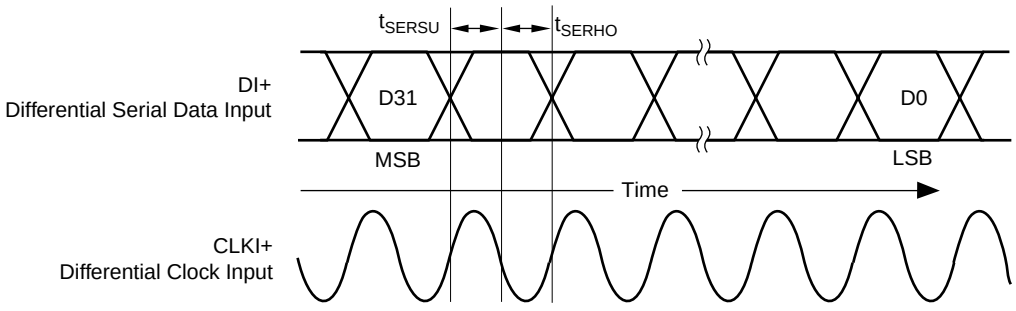


Figure 3: Data Output Timing



NOTE: Bit 31 (MSB) is received first, Bit 0 (LSB) is received last.

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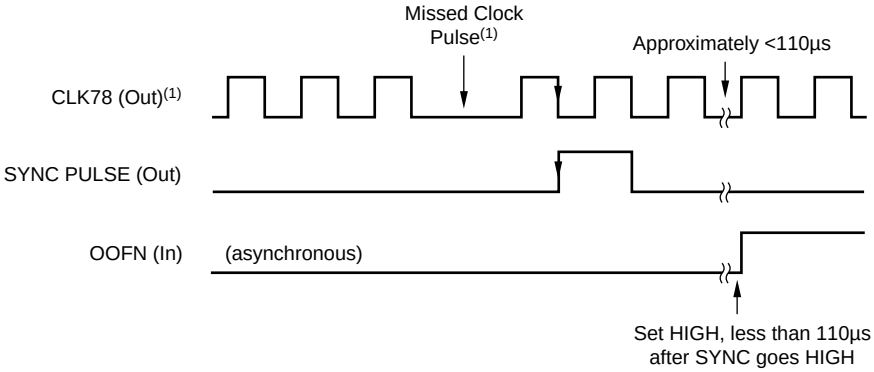
Figure 4: Framing Sequence



NOTE: (1) No missing clock pulse for CLK78 when VSC8132 is working as a dumb demux.

Once frame occurs and OOFN is set HIGH, the no framing will occur until OOFN is set LOW again. The VSC8132 will remain framed with SONET frame.

Table 1: AC Characteristics

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
t_{DATApd}	Data Valid From Falling Edge of 77.76MHz	230		1250	ps	External load = 5pf
t_{CLKRpd}	High-speed Clock Rising Edge to 77.76MHz Clock Rising Edge	2.5		8.0	ns	External load = 5pf
t_{CLKFpd}	High-Speed Clock Rising Edge to 77.76MHz Clock Falling Edge	2.3		7.1	ns	External load = 5pf
t_{DEDGE}	D[0:31] Edge Rate (10%-90%)	-		2.0	ns	External load = 5pf
$t_{CLKEDGE}$	77.76, 51.84, 38.88MHz Edge Rates (10%-90%)	-		2.0	ns	External load = 5pf
$t_{CONEDGE}$	Control Signals (SYNC, PARITY, DTALARM, and CKALARM) Edge Rate (10%-90%)	-		2.0	ns	External load = 5pf
t_{SERSU}	DI+ Setup Time with Respect to Falling Edge of CLKI+	100		-	ps	See Figure 3
t_{SERHO}	DI+ Hold Time with Respect to Falling Edge of CLKI+	75		-	ps	See Figure 3
f_{MAX}	Demux Input Maximum Clock Frequency	-		2.9	GHz	
$t_{CLK38Rpd}$	High-Speed Clock Rising Edge to 38.88MHz Clock Rising Edge.	2.0		6.3	ns	External load = 5pf
$t_{CLK38Fpd}$	High-Speed Clock Rising Edge to 38.88MHz Clock Falling Edge	2.0		5.9	ns	External load = 5pf
$t_{CLK51Rpd}$	High-Speed Clock Rising Edge to 51.84MHz Clock Rising Edge	2.0		6.0	ns	External load = 5pf
$t_{CLK51Fpd}$	High-Speed Clock Rising Edge to 51.84MHz Clock Falling Edge	2.0		5.9	ns	External load = 5pf
t_{PD1}, t_{PD2}	Data Invalid Window	0, 230		0, 1250	ps	

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DC Characteristics

Table 2: DC Characteristics (Over recommended operating conditions)

Parameters	*Description*	*Min*	*Typ*	*Max*	*Units*	*Conditions*
V_{OHttl}	Output HIGH Voltage (TTL)	2.4	—	—	V	I_{OH} = -1.0mA
V_{OLttl}	Output LOW Voltage (TTL)	—	—	0.5	V	I_{OL} = +1.0mA
V_{IHttl}	Input HIGH Voltage (TTL)	2.0	—	—	V	I_{IH} = 300µA
V_{ILttl}	Input LOW Voltage (TTL)	—	—	0.8	V	I_{IL} = -50µA
V_{OHpecl}	Output HIGH Voltage (HSPECL)	V_{CC}-1.02	—	V_{CC}-0.7	V	Output tied to 50Ω to V_{CC}-2.0V
V_{OLpecl}	Output LOW Voltage (HSPECL)	V_{CC}-2.0	—	V_{CC}-1.62	V	Output tied to 50Ω to V_{CC}-2.0V
$\Delta V_{DIFF(CLKI)}$	Demux Clock Input Absolute Voltage Differential Peak-to-Peak Swing (CLKI±)	400	—	1200	mV	AC-coupled, internally biased to $V_{CC}/2$
$\Delta V_{DIFF(DI)}$	Demux Serial Input Absolute Voltage Differential Peak-to-Peak Swing (DI±)	400	—	1200	mV	AC-coupled, internally biased to $V_{CC}/2$
V_{CC}	Supply Voltage	3.14	—	3.47	V	3.3V± ±5%
P_D	Power Dissipation	—	1.6	2.05	W	Outputs open, V_{CC} = V_{CC} max
I_{DD}	Supply Current	—	489	591	mA	Outputs open, V_{CC} = V_{CC} max

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{CC}) ..... -0.5V to +3.8V
DC Input Voltage (differential inputs) ..... -0.5V to V_{CC} +0.5V
Output Current (differential outputs) ..... ±50mA
Case Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Maximum Input ESD (Human Body Model) 1500V

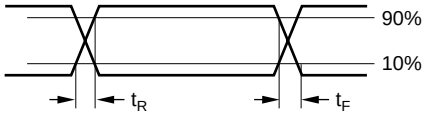
NOTE: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Recommended Operating Conditions

Power Supply Voltage (V_{CC}) ..... +3.3V±5%
Operating Temperature Range ..... 0°C Ambient to +85°C Case Temperature

Figure 5: Parametric Measurement Information

TTL Rise and Fall Time



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Package Pin Descriptions

Figure 6: Pin Diagram

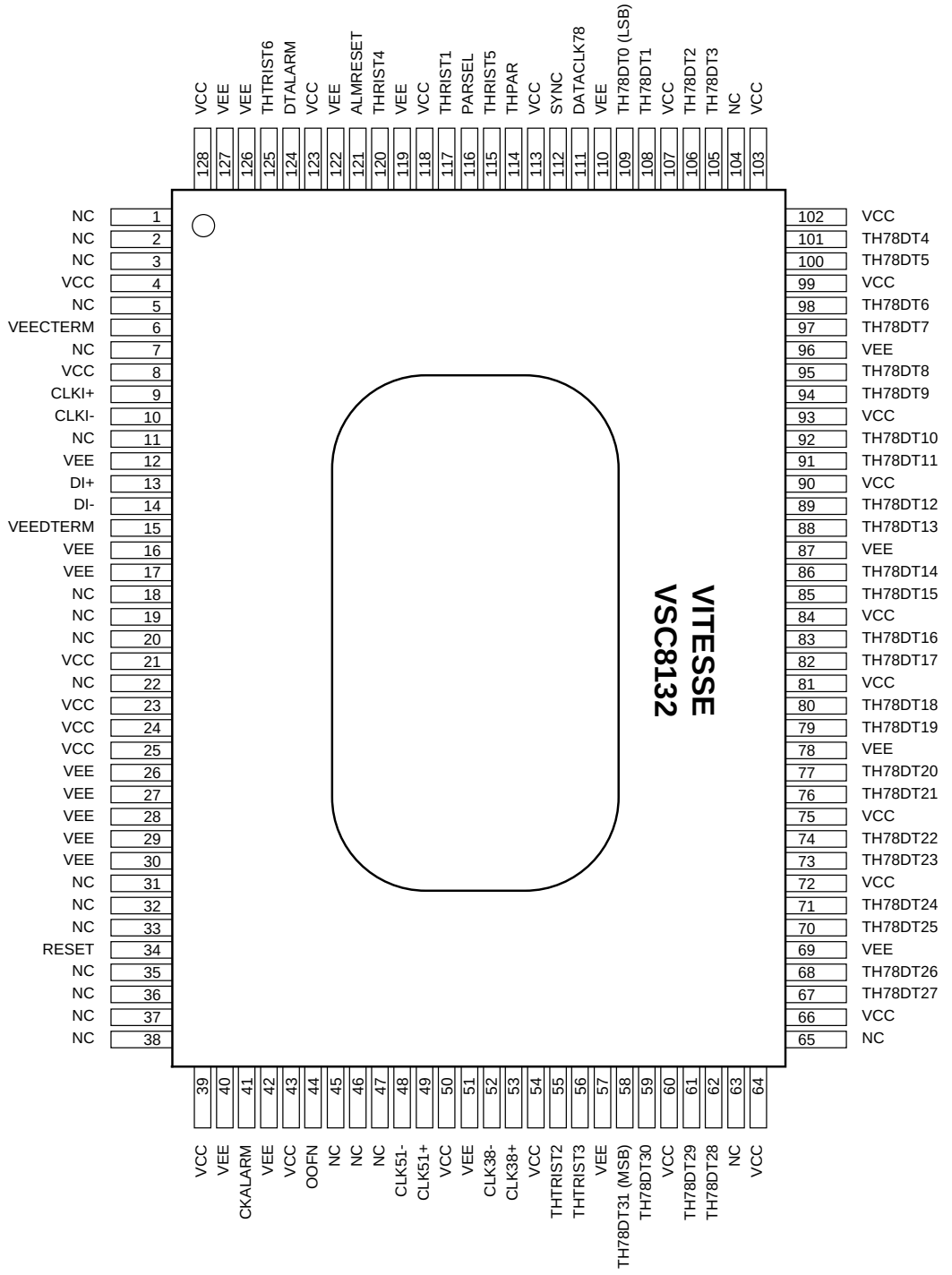

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Table 3: Pin Identifications

Pin	*Name*	*I/O*	*Level*	*Description*
1	NC	-	-	No Connect, Leave Unconnected
2	NC	-	-	No Connect, Leave Unconnected
3	NC	-	-	No Connect, Leave Unconnected
4	VCC	-	+3.3V	Power Supply
5	NC	-	-	No Connect, Leave Unconnected
6	VEECTERM	-	GND	50Ω Termination Ground for CLK±
7	NC	-	-	No Connect, Leave Unconnected
8	VCC	-	+3.3V	Power Supply
9	CLKI+	I	HSPECL	High-Speed Clock Input, True
10	CLKI-	I	HSPECL	High-Speed clock Input, Complement
11	NC	-	-	No Connect, Leave Unconnected
12	VEE	-	0V	Ground
13	DI+	I	HSPECL	High-Speed Serial Data Input, True. PECL levels, AC-coupled, internally biased to $V_{CC}/2$.
14	DI-	I	HSPECL	High-Speed Serial Data Input, Complement. PECL levels, AC-coupled, internally biased to $V_{CC}/2$.
15	VEEDTERM	-	GND	50Ω Termination Ground for DI±
16	VEE	-	0V	Ground
17	VEE	-	0V	Ground
18	NC	-	-	No Connect, Leave Unconnected
19	NC	-	-	No Connect, Leave Unconnected
20	NC	-	-	No Connect, Leave Unconnected
21	VCC	-	+3.3V	Power Supply
22	NC	-	-	No Connect, Leave Unconnected
23	VCC	-	+3.3V	Power Supply
24	VCC	-	+3.3V	Power Supply
25	VCC	-	+3.3V	Power Supply
26	VEE	-	0V	Ground
27	VEE	-	0V	Ground
28	VEE	-	0V	Ground
29	VEE	-	0V	Ground
30	VEE	-	0V	Ground
31	NC	-	-	No Connect, Leave Unconnected
32	NC	-	-	No Connect, Leave Unconnected
33	NC	-	-	No Connect, Leave Unconnected
34	RESET	I/O	TTL	Resets Framing Logic and Output Clocks

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Pin	*Name*	*I/O*	*Level*	*Description*
35	NC	-	-	No Connect, Leave Unconnected
36	NC	-	-	No Connect, Leave Unconnected
37	NC	-	-	No Connect, Leave Unconnected
38	NC	-	-	No Connect, Leave Unconnected
39	VCC	-	+3.3V	Power Supply
40	VEE	-	0V	Ground
41	CKALARM	O	TTL	Loss of clock output. Stays HIGH when loss of clock is detected.
42	VEE	-	0V	Ground
43	VCC	-	+3.3V	Power Supply
44	OOFN	I	TTL	Frame Detect Disable Input. Disables frame detection if set HIGH.
45	NC	-	-	No Connect, Leave Unconnected
46	NC	-	-	No Connect, Leave Unconnected
47	NC	-	-	NNo Connect, Leave Unconnected
48	CLK51-	O	HSPECL	Low-Speed Clock Output (51.84MHz), Complement
49	CLK51+	O	HSPECL	Low-Speed Clock Output (51.84MHz), True
50	VCC	-	+3.3V	Power Supply
51	VEE	-	0V	Ground
52	CLK38-	O	HSPECL	Low-Speed Clock Output (38.88MHz), Complement
53	CLK38+	O	HSPECL	Low speed Clock Output (38.88MHz), True
54	VCC	-	+3.3V	Power Supply
55	THTRIST2	I	TTL	Tri-State Inputs. Allows tri-stating of all output signals. Used for test only. Should be tied to V_{EE} during normal operation.
56	THTRIST3	I	TTL	Tri-State Inputs. Allows tri-stating of all output signals. Used for test only. Should be tied to V_{EE} during normal operation.
57	VEE	-	0V	Ground
58	TH78DT31	O	TTL	Low-Speed Parallel Data (MSB)
59	TH78DT30	O	TTL	Low-Speed Parallel Data
60	VCC	-	+3.3V	Power Supply
61	TH78DT29	O	TTL	Low-Speed Parallel dData
62	TH78DT28	O	TTL	Low-Speed Parallel Data
63	NC	-	-	No connect, leave unconnected
64	VCC	-	+3.3V	Power Supply
65	NC	-	-	No Connect, Leave Unconnected
66	VCC	-	+3.3V	Power Supply
67	TH78DT27	O	TTL	Low-Speed Parallel Data
68	TH78DT26	O	TTL	Low-Speed Parallel Data

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Pin	Name	I/O	Level	Description
69	VEE	-	0V	Ground
70	TH78DT25	O	TTL	Low-Speed Parallel Data
71	TH78DT24	O	TTL	Low-Speed parallel Data
72	VCC	-	+3.3V	Power Supply
73	TH78DT23	O	TTL	Low-Speed Parallel Data
74	TH78DT22	O	TTL	Low-Speed Parallel Data
75	VCC	-	+3.3V	Power Supply
76	TH78DT21	O	TTL	Low-Speed Parallel Data
77	TH78DT20	O	TTL	Low-Speed Parallel Data
78	VEE	-	0V	Ground
79	TH78DT19	O	TTL	Low-Speed Parallel Data
80	TH78DT18	O	TTL	Low-Speed Parallel Data
81	VCC	-	+3.3V	Power Supply
82	TH78DT17	O	TTL	Low-Speed Parallel Data
83	TH78DT16	O	TTL	Low-Speed Parallel Data
84	VCC	-	+3.3V	Power Supply
85	TH78DT15	O	TTL	Low-Speed Parallel Data
86	TH78DT14	O	TTL	Low-Speed Parallel Data
87	VEE	-	0V	Ground
88	TH78DT13	O	TTL	Low-Speed Parallel Data
89	TH78DT12	O	TTL	Low-Speed Parallel Data
90	VCC	-	+3.3V	Power Supply
91	TH78DT11	O	TTL	Low-Speed Parallel Data
92	TH78DT10	O	TTL	Low-Speed Parallel Data
93	VCC	-	+3.3V	Power Supply
94	TH78DT9	O	TTL	Low-Speed Parallel Data
95	TH78DT8	O	TTL	Low-Speed Parallel Data
96	VEE	-	0V	Ground
97	TH78DT7	O	TTL	Low-Speed Parallel Data
98	TH78DT6	O	TTL	Low-Speed Parallel Data
99	VCC	-	+3.3V	Power Supply
100	TH78DT5	O	TTL	Low-Speed Parallel Data
101	TH78DT4	O	TTL	Low-Speed Parallel Data
102	VCC	-	+3.3V	Power Supply
103	VCC	-	+3.3V	Power Supply
104	NC	-	-	No Connect, Leave Unconnected

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Pin	Name	I/O	Level	Description
105	TH78DT3	O	TTL	Low-Speed Parallel Data
106	TH78DT2	O	TTL	Low-Speed Parallel Data
107	VCC	-	+3.3V	Power Supply
108	TH78DT1	O	TTL	Low-Speed Parallel Data
109	TH78DT0	O	TTL	Low-Speed Parallel Data (LSB)
110	VEE	-	0V	Ground
111	DATACLK78	O	TTL	Low-Speed Clock Output (77.76MHz). A divide-by-32 version of the CLKI± input clock.
112	SYNC	O	TTL	Frame Detect Output. Set HIGH when frame detect occurs.
113	VCC	-	+3.3V	Power Supply
114	THPAR	O	TTL	Parity Output
115	THTRIST5	I	TTL	Tri-State Inputs. Allows tri-stating of all output signals. Used for test only. Should be tied to V_{EE} during normal operation.
116	PARSEL	I	TTL	Parity Select Input. HIGH for even; LOW for odd.
117	THTRIST1	I	TTL	Tri-State Inputs. Allow tri-stating of all output signals. Used for test only. Should be tied to V_{EE} during normal operation.
118	VCC	-	+3.3V	Power Supply
119	VEE	-	0V	Ground
120	THTRIST4	I	TTL	Tri-State Inputs. Allow tri-stating of all output signals. Used for test only. Should be tied to V_{EE} during normal operation.
121	ALMRESET	I	TTL	Alarm Reset. Resets and clocks out Loss of Clock and Loss of Data alarms.
122	VEE	-	0V	Ground
123	VCC	-	+3.3V	Power Supply
124	DTALARM	O	TTL	Loss of Data Output. Stays HIGH when loss of data is detected.
125	THTRIST6	I	TTL	Tri-state Inputs. Allow tri-stating of all output signals. Used for test only. Should be tied to V_{EE} during normal operation.
126	VEE	-	0V	Ground
127	VEE	-	0V	Ground
128	VCC	-	+3.3V	Power Supply

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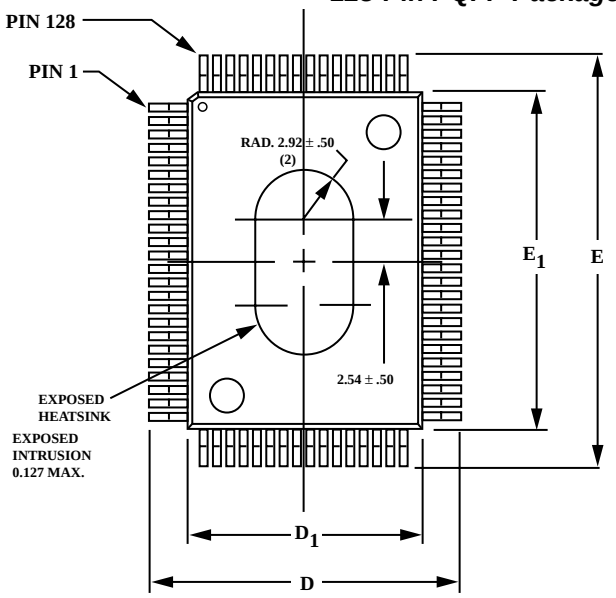
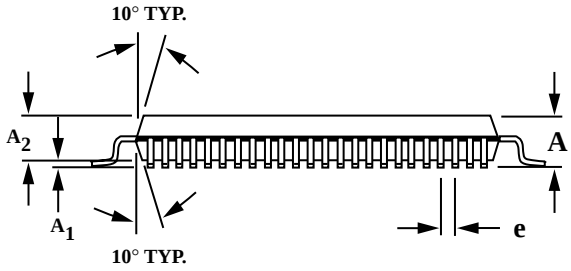
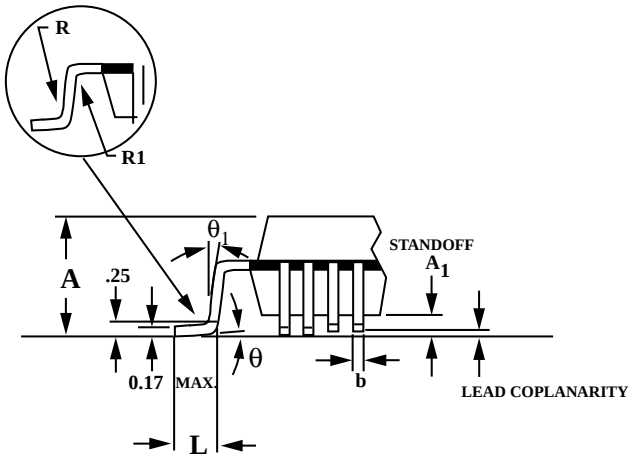
Package Information

128-Pin PQFP Package Drawing



Key	*mm*	*Tolerance*
A	2.35	MAX
A1	0.25	MAX
A2	2.00	+.10
D	17.20	±.20
D1	14.00	±.10
E	23.20	±.20
E1	20.00	±.10
L	.88	+.15/-.10
e	.50	BASIC
b	.22	±.05
θ	0°-7°	
R	.30	TYP
R1	.20	TYP





Notes: 1) Drawing is not to scale
2) All dimensions in mm
3) Package represented is also used for the 64, 80, & 100 PQFP packages. Pin count drawn does not reflect the 128 Package.

Package #: 101-267-7
Issue #: 1

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Package Thermal Considerations

The VSC8132 has been enhanced with a copper heat slug to provide a low thermal resistance path from the die to the exposed surface of the heat spreader. The thermal resistance is shown in Table 4.

Table 4: Thermal Resistance

Symbol	*Description*	*°C/W*
θ_{JC}	Thermal resistance from junction-to-case.	2.2
θ_{JA}	Thermal resistance from junction-to-ambient with no airflow, including conduction through the leads.	26.8

Thermal Resistance with Airflow

Thermal resistance with airflow is shown in Table 5. The thermal resistance value reflects all the thermal paths including through the leads in an environment where the leads are exposed. The temperature difference between the ambient airflow temperature and the case temperature should be the worst-case power of the device multiplied by the thermal resistance.

Table 5: Thermal Resistance with Airflow

Airflow	θ_{CA} *($^oC/W$)*
100 lfpm	19.8
200 lfpm	16.7
400 lfpm	14.6
600 lfpm	13.0

Maximum Ambient Temperature without Heatsink

The worst case ambient temperature without use of a heatsink is given by the equation:

$$T_{A(MAX)} = T_{C(MAX)} - P_{(MAX)}\theta_{CA}$$

where:

$T_{A(MAX)}$ Ambient air temperature
$T_{C(MAX)}$ Case temperature (+85^{o}C)
$P_{(MAX)}$ Power (2.05W)
θ_{CA} Theta case-to-ambient at appropriate airflow

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The results of this calculation are listed in Table 6.

Table 6: Maximum Ambient Air Temperature without Heatsink

Airflow	*Max Ambient Temperature (^oC)*
None	35.6
100 lfpm	44.4
200 lfpm	50.8
400 lfpm	55.1
600 lfpm	58.4

Note that ambient air temperature varies throughout the system based on the positioning and magnitude of heat sources and the direction of air flow.

Ordering Information

The order number for this product is formed by a combination of the device type and package type

VSC8132 **xx**

Device Type
2.488Gb/s 1:32 Demux, 3.3V

Package
QR: 128-Pin PQFP, 14x20x2mm Body

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