NTE8212
Integrated Circuit
Schottky, 8–Bit Input/Output Port

Description:

The NTE8212 input/output port is an integrated circuit in a 24–Lead DIP type package and consists of an 8–bit latch with three–state output buffers along with control and device selection logic. Also included is a service request flip–flop for the control and generation of interrupts to the microprocessor.

Features:

- Fully Parallel 8–Bit Data Register and Buffer
- Service Request Flip–Flop for Interrupt Generation
- Low Input Load Current: 0.25mA Max
- Three State Outputs
- Outputs Sink 15mA
- 3.65V Output High Voltge for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count

Absolute Maximum Ratings: $(T_A = +25°C$, Note 1 unless otherwise specified)

All Output or Supply Voltages . . . . −0.5V to +7V

All Input Voltages . . . . −1.0V to +5.5V

Output Currents 125mA

Operating Temperature Range . . . . 0° to +70°C

Storage Temperature Range . . . . −65° to +150°C

Note 1. Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics: (T_A = 0° to +70°C, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
DC Characteristics						
Input Load Current STB, DS_2, $\overline{CLR}$, DI_1 – DI_8 Inputs	$|I_{L1}|$	V_F = 0.45V	–	–	–0.25	mA
MD Input	$|I_{L2}|$		–	–	–0.75	mA
$\overline{DS_1}$ Input	$|I_{L3}|$		–	–	–1.0	mA
Input Leakage Current STB, DS, $\overline{CLR}$, DI_1 – DI_8 Inputs	$|I_{H1}|$	V_R = 5.25V	–	–	10	μA
MD Input	$|I_{H2}|$		–	–	30	μA
$\overline{DS_1}$ Input	$|I_{H3}|$		–	–	40	μA
Input Forward Voltge Clamp	V_C	I_C = –5mA	–	–	–1.0	V
Input "Low" Voltage	V_{IL}		–	–	0.85	V
Input "High" Voltage	V_{IH}		2.0	–	–	V
Output "Low" Voltage	V_{OL}	I_{OL} = 15mA	–	–	0.48	V
Output "High" Voltage	V_{OH}	I_{OH} = –1mA	3.65	–	–	V
Short Circuit Output Current	I_O5	V_O = 0V, V_{CC} = 5V	–15	–	–75	mA
Output Leakage Current, High Impedance State (DO_0 – DO_8)	I_O	V_O = 0.45V/5.25V	–	–	20	μA
Power Supply Current	I_{CC}		–	–	130	mA
AC Characteritics						
Pulse Width	t_{pw}	Input Pulse Amplitude = 2.5V, Input Rise & Fall Times = 5ns, **Between 1V and 2V** Measurement made at 1.5V with 15mA and 30pF Test Load	30	–	–	ns
Data to Output Delay	t_{pd}		–	–	30	ns
Write Enable to Output Delay	t_{we}		–	–	40	ns
data Setup Time	t_{set}		15	–	–	ns
Data Hold Time	t_h		20	–	–	ns
Reset to Output Delay	t_r		–	–	40	ns
Set to Output Delay	t_s		–	–	30	ns
Output Enable/Disable Time (Note 2)	t_e/t_d		–	–	45	ns
Clear to Output Delay	t_c		–	–	55	ns

Note 2. R_1 = 300Ω/10KΩ; R_2 = 600Ω/1KΩ

Capacitance: (T_A = +25°C, V_{CC} = 5V, V_{BIAS} = 2.5V, f = 1MHz, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	$\overline{DS_1}$, MD	–	–	12	pF
Input Capacitance	C_{IN}	DS_2, $\overline{CLR}$, STB, DI_1 – DI_8	–	–	9	pF
Output Capacitance	C_{OUT}	DO_1 – DO_8	–	–	12	pF

Note 3. This parameter is periodically sampled and not 100% tested.

Functional Description:

Data Latch

The 8 flip–flops that compose the data latch are of a "D" type design. The output (Q) of the flip–flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(NOTE: Clock (C) overrides Reset ($\overline{CLR}$).)

Output Buffer

The outputs of the data latch (Q) are connected to three–state, non–inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three–state).

This high–impedance state allows the designer to connect the NTE8212 directly to the microprocessor bi–directional data bus.

Control Logic

The NTE8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip–flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \bullet DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip–flop (SR) is asynchronously set.

Service Request Flip–Flop (SR)

The (SR) flip–flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip–flop is set it is in the non–interrupting state.

The output (Q) of the (SR) flip–flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non–inverting and is connected to the device selection logic ($\overline{DS}_1 \bullet DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \bullet DS_2$).

When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \bullet DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request (SR) flip–flop.

Note that the SR flip–flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

Pin Connection Diagram

$\overline{DS}_1$	1		24	V_{CC}
MD	2		23	$\overline{INT}$
DI_1	3		22	DI_8
DO_1	4		21	DO_8
DI_2	5		20	DI_7
DO_2	6		19	DO_7
DI_3	7		18	DI_6
DO_3	8		17	DO_6
DI_4	9		16	DI_5
DO_4	10		15	DO_5
STB	11		14	$\overline{CLR}$
GND	12		13	DS_2

24   13

1   12

1.300 (33.02) Max

.520
(13.2)

.225
(5.73)
Max

.100 (2.54)

.126
(3.22)
Min

1.100 (27.94)

.600 (15.24)