MB86933H

930 Series 32–BIT RISC EMBEDDED PROCESSOR

FUJITSU

ADVANCE INFORMATION

SEPTEMBER 1996

FEATURES

- 25 MHz (40ns/cycle) operating frequency
- SPARC V8 high–performance RISC architecture
- 1 KByte, direct mapped instruction cache
- Flexible locking mechanism for instruction cache
- 6 window, 104 word register file
- Fast interrupt response time
- 16 address spaces, 256 MByte each
- User and supervisor modes
- Data write buffer and instruction prefetch buffer
- On–chip programmable chip selects and wait–state generators
- Support for 8–, 16–, and 32–bit wide external memory
- On–chip DRAM controller for glue–less connection to DRAM
- On–chip interrupt controller
- On–chip clock generator circuit
- JTAG test interface
- Single vector trapping
- 0.8 micron gate, 3–level metal CMOS technology
- 160–pin QFP MB86933–compatible pinout

GENERAL DESCRIPTION

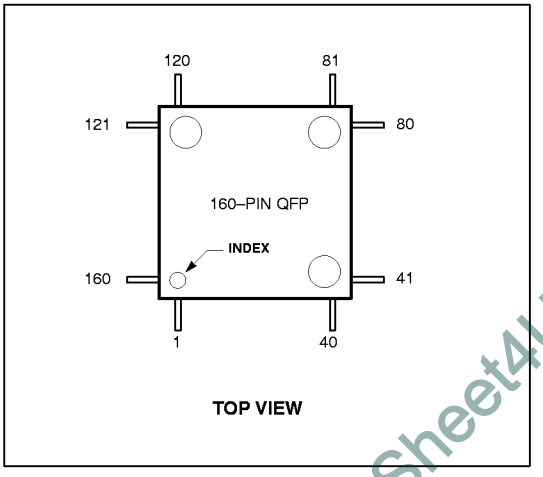
The MB86933H is targeted toward applications which require a high–performance, low–cost processor with high integration. The CPU is based on the SPARC V8 architecture, is code compatible with previous implementations, and is pin compatible with the MB86933. At 25 MHz, the processor executes at 25 MIPs peak and 22.5 MIPs sustained performance.

Included to maximize the performance of the system are a large register file, a 1KByte instruction cache, a data write buffer, and an instruction prefetch buffer.

Included to minimize external glue logic are chip–select outputs, programmable wait–state generators, an interrupt controller, and a complete DRAM controller. Also included is the ability to program each chip select region for different external data bus widths (8/16/32–bit). See MB86933H block diagram on page 3.

These features combine to allow the MB86933H to offer high performance and SPARC compatibility at a low cost to make it the right choice for a wide range of cost–sensitive, performance–oriented embedded designs.

PIN CONFIGURATION



PIN ASSIGNMENT — 160–PIN QFP

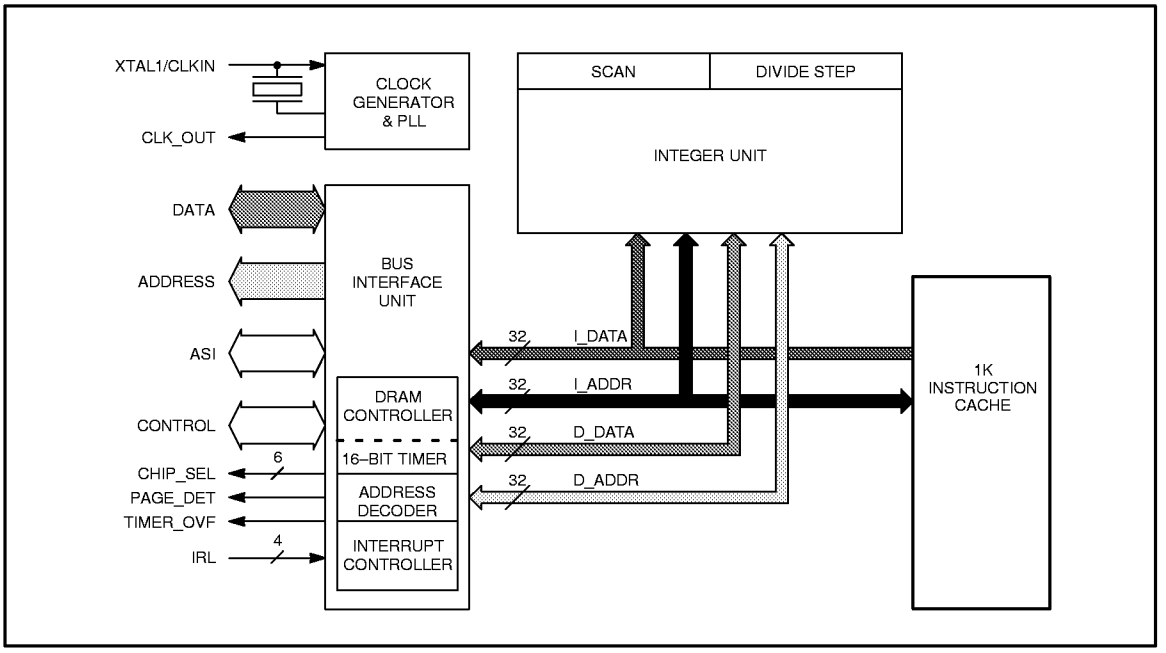
PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE	PIN NO.	PIN NAME	TYPE
1	ADR < 8 >	O	41	D < 27 >	I/O	81	D < 4 >	I/O	121	–BE < 0 >	O
2	ADR < 9 >	O	42	N.C.	—	82	D < 3 >	I/O	122	N.C.	—
3	ADR < 10 >	O	43	D < 26 >	I/O	83	D < 2 >	I/O	123	–BE < 1 >	O
4	ADR < 11 >	O	44	D < 25 >	I/O	84	D < 1 >	I/O	124	–BE < 2 >	O
5	ADR < 12 >	O	45	D < 24 >	I/O	85	D < 0 >	I/O	125	–BE < 3 >	O
6	VDD	—	46	D < 23 >	I/O	86	VSS	—	126	ASI < 0 >	O
7	VSS	—	47	D < 22 >	I/O	87	VDD	—	127	ASI < 1 >	O
8	ADR < 13 >	O	48	VSS	—	88	–MEXC	I	128	ASI < 2 >	O
9	ADR < 14 >	O	49	VDD	—	89	–READY	I	129	ASI < 3 >	O
10	ADR < 15 >	O	50	D < 21 >	I/O	90	–BREQ	I	130	–RAS1	—
11	ADR < 16 >	O	51	VSS	—	91	–AS	O	131	VSS	—
12	–CAS0	—	52	VDD	—	92	–RD/WR	O	132	VDD	—
13	ADR < 17 >	O	53	D < 20 >	I/O	93	–LOCK	O	133	–TRST	I
14	ADR < 18 >	O	54	D < 19 >	I/O	94	–BGRNT	O	134	–RESET	I
15	–CAS1	—	55	D < 18 >	I/O	95	–DWE	—	135	VDD	—
16	ADR < 19 >	O	56	VSS	—	96	–ERROR	O	136	VSS	—
17	ADR < 20 >	O	57	N.C.	—	97	VSS	—	137	–BMODE8	I
18	–CAS2	—	58	D < 17 >	I/O	98	VDD	—	138	VSS	—
19	ADR < 21 >	O	59	D < 16 >	I/O	99	–SAME_PAGE	O	139	VDD	—
20	VDD	—	60	N.C.	—	100	–CS < 0 >	O	140	–BMODE16	I
21	VSS	—	61	D < 15 >	I/O	101	VDD	—	141	N.C.	—
22	ADR < 22 >	O	62	D < 14 >	I/O	102	–CS < 1 >	O	142	TDI	I
23	–CAS3	—	63	VDD	—	103	–CS < 2 >	O	143	TMS	I
24	ADR < 23 >	O	64	D < 13 >	I/O	104	–CS < 3 >	O	144	VDD	—
25	ADR < 24 >	O	65	D < 12 >	I/O	105	VSS	—	145	VSS	—
26	ADR < 25 >	O	66	VDD	—	106	–CS < 4 >	O	146	IRL < 0 >	I
27	VSS	—	67	VSS	—	107	–CS < 5 >	O	147	IRL < 1 >	I
28	VDD	–	68	–RAS0	—	108	TCK	I	148	IRL < 2 >	I
29	ADR < 26 >	O	69	D < 11 >	I/O	109	VDD	—	149	IRL < 3 >	I
30	ADR < 27 >	O	70	D < 10 >	I/O	110	VSS	—	150	VSS	—
31	D < 31 >	I/O	71	D < 9 >	I/O	111	VDD	—	151	VDD	—
32	VDD	—	72	D < 8 >	I/O	112	XTAL2	O	152	TDO	O
33	VSS	—	73	D < 7 >	I/O	113	CLK_ECB	I	153	VSS	—
34	D < 30 >	I/O	74	VDD	—	114	VSS	—	154	VDD	—
35	D < 29 >	I/O	75	VSS	—	115	XTAL1	I	155	ADR < 2 >	O
36	VSS	—	76	VDD	—	116	CLKOUT1	O	156	ADR < 3 >	O
37	VDD	—	77	VSS	—	117	CLKOUT2	O	157	ADR < 4 >	O
38	VDD	—	78	D < 6 >	I/O	118	VDD	—	158	ADR < 5 >	O
39	VSS	—	79	VSS	—	119	VSS	—	159	ADR < 6 >	O
40	D < 28 >	I/O	80	D < 5 >	I/O	120	–TIMER_OVF	O	160	ADR < 7 >	O

ORDERING CODE

Clock Frequency (MHz)	Ordering Code	Package Type
25	MB86933H–25PF–G–B	Plastic QFP 160

Note: The ordering code for production level product. Early shipments of this device may be marked with "ES" to indicate that the part is not yet at full production status. Contact your local Fujitsu representative for additional information on "ES" level products.

BLOCK DIAGRAM



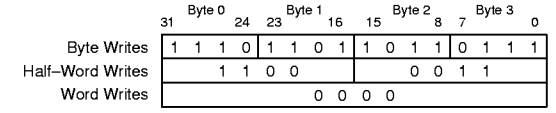
SIGNAL DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTION
–RESET	I A (L)	**SYSTEM RESET:** Asserting reset for at least 4 processor cycles after the clock has stabilized, causes the MB86933 to be initialized.
XTAL1, (CLK_IN) XTAL2	I/O O G (Q) I (Q)	**EXTERNAL OSCILLATOR:** The crystal inputs determine execution rate and timing of the MB86933H processor. Connecting a crystal to these pins forms a complete crystal oscillator circuit. The crystal oscillator frequency is the same as the processor operating frequency. When driving the processor with an external clock, XTAL2 pin should be left floating.
CLKOUT1	O G (Q) I (Q)	**CLOCK OUTPUT 1:** This is an output signal against which MB86933H bus transactions can be referenced. The CLKOUT1 frequency is the same as the frequency applied to XTAL1 and is the same as the processor operating frequency. CLKOUT1 is in phase with CLK_IN.
CLKOUT2	O G (Q) I (Q)	**CLOCK OUTPUT 2:** This is an output signal against which MB86933H bus transactions can be referenced. The CLKOUT2 frequency is the same as the frequency applied to XTAL1 and is the same as the processor operating frequency. CLKOUT2 is out of phase with CLK_IN.
–LOCK	O S (L) G (Z) I (1)	**BUS LOCK:** This is a control signal asserted by the processor to indicate to the system that the current bus transaction requires more than one transfer on the bus. The Atomic Load Store instruction for example requires contiguous bus transactions which cause the assertion of the bus lock signal. The bus may not be granted to another bus owner as long as –LOCK is active. –LOCK is asserted with the assertion of –AS and remains active until –READY is asserted at the end of the locked transaction.
–BREQ	I S (L)	**BUS REQUEST:** Asserted by another device on the bus to indicate that it wants ownership of the bus. The request must be answered with a bus grant (–BGRNT) from the MB86933H before the device can proceed by driving the bus. Once the bus has been granted, the device has ownership of the bus until it de–asserts –BREQ. The user should ensure that devices on the bus cannot monopolize the bus to the exclusion of the CPU. Inputs to –BREQ while –RESET is active are valid and cause Bus Grant to be asserted.
–BGRNT	O S (L) G (0) I (Q)	**BUS GRANT:** Asserted by the CPU in response to a request from a device wanting ownership of the bus. The CPU grants the bus to other devices only after all transfers for the current transaction are completed. All bus drivers are three–stated with the assertion of the bus grant signal.
–ERROR	O A (L) G (Q) I (Q)	**ERROR SIGNAL:** Asserted by the CPU to indicate that it has halted in an error state as a result of encountering a synchronous trap while traps are disabled. In this situation the CPU saves the PC and nPC registers, sets the tt value in the TBR, enters into an error state and asserts the –ERROR signal. The system can monitor the –ERROR pin and initiate a reset under the error condition. This pin is high on reset.
–MEXC	I S (L)	**MEMORY EXCEPTION:** Asserted by the memory system to indicate a memory error on either a data or instruction access. Assertion of this signal initiates either a data or instruction access exception trap in the IU. The current bus access is invalidated by asserting the –MEXC in the same cycle as the –READY signal. Assertion in any other bus cycle give indeterminate results. The IU ignores the contents of the data bus in cycles where –MEXC is asserted.
IRL< 3:0 > / IRQ<15:12>	I A (L)	**INTERRUPT REQUEST BUS:** Based on the mode selected in the on–chip interrupt controller, these pins are defined in two ways. In one mode (IRL) the value on these pins defines an external interrupt vector . IRL < 3:0 >=1111 forces a non–maskable interrupt. IRL value of 0000 indicates no pending interrupts. All other values indicate maskable interrupts as enabled in the PIL field of the processor status register (PSR). In this mode, interrupts should be latched and prioritized by external logic and should be held pending until acknowledged by the processor. In the other mode (IRQ), each pin represents a decoded interrupt source. When active, the values on pins IRQ<15:12> will cause the processor to vector to interrupts 15 through 12, respectively. The trigger for each IRQ pin can be set for high–level, low–level, rising edge, or falling edge.

1. In the following descriptions, signal names preceded by a minus sign (–) indicate an active low state. Dual function pins have two names separated by a slash (/).

<table>
<tr><th>SYMBOL</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>–TIMER_OVF</td><td>O
S (L)
G (Q)
I (Q)</td><td>TIMER UNDERFLOW: Asserted by the processor to indicate that the internal 16–bit timer has underflowed. This signal can be used to initiate a DRAM refresh cycle for the on–chip DRAM controller or can be used to generate periodic waveforms. The timer overflow signal can be programmed to be active for a single cycle or for three cycles after each underflow. On reset, the timer is turned off and –TIMER_OVF is high.</td></tr>
<tr><td>–SAME_PAGE</td><td>O
S (L)
G (1)
I (1)</td><td>SAME–PAGE DETECT: The –SAME_PAGE is used to take advantage of fast consecutive accesses within Fast Page Mode DRAM page boundaries. This signal is an output but also goes internally to the on–chip DRAM controller. It is asserted by the processor when the current address is within the chip select 4 region and is also within the same page as the previous memory access The –SAME_PAGE signal is asserted with –AS and remains active for one processor cycle. –SAME_PAGE is never asserted in the first transaction following a transaction by another device on the bus. The page size is specified by writing the SAME–PAGE MASK register.</td></tr>
<tr><td>–CS0, –CS1,
–CS2, –CS3,
–CS4, –CS5</td><td>O
S (L)
G (1)
I (1)</td><td>CHIP SELECTS: These outputs are asserted when the value on the address bus matches the address range in one of the corresponding ADDRESS RANGE registers. The signals are used to decode the current address into one of six address ranges. Address ranges should not overlap. Each address range has a corresponding wait specifier which is used to automatically assert the –READY signal after a user defined number of processor clock cycles. This allows a variety of memory and I/O devices with different access times to be connected to the MB86933H without the need for additional logic. On the MB86933H, chip select 4 is defined to support the on–chip DRAM controller.</td></tr>
<tr><td>ADR < 27:2 ></td><td>O
S (L)
G (Z)
I (1)</td><td>ADDRESS BUS: The 26–bit ADDRESS BUS (ADR27–ADR2) is an output which identifies the data or instruction address of a 32–bit word. Reads are always one word in size while byte, half–word, or word transaction sizes for writes are identified by separate byte–enable signals (–BE0–3). The address bus is valid for the duration of the bus transaction. ADR27–ADR16 (MA<11:0>)are also used for the DRAM address. The value on these pins when RAS_ falls is the DRAM row address. The value on these pins when CAS_ falls is the DRAM column address.</td></tr>
<tr><td>ASI < 3:0 ></td><td>O
S (L)
G (Z)
I (1)</td><td>ADDRESS SPACE IDENTIFIERS: The ADDRESS SPACE IDENTIFIERS are outputs which indicate to which of 16 available spaces the current ADDRESS BUS value corresponds. The ASI values are defined as follows:

<table>
<tr><th>ASI < 3:0 ></th><th>ADDRESS SPACE</th></tr>
<tr><td>0x1</td><td>Control Registers</td></tr>
<tr><td>0x2 – 0x7</td><td>Application Definable</td></tr>
<tr><td>0x8</td><td>User Instruction Space</td></tr>
<tr><td>0x9</td><td>Supervisor Instruction Space</td></tr>
<tr><td>0xA</td><td>User Data Space</td></tr>
<tr><td>0xB</td><td>Supervisor Data Space</td></tr>
<tr><td>0xC – 0xF</td><td>Application Definable</td></tr>
</table>
The ASI values specified as “application definable” can be used by supervisor mode instructions such as Load Alternate and Store Alternate. The ASI value is available in the same cycle in which the corresponding address value is asserted on the address bus. The ASI pins are valid for the duration of the bus transaction.</td></tr>
</table>

SYMBOL	TYPE	DESCRIPTION
–BE3–0	O S (L) G (Z) I (O)	**BYTE ENABLES (O):** These pins indicate whether the current store transaction is a byte, half–word or word transaction. –BE3–0 signals are available in the same cycle in which the corresponding address value is asserted on the address bus and is valid for the duration of the bus transaction. This bus should be used only to qualify store transactions. For read transactions all sub–word requests are read (and replaced in the cache) as words. For loads the appropriate byte or half–word is extracted by the integer unit. Possible values for –BE3–0 are as follows:  BE < 2:3 > are also used in 8 and 16–bit accesses where they are used as the lower two address bits. In these modes they are defined as follows: Bus Mode / Byte / BE < 2:3 > 8–bit: 0 / 0 0; 1 / 0 1; 2 / 1 0; 3 / 1 1 16–bit: 0 & 1 / 0 0; 2 & 3 / 1 0 For 16–bit wide buses, BE<1:0> are used as byte enables during stores. BE<1> is valid for the high order byte while BE<0> is valid for the low order byte.
D < 31:0 >	I/O S (L) G (Z) I (Z)	**DATA BUS:** The bus interface has 32 bidirectional data pins (D31–D0) to transfer data in thirty–two bit quantities. D (31) corresponds to the most significant bit of the 32–bit word. A double word is aligned on an 8–byte boundary, a word is aligned on a 4–byte boundary, and a half–word is aligned on a 2–byte boundary. If a load or store of any of these quantities is not properly aligned, a Not Aligned Trap will occur in the processor. In write bus cycles, the point at which data is driven onto the bus depends on the type of the preceding cycle. If the preceding cycle was a write, data is driven in the cycle immediately following the cycle in which –READY was asserted. If the preceding cycle was a read, data is driven one cycle after the cycle in which –READY was asserted to minimize bus contention between the processor and the system. For a given chip select region, pins D[7:0] are used when the 8–bit wide bus is used and D[15:0] are used when 16–bit wide bus is used.
–AS	O S (L) G (Z) I (1)	**ADDRESS STROBE:** A control signal asserted by the MB86933H or other bus master to indicate the start of a new bus transaction. A bus transaction begins with the assertion of –AS and ends with the assertion of –READY. –AS remains asserted for 1 clock cycle. During cycles in which neither the processor nor another bus master is driving the bus the bus is idle, and –AS remains de–asserted.
RD/–WR	O S (L) G (Z) I (1)	**READ/BUS TRANSACTION:** This signal specifies whether the current bus transaction is a read or a write operation. When –AS is asserted and RD/–WR is low, then the current transaction is a write. With –AS asserted and RD/–WR high, the current transaction is a read. RD/–WR remains active for the duration of the bus transaction and is de–asserted with the assertion of –READY.

SYMBOL	TYPE	DESCRIPTION
–READY	I S (L)	**READY:** This is a control signal asserted by the external memory system to indicate that the current bus transaction is being completed and that it is ready to start with the next bus transaction in the following cycle. In case of a fetch from memory, the processor will strobe the value on the data bus at the rising edge of CLK_IN following the assertion of –READY. For the case of a write, the memory system will assert –READY when the appropriate access time has been met. In most cases, no additional logic is required to generate the –READY signal. On–chip circuitry can be programmed to assert –READY based on the address of the current transaction. The external system can override the internal ready generator to terminate the current bus cycle early. Up to 6 address ranges each with different transaction times can be programmed.
CLK_ECB	I	**EXTERNAL CLOCK BYPASS:** Tying this signal high causes the CLK_IN signal to bypass the Phases Lock Loop (PLL). This signal is used for testing of the chip.
–BMODE8	I S (L)	**8–BIT BOOT MODE:** This signal is sampled during reset and causes read accesses memory mapped to –CS0 to assume 8–bit ROM memory. The MB86933H generates four sequential fetches to assemble a complete instruction or data word before continuing. Bytes are fetched in sequence (0,1,2,3) as encoded by –BE[2] and –BE[3] (00, 01, 02, 03). If left unconnected, a weak pull–up on this pin (and –BMODE16 pin) causes the processor to default to 32–bit mode.
–BMODE16	I S (L)	**16–BIT BOOT MODE:** This signal is sampled during reset and causes read accesses memory mapped to –CS0 to assume 16–bit ROM memory. The MB86933H generates two sequential fetches to assemble a complete instruction or data word before continuing. Half words are fetched in sequence (0,1) as encoded by –BE[2]. If left unconnected, a weak pull–up on this pin (and –BMODE8 pin) causes the processor to default to 32–bit mode.
–RAS0, –RAS1	O	**DRAM ROW ADDRESS STROBES:** The MB86933H can support up to two banks of DRAM. –RAS0 is the row address strobe for bank0. –RAS1 is the row address strobe for bank1. Note that the row address for the DRAM appears on pins ADR[27:16].
–CAS0, –CAS1, –CAS2, –CAS3	O	**DRAM COLUMN ADDRESS STROBES:** The MB86933H supports byte, half–word, and word accesses to DRAM. –CAS0 is used for accesses to byte0, –CAS1 is used for accesses to byte1, –CAS2 is used for accesses to byte2, –CAS3 is used for accesses to byte3. Note that the column address for the DRAM appears on pins ADR[27:16].
–DWE	O	**DRAM WRITE ENABLE:** When this signal is deasserted (high) an access to DRAM is a read. When asserted (low), an access to DRAM is a write.
TCK	I	**TEST CLOCK:** JTAG compatible test clock input.
TMS	I	**TEST MODE:** JTAG compatible test mode select pin.
TDI	I	**TEST DATA IN:** JTAG compatible test data input.
TDO	O	**TEST DATA OUT:** JTAG compatible test data output.
–TRST	I	**TEST RESET:** Asynchronous reset for JTAG logic. If not using JTAG, this signal must be pulled low.

NOTE:
- I = Input Only Pin
- O = Output Only Pin
- I/O = Either Input or Output Pin
- – = Pins "must be" connected as described
- A (L) = Asynchronous: Inputs may be asynchronous to CLKOUT1.
- S (L) = Synchronous: Inputs must meet setup and hold times relative to CLK_IN Outputs are Synchronous to CLK_IN
- G (...) = While the bus is granted to another bus master (–BGRNT=asserted), the pin is
  - G (1) is driven to V_{CC}
  - G (0) is driven to V_{SS}
  - G (Z) floats
  - G (Q) is a valid output
- I (...) = While the bus is between bus cycles (or being reset) and is not granted to another bus master, the pin is
  - I (1) is driven to V_{CC}
  - I (0) is driven to V_{SS}
  - I (Z) floats
  - I (Q) is a valid output

OVERVIEW

The Fujitsu MB86933H is a high–performance, 32–bit RISC processor which executes at 25 MIPs peak and 22.5 MIPs sustained performance with 25 MHz clock frequency. Like its predecessors, the MB86933H is based on the SPARC V8 architecture and is upward code compatible with previous implementations. More importantly, the MB86933H has been developed specifically with the needs of embedded applications in mind and offers high performance and low cost for these applications.

The MB86933H instruction set is streamlined and hardwired for fast execution with most instructions executing in a single cycle. The Integer Unit (IU) features a 5–stage pipeline which has been designed to handle data interlocks, has an optimized branch handler for efficient control transfers, and a bus interface to handle single cycle bus accesses to on–chip memory.

KEY FEATURES

Fast Instruction Execution: Simple functions make up the bulk of instructions in most programs so that execution speed can be greatly improved by designing these instructions to execute in as short a time as possible. The majority of instructions execute in one cycle with only a few of the more complex, such as integer multiply, taking additional cycles.

On–chip Instruction Cache: To decouple the speed of the processor from the memory subsystem a 1 KByte direct mapped instruction cache is included on chip. It is possible to individually lock lines in the cache to ensure deterministic response and higher performance for critical or frequently recurring routines.

Large Register Set: The large register set (104 registers) reduces the number of required accesses to data memory. The registers are organized into six overlapping groups called register windows which allows registers to be reserved for high priority tasks, such as interrupts, or for recurring requirements such as operating system working registers. The overlapping windows also simplify parameter passing during procedure linkage and reduce code in most programs.

Hardware Multiplier: The MB86933H also includes hardware for integer multiply. The hardware support significantly improves the performance of these operations with 32–bit integer multiplies executing in 5 clock cycles, 16–bit integer multiplies in 3 cycles, 8–bit integer multiplies in 2 cycles, and a multiply by zero can complete in a single cycle.

Interrupt Controller: An on–chip interrupt controller is provided on the MB86933H. Four interrupt pins can either be programmed to act as an encoded external interrupt vector providing for up to 15 interrupts or as four individual interrupt lines.

Bus Interface: The requirement for glue logic between the MB86933H and the system is removed by providing programmable chip selects and programmable wait–state circuitry. Each chip select region can be programmed to support either 8–bit, 16–bit, or 32–bit wide memory. Multiple bus masters are supported through a simple handshake protocol.

Instruction Prefetch Buffer: A one–word prefetch buffer is provided to increase performance when instruction cache misses occur.

Data Write Buffer: A one–word write buffer is provided to decouple writes from internal instruction execution. Data can be posted to the write buffer and execution from internal cache can continue in parallel while the store completes to external memory.

DRAM Controller: Present on the MB86933H is a complete DRAM controller which provides glueless connection to up to two banks of DRAM memory. Support for either 16–bit or 32–bit wide DRAM memory banks is provided.

Clock Generator: To simplify the clock design a crystal can be connected directly to the on–chip oscillator or an external clock source can be used. A built–in phase–locked loop minimizes the skew between on– and off–chip clocks.

Enhanced Instruction Set: An integer divide–step instruction cuts divide times by a factor of 10 over previous SPARC implementations. A scan instruction supports a single cycle search for the most significant 1 or 0 in a word.

Fully Static Circuit Design: Embedded applications that need a means to reduce power consumption can take advantage of the MB86933H's fully static design. The processor clock can be slowed or stopped for arbitrary periods of time to reduce operating current with no loss of internal state. Noise immunity is improved as well. (Note: stopping the clock will result in the Phase–Locked Loop losing lock. Lock must be re–established before normal operation can be resumed.)

Test and Debug Interface: The MB86933H supports production test through industry standard JTAG boundary scan.

CPU

The MB86933H core is a high–performance full–custom implementation of the SPARC V8 architecture. The core is compact to leave room for peripheral integration and yet is designed in a way to allow the major blocks to be customized for varying application requirements. The core is made up of three functional units: the Instruction block, the Address block and the Execute block. (See Figure 1.)

A five–stage instruction pipeline is responsible for decoding all instructions and generating the control signals to the other blocks. The 5–stage pipeline consists of Fetch (F), Decode (D), Execute (E), Memory (M) and Writeback (W). Instruction memory is addressed and returns instructions in the (F) stage, the register file is addressed and returns operands in the (D) stage, the ALU computes results in the (E) stage, external memory is addressed in the (M) stage, and the register file is written back in the (W) stage.

ADDRESS SPACE

The MB86933H offers a large addressing range and allows separate user and supervisor spaces to be defined. In addition to 28 address lines, 4 alternate address space identifiers (ASIs) distinguish between protected and unprotected space. Of the 16 possible ASI values, two define accesses to user data and user instruction space while the remaining ASI values define supervisor space.

Anytime a reset, synchronous trap or asynchronous trap occurs, the processor is placed into the supervisor mode. In this mode, the processor executes instructions and moves data out of supervisor space. While in supervisor mode, the processor also has access to the remaining ASI values. Except for those mentioned and those reserved for control register space, the remaining ASI values can be used to access other alternate data spaces defined by the application.

The distinction of user versus supervisor space allows the hardware to protect against accidental or un–authorized access to system resources. For real–time operating system (RTOS) development for example, the separate spaces provide a mechanism for effectively partitioning RTOS space from user space.

TABLE 1. MB86933H Instruction Set

<table>
<tr><th>LOGICAL</th><th>ARITHMETIC/SHIFT</th><th>DATA MOVEMENT</th></tr>
<tr><td>CONDITION CODES UNCHANGED
AND
OR
XOR
AND
NOT
OR NOT
XNOR

CONDITION CODES SET
AND
OR
XOR
AND NOT
OR NOT
XNOR</td><td>CONDITION CODES UNCHANGED
ADD
SUBTRACT
MULTIPLY (SIGNED/UNSIGNED)
SCAN
SETHI
SHIFT LEFT LOGICAL
SHIFT RIGHT LOGICAL
SHIFT RIGHT ARITHMETIC

CONDITION CODES SET
ADD
SUBTRACT
MULTIPLY (SIGNED/UNSIGNED)
MULTIPLY STEP
DIVIDE STEP

EXTENDED AND CONDITION CODES UNCHANGED
ADD
SUBTRACT

EXTENDED AND CONDITION CODES SET
ADD
SUBTRACT
TAGGED AND CONDITION CODES SET (WITH AND WITHOUT TRAP ON OVERFLOW)
ADD
SUBTRACT</td><td rowspan="3">TO USER/SUPERVISOR SPACE SIGNED
LOAD BYTE
LOAD HALF–WORD
LOAD WORD
LOAD DOUBLE WORD
STORE BYTE
STORE HALF–WORD
STORE WORD
STORE DOUBLE WORD

TO USER SPACE UNSIGNED
LOAD BYTE
LOAD HALF–WORD

TO ALTERNATE SPACE SIGNED
LOAD BYTE
LOAD HALF–WORD
LOAD WORD
LOAD DOUBLE WORD
STORE BYTE
STORE HALF–WORD
STORE WORD
STORE DOUBLEWORD

TO ALTERNATE SPACE UNSIGNED
LOAD BYTE
LOAD HALF–WORD

ATOMIC OPERATION IN USER SPACE
SWAP WORD
LOAD/STORE UNSIGNED BYTE

ATOMIC OPERATION IN ALTERNATE SPACE
SWAP WORD
LOAD/STORE UNSIGNED BYTE</td></tr>
<tr><td>CONTROL TRANSFER</td><td></td></tr>
<tr><td>CONDITIONAL BRANCH
CONDITIONAL TRAP
CALL
RETURN
SAVE
RESTORE
JUMP AND LINK</td><td></td></tr>
<tr><td colspan="2">READ/WRITE CONTROL REGISTER</td><td></td></tr>
<tr><td colspan="2">READ PSR
WRITE PSR
READ TBR
WRITE TBR

READ WIM
WRITE WIM
READ Y
WRITE Y

RDASR
WRASR</td><td></td></tr>
</table>

REGISTERS

The MB86933H register set is divided into those used for general–purpose functions and those used for control and status.

The 104 general–purpose registers are divided into 6 global registers and 6 overlapping blocks or "windows". Each window contains 24 registers. Of these, 8 are local to the window, 8 "out" registers overlap with the next window and 8 "in" registers overlap with the previous window. (See Figure 2.)

This organization makes it easy to pass parameters to subroutines. Parameters that are to be passed along are written to the "out" registers and the subsequent procedure call decrements the window pointer to make a new set of registers available. The passed parameters are now available to the subroutine in the current window's "in" registers.

Register windows improve performance in embedded applications because they function as local variable caches which retain either interrupt, subroutine, context or operating system variables with no additional overhead. In addition, code can be reduced by exploiting the efficient execution of procedure linkage by preventing in–lining compiler optimizations.

The registers that make up the register file each have three read–only and one write–only port. The use of a four–port register file allows even store instructions, which may require that three operands be read out of the register file, to proceed at one instruction per cycle.

The control and status registers include those defined by the SPARC architecture (see Table 1) and those mapped into alternate address space to control peripheral functions (see Table 2).

INSTRUCTION SET

The MB86933H is upward code compatible with other SPARC V8 processors. Additional instructions, previously not directly supported, have been added to improve performance in embedded applications. Integer multiply, integer divide step, and scan for first changed bit have been added to the already powerful SPARC instruction set. See Table 1 for a list of supported instructions.

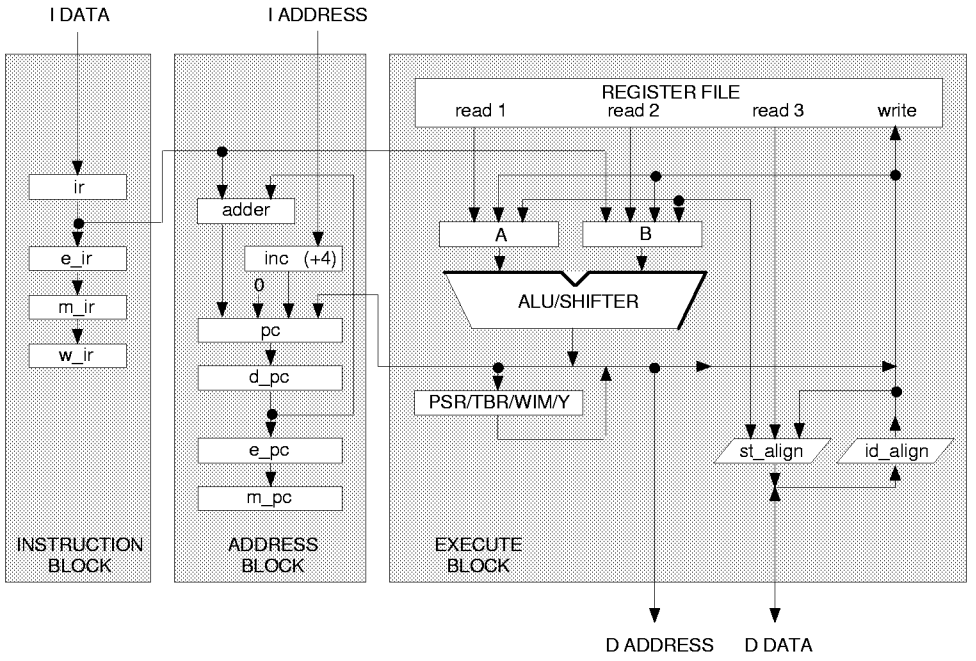


Figure 1. MB86933H Integer Unit Data Path

INTERRUPTS

A key measure of a processor's suitability for use in embedded application is in its ability to handle interrupts with a minimum of delay and in a deterministic fashion. The MB86933H implementation has been tailored to insure not only low average latency but low maximum latency as well.

Interrupt response time is made up of the sum of the times it takes the processor to finish its current task after recognizing an interrupt, and the time it takes to begin executing interrupt service routine instructions. The MB86933H implements numerous features to minimize both factors.

To minimize the time it takes to finish the current task, the MB86933H is designed so that tasks can either be interrupted or completed in a minimum number of cycles. Implementation details that accomplish this aim include an integer divide operation that is interruptible through the use of a divide step instruction and a fast multiply operation to minimize non–interruptible instruction execution.

To minimize the time required to start executing the interrupt service routine the processor switches to a new register window when an interrupt is detected. This feature allows the service routine to be executed without first requiring that the current registers be saved.

INTERRUPT CONTROLLER

The SPARC V8 architecture, and the MB86933H in particular, provides for up to 15 separate external interrupt sources. The MB86933H has four external interrupt pins and an on–chip interrupt controller (IRC) which can support two modes of operation.

Mode 0 (IRL mode): In mode 0 the input on the four external pins is interpreted as an encoded interrupt vector. This mode allows for external logic to generate any one of the 15 possible interrupts ("0" represents "no interrupt request"). In this mode of operation it is assumed that the external interrupt source maintains the interrupt vector on the pins until it is explicitly cleared by writing to an external memory mapped location. Note that this mode is the same as that on the MB86930/932/933 and is compatible with the MB86940 companion chip.

Mode 1 (IRQ mode): In the mode 1 the four pins are considered to be four separate interrupt sources mapping to interrupts 12 through 15. Note this mode is the same as that on the MB86931

Figure 3 shows a block diagram of the IRC in mode 1.

The Trigger Mode Control logic selects one of four trigger modes for each of the four channels: high level, low level, rising edge, or falling edge. The processor controls the triggers by writing to the Trigger Mode register.

The IRQ latch captures each of the four interrupt requests. The system processor reads the latch via the Request Sense register and clears the latch by writing to the Request Clear register. The example assembly language program below shows the code sequence for writing to the Request Clear register of channel 12.

The IRQ Mask logic allows selective masking of the interrupts. The processor controls masking by writing to the Mask register.

```
-------------------------------------------------------
     . . . .
     . . . .
! define Request Clear Register #define rqc 0x20c
! define a valid memory location #define rqs_loc 0x1000
! define control register ASI address space #define casi 0x1

    . . . .
    . . . .   ! Request Clear;
    set         rqc, %10
    set         0x1000,  %17
    set         rqs_loc,  %16     !memory location defined in main prog
    st          %g0,  [%16]
    sta         %17,  [%10]  casi   !write to Request Clear register
     . . . .
     . . . .
```

A write to Request Clear register must be preceeded by the store of 0x0 to any valid memory location to prevent the previous high value bits on the data bus from unintentionally setting other bits of the Clear Request register.

The Priority Encoder prioritizes the interrupt requests and encodes the highest priority pending interrupt that is not masked. pin IRL3 maps to interrupt 15, IRL2 maps to interrupt 14, IRL1 maps to interrupt 13 and IRL0 maps to interrupt 12.

The IRL latch captures the encoded interrupt level number that is generated by the priority encoder.

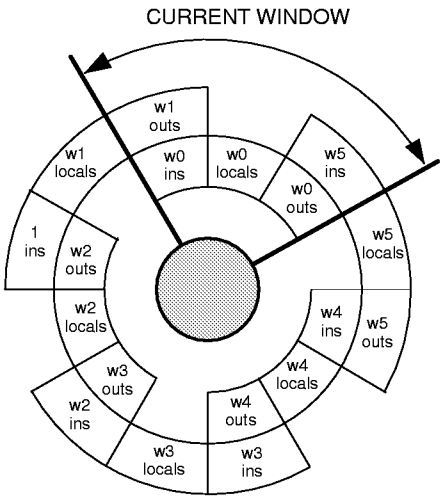


Figure 2. General–Purpose Register Organization

INSTRUCTION CACHE

The MB86933H has an on–chip, 1KByte, direct–mapped, sectored instruction cache. The line length of the cache is 16 bytes. Lines are subdivided into four sub–blocks, each four bytes wide. On a cache miss, the cache is updated in sub–block increments. Also, on a cache miss the instruction prefetch buffer fetches the next sequential anticipating that it will be needed to fill then next instruction cache miss.

The cache can be used in either normal mode or one of two lock modes.

Global locking allows the entire content of the instruction cache to be frozen. A bit in the cache control register enables or disables global locking.

Local locking makes it possible to dynamically lock selected instructions on a line–by–line basis. This feature gives the flexibility, for example, to assure deterministic response for certain critical routines by locking the routine's code into the cache while still allowing other locations to be used as a cache. Note, however, that because the cache is direct–mapped, code which would normally map into the locked cache locations will not be cached.

BUS INTERFACE

The Bus Interface Unit (BIU) is designed to simplify the interface between the MB86933H and the rest of the system. Separate address and data buses make de–multiplexing unnecessary. Simple control signals make it easy to build fast systems.

The BIU includes two features to increase performance when accessing external memory – an instruction prefetch buffer to support efficient instruction fetches and a write buffer to support data writes.

A key measure of a processor's suitability for use in embedded application is in its ability to handle interrupts with a minimum of delay and in a deterministic fashion. The MB86933H implementation has been tailored to insure not only low average latency but low maximum latency as well.

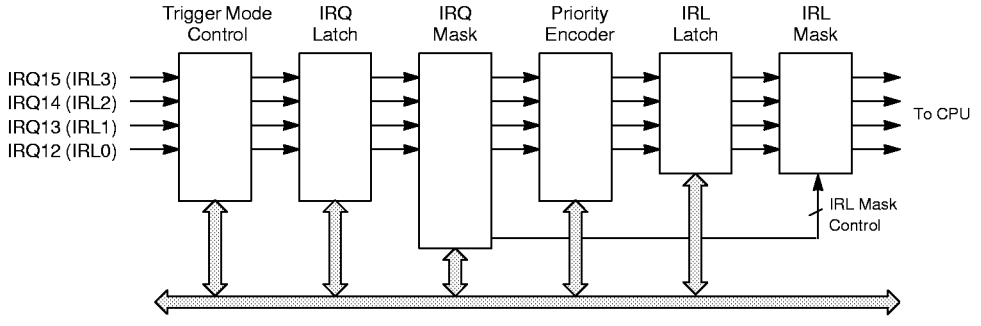


Figure 3. IRC Block Diagram (In Mode 1)

The BIU also includes circuitry to enable the design of complex systems with a minimum requirement for external glue logic. The bus interface unit supports up to six regions of memory – each region with independently programmable wait–state generation, chip select generation, and programmable bus widths. This allows for the support of multiple width memories within a single system. There is also included a complete DRAM controller for glueless connection to DRAM.

Prefetch Buffer

Associated with the instruction cache and the BIU is a one–word prefetch buffer. After an instruction fetch which misses in the cache has been satisfied, the prefetch buffer will immediately initiate another instruction access to the next sequential address. Instructions are prefetched only when the BIU does not have another pending request for a bus transaction (eg. a write to memory).

Write Buffer

Also associated with the BIU is a one–word write buffer. For stores this buffer effectively hides the external memory latency. When a store occurs the data is posted to the write buffer. The IU can then continue to execute from internal cache while the write buffer completes the store to external memory.

Chip Selects

As on the other 930 Series chips, there are six chip selects. Each chip select can be associated with a region of memory and will determine the characteristics for that region. Associated with each chip select is a wait state generator which can be set to internally terminate an external memory access after a preprogrammed number of cycles. Also associated with each chip select (except chip select 0) are control bits which determine the external bus width. The bus width for each memory region can be set to 8–bit, 16–bit or 32–bit.

Chip select 0 is dedicated for boot code. It can be programmed to be 8–bit, 16–bit, or 32–bit wide based on two external pins: BMODE8_ and BMODE16_. When the DRAM controller is used, chip select 4 is dedicated for the DRAM controller support. It should be noted that while on previous 930 Series family members the "samepage" circuitry could be associated with any chip select, on the MB86933H "samepage" is specifically associated with chip select 4.

Byte, halfword, and word operations are supported on all bus widths (8–, 16–, and 32–bit). It should be noted that all loads (byte, halfword, word) return a total of 32 bits (possibly with multiple accesses) regardless of the width of the bus. This is done to be compatible with other 930 Series family member where the minimum granularity of the on–chip data cache is one word.

DRAM Controller

The MB86933H provides all the necessary logic to directly connect up to 16 MB of fast page–mode DRAM without external glue logic (or 128 MB with external buffers). Address multiplexing is performed internally and the DRAM row and column addresses (MA<11:0>) are output on the ADR<27:16> pins. Two –RAS lines allow access to up to two banks of memory. Each –RAS signal controls a bank of memory. Each bank is configurable in both depth and width. The width can be programmed to be either 32–bit wide or, for low cost systems, 16–bit wide. Four –CAS signals allow for byte, halfword, and word stores to memory. Each –CAS signal controls a byte in a 32 bit word. –CAS0 controls accesses to byte 0, etc. Internal "samepage" detect logic is provided to allow for a minimum 2–cycle samepage access to the DRAM. An internal refresh timer is used to generate a –CAS before –RAS refresh cycles automatically at programmable intervals. The –DWE (DRAM Write Enable) pins determines whether a read or write access is being made to DRAM.

DRAM configurations supported by the MB86933H:

DRAM Size	(RAS bits x CAS bits)
256Kxn	(9x9)
512Kxn	(10x9)
1Mxn	(10x10)
2Mxn	(11x10)
2Mxn	(12x9)
4Mxn	(11x11)
4Mxn	(12x10)
16Mxn	(12x12)

where n = 1, 4, 8, 16

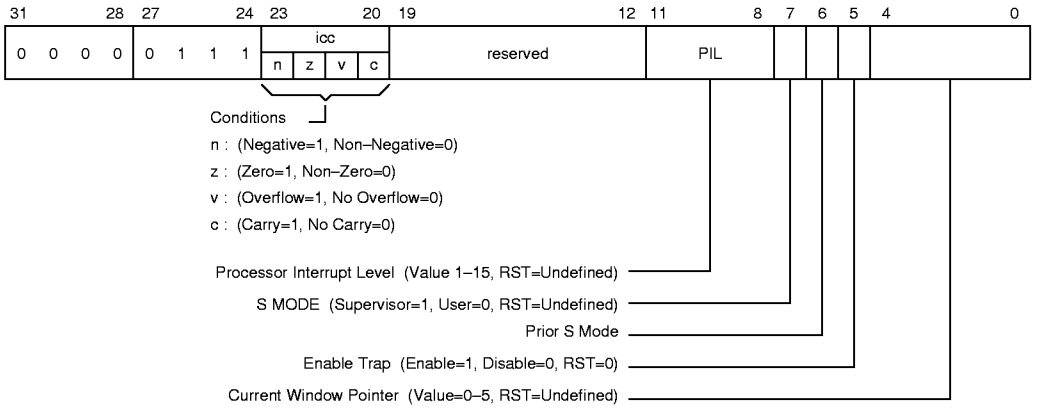
CLOCK GENERATOR

The on–chip clock generator provides a means to directly connect the MB86933H to either a crystal oscillator or an external clock source. For either case, the external frequency is the same as the chip operating frequency.

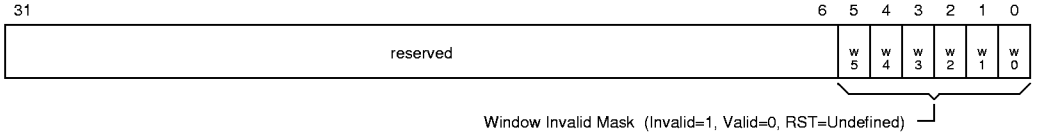
A clock output signal provides the system with a reference by which external timing can be synchronized when not using an external clock source. The skew between the internal clock and an external input clock source is minimized by the inclusion of an on–chip phase lock loop circuit.

TABLE 1. MB86933H Control and Status Registers (All registers are read/write)

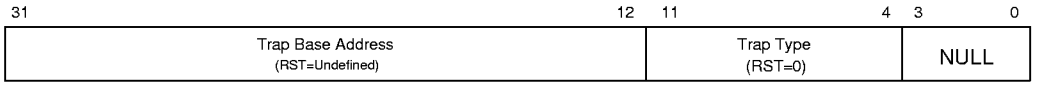
Processor State Register | **PSR**



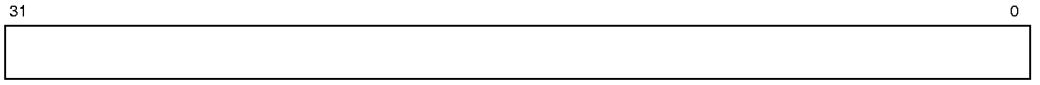
Window Invalid Mask | **WIM**



Trap Base Register | **TBR**



Y Register | **Y**



Ancillary State Register 17 | **ASR 17**

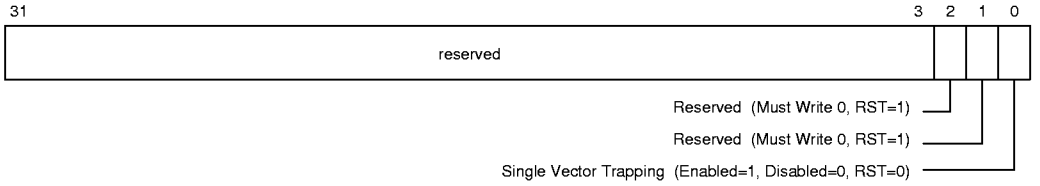
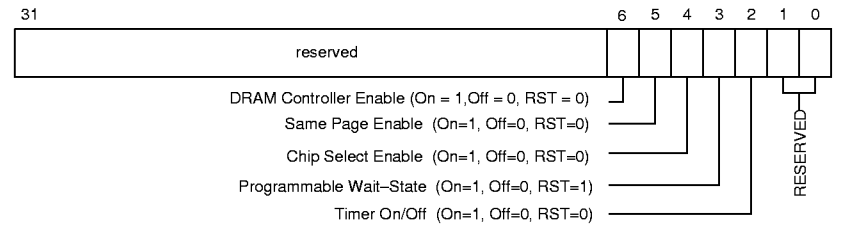


TABLE 2. MB86933H Memory Mapped Control Registers (All registers are read/write)

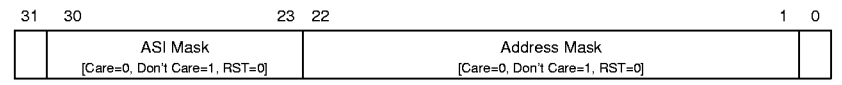
System Support Control

ASI	ADDRESS
0x 1	0x 0000 0080



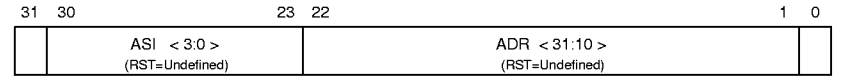
Same Page Mask

ASI	ADDRESS
0x 1	0x 0000 0120



Address Range[1]

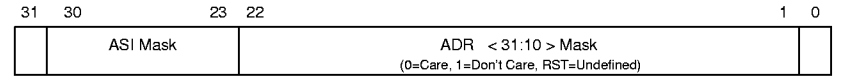
ASI	ADDRESS
0x 1	CS1 0x 0000 0124 CS2 0x 0000 0128 CS3 0x 0000 012C CS4 0x 0000 0130 CS5 0x 0000 0134



NOTE: CS0 is hardwired to ASI=0x9 ADR < 31:10 > = < 0..0 >

Address Mask

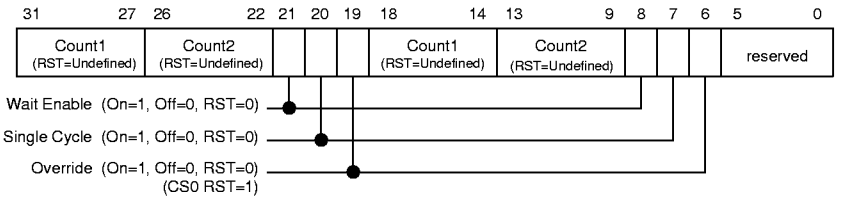
ASI	ADDRESS
0x 1	CS0 0x 0000 0140 CS1 0x 0000 0144 CS2 0x 0000 0148 CS3 0x 0000 014C CS4 0x 0000 0150 CS5 0x 0000 0154



NOTE: CS0 ADR < 14:10 > = 1, ADR < 31:15 > = 0 at reset ASI = 0x9

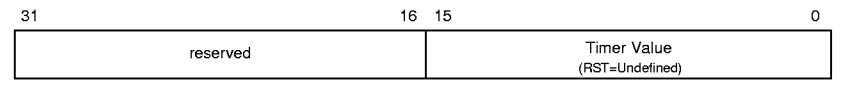
Wait State Specifier

ASI	ADDRESS
0x 1	CS1,CS0 0x 0000 0160 CS3,CS2 0x 0000 0164 CS5,CS4 0x 0000 0168



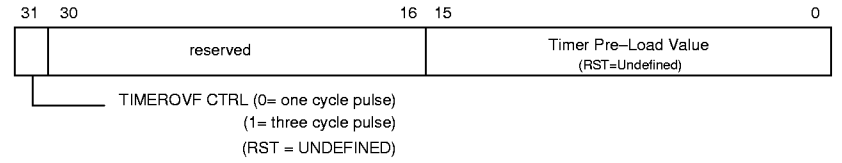
Timer

ASI	ADDRESS
0x 1	0x 0000 0174



Timer Pre–Load

ASI	ADDRESS
0x 1	0x 0000 0178

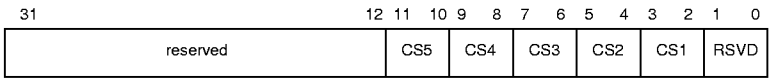


1. This register is Write Only

TABLE 2. MB86933H Memory Mapped Control Registers (All registers are read/write) (Continued)

Bus Width

ASI	ADDRESS
0x 1	0x 0000 016C



BUS WIDTH FOR DIFFERENT CHIP SELECTS. NOTE THAT CS0 IS PROGRAMMED USING 2 PINS, BMODE16 AND BMODE8

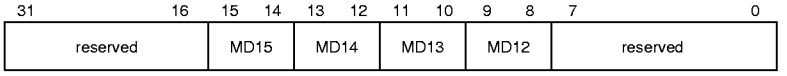
BWX	BUS WIDTH
1 1	RESERVED
1 0	16–BIT BUS
0 1	8–BIT BUS*
0 0	32–BIT BUS

(RST = 00)

*Not applicable to CS4

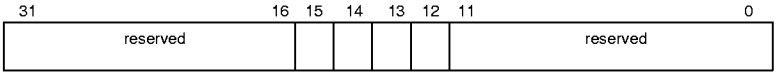
Trigger Mode 0

ASI	ADDRESS
0x 1	0x 0000 0200



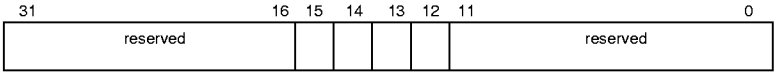
Request Sense[2]

ASI	ADDRESS
0x 1	0x 0000 0208



Request Clear[1]

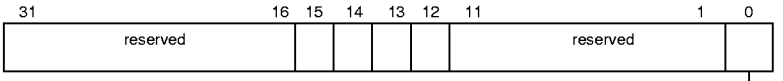
ASI	ADDRESS
0x 1	0x 0000 020C



(1 = clear)

Mask

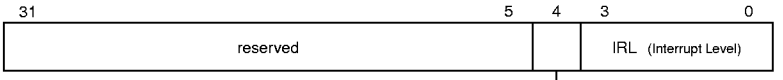
ASI	ADDRESS
0x 1	0x 0000 0210



(1 = mask) MKIRL (1 = Mask IRL Output)

Latch Clear

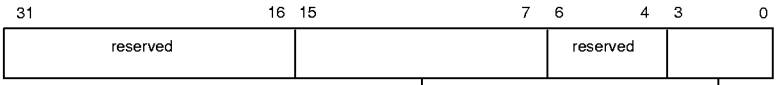
ASI	ADDRESS
0x 1	0x 0000 0214



Clear Latch (1=Clear IRL Latch)

DRAM Bank Configuration

ASI	ADDRESS
0x 1	bank 0: 0x 0000 07D0 bank 1: 0x 0000 07D4



Bank Starting Address (Bits 27:19 of the starting address of the bank)

DRAM TYPE	DEPTH x n	(RAS ADR BITS x CAS ADR BITS)
0000	256K x n	(9x9)
0001	512K x n	(10x9)
0010	1M x n	(10x10)
0011	reserved	
0100	2M x n	(11x10)
0101	2M x n	(12x9)
0110	4M x n	(11x11)
0111	4M x n	(12x10)
1000	16M x n	(12x12)
1001–1111	reserved	

BUS OPERATION

The Bus Interface Unit (BIU) has the logic which allows the MB86933H to interface with the system. The system interface is made up of the address and data buses, the interrupt request bus and various control signals. The BIU is either handling requests for external memory operations, arbitrating for bus access, or idle.

Operation of the BIU

In the case of a write to external memory, the BIU makes use of a write buffer which can hold a one–word write transaction. When the BIU receives a request for a write transaction it stores the write data and address in the write buffer allowing the IU to continue operating out of on–chip instruction cache. The BIU then proceeds to complete the write to external memory. In most cases the write buffer will hide external memory latency from the IU. The exceptions are in cases where the write buffer is still filled from a previous transaction or if the subsequent IU cycle results in an instruction cache miss. In these cases, IU execution is held until the write buffer is emptied.

The BIU includes a one–stage prefetch buffer for instruction fetches. This buffer is used to fetch the next sequential instructions after an instruction cache miss. The instruction is prefetched only if the BIU does not have a request for a bus transaction from the IU nor is any external device requesting use of the bus. The prefetch buffer operation is suspended if the buffer is full. This occurs if the prefetched instruction is a hit in the instruction cache. The buffer restarts after another instruction cache miss. If an exception occurs during an instruction prefetch, the exception is not sent to the IU unless the instruction is actually requested by the IU. The prefetch buffer operates only when the instruction cache in enabled.

Exception Handling

The external memory system can indicate an exception during a memory operation. The BIU signals the appropriate data or instruction exception to the IU which will trap accordingly.

Bus Cycles

Timings 1 through 19 illustrate representative combinations of bus cycles.

Load

Regardless of the external bus size (8, 16, or 32 bits), all instruction fetches and loads (including load byte and load half word) retrieve a 32–bit quantity. This is done for compatibility with 930 Series processors with data cache where the smallest granularity in the cache is one word. Bus sizes can be programmed based on chip select regions to be 8, 16, or 32 bit wide.

Load (32–bit wide bus)

Whenever a load from data memory is requested or an instruction cache miss occurs, the BIU performs a read from external memory (see Timing 1).

With a 32–bit external data bus, a read transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one cycle. At the same time the ADR< 27:2 > and ASI< 3:0 > bits are driven with the location to be read. The BIU drives the RD/–WR signal high to indicate a read transaction. Since all loads retrieve 32 bits, –BE<0:3> are not used when the bus is 32–bit wide and are all driven low.

The external memory system responds with the read data on pins D< 31:0 >. It also asserts the –READY signal when the data is ready. For slow memory, the –READY signal can be delayed until data is valid.

A load double operation is treated as back–to–back reads.

Load (16–bit wide bus)

When the bus is programmed to be 16 bits wide (defined by the chip select region) every load will retrieve 32–bits. Timing 2. shows a load (Byte, half word, word) operating with an 16–bit bus. For the ldb and ldh the IU masks off the bits which are not required. For a 16–bit bus the –BE<2> pin is defined to be the ADR<1> address bit. –BE<2> as well as BE<0:1> are unused and are driven low.

Load (8–bit wide bus)

When the bus is programmed to be 8 bits wide (defined by the chip select region) every load will retrieve 32–bits. Timing 3. shows a load (Byte, half word, word) operating with an 8–bit bus. For the ldb and ldh the IU masks off the bits which are not required. For a 8–bit bus –BE<2:3> are the ADR<1:0> address bits. –BE<0:1> are unused and are driven low.

Load with Exception

If the external memory system sees a memory exception it can terminate the current memory transaction by asserting the –MEXC and –READY signals. The data on the data bus is ignored by the MB86933H.

Store

Unlike loads, stores are sized to programmed bus size and require only the minimum number of bus cycles to complete the store. For example, only two bus cycles are required to do a sth on a 8–bit bus.

Store (32–bit wide bus)

A write transaction begins with the BIU asserting –AS, to indicate a new bus transaction. The –AS signal is de–asserted after one phase. At the same time the ADR <27:2> and ASI <3:0> pins are driven with the location to be written while the D < 31:0 > pins have corresponding write data. The –BE<0:3> are the high to low order byte enables, respectively and indicate which bytes to write for a given type of store operation (byte, half–word or word). The BIU drives the RD/–WR signal low to indicate a write transaction.

The external memory system responds by asserting the –READY signal when it has stored the data. Or, if the internal wait state generator is enabled, –READY is generated internally to the MB86933H.

A store double operation is treated as back–to–back writes. (see Timing 5.)

Store (16–bit wide bus)

Stores to 16–bit memory are sized to the bus. That is, for a 16–bit bus, a store word requires two cycles while a store halfword or store byte requires a single cycle. Timing 6., 7., 8. show the timing for different types of stores. For a 16–bit bus, the –BE<2> is defined to be ADR<1>. –BE<3> is unused and is driven low. –BE<1:0> are defined to be the high and low order byte enables, respectively.

Store (8–bit wide bus)

Stores to 8–bit memory are sized to the bus. That is, for an 8–bit bus, a store word requires four cycles, a store halfword requires two cycles, and store byte requires a single cycle. Timing 9., 10., 11. show the timing for different types of stores. For a 8–bit bus, the –BE<2:3> are defined to be ADR<1:0>. –BE<1:0> are unused and are driven low.

Store with Exception

If an access exception occurs on a write, the external memory system can terminate the current memory transaction by asserting the –MEXC and –READY signals. The external memory system is expected to ignore the data on the data bus in this situation.

Atomic Load Store

An atomic load store executes as a load followed by a store with no operation allowed in between. The –LOCK signal is asserted to indicate that the bus is being used for more than one external memory operation.

There is one cycle between the termination of the read and the beginning of the write to provide time for the switching of the data bus drivers.

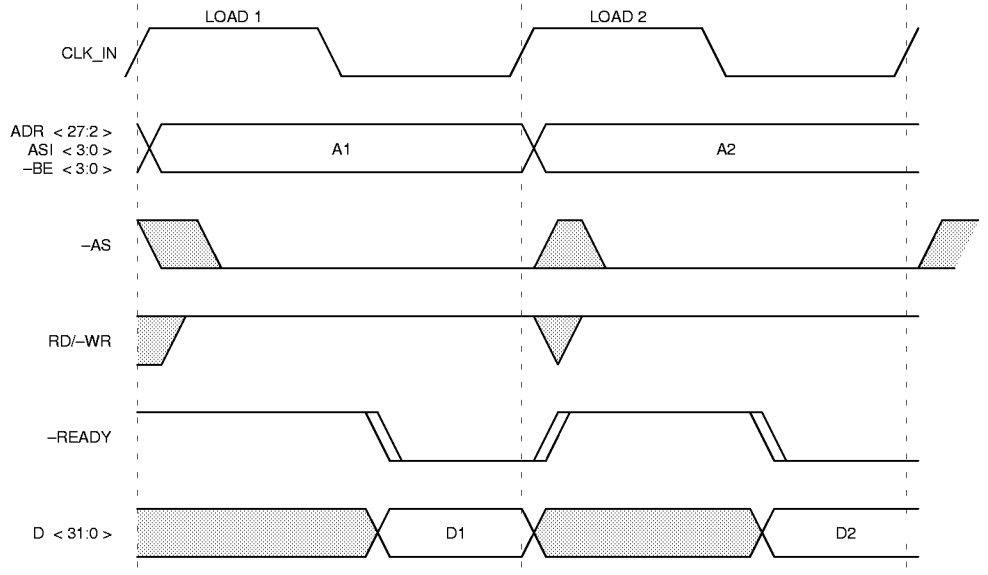
DRAM Bus Timings

During a DRAM access the row and column address,are output on ADR<27:16> pins. Timing diagram 14 shows 2 back–to–back DRAM reads which are not in the same page. Timing 15 shows a DRAM write followed by a DRAM read, again not in the same page. Timing 16 shows both samepage reads and writes. Note that the BIU always inserts an idle cycle in between a read and a write. Timing 17 shows a read followed by a refresh. The on–chip timer is used as a refresh counter.

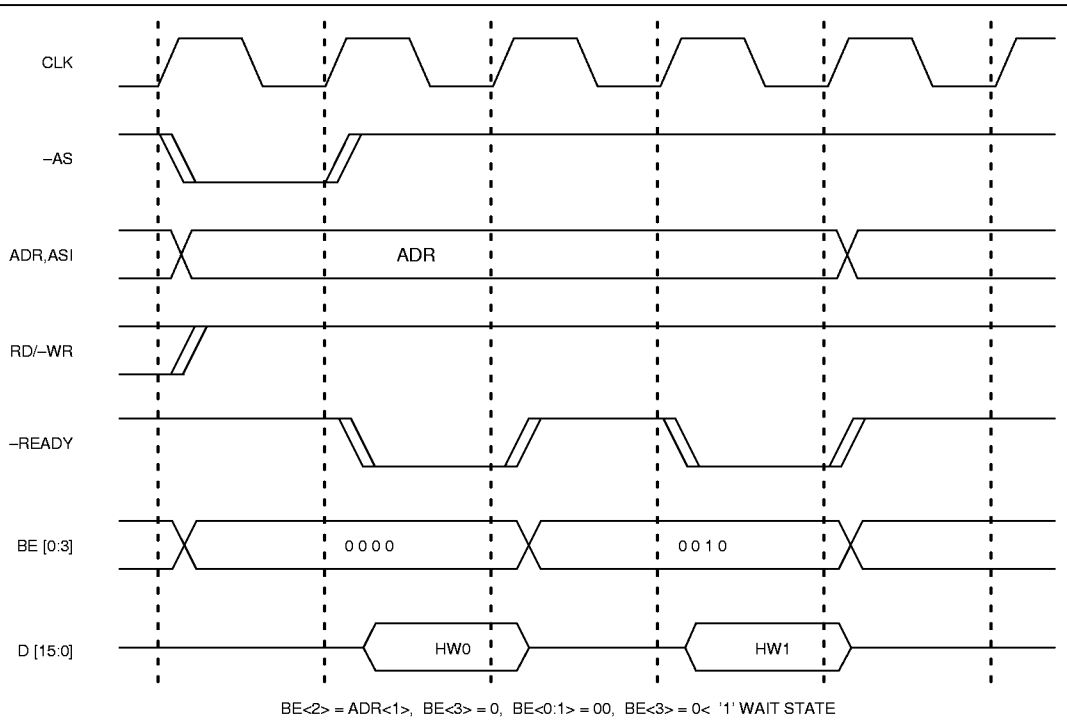
External Bus Request and Grant

Any external device can request ownership of the bus by asserting the –BREQ signal. The BIU asserts the –BGRNT signal to indicate that it is relinquishing control of the bus and also three–states all of its bus drivers. In the following cycle, the external device can complete its transaction. On completion of its transaction the external device de–asserts the –BREQ signal. The BIU responds by de–asserting the –BGRNT signal in the following cycle.

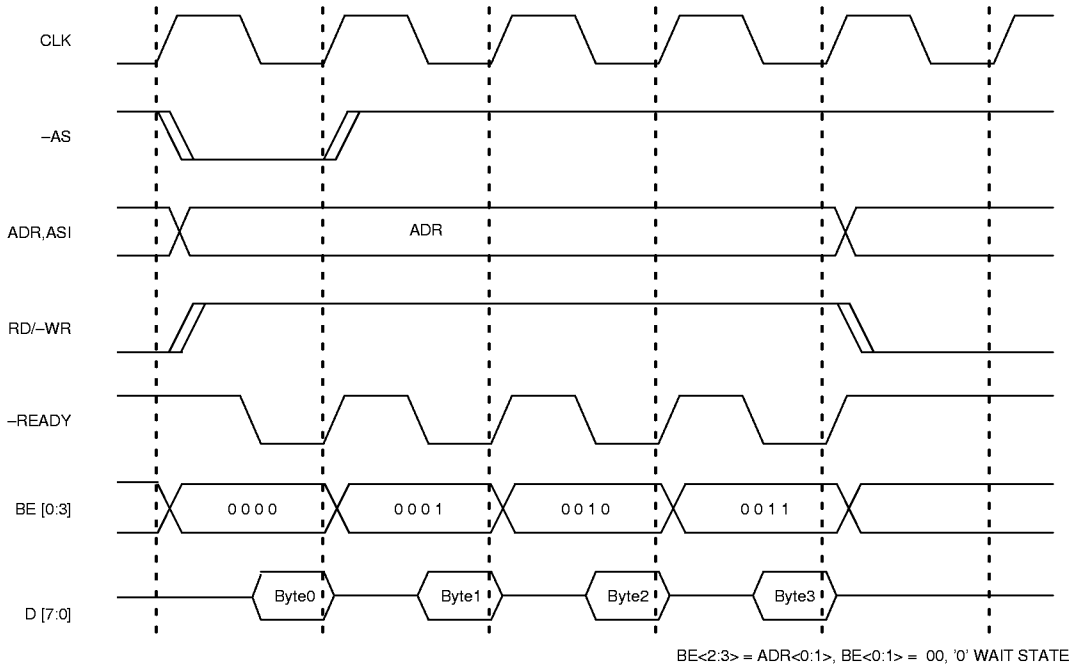
The MB86933H is the default owner of the bus.



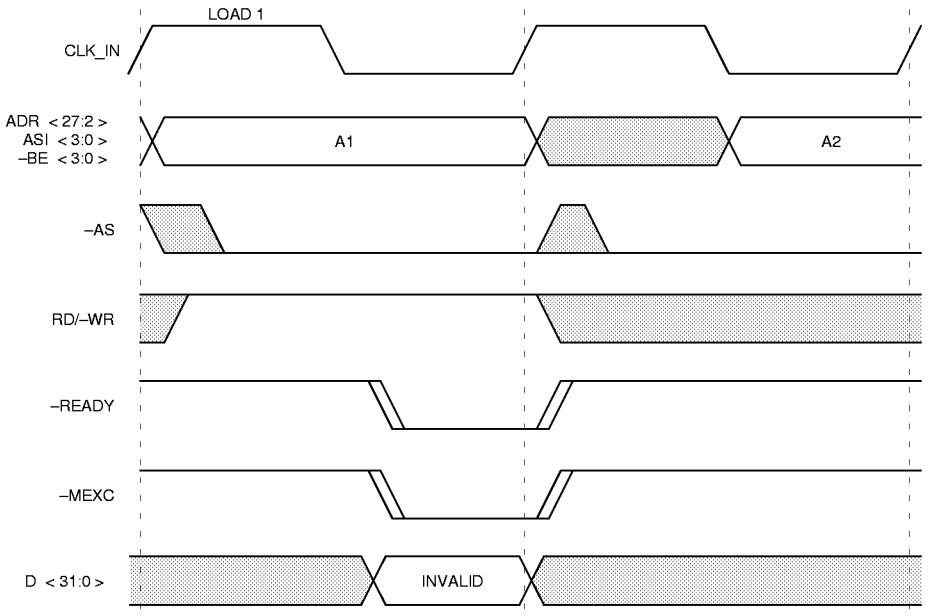
Timing 1. Typical Back–to–Back Loads with 32–Bit Wide Bus (Same as Load Double)



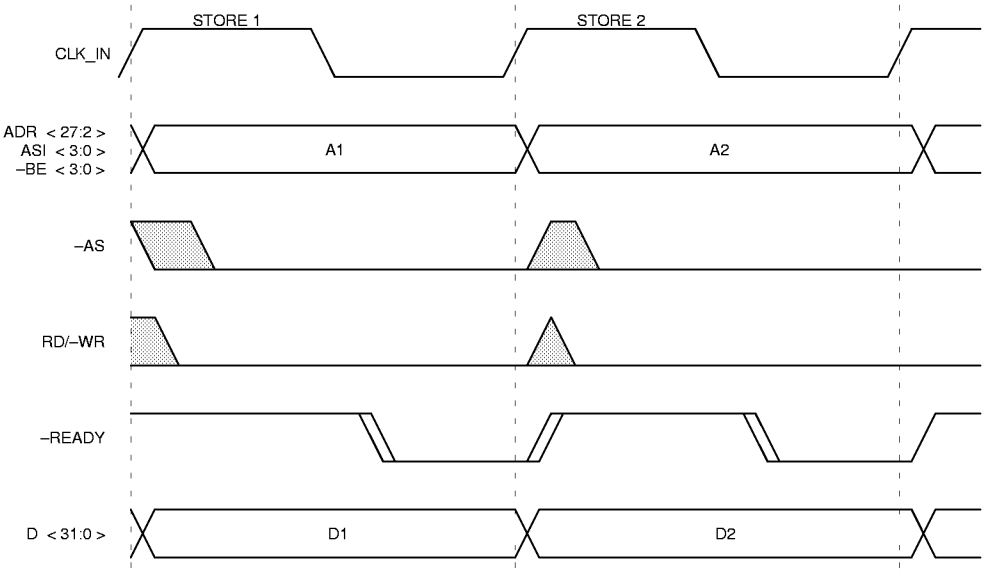
Timing 2. Load with 16–Bit Wide Bus



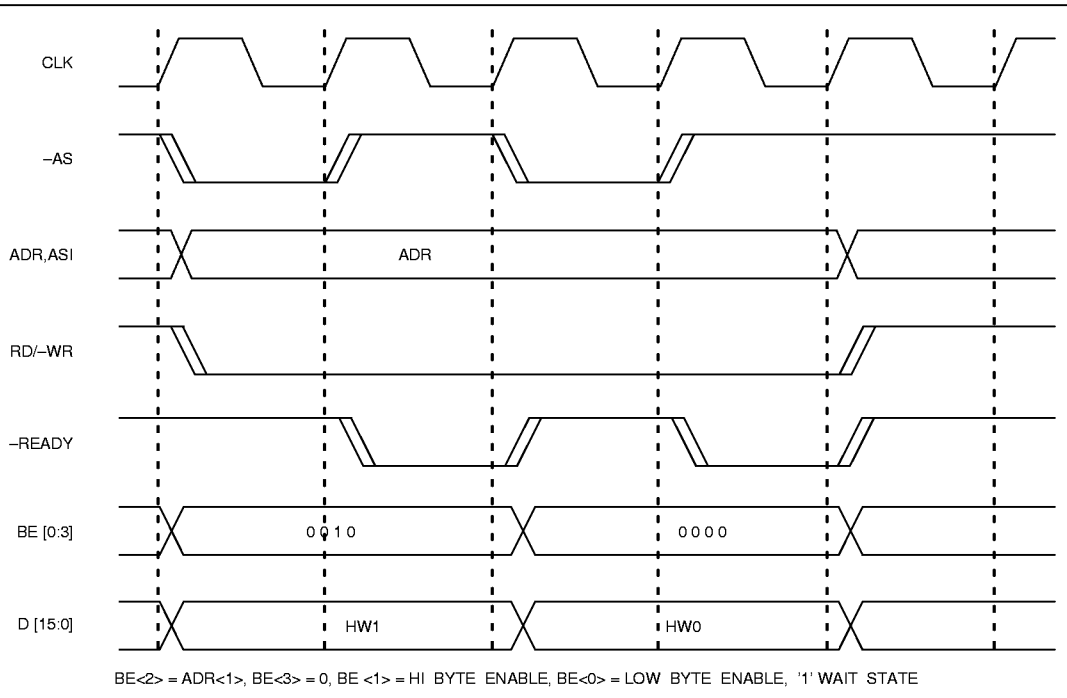
Timing 3. Load with 8–Bit Wide Bus



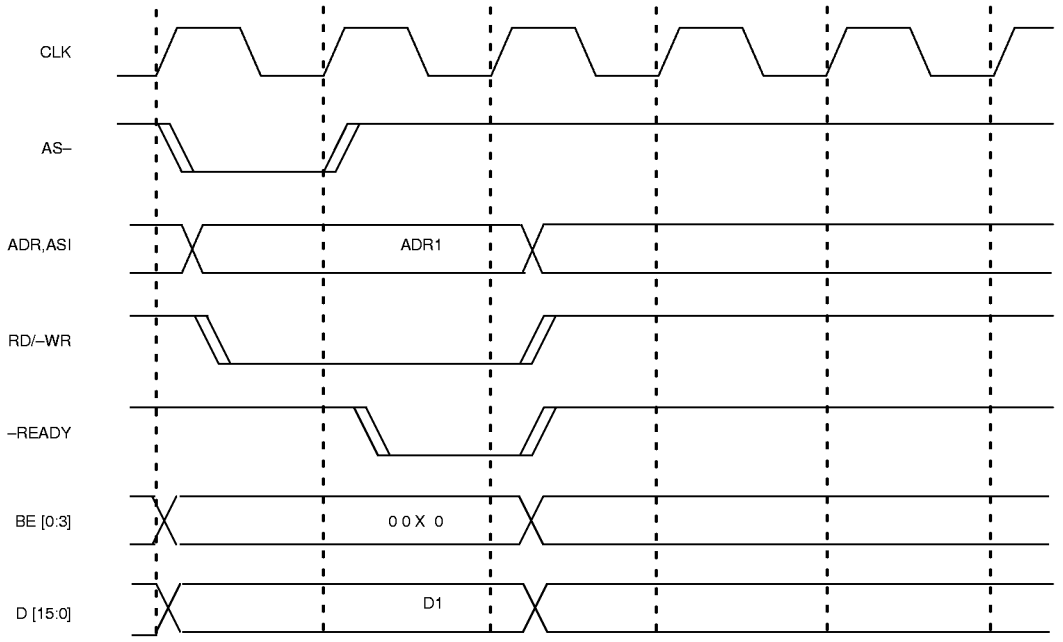
Timing 4. Load with Exception – 32–Bit Wide Bus



Timing 5. Typical Back–to–Back Stores – 32–Bit Wide Bus (Same as Store Double)

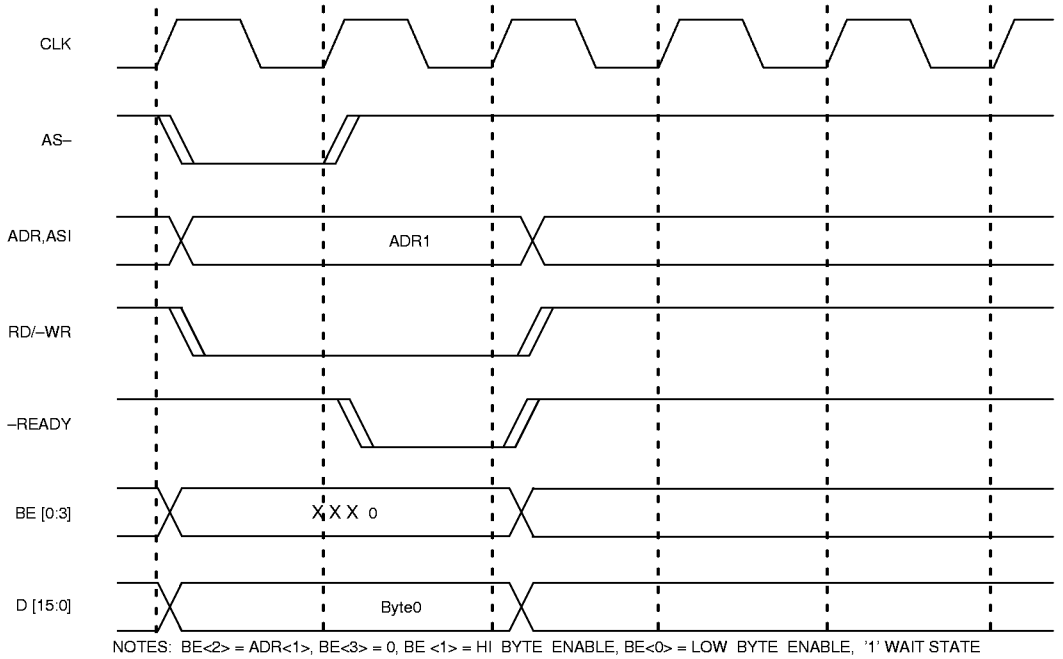


Timing 6. Store Word with 16–Bit Bus



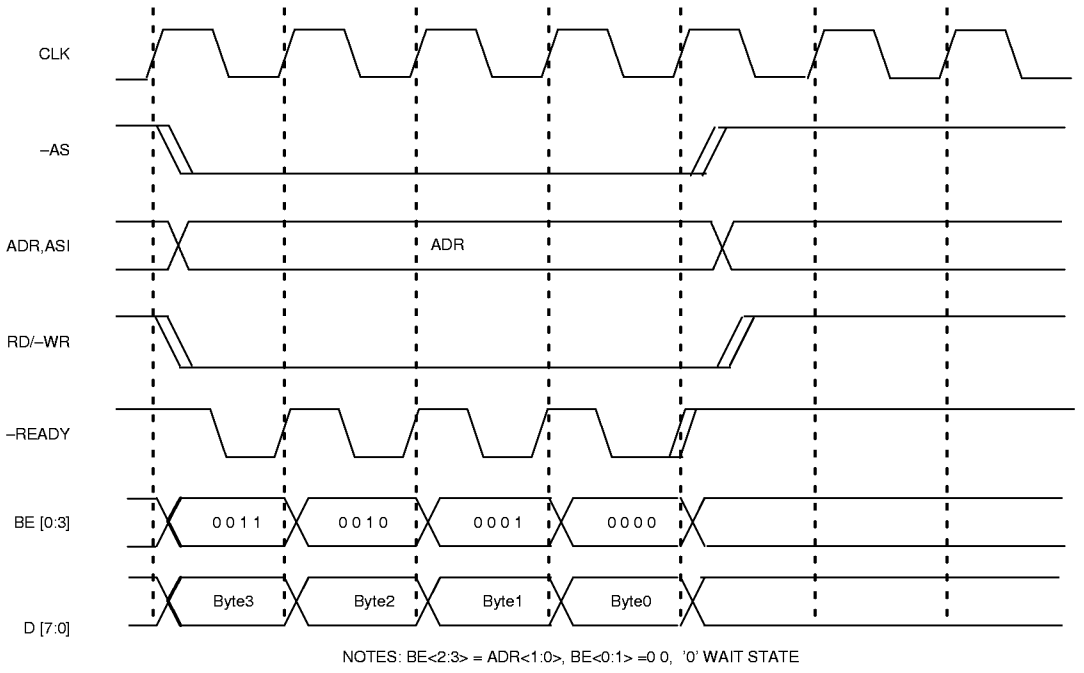
NOTES: BE<2> = ADR<1>, BE<3> = 0, BE <1> = HI BYTE ENABLE, BE<0> = LOW BYTE ENABLE, '1' WAIT STATE

Timing 7. Store Half Word with 16–Bit Bus



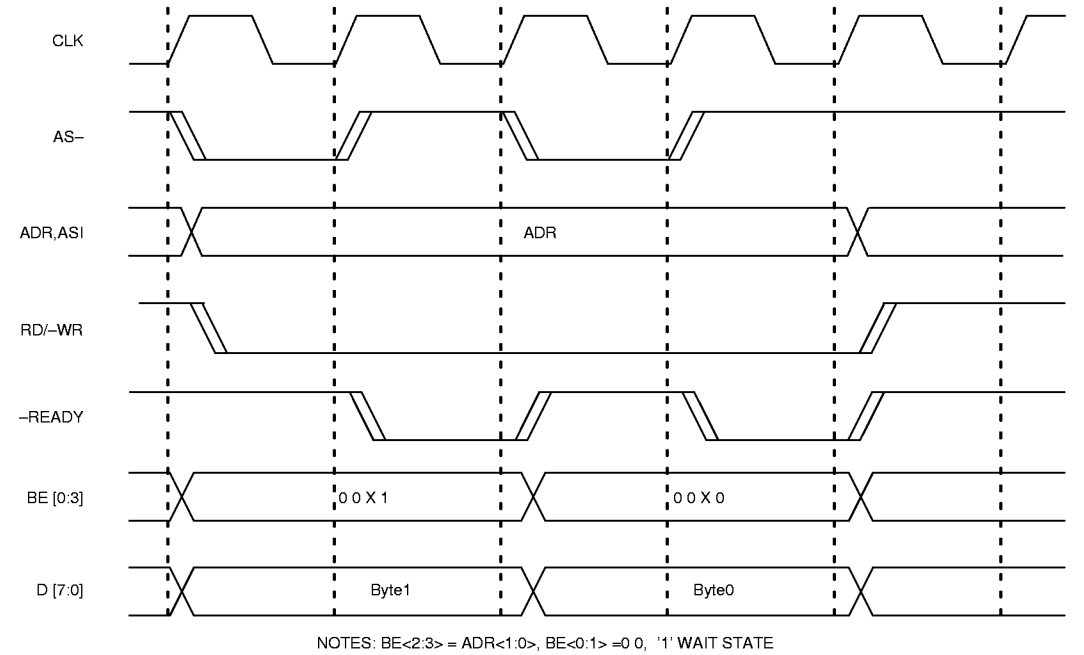
NOTES: BE<2> = ADR<1>, BE<3> = 0, BE <1> = HI BYTE ENABLE, BE<0> = LOW BYTE ENABLE, '1' WAIT STATE

Timing 8. Store Byte with 16–Bit Bus



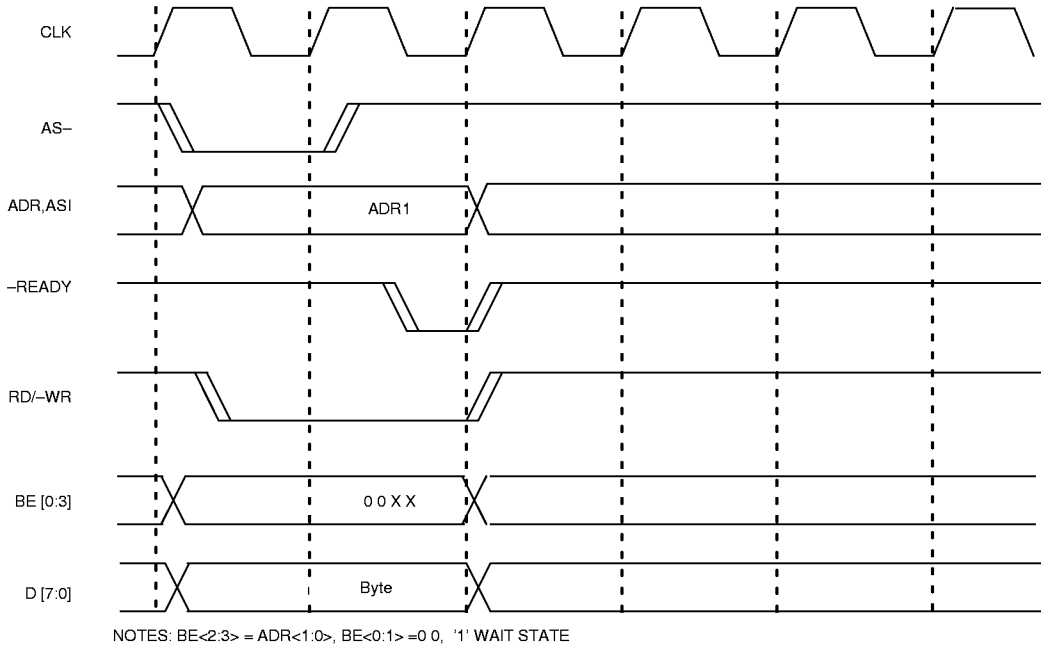
NOTES: BE<2:3> = ADR<1:0>, BE<0:1> =0 0, '0' WAIT STATE

Timing 9. Store Word with 8–Bit Bus

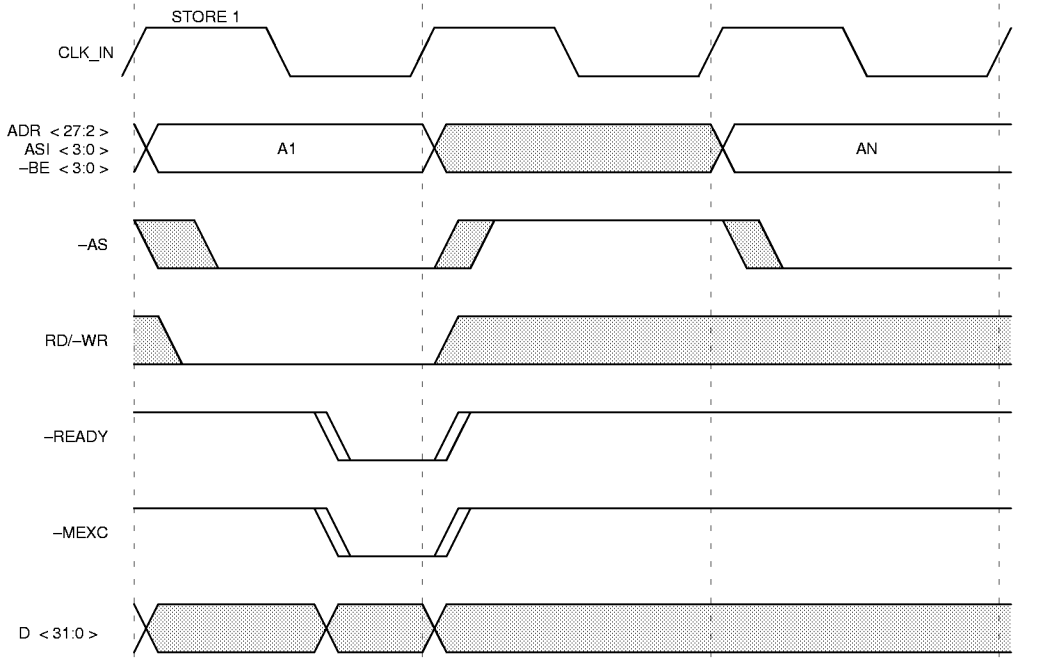


NOTES: BE<2:3> = ADR<1:0>, BE<0:1> =0 0, '1' WAIT STATE

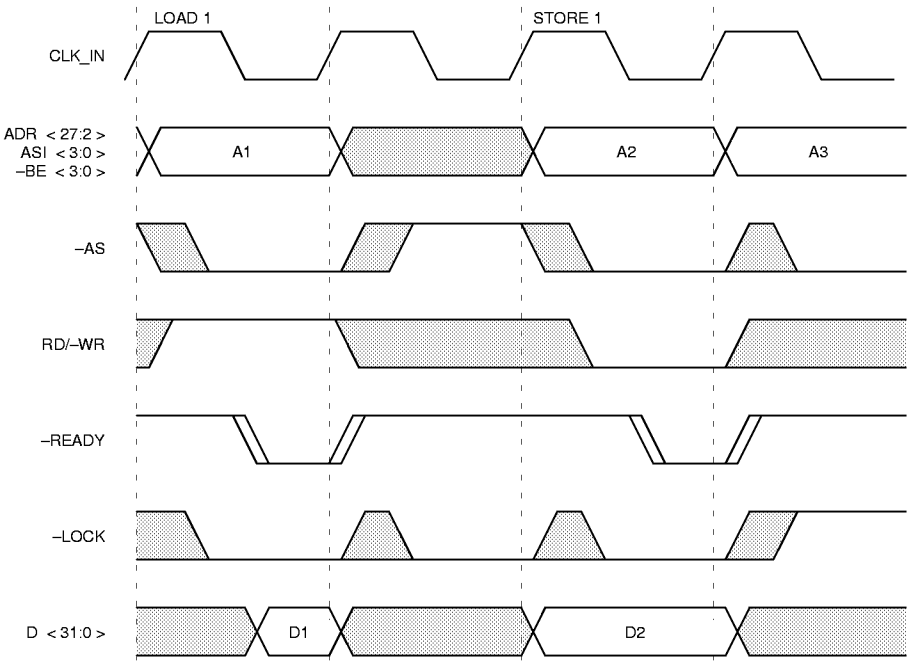
Timing 10. Store Half–Word with 8–Bit Bus



Timing 11. Store Byte with 8–Bit Bus

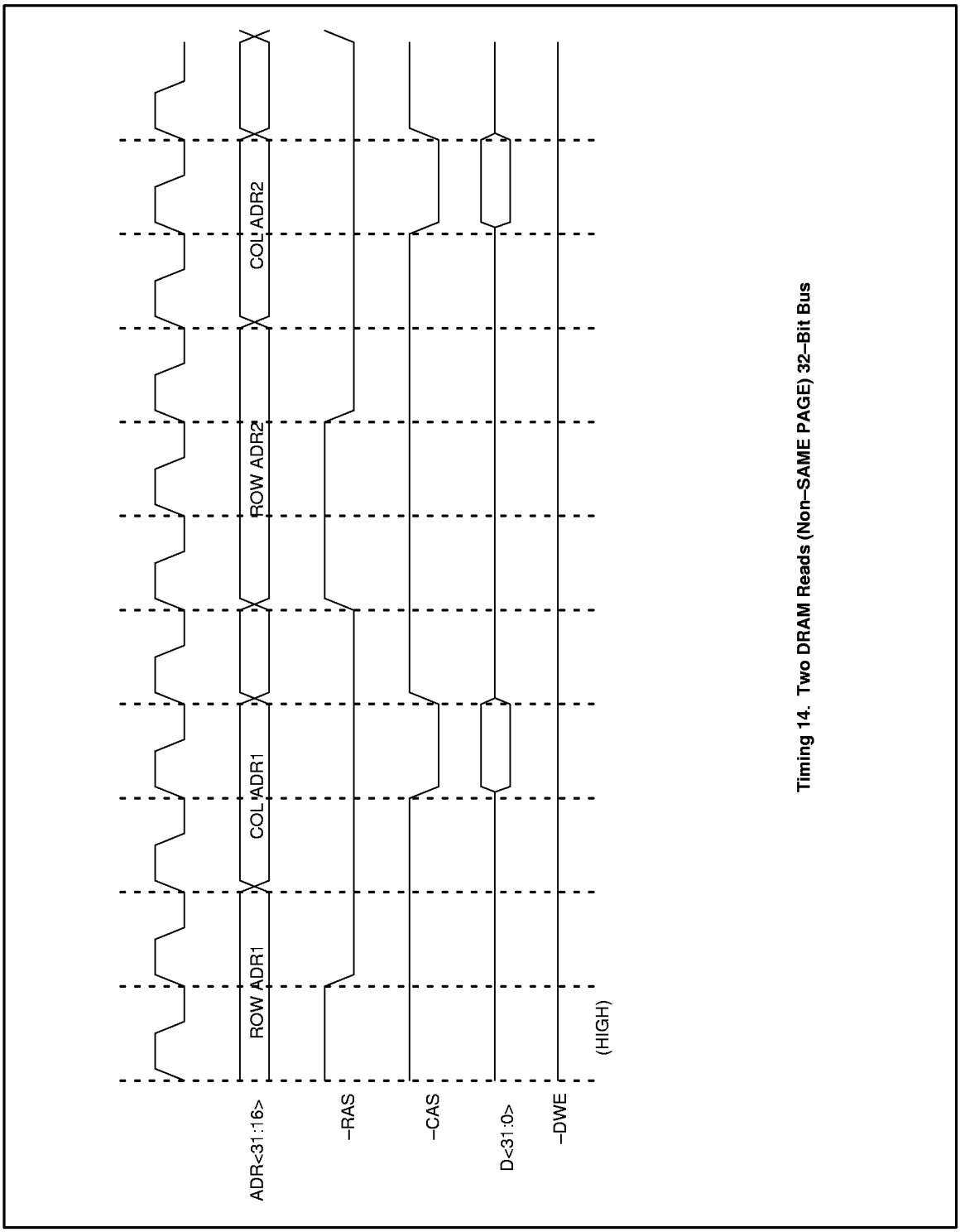


Timing 12. Store with Exception

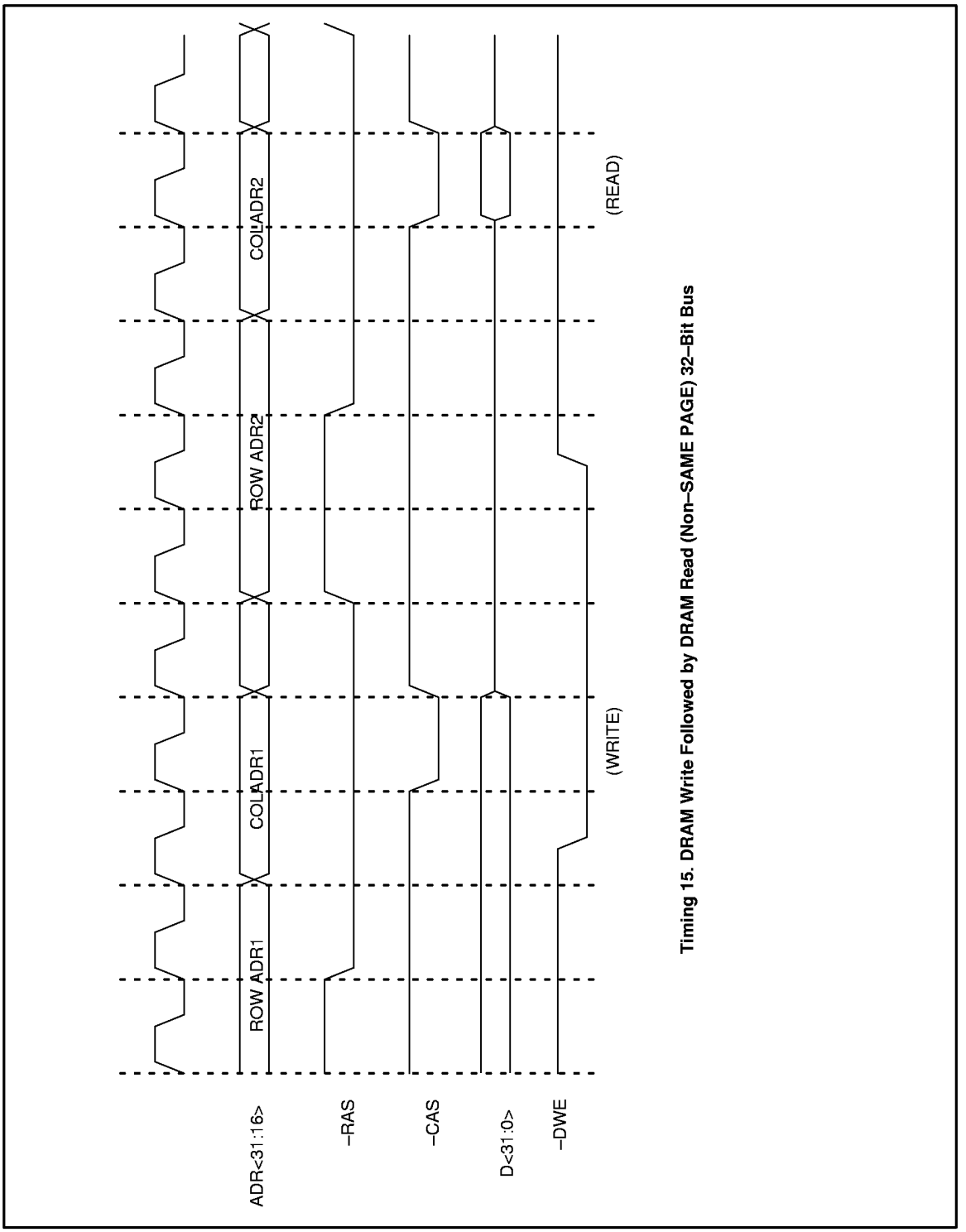


Note: A load followed by a store requires an intervening clock cycle on the bus while a store followed by a load can occur in consecutive clock cycles.

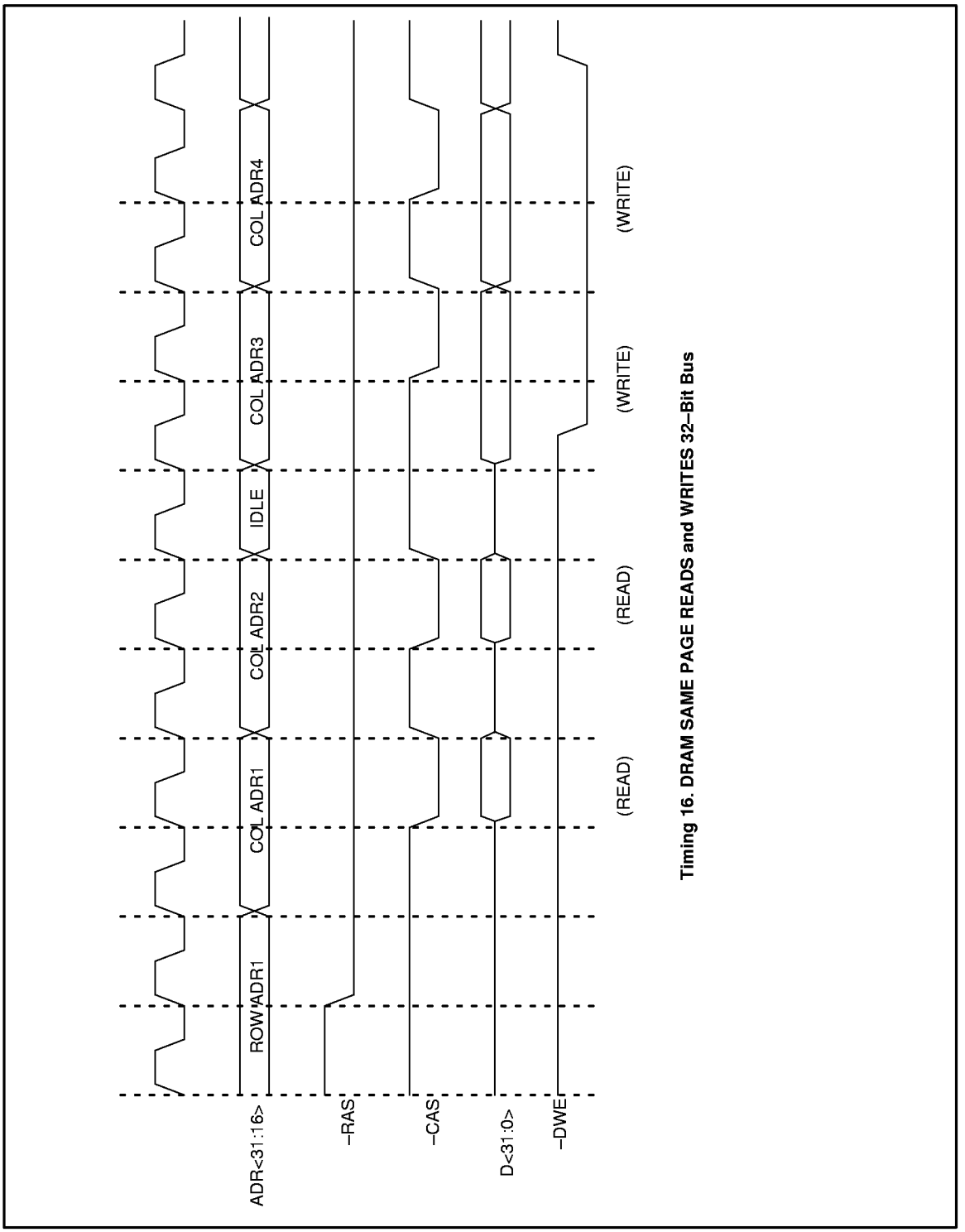
Timing 13. Atomic Operation



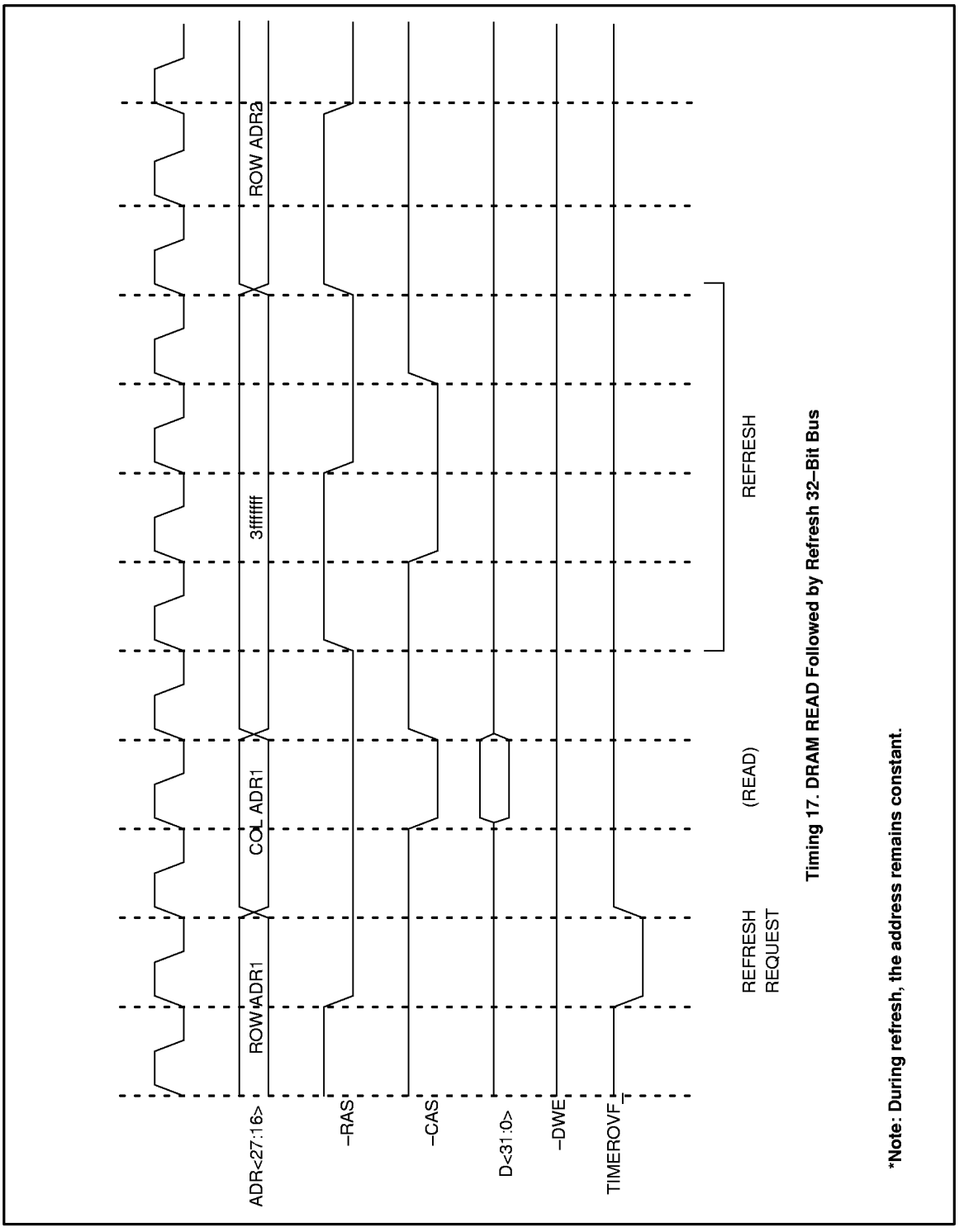
Timing 14. Two DRAM Reads (Non–SAME PAGE) 32–Bit Bus



Timing 15. DRAM Write Followed by DRAM Read (Non–SAME PAGE) 32–Bit Bus

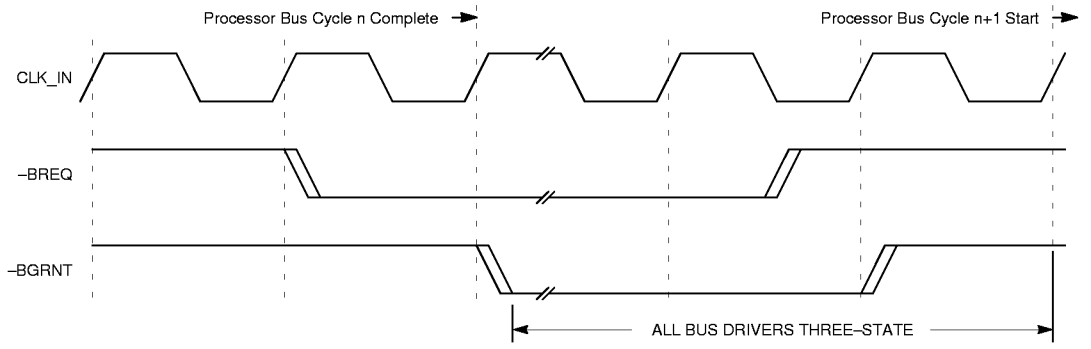


Timing 16. DRAM SAME PAGE READS and WRITES 32−Bit Bus



Timing 17. DRAM READ Followed by Refresh 32–Bit Bus

***Note: During refresh, the address remains constant.**



Timing 18. Bus Request and Grant Cycle

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Conditions	Min.	Max.	Units
V_{CC}	Supply voltage		–0.3	6	V
V_I	Input voltage		–0.3	V_{CC} + 0.3	V
T_J	Operating junction temperature			125	°C

Notes:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operation section of this specification is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods may affect device reliability.

Recommended Connections:

1. Power and ground connections must be made to multiple V_{CC} and V_{SS} pins. Every MB86933H based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "N.C." must not be connected in the system.
2. Liberal decoupling capacitance should be placed near the MB86933H. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.
3. Low inductance capacitors and interconnections are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA and QFP packages will offer the lowest possible inductance.
4. For reliable operation, alternate bus masters must drive any pins that are three–stated by the MB86933H when it has granted the bus, in particular –LOCK, ADR < 27:2 >, ASI < 3:0 >, –BE0–3, D < 31:0 >, –AS, and RD/–WR must be driven by alternate bus master. These pins are normally driven by the processor during active and idle bus states and don't require external pullups. N.C. pins must always remain unconnected.

PACKAGE THERMAL CHARACTERISTICS[2]

Symbol	Parameter	Package	Value			Units
$\varnothing_{JC}$	Thermal resistance junction to case	160 Plastic QFP	5.0			°C/W
			0 m/s	1 m/s	3 m/s	
$\varnothing_{JA}$	Thermal resistance junction to ambient	160 Plastic QFP	57	47	37	°C/W

DC SPECIFICATIONS[3] V_{CC} = 5V ± 5%

Symbol	Parameter	Conditions	Freq.	Min.	Typ.	Max.	Units
V_{IL}	Input low voltage		–	0	–	0.8	V
V_{IH}	Input high voltage (All pins except XTAL1)		–	2.0	–	V_{CC}	V
	Input high voltage (Pin XTAL1)		–	2.8	–	V_{CC}	V
V_{OL}	Output low voltage	I_{OL} = 3.2mA	–	0	–	0.45	V
V_{OH}	Output high voltage	I_{OH} = –0.4mA	–	2.4	–	V_{CC}	V
I_{LI}	Input leakage current	V_{IN} = 0 or V_{CC}	–	–10	–	10	µA
I_{LZ}	3–state output leakage current	V_{OUT} = 0 or V_{CC}	–	–10	–	10	µA
I_{CC} *1	Operating power supply current		25 MHz	–	289	327	mA
C_{PIN}	Pin capacitance (All pins except XTAL2)	V_{CC} = V_I = 0 f = 1 MHz	–	–	–	13	pF
	Pin capacitance (Pin XTAL2)		–	–	–	16	pF

*1 Note: Use I_{CC} (typ) values to calculate maximum case and ambient temperature allowed. Note that maximum junction temperature of die is 125°C. For example, Allowed ambient temp = 125°C.– (I_{CC}) • (5.25V) • $\varnothing_{JA}$

*2 Note: All numbers for package thermal characteristics assume multilayer PCB. A multilayer board is defined as a PC Board with at least 4 metal routing layers.

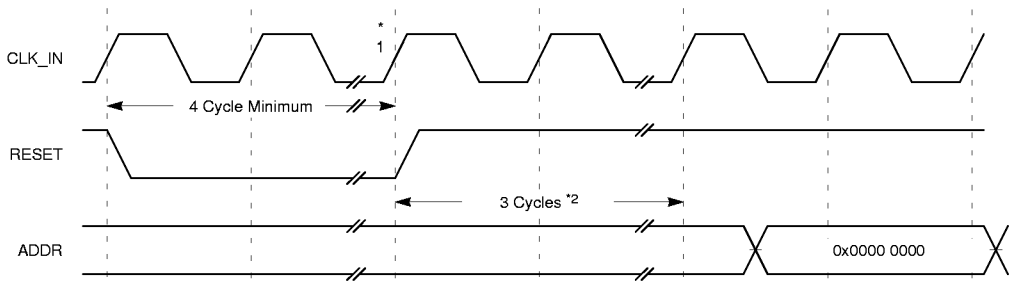
AC CHARACTERISTICS[1,2,4,5] V_{CC} = 5V ± 5%

Symbol	Parameter Description		MHz		Units
			Min.	Max.	
t1	CLKIN period		40	100	ns
t2	CLKIN high time		10		ns
t3	CLKIN low time		14		ns
t4	CLKIN rise time			4	ns
t5	CLKIN fall time			4	ns
t6	CLKIN to CLKOUT1		0	8	ns
t7	CLKIN to CLKOUT2 delay		25	33	ns
t8	CLKOUT1, CLKOUT2 high time		0.35xPeriod		ns
t9	CLKOUT1, CLKOUT2 low time		0.4xPeriod		ns
t10	CLKOUT1, CLKOUT2 fall time			3	ns
t11	CLKOUT1, CLKOUT2 rise time			4	ns
t12	D < 31:0 >	Output valid delay		23.5	ns
		Output hold	2		
	ADR < 27:2 >	Output valid delay		22	ns
		Output hold	2		
	ADR < 27:2 > [DRAMC]	Output valid delay		26	ns
		Output hold	2		
	–BE0–3	Output valid delay		24	ns
		Output hold	2		
	–BE0–3 8/16–bit mode	Output valid delay		28	ns
		Output hold	2		
	ASI < 3:0 >	Output valid delay		23.5	ns
		Output hold	2		
t13	–CS	Output valid delay		24	ns
		Output hold	2		
t14	–SAME_PAGE	Output valid delay		23	ns
		Output hold	2		
t15	RD/–WR	Output valid delay		18	ns
		Output hold	2		
t16	–LOCK	Output valid delay		19	ns
		Output hold	2		
t17	–AS	Output valid delay		20	ns
		Output hold	2		
t18	–TIMER_OVF	Output valid delay		20	ns
		Output hold	2		
t19	–BGRNT	Output valid delay		20	ns
		Output hold	2		

AC CHARACTERISTICS[1,2,4] V_{CC} = 5V ± 5%

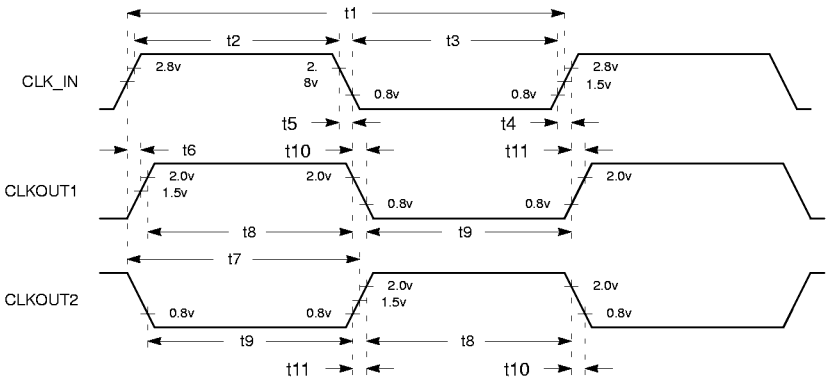
Symbol	Parameter Description		MHz		Units
			Min.	Max.	
t20	ERROR	Output valid delay		22	ns
		Output hold	2		
t21	–RAS	Output valid delay		13	ns
		Output hold	2		
t22	–CAS	Output valid delay		13	ns
		Output hold	2		
t23	–DWE	Output valid delay		32.5	ns
		Output hold	2		
t24	–MEXC input setup time		14		ns
	–MEXC input setup time [8/16–bit mode]		20		ns
t25	–READY input setup time		14		ns
	–READY input setup time [8/16–bit mode]		20		ns
t26	D < 31:0 > input setup time		11		ns
t27	–BREQ input setup time		10		ns
t28	IRL input setup time		16		ns
t29	IRL input hold time		2		ns
t30	–MEXC input hold time		2		ns
t31	–READY input hold time		2		ns
t32	D < 31:0 > input hold time		2		ns
t33	–BREQ input hold time		2		ns

1. Parameters are valid over specified temperature range and supply voltage range unless otherwise noted.
2. All voltage measurements are referenced to ground. All time measurements are referenced at input and output levels of 1.5V. For testing, all inputs swing between 0.4V and 2.4V (Except XTAL1 which swings from 0.4V to 3.0V). Input rise and fall times are 2ns or less.
3. Not more than one output may be shorted at a time for a maximum duration of one second.
4. Timing specifications apply to frequency of operation listed at top of column.
5. All output timings are based on a 50pF load.
7. These specs will be improved in the future.
8. Data bus output driver control is same as for RD/–WR so timing is similar.



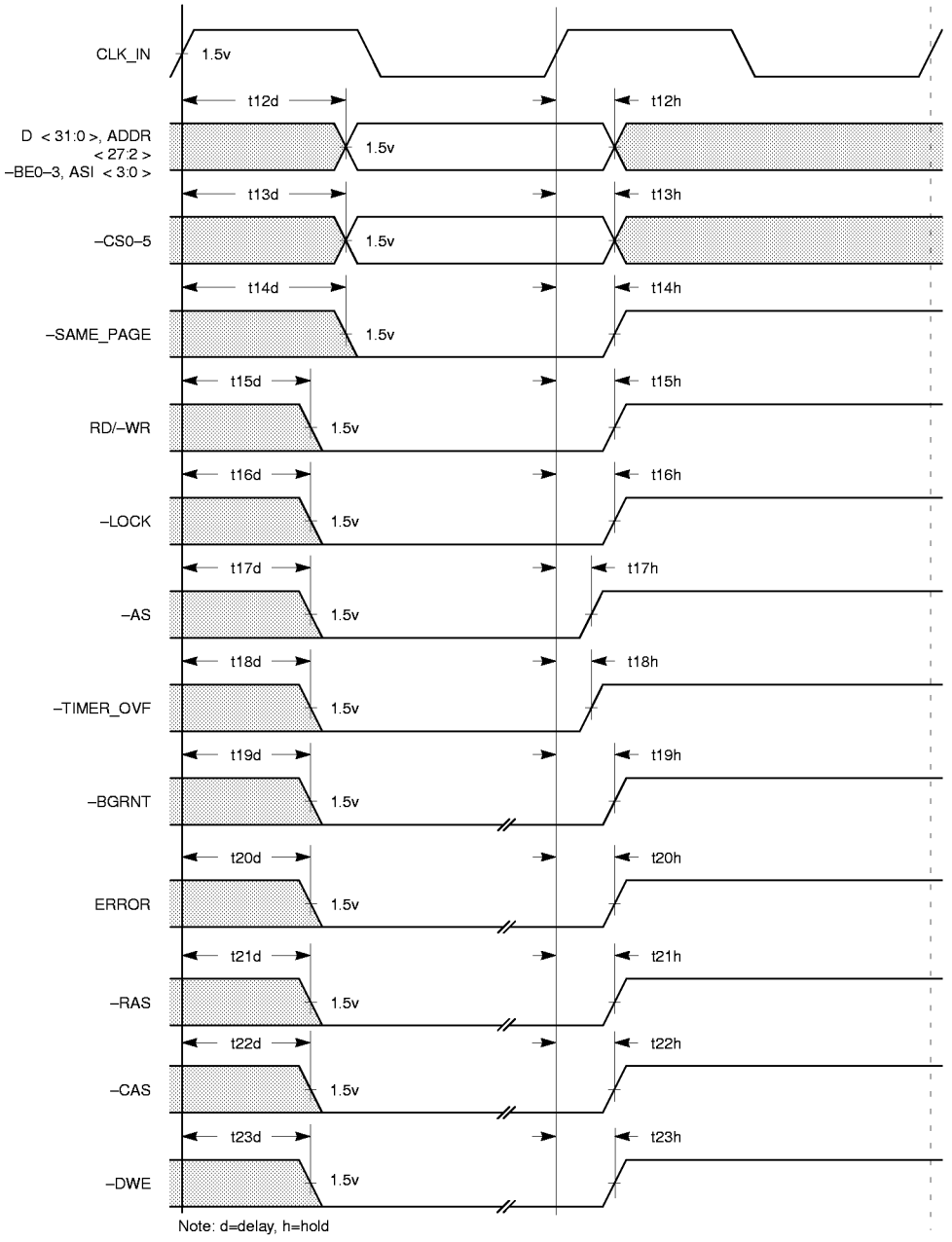
*1. CLK_IN must be stable for at least 100µs before RESET is de–asserted.
*2. When RESET hold time (3ns) is met.

Timing 19. Reset Timing

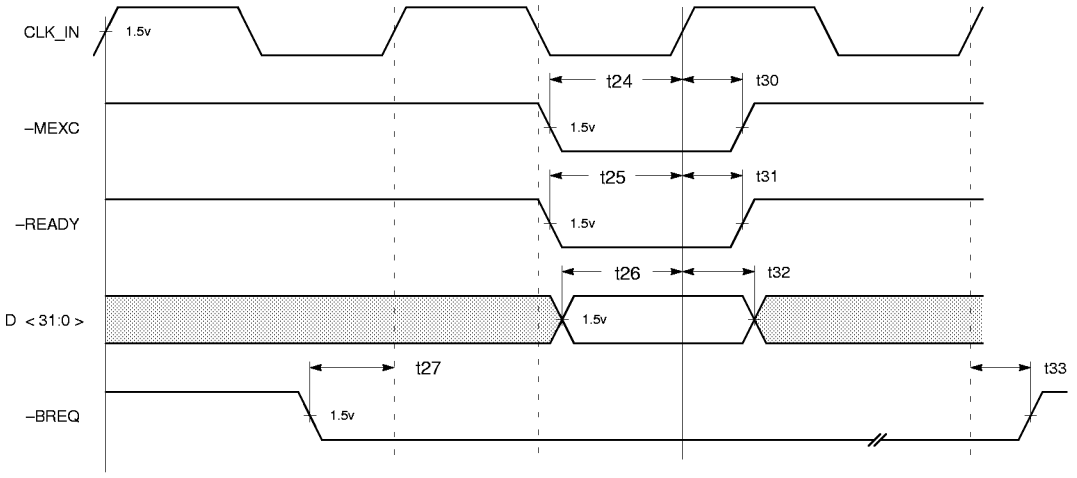


Note: CLKOUT1 and CLKOUT2 are derived from non–overlapping internal clocks, however, the relative timing of these signals is not tested.

Timing 20. Clock Timing

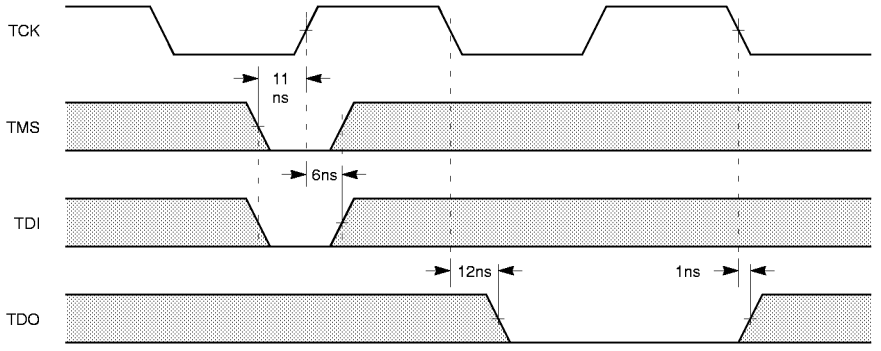


Timing 21. I/O Output Timing



NOTE: d=delay, h=hold

Timing 22. I/O Output Timing



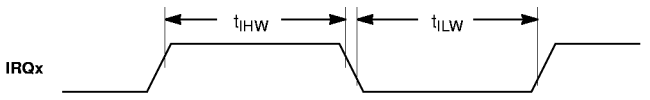
NOTE: These specifications are based on sample characterization and should be considered as typical values.

Timing 23. JTAG Timing

Interrupt Signal, Interrupt Input Width

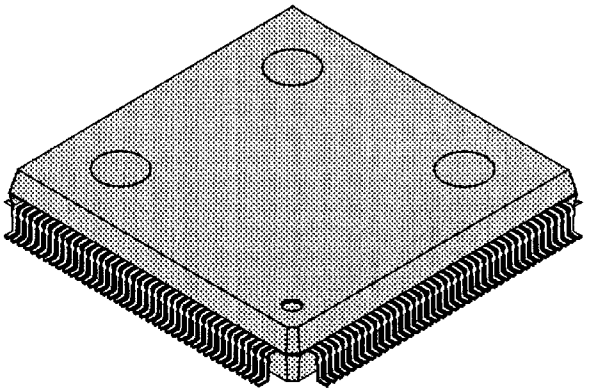
Symbol	Description	MHz		Unit
		Min.	Max.	
T_{IHW}	IRQ input High level duration [1]	3 t_{CLK}+10	–	ns
T_{ILW}	IRQ input Low level duration [2]	3 t_{CLK}+10	–	ns

1. In HIGH Level or RISING–EDGE trigger mode, if this width is satisfied, the interrupt request FLIP–FLOP is set.
2. In LOW Level or FALLING–EDGE trigger mode, if this width is satisfied, the interrupt request FLIP–FLOP is set.



Timing 24. Interrupt Request Timing Diagram

160-LEAD QUAD FLAT PACK (QFP)



Ordering Info.: MB86933H–25PF–G–B

160-LEAD QUAD FLAT PACK (QFP)