19-3118; Rev 1; 6/04

MAXIM

3.2Gbps SFP VCSEL Driver with Diagnostic Monitors

General Description

The MAX3740A is a high-speed VCSEL driver for small-form-factor (SFF) and small-form-factor pluggable (SFP) fiber optic LAN transmitters. It contains a bias generator, a laser modulator, and comprehensive safety features. The automatic power control (APC) adjusts the laser bias current to maintain average optical power over changes in temperature and laser properties. The driver accommodates common cathode and differential configurations.

The MAX3740A operates up to 3.2Gbps. It can switch up to 15mA of laser modulation current and source up to 15mA of bias current. Adjustable temperature compensation is provided to keep the optical extinction ratio within specifications over the operating temperature range. The MAX3740A interfaces with the Dallas DS1858 to meet SFF-8472 timing and diagnostic requirements. The MAX3740A accommodates various VCSEL packages, including low-cost TO-46 headers.

The MAX3740A safety circuit detects faults that could cause hazardous light levels and disables the VCSEL output. The safety circuits are compliant with SFF and SFP multisource agreements (MSA).

The MAX3740A is available in a compact 4mm x 4mm, 24-pin thin QFN package and operates over the -40°C to +85°C temperature range.

Applications

Multirate (1Gbps to 3.2Gbps) SFP/SFF Modules

Gigabit Ethernet Optical Transmitters

Fibre Channel Optical Transmitters

Infiniband Optical Transmitters

Features

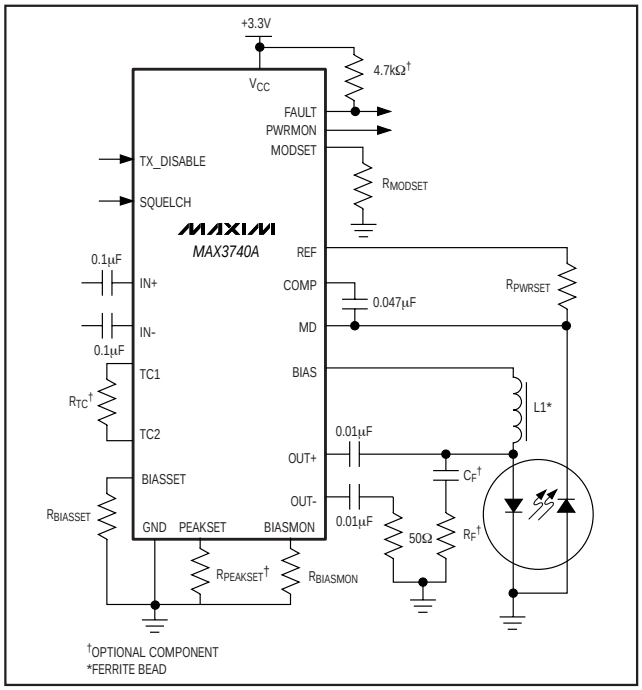
- **Supports all SFF-8472 Digital Diagnostics**
- **2mA to 15mA Modulation Current**
- **1mA to 15mA Bias Current**
- **Optional Peaking Current to Improve VCSEL Edge Speed**
- **Supports Common Cathode and Differential Configuration**
- **Automatic Power Control**
- **Safety Circuits Compliant with SFF and SFP MSAs**
- **4mm × 4mm 24-Pin Thin QFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX3740AETG	-40°C to +85°C	24 Thin QFN (4mm x 4mm)
MAX3740AETG+	-40°C to +85°C	24 Thin QFN (4mm x 4mm)

+Denotes lead-free package.

Typical Application Circuit



3.2Gbps SFP VCSEL Driver with Diagnostic Monitors

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) .....-0.5V to 6.0V
Voltage at TX_DISABLE, IN+, IN-, FAULT, SQUELCH TC1, TC2, MODSET, PEAKSET, BIASSET, BIAS, BIASMON, COMP, MD, REF, PWRMON .....-0.5V to (V_{CC} + 0.5V)
Voltage at OUT+, OUT-.....(V_{CC} - 2V) to (V_{CC} + 2V)
Current into FAULT ..... -1mA to +25mA
Current into OUT+, OUT-.....60mA

Continuous Power Dissipation (T_A = +85°C)
24-Lead Thin QFN
(derate 20.8mW/°C above +85°C).....1354mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-55°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, TC1 and TC2 are shorted, PEAKSET open, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{CC}	SQUELCH set low, TX_DISABLE set low, peaking is not used (Note 1)	I_{MOD} = 2mA$_{P-P}$		32		mA
			I_{MOD} = 15mA$_{P-P}$		55	68	
		Additional current when peaking is used (Note 2)			15	20	
		Additional current when SQUELCH is high			5	10	
	$I_{CC-SHDN}$	Total current when TX_DISABLE is high			3.9	5	
FAULT OUTPUT							
Output High Voltage	V_{OH}	R_{LOAD} = 10kΩ to 2.97V		2.4			V
Output Low Voltage	V_{OL}	R_{LOAD} = 4.7kΩ to 3.63V				0.4	V
TX_DISABLE INPUT							
Input Impedance				4.7		10.0	kΩ
Input High Voltage	V_{IH}			2.0			V
Input Low Voltage	V_{IL}					0.8	V
Power-Down Time		The time for I_{CC} to reach $I_{CC-SHDN}$ when TX_DISABLE transitions high			50		µs
SQUELCH							
Squelch Threshold				25		85	mV$_{P-P}$
Squelch Hysteresis				10			mV$_{P-P}$
Time to Squelch Data		(Note 3)		0.02		5.00	µs
Time to Resume from Squelch		(Note 3)		0.02		5.00	µs
BIAS GENERATOR (Note 4)							
Bias Current	I_{BIAS}	Minimum				1	mA
		Maximum		15			
Accuracy of Programmed Bias Current	ΔBIAS	5mA ≤ I_{BIAS} ≤ 15mA		-8		+8	%
		1mA ≤ I_{BIAS} ≤ 5mA		-12		+12	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, TC1 and TC2 are shorted, PEAKSET open, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bias Current During Fault	I_{BIAS_OFF}	Current out of the BIAS pin		1.5	10	µA
BIASMON Gain		1mA < I_{BIAS} < 3mA	0.0875	0.105	0.1375	mA/mA
		3mA ≤ I_{BIAS} ≤ 15mA	0.085	0.105	0.125	
BIASMON Stability		(Notes 5,6)	-10		+10	%
AUTOMATIC POWER CONTROL (APC)						
MD Nominal Voltage	V_{MD}	APC loop is closed	1	V_{REF} - 0.2	2	V
Voltage at REF	V_{REF}		1.2	1.8	2.2	V
MD Voltage During Fault				0		V
MD Input Current		Normal operation (FAULT = low)	-2	0.7	+2	µA
APC Time Constant		C_{COMP} = 0.047µF (Note 6)	5	20		µs
PWRMON Nominal Gain		V_{PWRMON} / (V_{REF} - V_{MD})	1.85	2.15	2.45	V/V
LASER MODULATOR (Note 7)						
Data Input Voltage Swing	V_{ID}	Minimum			250	mV_{P-P}
		Maximum	2200			
Output Resistance		Single-ended resistance at OUT+		80	105	Ω
		Single-ended resistance at OUT-		72	100	
Modulation Current	I_{MOD}	Minimum			2	mA_{P-P}
		Maximum	15			
Minimum Peaking Current Range				0.2		mA
Maximum Peaking Current Range				2		mA
Peaking Current Duration				80		ps
Tolerance of Programmed Modulation Current		TC1 is shorted to TC2	-10		+10	%
Minimum Programmable Temperature Coefficient				0		ppm/°C
Maximum Programmable Temperature Coefficient		Temperature range 0°C to +70°C		+5000		ppm/°C
Modulation Transition Time	t_R, t_F	5mA ≤ I_{MOD} ≤ 15mA, 20% to 80% (Note 6)		65	95	ps
Deterministic Jitter	DJ	5mA ≤ I_{MOD} ≤ 15mA, 3.2Gbps (Notes 6, 8)		12	20	ps_{P-P}
Random Jitter	RJ	(Note 6)		1.3	4	ps_{RMS}
Laser Modulation During Fault or while Squelch is Active	I_{MOD_OFF}			15	50	$µA_{P-P}$
Input Resistance		Differential resistance	85	100	115	Ω
Input Bias Voltage	V_{IN}			V_{CC} - 0.3		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +2.97V to +3.63V, T_A = -40°C to +85°C. Typical values are at V_{CC} = +3.3V, TC1 and TC2 are shorted, PEAKSET open, T_A = +25°C, unless otherwise noted.)

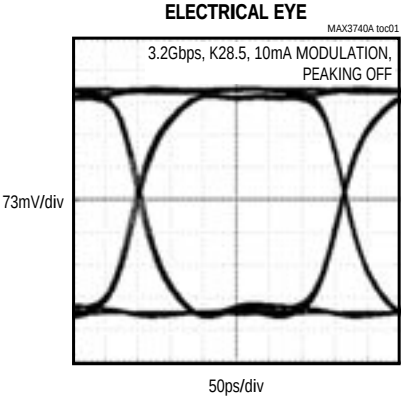
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SAFETY FEATURES (see the *Typical Operating Characteristics* section)						
High-Current Fault Threshold	V_{BMTH}	$V_{BIASMON}$ > V_{BMTH} causes a fault	0.7	0.8	0.9	V
V_{BIAS} Fault Threshold	V_{BTH}	V_{BIAS} referenced to V_{CC}	-0.250	-0.2	-0.150	V
Power-Monitor Fault Threshold	V_{PMTH}	V_{PWRMON} > V_{PMTH} causes a fault	0.7	0.8	0.9	V
TX Disable Time	$t_{\_OFF}$	Time from rising edge of TX_DISABLE to I_{BIAS} = I_{BIAS_OFF} and I_{MOD} = I_{MOD_OFF} (Note 6)		1.8	5	µs
TX Disable Negate Time	$t_{\_ON}$	Time from rising edge of TX_DISABLE to I_{BIAS} and I_{MOD} at 99% of steady state (Note 6)		55	500	µs
Fault Reset Time	$t_{\_INIT1}$	Time to set V_{FAULT} = low after power-on or after rising edge of TX_DISABLE (Note 6)		60	200	ms
Power-On Time	$t_{\_INIT2}$	Time after power-on to transmitter-on with TX_DISABLE low (Note 6)		60	200	ms
Fault Assert Time	$t_{\_FAULT}$	Time from fault occurrence to V_{FAULT} = high; C_{FAULT} < 20pF, R_{FAULT} = 4.7kΩ (Note 6)		1.4	50	µs
Fault Delay Time	$t_{\_FLTDLY}$	Time from fault to I_{BIAS} = I_{BIAS_OFF} and I_{MOD} = I_{MOD_OFF} (Note 6)		1	5	µs
TX_DISABLE Reset	$t_{\_RESET}$	Time TX_DISABLE must be held high to reset FAULT (Note 6)			1	µs

Note 1: Supply current measurements exclude I_{BIAS} from the total current.
Note 2: Tested with R_{PEAK} = 1.18kΩ.
Note 3: Measured by applying a pattern that contains 20µs of K28.5, followed by 5µs of zeros, then 20µs of K28.5, followed by 5µs of ones. Data rate is equal to 2.5Gbps, with inputs filtered using 1.8GHz Bessel filters.
Note 4: V_{BIAS} < V_{CC} - 0.7V.
Note 5: Variation of bias monitor gain for any single part over the range of V_{CC}, temperature, 3mA < I_{BIAS} < 15mA.
Note 6: Guaranteed by design and characterization.
Note 7: Measured electrically with a 50Ω load AC-coupled to OUT+.
Note 8: Deterministic jitter is the peak-to-peak deviation from the ideal time crossings measured with a K28.5 bit pattern at 3.2Gbps

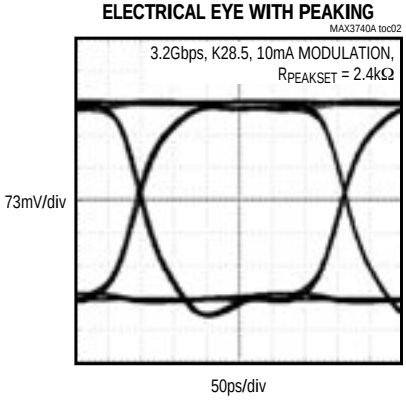
Typical Operating Characteristics

(V_{CC} = +3.3V, R_{TC} = 0Ω, PEAKSET open, measured electrically with a 50Ω load AC-coupled to OUT+, T_A = +25°C, unless otherwise noted.)

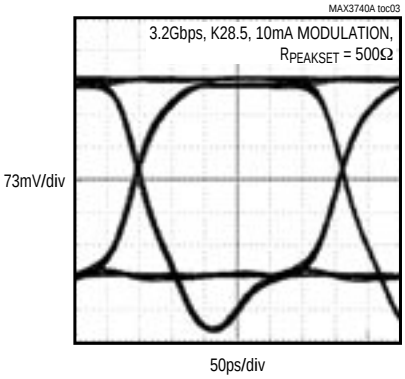
ELECTRICAL EYE



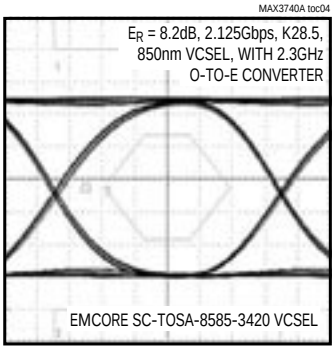
ELECTRICAL EYE WITH PEAKING



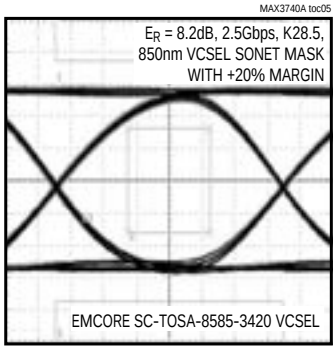
ELECTRICAL EYE WITH MAX PEAKING



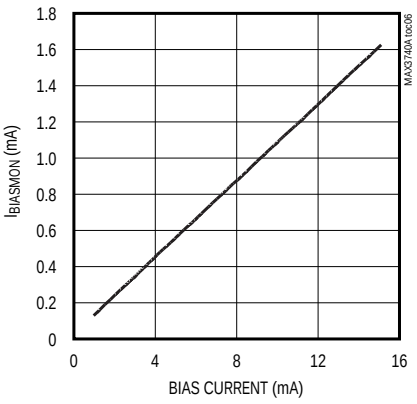
OPTICAL EYE



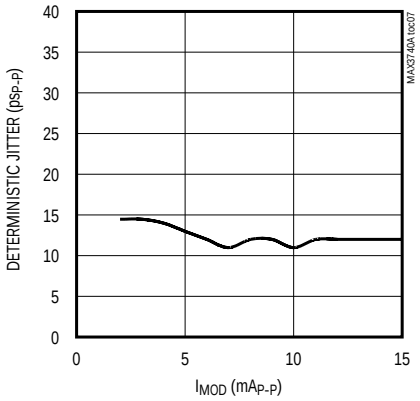
OPTICAL EYE



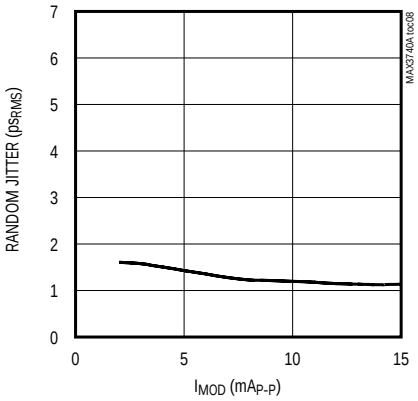
$I_{BIASMON}$ vs. BIAS CURRENT



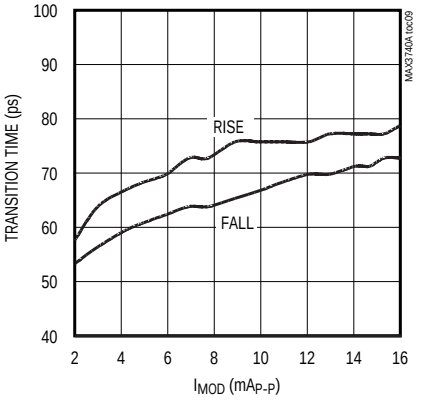
DETERMINISTIC JITTER vs. MODULATION CURRENT



RANDOM JITTER vs. MODULATION CURRENT



TRANSITION TIME vs. MODULATION CURRENT

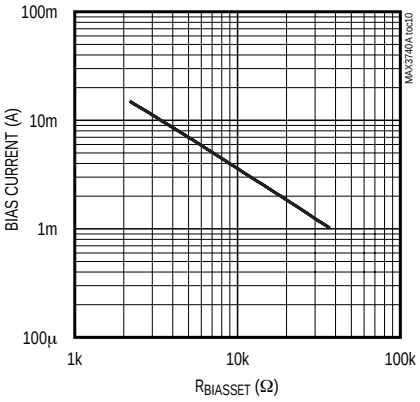


3.2Gbps SFP VCSEL Driver with Diagnostic Monitors

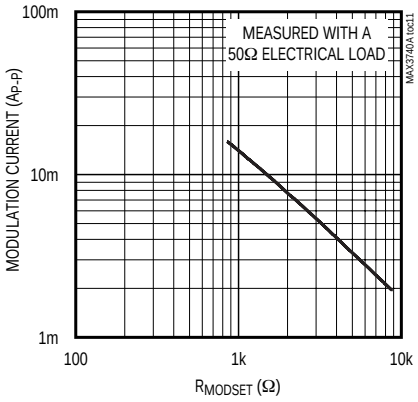
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_{TC} = 0Ω, PEAKSET open, measured electrically with a 50Ω load AC-coupled to OUT+, T_A = +25°C, unless otherwise noted.)

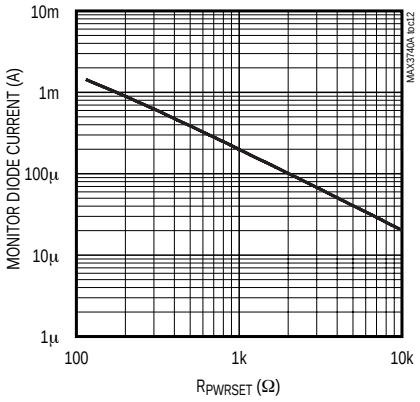
BIAS CURRENT vs. $R_{BIASSET}$



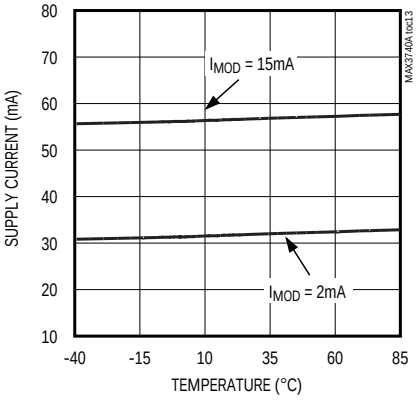
MODULATION CURRENT vs. R_{MODSET}



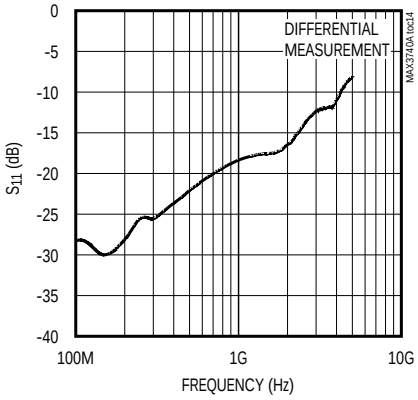
MONITOR DIODE CURRENT vs. R_{PWRSET}



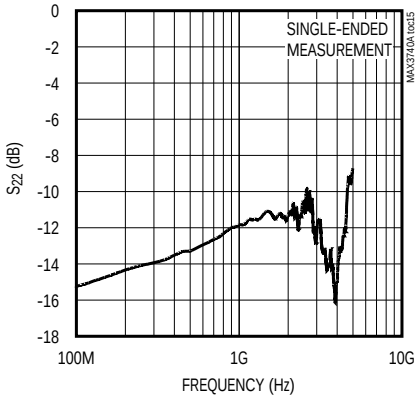
SUPPLY CURRENT vs. TEMPERATURE



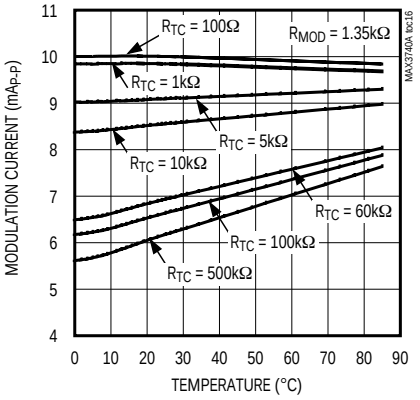
INPUT RETURN LOSS



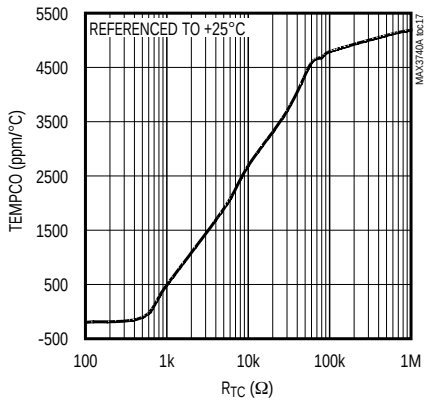
OUTPUT RETURN LOSS



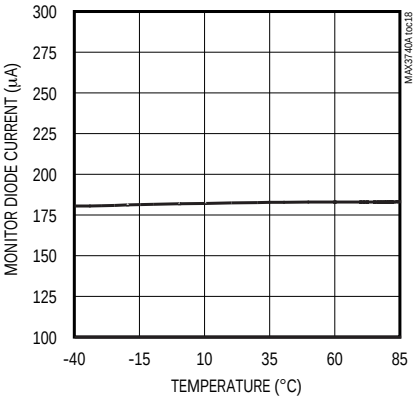
MODULATION CURRENT vs. TEMPERATURE



MODULATION CURRENT TEMPCO vs. R_{TC}



MONITOR DIODE CURRENT vs. TEMPERATURE

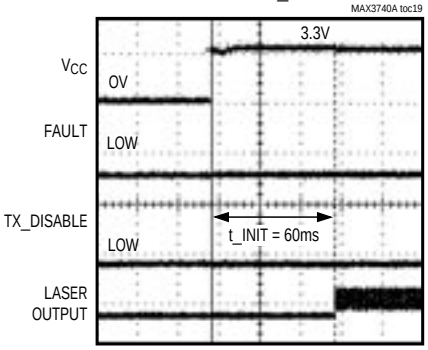


Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, R_{TC} = 0Ω, PEAKSET open, measured electrically with a 50Ω load AC-coupled to OUT+, T_A = +25°C, unless otherwise noted.)

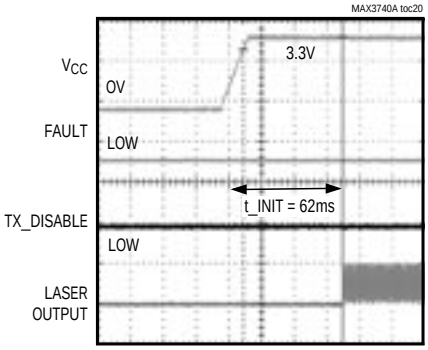
HOT PLUG WITH TX_DISABLE LOW

MAX3740A toc19



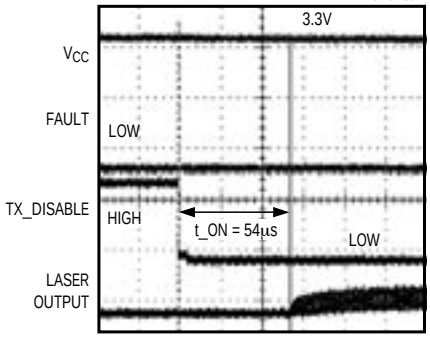
STARTUP WITH SLOW RAMPING SUPPLY

MAX3740A toc20



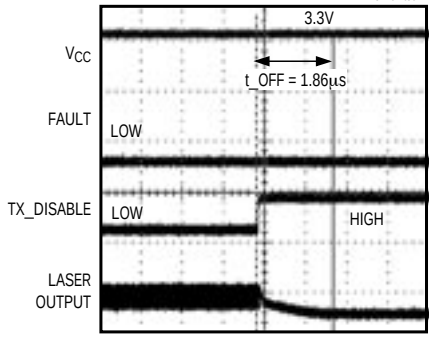
TX_DISABLE NEGATE TIME

MAX3740A toc21



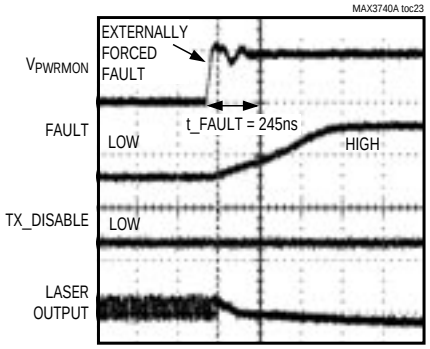
TRANSMITTER DISABLE

MAX3740A toc22



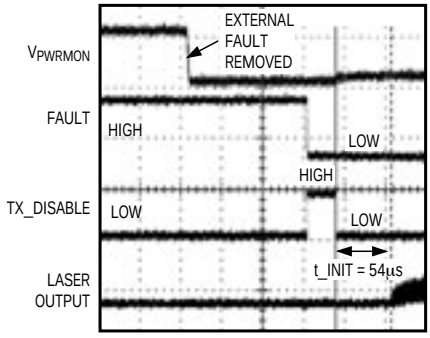
RESPONSE TO FAULT

MAX3740A toc23



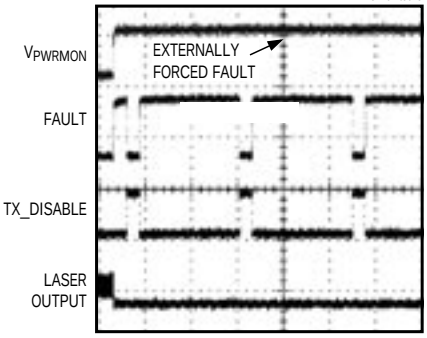
FAULT RECOVERY TIME

MAX3740A toc24



FREQUENT ASSERTION OF TX_DISABLE

MAX3740A toc25



3.2Gbps SFP VCSEL Driver with Diagnostic Monitors

Pin Description

PIN	NAME	FUNCTION
1, 10, 13	GND	Ground
2	TX_DISABLE	Transmit Disable. Driver output is disabled when TX_DISABLE is high or left unconnected. The driver output is enabled when the pin is asserted low.
3	IN+	Noninverted Data Input
4	IN-	Inverted Data Input
5	FAULT	Fault Indicator. Open-drain output with ESD protection. FAULT is asserted high during a fault condition.
6	SQUELCH	Squelch Enable. Squelch is enabled when the pin is set high. Squelch is disabled when the pin is set low or left open.
7, 16, 20	V_{CC}	+3.3V Supply Voltage
8	TC1	Temperature Compensation Set Pin 1. A resistor placed between TC1 and TC2 (R_{TC}) programs the temperature coefficient of the modulation current.
9	TC2	Temperature Compensation Set Pin 2. A resistor placed between TC1 and TC2 (R_{TC}) programs the temperature coefficient of the modulation current.
11	MODSET	Modulation Set. A resistor connected from MODSET to ground (R_{MODSET}) sets the desired modulation current amplitude.
12	PEAKSET	Peaking Current Set. A resistor connected between PEAKSET and ground ($R_{PEAKSET}$) programs the peaking current amplitude. To disable peaking, leave PEAKSET open.
14	OUT-	Inverted Modulation-Current Output
15	OUT+	Noninverted Modulation-Current Output
17	BIASSET	Bias Current Set. When a closed-loop configuration is used, connect a 1.7kΩ resistor between ground and BIASSET to set the maximum bias current. When an open configuration is used, connect a resistor between BIASSET and ground ($R_{BIASSET}$) to program the VCSEL bias current.
18	BIAS	Bias Current Output
19	BIASMON	Bias Current Monitor. The output of BIASMON is a sourced current proportional to the bias current. A resistor connected between BIASMON and ground ($R_{BIASMON}$) can be used to form a ground-referenced bias monitor.
21	COMP	Compensation Pin. A capacitor between COMP and MD compensates the APC. A typical value of 0.047µF is recommended. For open-loop configuration, short the COMP pin to GND to deactivate the APC.
22	MD	Monitor Diode Connection
23	REF	Reference Pin. Reference monitor used for APC. A resistor between REF and MD (R_{PWRSET}) sets the photo monitor current when the APC loop is closed.
24	PWRMON	Average Power Monitor. The pin is used to monitor the transmit optical power. For open-loop configuration, connect PWRMON to GND.
EP	Exposed Pad	Ground. Must be soldered to the circuit board ground for proper thermal and electrical performance. See the *Layout Considerations* section.

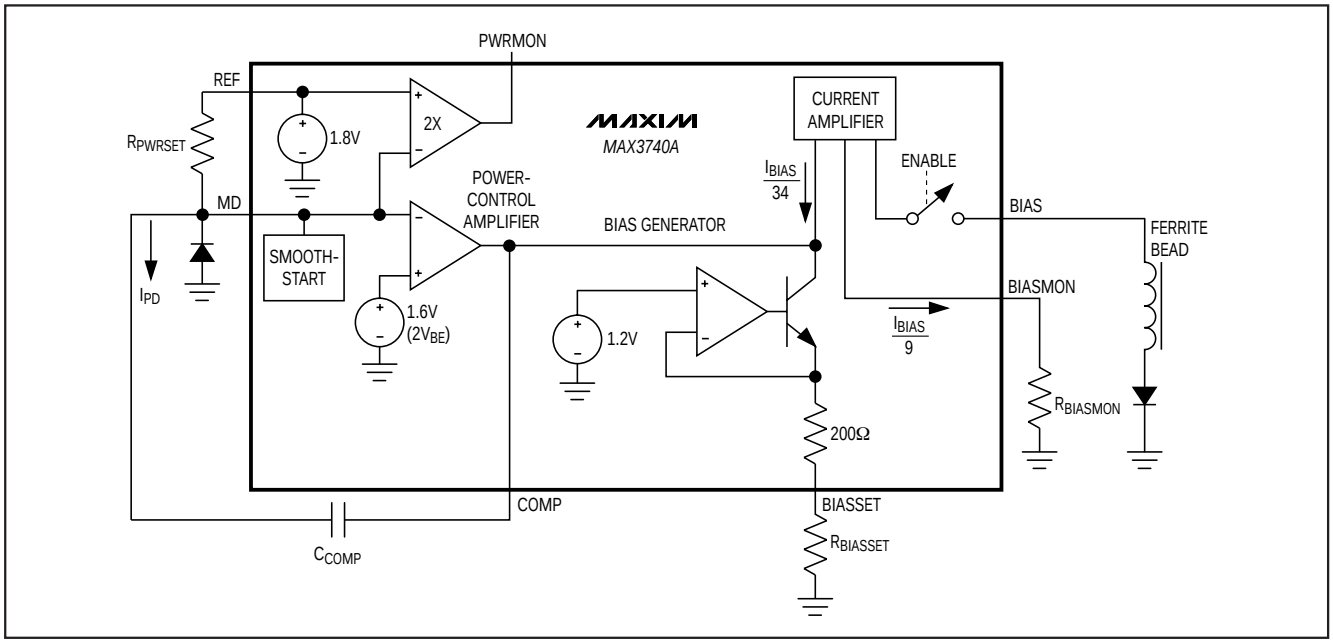


Figure 1. Bias Generator

Detailed Description

The MAX3740A contains a bias generator with automatic power control (APC), safety circuit, and a laser modulator with optional peaking compensation.

Bias Generator

Figure 1 shows the bias generator circuitry that contains a power-control amplifier and smooth-start circuitry. An internal PNP transistor provides DC laser current to bias the laser in a light-emitting state. The APC circuitry adjusts the laser-bias current to maintain average power over temperature and changing laser properties. The smooth-start circuitry prevents current spikes to the laser during power-up or enable, ensuring compliance with safety requirements and extending the life of the laser.

The MD input is connected to the cathode of a monitor diode, which is used to sense laser power. The BIAS output is connected to the anode of the laser through an inductor or ferrite bead. The power-control amplifier drives a current amplifier to control the laser's bias current. During a fault condition, the bias current is disabled.

The PWRMON output provides a voltage proportional to average laser power given by:

$$V_{PWRMON} = 2 \times I_{PD} \times R_{PWRSET}$$

The BIASMON output provides a current proportional to the laser bias current given by:

$$I_{BIASMON} = I_{BIAS} / 9$$

When APC is not used (no monitor diode, open-loop configuration) connect the COMP and PWRMON pins to GND. In this mode, the bias current is set by the resistor $R_{BIASSET}$. When a closed-loop configuration is used, connect a 1.7kΩ resistor between ground and BIASSET to set the maximum bias current.

Safety Circuit

The safety circuit contains an input disable (TX_DISABLE), a latched fault output (FAULT), and fault detectors (Figure 2). This circuit monitors the operation of the laser driver and forces a shutdown (disables laser) if a fault is detected (Table 1). Table 2 contains the circuit's response to various single-point failures. The transmit fault condition is latched until reset by a toggle of TX_DISABLE or V_{CC}. The FAULT pin should be pulled high with a 4.7kΩ to 10kΩ resistor.

Table 1. Fault Conditions

PIN	FAULT CONDITION
BIAS	$V_{BIAS} > V_{CC} - 0.2V$
BIASMON	$V_{BIASMON} > 0.8V$
PWRMON	$V_{PWRMON} > 0.8V$

Table 2. Circuit Response to Various Single-Point Faults (Closed-Loop APC Configuration)

PIN NAME	CIRCUIT RESPONSE TO V_{CC} SHORT	CIRCUIT RESPONSE TO GND SHORT
FAULT	Does not affect laser power.	Does not affect laser power.
TX_DISABLE	Modulation and bias current are disabled.	Normal condition for circuit operation.
IN+	Does not affect laser power.	Does not affect laser power.
IN-	Does not affect laser power.	Does not affect laser power.
SQUELCH	Does not affect laser power.	Does not affect laser power.
TC1	Does not affect laser power.	Does not affect laser power.
TC2	The laser modulation is increased, but average power is not affected.	Modulation current is disabled.
MODSET	Modulation current is disabled.	The laser modulation is increased, but average power is not affected.
PEAKSET	Does not affect laser power.	Does not affect laser power.
OUT+	Modulation current is disabled.	Modulation current is disabled.
OUT-	Does not affect laser power.	Does not affect laser power.
BIASSET	Laser bias is disabled.	Fault state* occurs.
BIAS	Fault state* occurs. Note that VCSEL emissions may continue; care must be taken to prevent this condition.	Disables VCSEL.
BIASMON	Fault state* occurs.	Does not affect laser power.
COMP	The bias current is reduced, and the average power of the laser output is reduced.	I_{BIAS} increases to the value determined by $R_{BIASSET}$; if the bias monitor fault threshold is exceeded, a fault is signaled.
MD	I_{BIAS} increases to the value determined by $R_{BIASSET}$; if the bias-monitor fault threshold is exceeded, a fault is signaled.	The bias current is reduced, and the average power of the laser output is reduced.
REF	I_{BIAS} increases to the value determined by $R_{BIASSET}$; if the bias-monitor fault threshold is exceeded, a fault is signaled.	The bias current is reduced, and the average power of the laser output is reduced.
PWRMON	Fault state* occurs.	Does not affect laser power.

**A fault state asserts the FAULT pin, disables the modulator output, and disables the bias output.*

Modulation Circuit

The modulation circuitry consists of an input buffer, a current mirror, and a high-speed current switch (Figure 3). The modulator drives up to 15mA of modulation into a 50Ω VCSEL load.

The amplitude of the modulation current is set with resistors at MODSET and temperature coefficient (TC1, TC2) pins. The resistor at MODSET (R_{MODSET}) programs the temperature-stable portion of the modulation current, and the resistor between TC1 and TC2 (R_{TC}) programs the temperature coefficient of the modulation current. For appropriate R_{TC} and R_{MODSET} values, see the *Typical Operating Characteristics* section.

Design Procedure

Select Laser

Select a communications-grade laser with a rise time of 260ps or better for 1.25Gbps, or 130ps or better for 2.5Gbps applications. Use a high-efficiency laser that requires low modulation current and generates a low-voltage swing. Trim the leads to reduce laser package inductance. The typical package leads have inductance of 25nH per inch (1nH/mm). This inductance causes a large voltage swing across the laser. A compensation filter network can also be used to reduce ringing, edge speed, and voltage swing (see the *Designing the Compensation Filter Network* section).

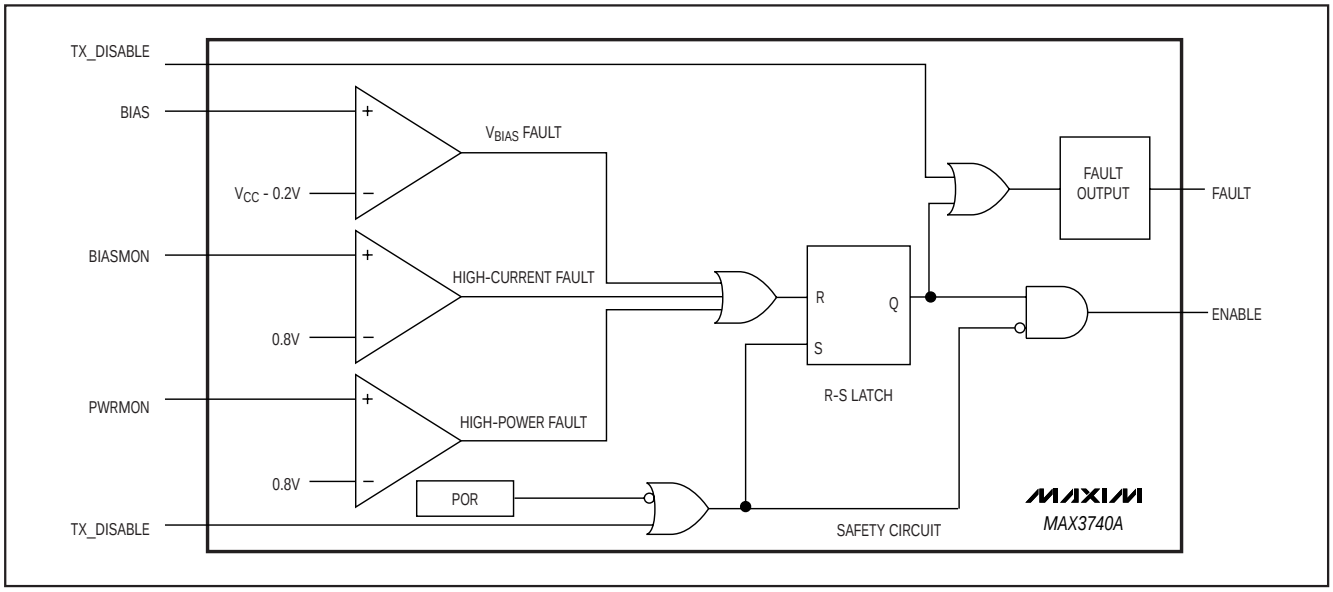


Figure 2. Safety Circuit

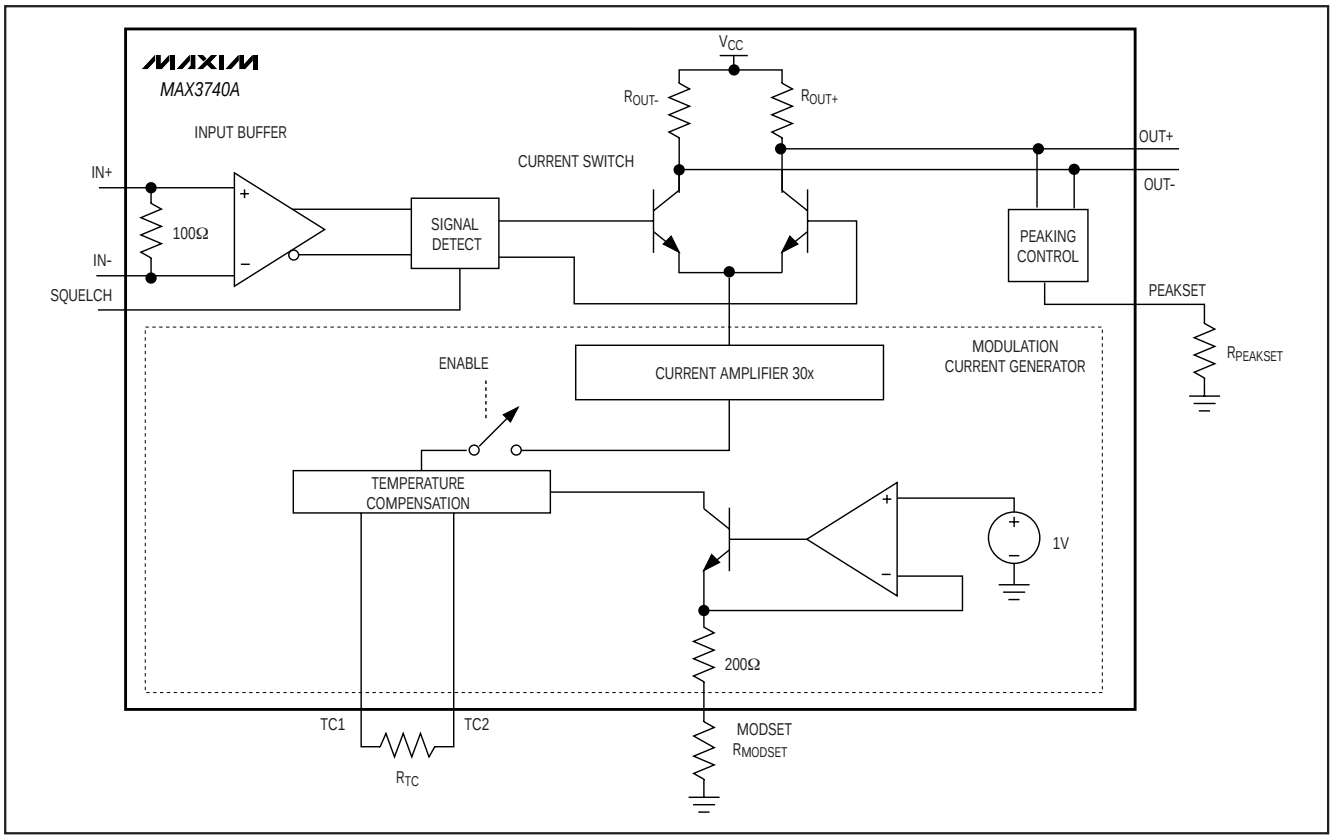


Figure 3. Modulation Circuit

3.2Gbps SFP VCSEL Driver with Diagnostic Monitors

Programming Modulation Current

The modulation current output of the MAX3740A is controlled by a resistor (R_{MODSET}) placed between MODSET and ground. The R_{MODSET} resistor controls the amount of current being sourced to the VCSEL. The modulation current is given by the following:

$$I_{MOD} = \left[\left(I_{MODSET}\right) \times 30\right] \times \left[\frac{R_{OUT+}}{R_{OUT+} + R_{LOAD}}\right]$$

$$I_{MOD} = \left[\left(\frac{1}{200 + R_{MODSET}}\right) \times 30\right] \times \left[\frac{R_{OUT+}}{R_{OUT+} + R_{LOAD}}\right]$$

It is important to note that the modulation current being sourced by the MAX3740A is affected by the load impedance of the VCSEL. The Modulation Current vs. R_{MODSET} graph in the *Typical Operating Characteristics* shows the current into a 50Ω electrical load.

Programming Bias Current

The bias current output of the MAX3740A is controlled by a resistor ($R_{BIASSET}$) placed between BIASSET and ground. In open-loop operation the $R_{BIASSET}$ controls the bias current level of the VCSEL. In closed-loop operation the $R_{BIASSET}$ controls the maximum bias current provided by the APC. The bias current is given by the following:

$$I_{BIAS} = \left(I_{BIASSET}\right) \times 34$$

$$I_{BIAS} = \left(\frac{1.2}{200 + R_{BIASSET}}\right) \times 34$$

The Bias Current vs. $R_{BIASSET}$ graph is also shown in the *Typical Operating Characteristics*.

Photodiode Selection

To ensure stable operation of the APC circuit, the time constant of the MD node should be shorter than the APC time constant. (t_{APC} = 5µs if C_{APC} = 0.047µF).

$$t_{MD} \le \frac{t_{APC}}{20},\ R_{MD} \times C_{MD} \le \frac{5\mu s}{20} = 250ns$$

For typical I_{PD} = 400µA, R_{PWRSET} = 500Ω, select a photodiode with capacitance less than 500pF.

Programming Modulation-Current Tempco

Compute the required modulation tempco from the slope efficiency of the laser at T_A = +25°C and at a higher temperature. Then select the value of R_{TC} from the *Typical Operating Characteristics*. For example, suppose a laser has a slope efficiency (SE) of 0.021mW/mA at +25°C, which reduces to 0.018mW/mA at +85°C. The temperature coefficient is given by the following:

$$\text{Laser tempco} = \frac{(SE_{85} - SE_{25})}{SE_{25} \times (85 - 25)} \times 1E6$$

$$= -2380ppm/°C$$

From the *Typical Operating Characteristics*, the value of R_{TC}, which offsets the tempco of the laser, is 9kΩ. If modulation temperature compensation is not desired, short TC1 and TC2.

Programming the APC Loop

Program the average optical power by adjusting R_{PWRSET}. To select the resistance, determine the desired monitor current to be maintained over temperature and lifetime. See the Monitor Diode Current vs. R_{PWRSET} graph in the *Typical Operating Characteristics* section, and select the value of R_{PWRSET} that corresponds to the required current.

Input Termination Requirements

The MAX3740A data inputs are SFP MSA compatible. On-chip 100Ω differential input impedance is provided for optimal termination (Figure 4). Because of the on-chip biasing network, the MAX3740A inputs self-bias to the proper operating point to accommodate AC-coupling.

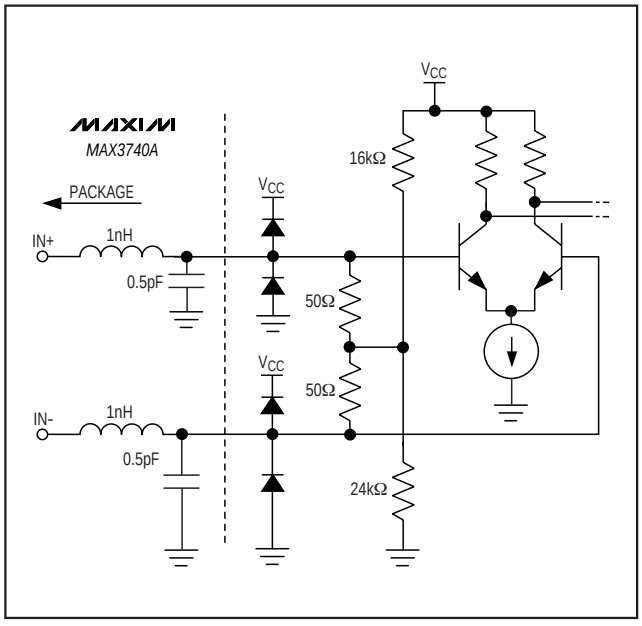


Figure 4. Simplified Input Structure

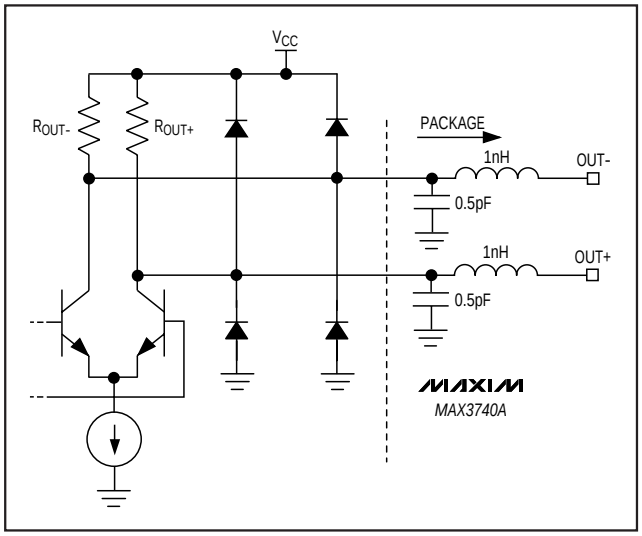


Figure 5. Simplified Output Structure

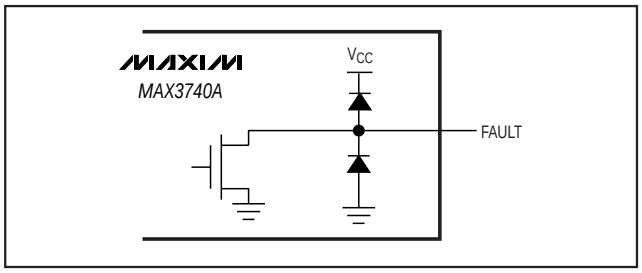


Figure 6. Fault Circuit Interface

Applications Information

Interface Models

Figures 4 and 5 show simplified input and output circuits for the MAX3740A laser driver. Figure 6 shows the fault circuit interface.

Layout Considerations

To minimize inductance, keep the connections between the MAX3740A output pins and laser diode as short as possible. Use good high-frequency layout techniques and multilayer boards with uninterrupted ground planes to minimize EMI and crosstalk.

Designing the Compensation Filter Network

Laser package inductance causes the laser impedance to increase at high frequencies, leading to ringing, overshoot, and degradation of the laser output. A laser compensation filter network can be used to reduce the laser impedance at high frequencies, thereby reducing output ringing and overshoot.

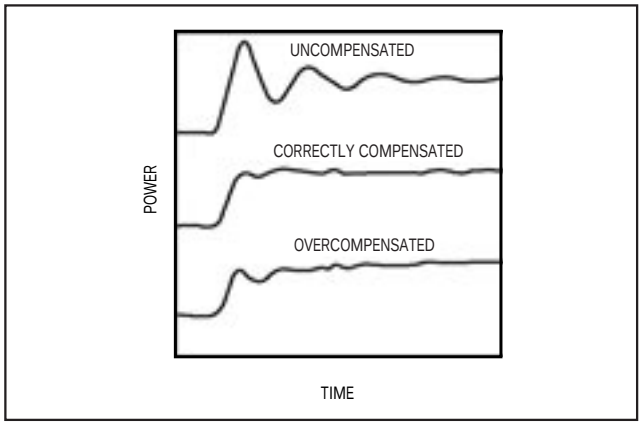


Figure 7. Laser Compensation

The compensation components (R_F and C_F) are most easily determined by experimentation. Begin with R_F = 50Ω and C_F = 1pF. Increase C_F until the desired transmitter response is obtained (Figure 7). Refer to Application Note HFAN-2-0: *Interfacing Maxim Laser Drives with Laser Diodes* for more information.

Exposed-Pad (EP) Package

The exposed pad on the 24-pin thin QFN provides a very low thermal resistance path for heat removal from the IC. The pad is also electrical ground on the MAX3740A and must be soldered to the circuit board ground for proper thermal and electrical performance. Refer to Maxim Application Note HFAN-08.1: *Thermal Considerations for QFN and Other Exposed-Pad Packages* for additional information.

Laser Safety and IEC 825

The International Electrotechnical Commission (IEC) determines standards for hazardous light emissions from fiber optic transmitters. IEC 825 defines the maximum light output for various hazard levels. The MAX3740A provides features that facilitate compliance with IEC 825. A common safety precaution is single-point fault tolerance, whereby one unplanned short, open, or resistive connection does not cause excess light output. Using this laser driver alone does not ensure that a transmitter design is compliant with IEC 825. The entire transmitter circuit and component selections must be considered. Customers must determine the level of fault tolerance required by their applications, recognizing that Maxim products are not designed or authorized for use as components in systems intended for surgical implant into the body, for applications intended to support or sustain life, or for any other application where the failure of a Maxim product could create a situation where personal injury or death may occur.

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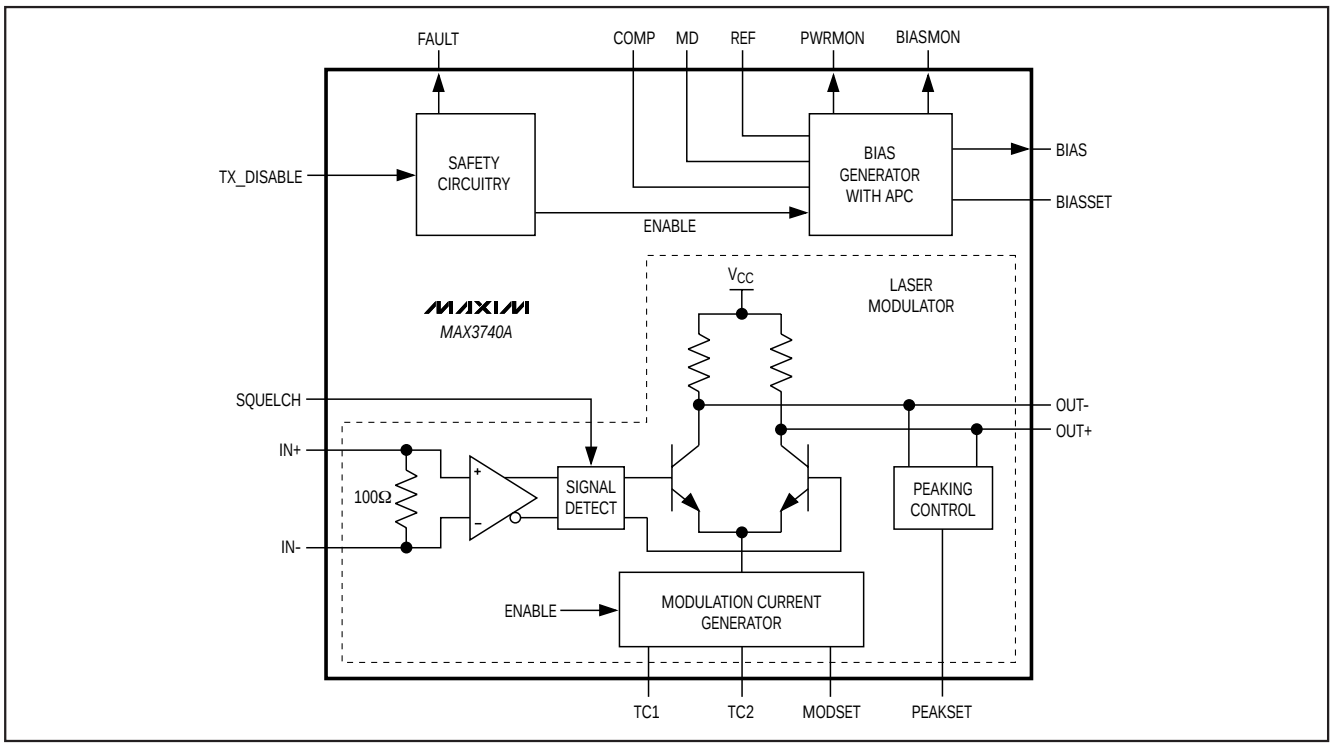
Functional Diagram

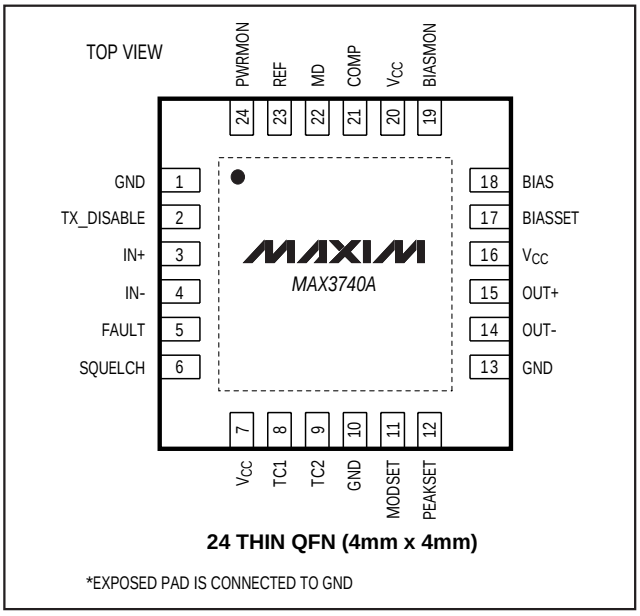


Chip Information

TRANSISTOR COUNT: 3806

PROCESS: SiGe BIPOLAR

Pin Configuration



24 THIN QFN (4mm x 4mm)

*EXPOSED PAD IS CONNECTED TO GND

Package Information

For the latest package outline information, go to **www.maxim-ic.com/packages**.

PART	PACKAGE TYPE	PACKAGE CODE
MAX3740AETG	24 Thin QFN (4mm x 4mm x 0.8mm)	T2444-1