

SANYO

No.2590

LA7096Monolithic Linear IC
VTR AUDIO SIGNAL RECORDING/PLAYBACK PROCESSOR**Functions**

- . Tape head select switches
- . Power supply switch for OSC bias circuit
- . Equalizer amp, line amp, ALC

Features

- . The LA7096 is an IC that provides various functions (including two tape head select switches and a power supply switch for the OSC bias circuit) required for VTR audio signal recording/playback. The LA7096 is fabricated on a single chip and requires a minimum number of peripheral parts.

Maximum Ratings at Ta=25°C

			unit
Maximum Supply Voltage	V_{CCmax}	15	V
Allowable Power Dissipation	P_{dmax} (Ta=65°C)	600	mW
Operating Temperature	Topg	-10 to +65	°C
Storage Temperature	Tstg	-55 to +125	°C
Pin 1 Input Voltage	V_{1IN}	130(±65)	Vp-p
Pin 1 Input Current	I_{1IN}	±1.5	mA

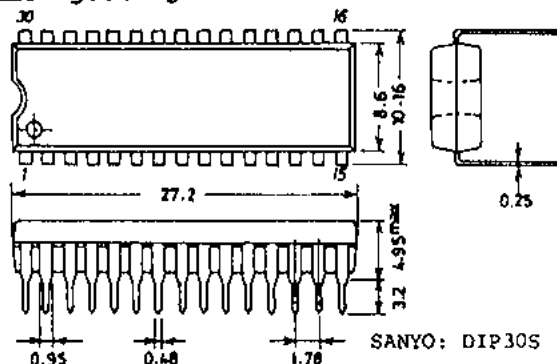
Recommended Operating Conditions at Ta=25°C

			unit
Recommended Operating Voltage	V_{CC}	12.0	V
Operating Voltage Range	V_{opr}	11.5 to 12.5	V

Electrical Characteristics at Ta=25°C, $V_{CC}=12V$, $f=1kHz$, 0 dBv: 1.0Vrms

		min	typ	max	unit
Current Dissipation (EE)	I_{CCE} Quiescent	14.0	18.0	23.0	mA
	(PB) I_{CCP} "	13.5	17.5	22.5	mA
	(REC) I_{CCR} "	11.5	15.5	20.5	mA
Overall Gain at PB Mode	V_{GPB} EQ IN to LINE OUT, $V_o=-5dBv$	67.0	68.5	70.0	dB
[Equalizer Amp]					
Open-Loop Voltage Gain	V_{GOE} $V_o=-5dBv$	60.0	65.0		dB
Equivalent Input Noise Voltage	V_{NIE} $R_g=2.2k\Omega$, DIN audio filter	1.0	1.8		μV_{rms}
Input Resistance	Z_{LINE}	140			kohm

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Case Outline 3061-D30SNIC
(unit:mm)

The application circuit diagrams and circuit constants herein are included as an example and provide no guarantee for designing equipment to be mass produced. The information herein is believed to be accurate and reliable. However, no responsibility is assumed by SANYO for its use, nor for any infringements of patents or other rights of third parties which may result from its use.

Specifications and information herein are subject to change without notice.

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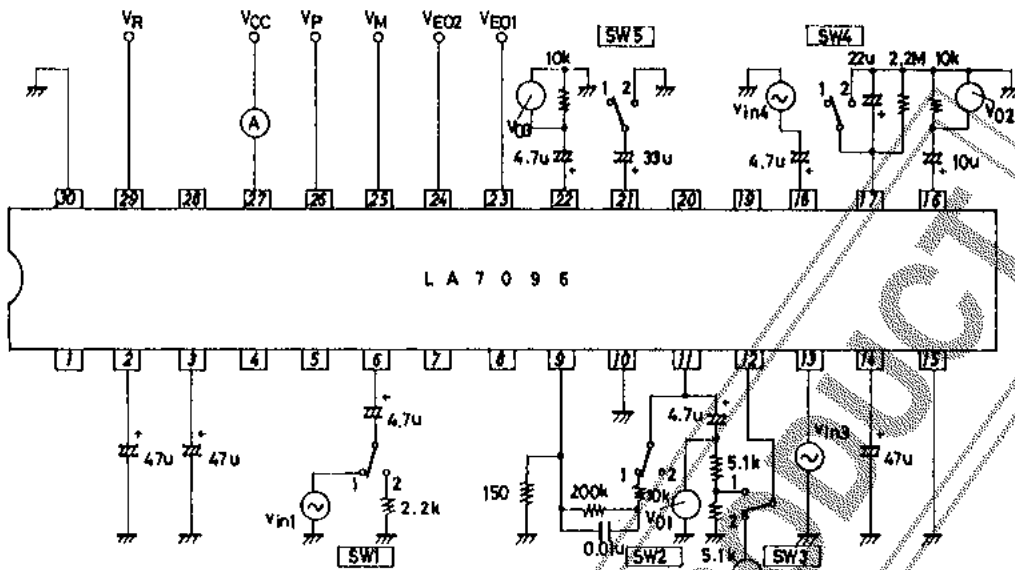
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			min	typ	max	unit
[Line Amp]						
Voltage Gain (PB Input)	$V_{G_{LP}}$	$V_0 = -5\text{dBv}$	32.5	34.0	35.5	dB
(EE, REC Input)	$V_{G_{LR}}$	"	32.5	34.0	35.5	dB
Total Harmonic Distortion	THD_L	"		0.15	0.4	%
Output Noise Voltage	V_{NOL}	PB mute ON, DIN audio filter		-71.0	-65.0	dBv
Input Resistance (PB Input)	Z_{IN1}			35.0		kohm
(EE, REC Input)	Z_{IN2}			35.0		kohm
Maximum Output Voltage	V_{OML}	THD=3%	2.7	3.2		Vrms
Output Voltage at ALC Mode	V_{OA}	$V_{in} = -30\text{dBv}$	-3.0	-1.5	0	dBv
ALC Effect	ALC	$V_{in} = -30$ to -10dBv		1.0	3.0	dB
Total Harmonic Distortion at ALC Mode	THD_A	$V_{in} = -30\text{dBv}$		0.2	0.6	%
[Recording Amp]						
Voltage Gain (Open Loop)	$V_{G_{OR}}$	$V_0 = -5\text{dBv}$	35.0	40.0		dB
(Closed Loop)	$V_{G_{CR}}$	"	11.5	12.5	13.5	dB
Total Harmonic Distortion	THD_R	"		0.2	0.6	%
Input Resistance	Z_{INR}			35.0		kohm
Maximum Output Voltage	V_{OMR}	THD=3%	2.5	3.0		Vrms
[Muting Circuit]						
ON-State Voltage	V_{MON}	Pin25 DC	3.0		10	V
OFF-State Voltage	V_{MOF}	"	0		1.0	V
Muting Attenuation (PB)	M_P		85.0	90.0		dB
(REC)	M_R		75.0	80.0		dB
[PB/EE Select Circuit]						
PB Mode Hold Voltage	V_{PP}	Pin26 DC	3.8		10	V
EE Mode Hold Voltage	V_{PE}	"	0		1.0	V
[REC/EE Select Circuit]						
REC Mode Hold Voltage	V_{RR}	Pin29 DC	4.0		10	V
EE Mode Hold Voltage	V_{RE}	"	0		1.0	V
[Equalizer Select Circuit]						
Switch ON-State Voltage	V_{EON}	Pins23,24 DC	3.0		10	V
Switch OFF-State Voltage	V_{EOF}	"	0		0.8	V
[Head Select Switch]						
Pin 1 ON-State Resistance	R_{ON1}	$I_1 = \pm 1\text{mA}$		10	20	ohm
Pin 5 ON-State Resistance	R_{ON5}	$I_5 = \pm 1\text{mA}$		5	10	ohm
Pin 1 Leakage Current	I_{L1}	$V_1 = \pm 50\text{V}$			± 10	μA
Pin 5 Leakage Current	I_{L5}	$V_5 = \pm 0.1\text{V}$			± 2	μA

LA7096

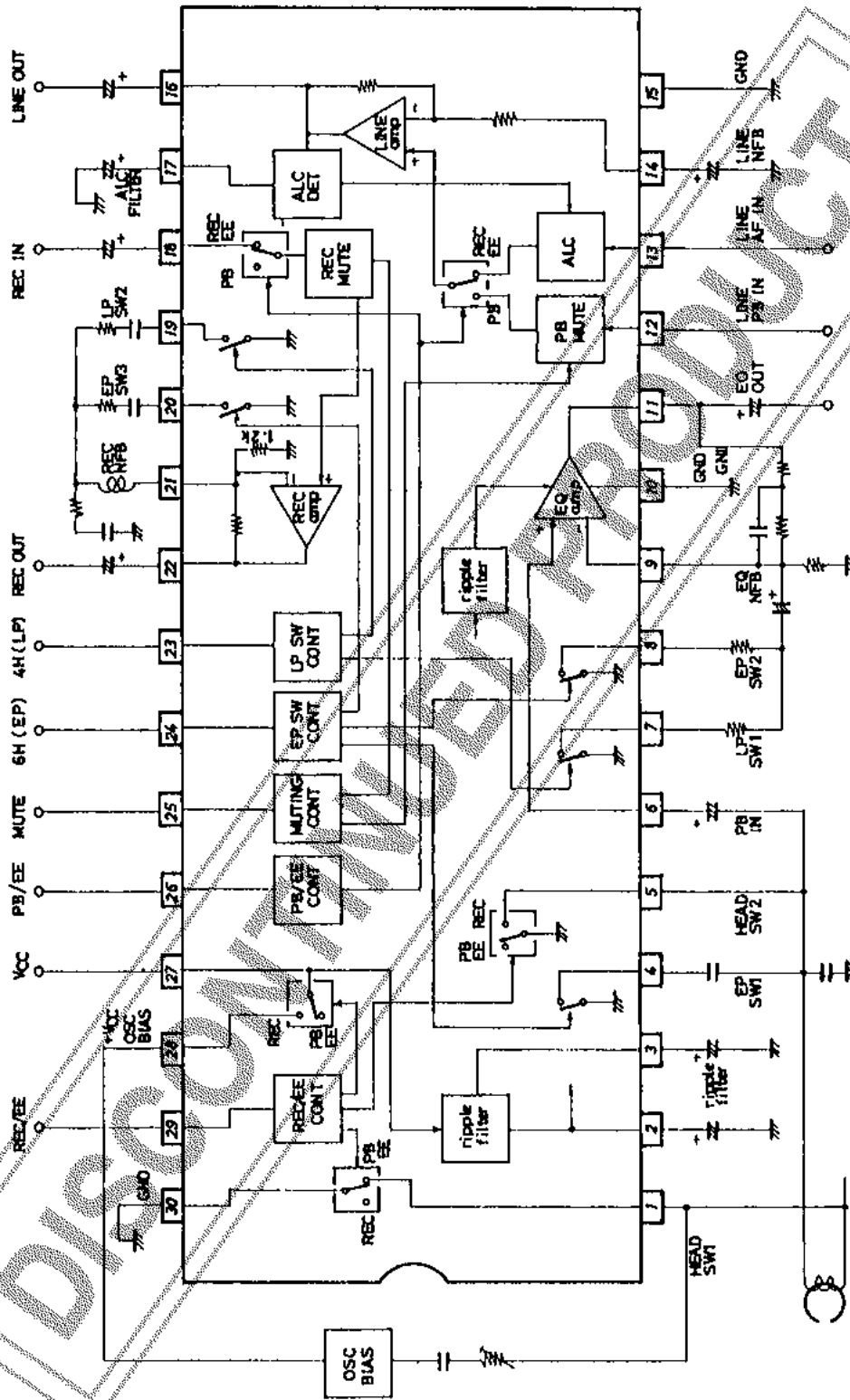
Test Circuit



Switch Operating Table

Item (Symbol)	SW1	SW2	SW3	SW4	SW5	VM	VP	VR	Input	Test
ICCE	2	1	1	2	1	GND	GND	GND	-	A
ICCP	2	1	1	2	1	GND	VCC	GND	-	A
ICCR	2	1	1	2	1	GND	GND	VCC	-	A
VGPB	1	1	1	2	1	GND	VCC	GND	VIN1	V02
VG0E	1	2	2	2	1	GND	VCC	GND	VIN1	V01
VNIL	2	1	2	2	1	GND	VCC	GND	-	V01
VGLP, THDL, VOML	2	1	2	2	1	GND	VCC	GND	VIN2	V02
VGLR	2	1	1	2	1	GND	GND	GND	VIN3	V02
VNOL	2	1	2	2	1	VCC	VCC	GND	-	V02
VOA, ALC, THDA	2	1	2	1	1	GND	GND	GND	VIN3	V02
VGOR	2	1	2	2	2	GND	GND	GND	VIN4	V03
VGCR, THDR, VOMR	2	1	2	2	1	GND	GND	GND	VIN4	V03
MP	1	1	1	2	1	VCC	VCC	GND	VIN1	V02
MR	2	1	1	2	1	VCC	GND	GND	VIN4	V03

Block Diagram



Sample Application Circuit

