
HD404669 Series

Low-Voltage AS Microcomputers with On-Chip DTMF Generation Circuit

HITACHI

ADE-202-083B

Rev. 3.0

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Description

The HD404669 Series microcomputers incorporate a DTMF generation circuit, two comparators, and a serial interface on chip. They also provide input and output pins with large current handling capacities. Thus they are 4-bit single-chip microcomputers that are optimal for use in multifunction telephones, cordless telephones, and other communications equipment.

HD404669 Series microcomputers have a 32.768 kHz sub-oscillator for realtime clock use, providing a time counting facility, and a variety of power supply modes to reduce current drain.

The HD407A4669 is a ZTAT™ microcomputer with on-chip PROM that drastically shortens development time and ensures a smooth transition from debugging to mass production. (The PROM programming specifications are the same as for the 27256 type.)

ZTAT™: Zero Turn-Around Time ZTAT is a trademark of Hitachi, Ltd.

Features

- 1,152-digit × 4-bit RAM
- I/O pins: 47
 - High-current I/O pins (source: 10 mA max.): 4
 - High-current I/O pins (sink: 15 mA max.): 5
- Timer counters: 3
- Input capture: one 8-bit channel
- Timer outputs: 2 (with PWM output capability)
- Event input: 1 (edge-programmable)
- Clock synchronous 8-bit serial interface: 1
- DTMF generation circuit
- Comparator: 2 channels
- System clock oscillator
 - Ceramic oscillator, crystal oscillator, or external clock operation possible

HD404669 Series

- Subsystem clock oscillator
32.768 kHz crystal oscillator for realtime clock use
- Interrupts
 - External: 5 (including 3 edge-programmable)
 - Internal: 4
- Subroutine stack: max. 16 levels including interrupts
- Low-power modes: 4
- System clock division software switching (1/4, 1/8, 1/16, 1/32)
- Instruction execution time
 - Min. 1 μ s ($f_{OSC} = 4$ MHz, 1/4 clock division)
 - Min. 0.5 μ s ($f_{OSC} = 8$ MHz, 1/4 clock division)
- Operating voltage
 - 1.8 V to 5.5 V
 - 2.2 V to 5.5 V (ZTAT™)

Ordering Information

| Type | Product Name | Model Name | ROM (Words) | RAM (Digits) | Package |
|-------------------------------------|--------------|-------------|-------------|--------------|-----------------------------------|
| Mask ROM (standard version) | HD404668 | HD404668H | 8,192 | 1,152 | 64-pin plastic QFP (FP-64A) |
| | HD4046612 | HD4046612H | 12,288 | | |
| | HD404669 | HD404669H | 16,384 | | |
| | HCD404669 | HCD404669 | 16,384 | | Chip ^{*1*2} |
| Mask ROM (high-speed version) | HD40A4668 | HD40A4668H | 8,192 | | 64-pin plastic QFP (FP-64A) |
| | HD40A46612 | HD40A46612H | 12,288 | | |
| | HD40A4669 | HD40A4669H | 16,384 | | |
| ZTAT™ (high-speed version) | HD407A4669 | HD407A4669H | 16,384 | | |

Note: 1. ZTAT™ chip shipment is not supported.
2. The specifications of shipped chips differ from those of the package product. Please contact our sales staff for details.

Cautions about Operation

The mask ROM and ZTAT™ versions have been confirmed as fully meeting the reference values for electrical characteristics shown in this data sheet. However, actual performance figures, operating margins, noise margins, and other properties may vary due to differences in the manufacturing process, internal

HD404669 Series

wiring patterns, etc. Users are therefore requested to confirm the operation of individual products by conducting evaluation tests under conditions equivalent to those in the actual application system.

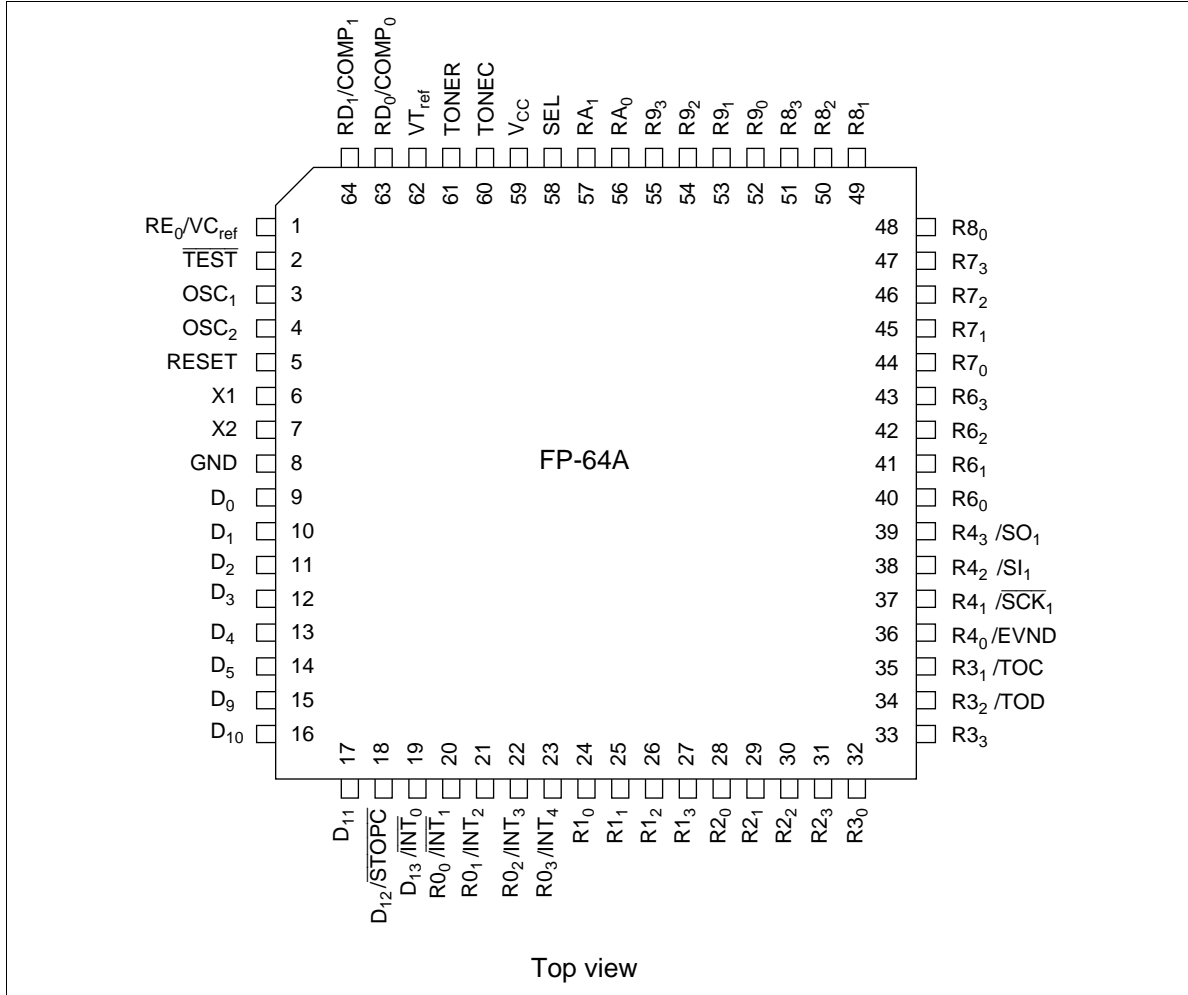
List of Functions

| Product name | | Standard version | HD404668 | HD4046612 | HD404669 | HCD404669 | |
|---------------------------------------|------------------------|--------------------|---|------------|-----------|------------|-----------------------------|
| | | High-speed version | HD40A4668 | HD40A46612 | HD40A4669 | —— | HD407A4669 |
| ROM (Words) | | | 8,192 | 12,288 | 16,384 | 16,384 | 16,384PROM |
| RAM (Digits) | | | 1,152 | | | | |
| I/O | | | 52 (max) | | | | |
| | Large-current I/O pins | | 4 (Source 10mA max), 5 (Sink 15 mA max) | | | | |
| Timer / Counter | | | 3 | | | | |
| | Input capture | | 8 bit × 1 | | | | |
| | Timer output | | 2 (PWM output possible) | | | | |
| | Event input | | 1 (edge selection possible) | | | | |
| Serial interface | | | 1 (8-bit clock synchronous) | | | | |
| DTMF generation circuit | | | Available | | | | |
| Comparator | | | 2 | | | | |
| Interrupt | External | | 5 (edge selection possible for 3) | | | | |
| | Internal | | 4 | | | | |
| Low-Power Dissipation Mode | | | 4 | | | | |
| | Stop mode | | Available | | | | |
| | Watch /mode | | Available | | | | |
| | Standby mode | | Available | | | | |
| | Subactive mode | | Available | | | | |
| Main Oscillator | Ceramic oscillation | | 400 kHz, 800 kHz, 2 MHz, 3.58 MHz, 4 MHz, 7.16 MHz*, 8 MHz* | | | | |
| | Crystal oscillation | | 400 kHz, 800 kHz, 2 MHz, 3.58 MHz, 4 MHz, 7.16 MHz*, 8 MHz* | | | | |
| Sub oscillator | Crystal oscillation | | 32.768 kHz | | | | |
| Minimum instruction execution time | Standard version | | 1 μs (f _{osc} = 4 MHz, 1/4 frequency division) | | | | |
| | High-speed version | | 0.5 μs (f _{osc} = 8 MHz, 1/4 frequency division) | | | | |
| Operating voltage (V) | | | 1.8 to 5.5 | | | 1.8 to 5.5 | 2.2 to 5.5 |
| Package | | | 64-pin plastic QFP (FP-64A) | | | Chip | 64-pin plastic QFP (FP-64A) |
| Guaranteed operation temperature (°C) | | | -20 to +75 | | | +75°C | -20 to +75 |

Note: * Applies to high-speed versions (HD40A4668, HD40A46612, HD40A4669, HD407A4669).

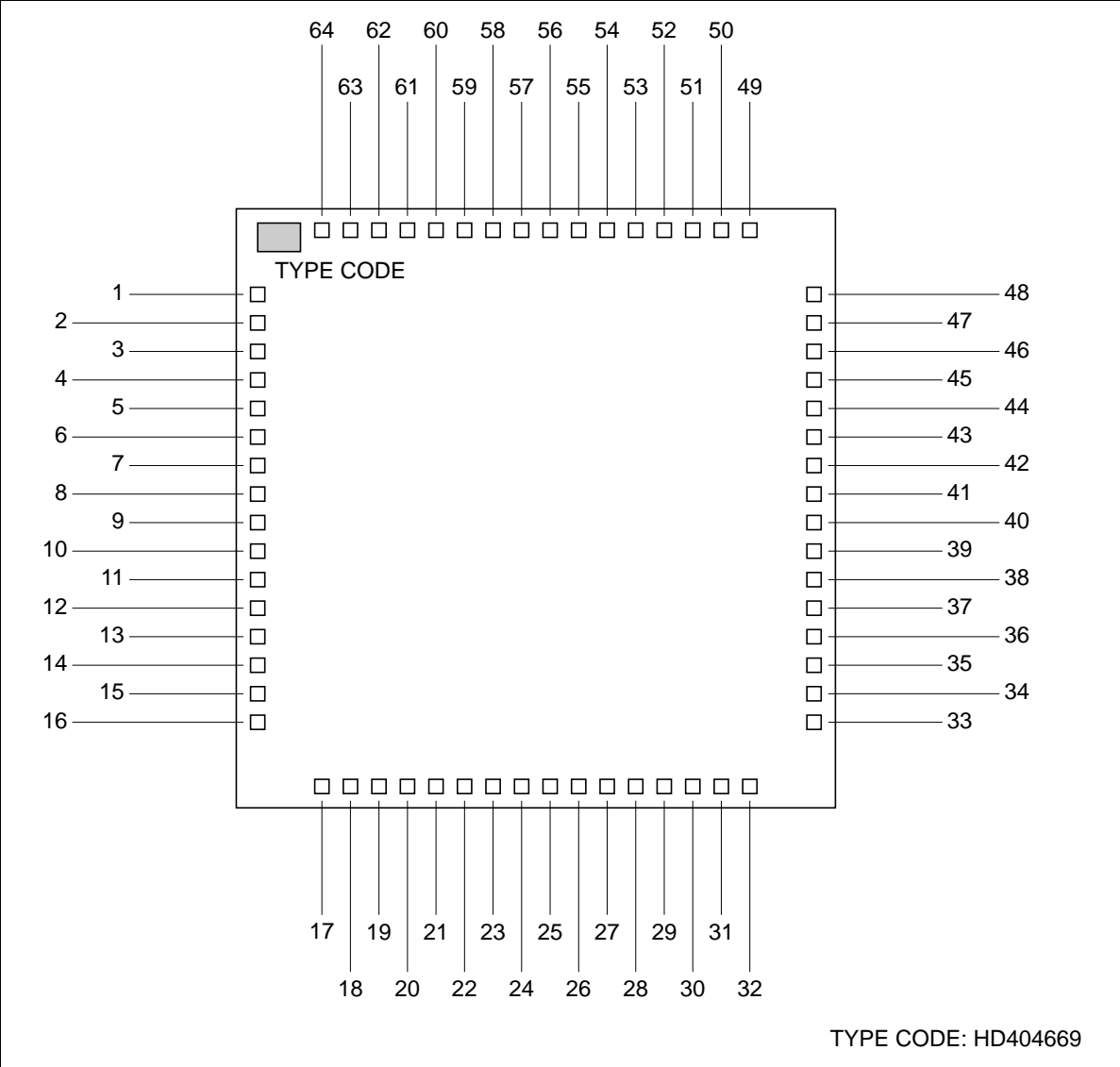
HD404669 Series

Pin Arrangement



Pad Arrangement

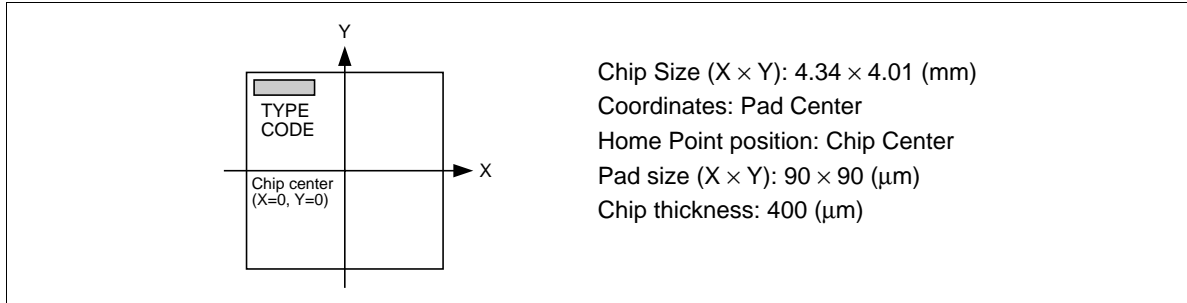
HCD404669



HD404669 Series

Bonding Pad Coordinates

HCD404669



| Pad No. | Pad Name | Coordinates | | Pad No. | Pad Name | Coordinates | | Pad No. | Pad Name | Coordinates | | Pad No. | Pad Name | Coordinates | |
|---------|----------|-------------|-------|---------|----------|-------------|-------|---------|----------|-------------|-------|---------|-----------------|-------------|------|
| | | X | Y | | | X | Y | | | X | Y | | | X | Y |
| 1 | RE0 | -1983 | 1444 | 17 | D11 | -1607 | -1819 | 33 | R33 | 1983 | -1444 | 49 | R81 | 1587 | 1819 |
| 2 | TESTN | -1983 | 1252 | 18 | D12 | -1394 | -1819 | 34 | R32 | 1983 | -1252 | 50 | R82 | 1374 | 1819 |
| 3 | OSC1 | -1983 | 1062 | 19 | D13 | -1181 | -1819 | 35 | R31 | 1983 | -1060 | 51 | R83 | 1161 | 1819 |
| 4 | OSC2 | -1983 | 871 | 20 | R00 | -968 | -1819 | 36 | R40 | 1983 | -867 | 52 | R90 | 948 | 1819 |
| 5 | RESET | -1983 | 657 | 21 | R01 | -755 | -1819 | 37 | R41 | 1983 | -675 | 53 | R91 | 735 | 1819 |
| 6 | X1 | -1983 | 466 | 22 | R02 | -541 | -1819 | 38 | R42 | 1983 | -483 | 54 | R92 | 522 | 1819 |
| 7 | X2 | -1983 | 275 | 23 | R03 | -329 | -1819 | 39 | R43 | 1983 | -291 | 55 | R93 | 309 | 1819 |
| 8 | GND | -1983 | 84 | 24 | R10 | -117 | -1819 | 40 | R60 | 1983 | -99 | 56 | RA0 | 93 | 1819 |
| 9 | D0 | -1983 | -108 | 25 | R11 | 96 | -1819 | 41 | R61 | 1983 | 93 | 57 | RA1 | -177 | 1819 |
| 10 | D1 | -1983 | -299 | 26 | R12 | 309 | -1819 | 42 | R62 | 1983 | 285 | 58 | SEL | -329 | 1819 |
| 11 | D2 | -1983 | -490 | 27 | R13 | 522 | -1819 | 43 | R63 | 1983 | 478 | 59 | V _{CC} | -542 | 1819 |
| 12 | D3 | -1983 | -680 | 28 | R20 | 735 | -1819 | 44 | R70 | 1983 | 670 | 60 | TONEC | -755 | 1819 |
| 13 | D4 | -1983 | -871 | 29 | R21 | 948 | -1819 | 45 | R71 | 1983 | 862 | 61 | TONER | -968 | 1819 |
| 14 | D5 | -1983 | -1062 | 30 | R22 | 1161 | -1819 | 46 | R72 | 1983 | 1054 | 62 | VTREF | -1181 | 1819 |
| 15 | D9 | -1983 | -1253 | 31 | R23 | 1374 | -1819 | 47 | R73 | 1983 | 1246 | 63 | RD0 | -1394 | 1819 |
| 16 | D10 | -1983 | -1444 | 32 | R30 | 1587 | -1819 | 48 | R80 | 1983 | 1444 | 64 | RD1 | -1607 | 1819 |

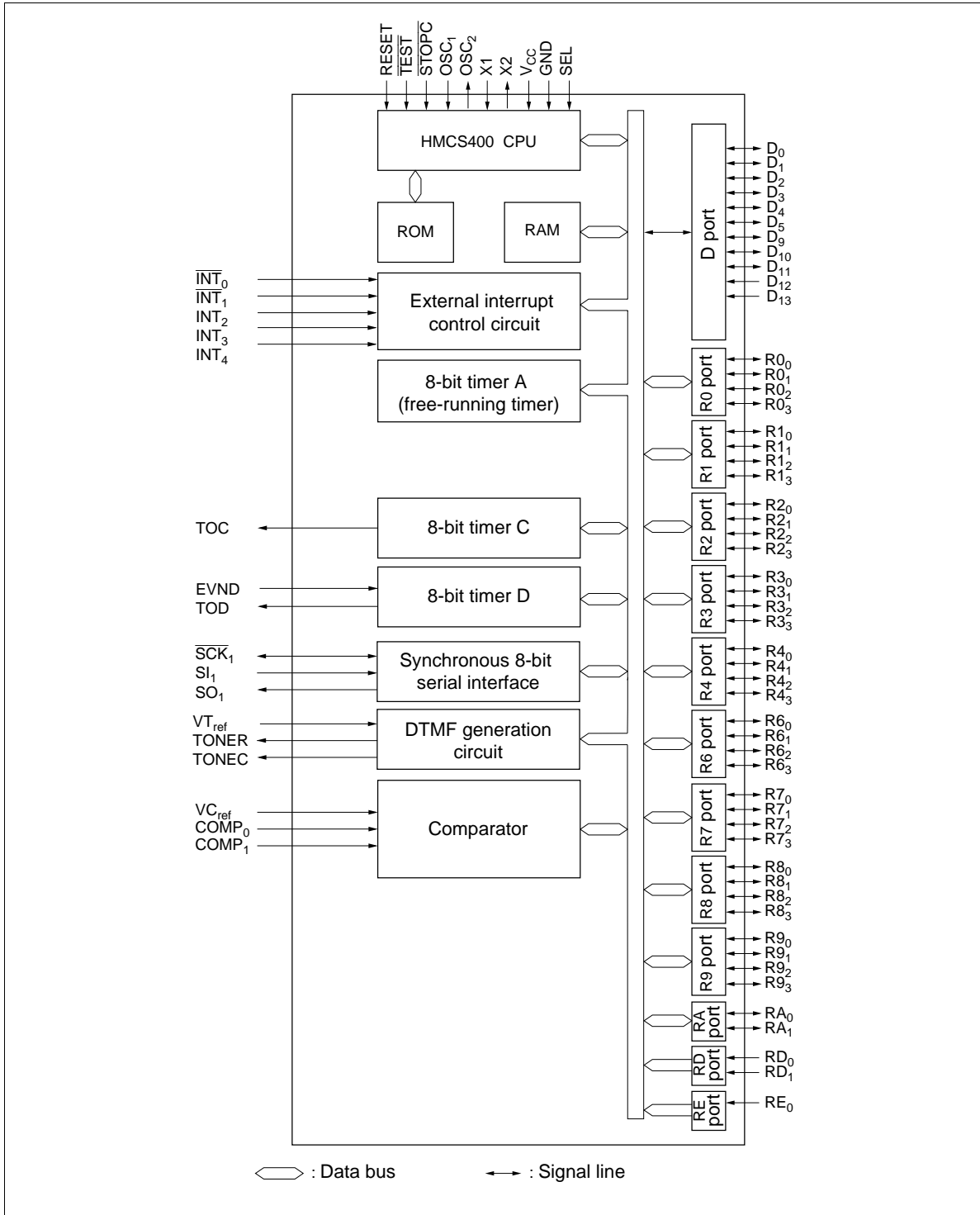
Pin Description

| Item | Symbol | Pin Number | | Function |
|------------------|--|---|-------|---|
| | | FP-64A, chip | I/O | |
| Power supply | V_{CC} | 59 | – | Applies power voltage |
| | GND | 8 | – | Connected to ground |
| Test | \overline{TEST} | 2 | I | Used for factory testing only: Connect this pin to V_{CC} |
| Reset | RESET | 5 | I | Resets the MCU |
| Oscillator | OSC ₁ | 3 | I | Input/output pins for the internal oscillator circuit: Connect them to a ceramic oscillator ,crystal oscillator or connect OSC ₁ to an external oscillator circuit |
| | OSC ₂ | 4 | O | |
| | X1 | 6 | I | Used for a 32.768-kHz crystal for clock purposes. If not to be used, fix the X1 pin to V_{CC} and leave the X2 pin open. |
| | X2 | 7 | O | |
| Port | D ₀ –D ₅ , D ₉ –D ₁₁ | 9-17 | I/O | Input/output pins addressed by individual bits; D ₀ to D ₃ are source high-current input/output pins. A maximum 10 mA current can be supplied to each pin. D ₄ , D ₅ , and D ₉ to D ₁₁ are sink high-current input/output pins. A maximum 15 mA current can be supplied to each pin. |
| | D ₁₂ , D ₁₃ | 18, 19 | I | Input pins addressable by individual bits |
| | R0 ₀ –R4 ₃ , R6 ₀ –RA ₁ | 20–57 | I/O | Input/output pins addressable in 4-bit units |
| | RD ₀ , RD ₁ , RE ₀ | 63, 64, 1 | I | Input pins addressable in 4-bit units |
| | Interrupt | \overline{INT}_0 , \overline{INT}_1 , INT ₂ –INT ₄ | 19-23 | I |
| Stop clear | \overline{STOPC} | 18 | I | Input pin for transition from stop mode to active mode |
| Serial interface | SCK ₁ | 37 | I/O | Serial interface clock input/output pin |
| | SI ₁ | 38 | I | Serial interface receive data input pin |
| | SO ₁ | 39 | O | Serial interface transmit data output pin |
| Timer | TOC, TOD | 35, 34 | O | Timer output pins |
| | EVND | 36 | I | Event input pin |
| DTMF | TONER | 61 | O | Output pin for DTMF row signals |
| | TONEC | 60 | O | Output pin for DTMF column signals |
| | VT _{ref} | 62 | – | Reference voltage pin for DTMF signals. Voltage conditions are: $V_{CC} \geq VT_{ref} \geq GND$ |

HD404669 Series

| Item | Symbol | Pin Number | | Function |
|------------------------------------|--|--------------|-----|--|
| | | FP-64A, chip | I/O | |
| Voltage comparator | COMP ₀ , COMP ₁ | 63, 64 | I | Comparator analog input pins. |
| | VC _{ref} | 1 | – | Analog input pin threshold voltage reference level power supply pin. |
| Frequency division ratio selection | SEL | 58 | I | Pin that selects the system clock division ratio immediately after a reset and when returning from stop mode to active mode. Connect to Vcc voltage to select division-by-4, or to GND potential to select division-by-32. |

Block Diagram



HD404669 Series

Memory Map

ROM Memory Map

The ROM memory map is shown in figure 1 and described below.

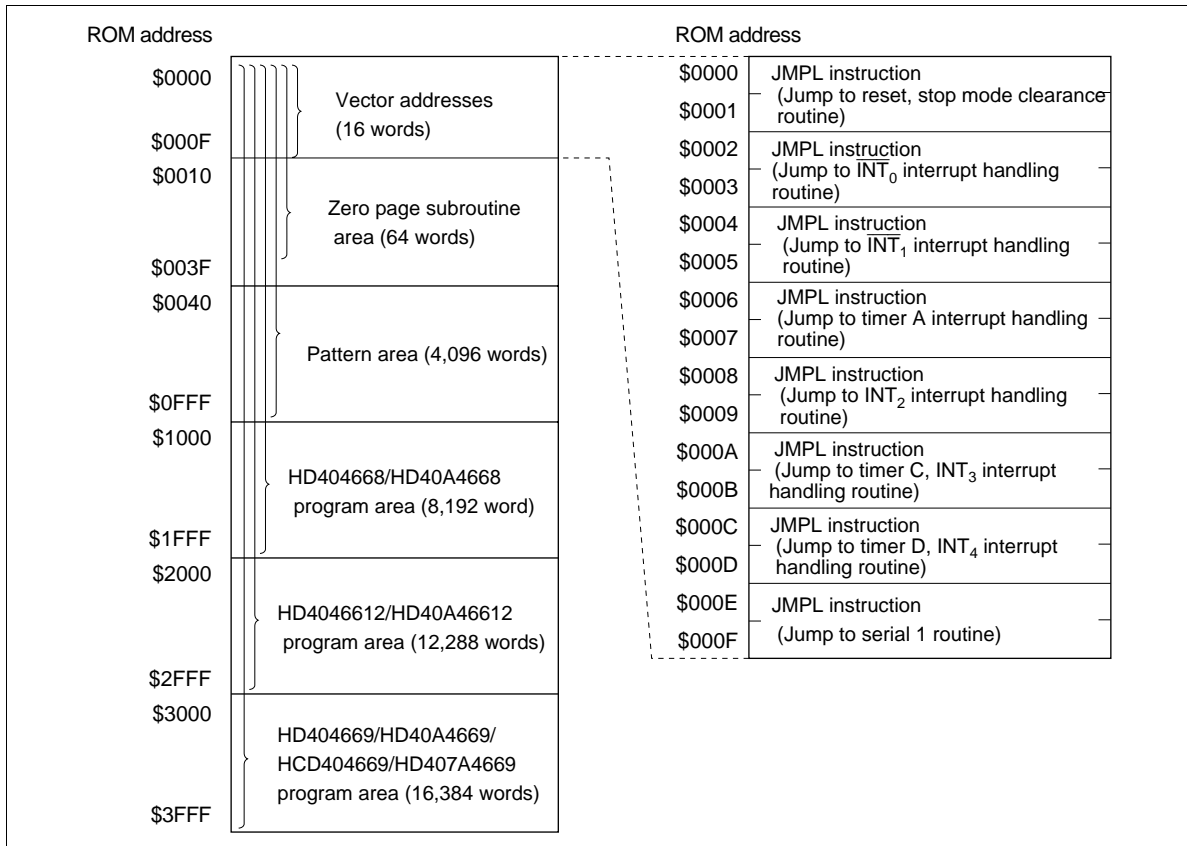


Figure 1 ROM Memory Map

Vector Address Area (\$0000–\$000F): Reserved for JMWPL instructions that branch to the start addresses of the reset and interrupt routines. After MCU reset or an interrupt, program execution continues from the vector address.

Zero-Page Subroutine Area (\$0000–\$003F): Reserved for subroutines. The program branches to a subroutine in this area in response to the CAL instruction.

Pattern Area (\$0000–\$0FFF): Contains ROM data that can be referenced with the P instruction.

Program Area (\$0000–\$1FFF: HD404668, HD40A4668; \$0000–\$2FFF: HD4046612, HD40A46612; \$0000–\$3FFF: HD404669, HD40A4669, HD407A4669, HCD404669): Used for program coding.

RAM Memory Map

The MCU contains a RAM area consisting of a memory register area, a data area, and a stack area. In addition, an interrupt control bits area, special function register area, and register flag area are mapped onto the same RAM memory space. The RAM memory map is shown in figure 2 and described below.

RAM-Mapped Register Area (\$000–\$03F):

- **Interrupt Control Bits Area (\$000–\$003)**

This area is used for interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

- **Special Function Register Area (\$004–\$01F, \$024–\$03F)**

This area is used as mode registers and data registers for external interrupts, serial interface, timers, DTMF, comparator, and as data control registers for I/O ports. The structure is shown in figures 2 and 5. These registers can be classified into three types: write-only (W), read-only (R), and read/write (R/W). RAM bit manipulation instructions cannot be used for these registers.

- **Register Flag Area (\$020–\$023)**

This area is used for the DTON, WDON, and other register flags and interrupt control bits (figure 3). These bits can be accessed only by RAM bit manipulation instructions (SEM/SEMD, REM/REMD, and TM/TMD). However, note that not all the instructions can be used for each bit. Limitations on using the instructions are shown in figure 4.

HD404669 Series

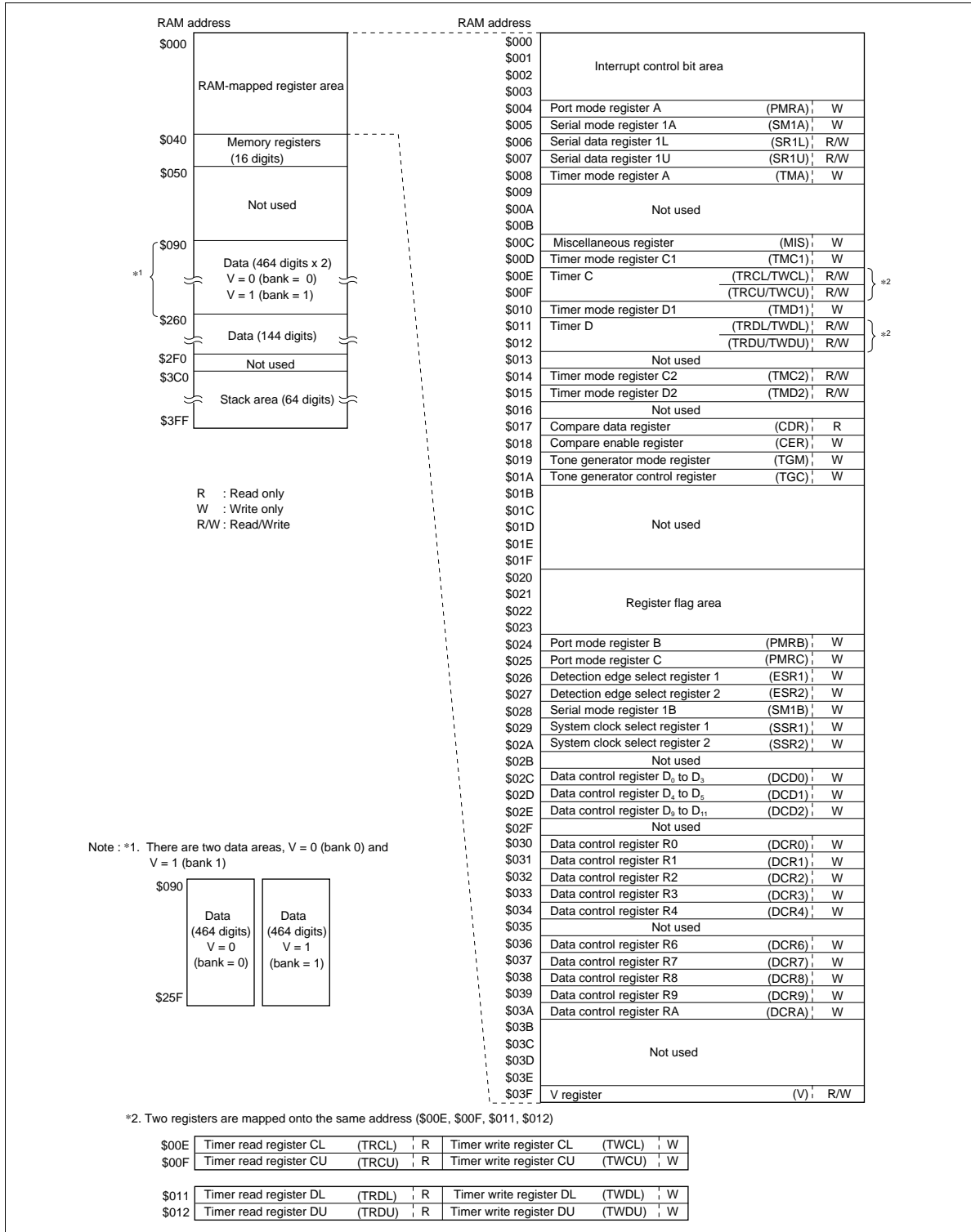


Figure 2 RAM Memory Map

| RAM address | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|--|--|--|--|
| \$000 | IM0 ($\overline{\text{INT}}_0$ interrupt mask) | IF0 ($\overline{\text{INT}}_0$ interrupt request flag) | RSP (Reset stack pointer) | IE (Interrupt enable flag) |
| \$001 | IMTA (Timer A interrupt mask) | IFTA (Timer A interrupt request flag) | IM1 ($\overline{\text{INT}}_1$ interrupt mask) | IF1 ($\overline{\text{INT}}_1$ interrupt request flag) |
| \$002 | IMTC (Timer C interrupt mask) | IFTC (Timer C interrupt request flag) | Not used | Not used |
| \$003 | IMS1 (Serial 1 interrupt mask) | IFS1 (Serial 1 interrupt request flag) | IMTD (Timer D interrupt mask) | IFTD (Timer D interrupt request flag) |

Interrupt control bits area

| RAM address | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------|---|---|---|---|
| \$020 | DTON (DTON flag) | Not used | WDON (Watchdog on flag) | LSON (Low speed on flag) |
| \$021 | RAME (RAM enable flag) | Not used | ICEF (Input capture error flag) | ICSF (Input capture status flag) |
| \$022 | IM3 (INT_3 interrupt mask) | IF3 (INT_3 interrupt request flag) | IM2 (INT_2 interrupt mask) | IF2 (INT_2 interrupt request flag) |
| \$023 | Not used | Not used | IM4 (INT_4 interrupt mask) | IF4 (INT_4 interrupt request flag) |

Register flag area

IF : Interrupt Request Flag
 IM : Interrupt Mask
 IE : Interrupt Enable Flag
 SP : Stack Pointer

Figure 3 Configuration of Interrupt Control Bits and Register Flag Areas

HD404669 Series

Bits in the interrupt control bits area and register flag area can be set and reset by the SEM or SEMD instruction and the REM or REMD instruction, and tested by the TM or TMD instruction. They are not affected by any other instructions. The following restrictions apply to individual bits.

| | SEM/SEMD | REM/REMD | TM/TMD |
|----------|-----------------------------|--------------|-----------|
| IE | Allowed | Allowed | Allowed |
| IM | | | |
| LSON | | | |
| IF | Not executed | Allowed | Allowed |
| ICSF | | | |
| ICEF | | | |
| RAME | | | |
| RSP | Not executed | Allowed | Inhibited |
| WDON | Allowed | Not executed | Inhibited |
| DTON | Not executed in active mode | Allowed | Allowed |
| | Used in subactive mode | | |
| Not used | Not executed | Not executed | Inhibited |

Note: WDON is reset by MCU reset or by $\overline{\text{STOPC}}$ enable for stop mode cancellation.
 DTON is always reset in active mode.
 If the TM or TMD instruction is executed for the inhibited bits or non-existing bits, the value in ST becomes invalid.

Figure 4 Usage Limitations of RAM Bit Manipulation Instructions

HD404669 Series

| | Bit 3 | Bit 2 | Bit 1 | Bit 0 | | | | |
|-----------------|---|---|---|-------------------------------------|-------------------------------|---|----------------------------------|--------------------------|
| \$000 | Interrupt control bits area | | | | | | | |
| \$001 | | | | | | | | |
| \$002 | | | | | | | | |
| \$003 | | | | | | | | |
| PMRA \$004 | | | R4 ₂ /SI ₁ | R4 ₃ /SO ₁ | | | | |
| SM1A \$005 | R4 ₁ /SCK ₁ | Serial transfer clock speed selection 1 | | | | | | |
| SR1L \$006 | Serial data register 1 (lower) | | | | | | | |
| SR1U \$007 | Serial data register 1 (upper) | | | | | | | |
| TMA \$008 | Timer A/time base | Clock source setting (timer A) | | | | | | |
| \$009 | | | | | | | | |
| \$00A | | | | | | | | |
| \$00B | | | | | | | | |
| MIS \$00C | | | | | MOS pull-up/pull-down control | R4 ₃ /SO ₁ PMOS control | Interrupt frame period selection | |
| TMC1 \$00D | Reload on/off | Clock source setting (timer C) | | | | | | |
| TRCL/TWCL \$00E | Timer C register (lower) | | | | | | | |
| TRCU/TWCU \$00F | Timer C register (upper) | | | | | | | |
| TMD1 \$010 | Reload on/off | Clock source setting (timer D) | | | | | | |
| TRDL/TWDL \$011 | Timer D register (lower) | | | | | | | |
| TRDU/TWDU \$012 | Timer D register (upper) | | | | | | | |
| \$013 | | | | | | | | |
| TMC2 \$014 | | | | | Timer C output mode setting | | | |
| TMD2 \$015 | | | | | Input capture selection | Timer D output mode setting | | |
| \$016 | | | | | | | | |
| CDR \$017 | | | COMP ₁ comparison result | COMP ₀ comparison result | | | | |
| CER \$018 | Comparator operation selection | Comparator selection | | | | | | |
| TGM \$019 | TONEC output frequency | | TONER output frequency | | | | | |
| TGC \$01A | TONEC output | TONER output | DTMF enable | | | | | |
| \$01B | | | | | | | | |
| \$01C | | | | | | | | |
| \$01D | | | | | | | | |
| \$01E | | | | | | | | |
| \$01F | | | | | | | | |
| \$020 | | | | | | | | |
| \$021 | Register flag area | | | | | | | |
| \$022 | | | | | | | | |
| \$023 | | | | | | | | |
| PMRB \$024 | R0 ₂ /INT ₄ | R0 ₂ /INT ₃ | R0 ₁ /INT ₂ | R0 ₇ /INT ₁ | | | | |
| PMRC \$025 | D ₁₃ /INT ₀ | D ₁₂ /STOPC | R4 ₇ /EVND | | | | | |
| ESR1 \$026 | INT ₃ detection edge selection | | INT ₂ detection edge selection | | | | | |
| ESR2 \$027 | EVND detection edge selection | | INT ₄ detection edge selection | | | | | |
| SM1B \$028 | | | SO1 idle High/Low setting | Serial clock selection | | | | |
| SSR1 \$029 | *1 | *2 | DTMF speed setting | | | | | |
| SSR2 \$02A | DTMF speed setting | | OSC frequency division ratio switching | | | | | |
| \$02B | | | | | | | | |
| DCD0 \$02C | | | | | Port D ₃ DCR | Port D ₂ DCR | Port D ₁ DCR | Port D ₀ DCR |
| DCD1 \$02D | | | Port D ₅ DCR | Port D ₄ DCR | | | | |
| DCD2 \$02E | Port D ₁₁ DCR | Port D ₁₀ DCR | Port D ₉ DCR | | | | | |
| \$02F | | | | | | | | |
| DCR0 \$030 | | | | | Port R0 ₃ DCR | Port R0 ₂ DCR | Port R0 ₁ DCR | Port R0 ₀ DCR |
| DCR1 \$031 | Port R1 ₃ DCR | Port R1 ₂ DCR | Port R1 ₁ DCR | Port R1 ₀ DCR | | | | |
| DCR2 \$032 | Port R2 ₃ DCR | Port R2 ₂ DCR | Port R2 ₁ DCR | Port R2 ₀ DCR | | | | |
| DCR3 \$033 | Port R3 ₃ DCR | Port R3 ₂ DCR | Port R3 ₁ DCR | Port R3 ₀ DCR | | | | |
| DCR4 \$034 | Port R4 ₃ DCR | Port R4 ₂ DCR | Port R4 ₁ DCR | Port R4 ₀ DCR | | | | |
| \$035 | | | | | | | | |
| DCR6 \$036 | | | | | Port R6 ₃ DCR | Port R6 ₂ DCR | Port R6 ₁ DCR | Port R6 ₀ DCR |
| DCR7 \$037 | Port R7 ₃ DCR | Port R7 ₂ DCR | Port R7 ₁ DCR | Port R7 ₀ DCR | | | | |
| DCR8 \$038 | Port R8 ₃ DCR | Port R8 ₂ DCR | Port R8 ₁ DCR | Port R8 ₀ DCR | | | | |
| DCR9 \$039 | Port R9 ₃ DCR | Port R9 ₂ DCR | Port R9 ₁ DCR | Port R9 ₀ DCR | | | | |
| DCRA \$03A | | | Port RA ₁ DCR | Port RA ₀ DCR | | | | |
| \$03B | | | | | | | | |
| \$03C | | | | | | | | |
| \$03D | | | | | | | | |
| \$03E | | | | | | | | |
| V \$03F | | | | Bank setting | | | | |

: Not used *1: 32kHz oscillation stop setting
 *2: 32kHz frequency division ratio switching

Figure 5 Special Function Register Area

HD404669 Series

Memory Register (MR) Area (\$040–\$04F): Consisting of 16 addresses, this area (MR0–MR15) can be accessed by register-register instructions (LAMR and XMRA). The structure is shown in figure 6.

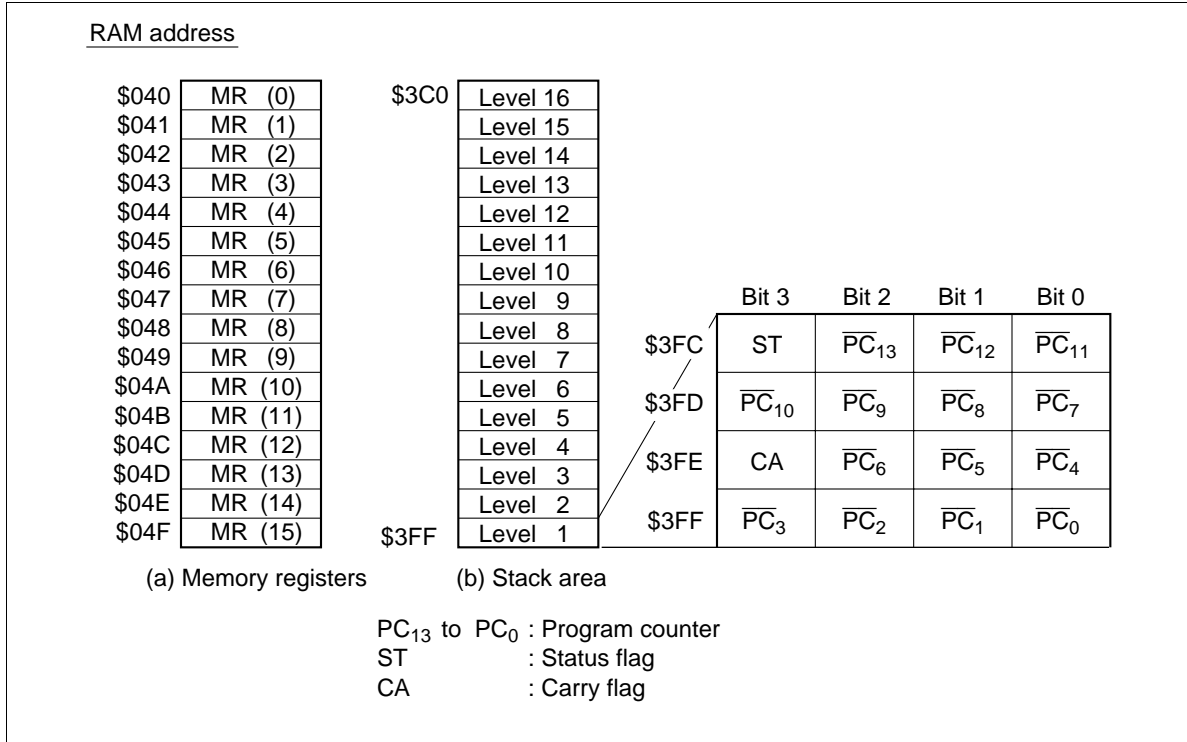


Figure 6 Configuration of Memory Registers and Stack Area, and Stack Position

Data Area (\$090–\$2EF): 464 digits from \$090 to \$25F have two banks, which can be selected by setting the bank register (V: \$03F). Before accessing this area, set the bank register to the required value (figure 7). The area from \$026 to \$2EF is accessed without setting the bank register.

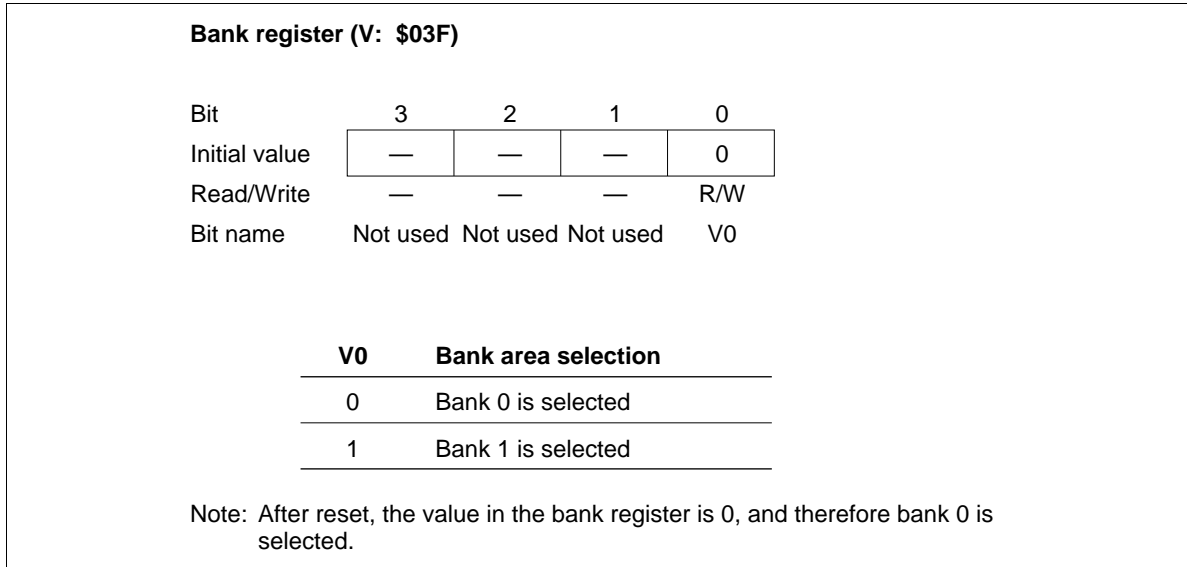


Figure 7 Bank Register (V)

Stack Area (\$3C0–\$3FF): Used for saving the contents of the program counter (PC), status flag (ST), and carry flag (CA) at subroutine call (CAL or CALL instruction) and for interrupts. This area can be used as a 16-level nesting subroutine stack in which one level requires four digits. The data to be saved and the save conditions are shown in figure 6.

The program counter is restored by either the RTN or RTNI instruction, but the status and carry flags can only be restored by the RTNI instruction. Any unused space in this area is used for data storage.

HD404669 Series

Functional Description

Registers and Flags

The MCU has nine registers and two flags for CPU operations. They are shown in figure 8 and described below.

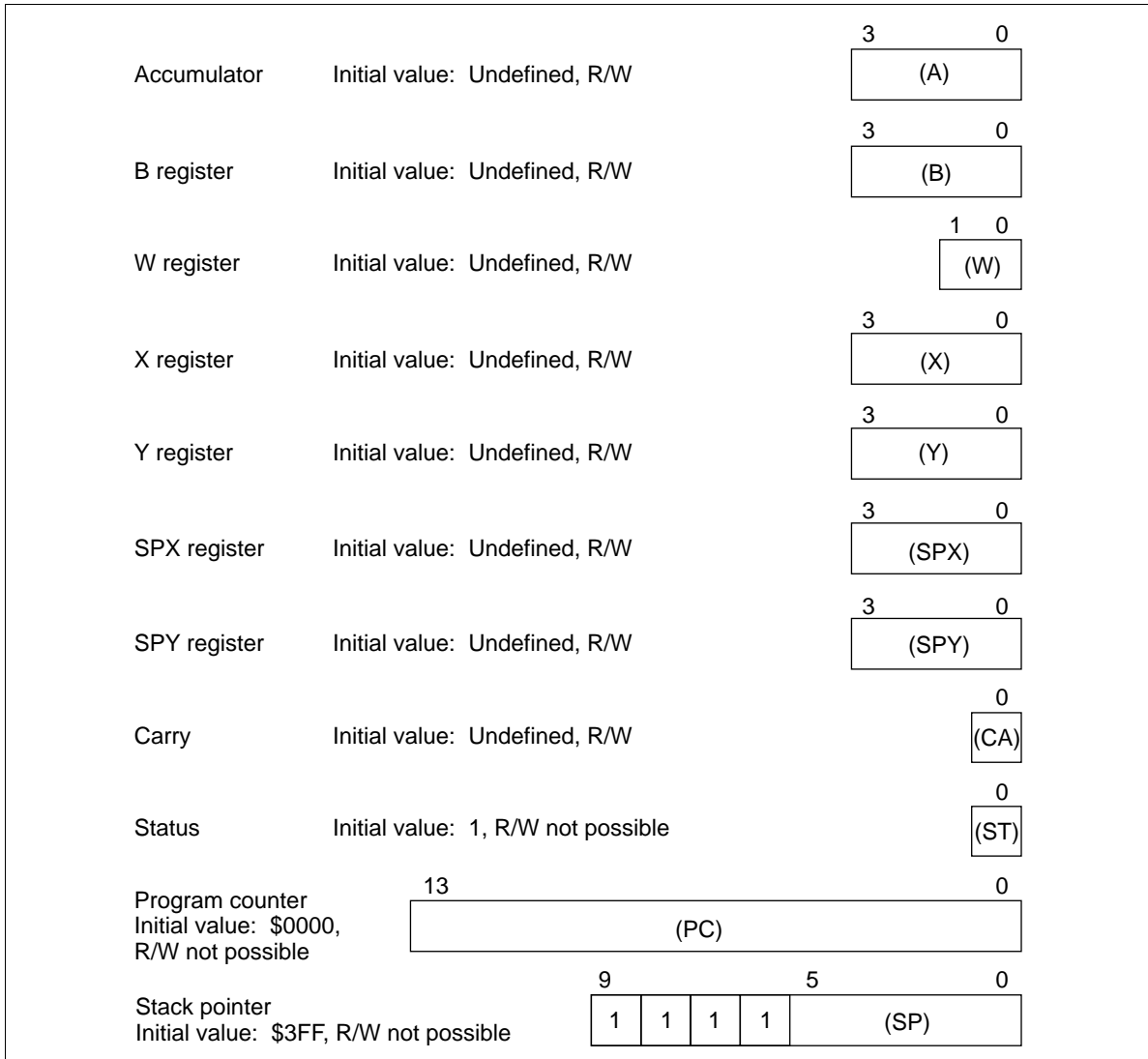


Figure 8 Registers and Flags

Accumulator (A) and B Register (B): A and B are 4-bit registers, and are used to hold the results of ALU (arithmetic and logical unit) operations and to transfer data between memory, I/O ports, and other registers.

W Register (W), X Register (X), and Y Register (Y): W is a 2-bit register and X and Y are 4-bit registers. These registers are used in RAM register indirect addressing. The Y register is also used in D port addressing.

SPX Register (SPX) and SPY Register (SPY): The SPX and SPY registers are 4-bit registers used to supplement the X and Y registers.

Carry Flag (CA): CA is a 1-bit flag that stores ALU overflow generated by an arithmetic operation. CA is set to 1 when an overflow is generated, and is cleared to 0 after operations in which no overflow occurred. CA is also affected by the carry set/carry clear instructions (SEC and REC), and by the rotate with carry instructions (ROTL and ROTR).

During interrupt handling, CA is saved on the stack, and is restored from the stack by the RTNI instruction. (but is not affected by the RTN instruction)

Status Flag (ST): ST is a 1-bit flag that stores the results of arithmetic instructions, compare instructions, and bit test instructions, and is used as the branch condition for the BR, BRL, CAL, and CALL conditional branch instructions.

The contents of the ST flag are held until the next arithmetic, compare, bit test, or conditional branch instruction is executed. After the execution of a conditional branch instruction, the value of ST is set to 1 without regard to the condition.

During interrupt handling, ST is saved on the stack, and is restored from the stack by the RTNI instruction. (but is not affected by the RTN instruction)

Program Counter (PC): The PC is a 14-bit counter that indicates the ROM address of the next instruction the CPU will execute.

Stack Pointer (SP): The SP is a 10-bit register that indicates the RAM address of the next stack frame in the stack area.

The SP is initialized to \$3FF by a reset. The SP is decremented by 4 by a subroutine call or by interrupt handling, and is incremented by 4 when the saved data has been restored by a return instruction.

The upper 4 bits of the SP are fixed at 1111; the maximum number of stack levels is thus 16.

In addition to the reset method described above, the SP can also be initialized to \$3FF by clearing the reset stack pointer (RSP) in the interrupt control bits area with a RAM bit manipulation instruction, i.e., REM or REMD.

HD404669 Series

Reset

The MCU can be reset by setting the RESET pin high or by setting the $\overline{\text{STOPC}}$ pin low*. When power is first applied, or when clearing subactive mode, watch mode, or stop mode, the RESET input must be held for at least t_{RC} to assure that the oscillation stabilization time (t_{RC}) condition is fulfilled.

Similarly, the $\overline{\text{STOPC}}$ pin input must be held for at least t_{RC} when clearing stop mode with a $\overline{\text{STOPC}}$ pin input to assure that the oscillator stabilizes.

In all other cases, the MCU is reset by a RESET input that is held for at least two instruction execution cycles.

Table 1 lists the section of the MCU that are initialized by a reset and the initial values.

Note: * The $\overline{\text{STOPC}}$ pin reset is only effective in stop mode.

Table 1 Initial Values After MCU Reset

| Item | Abbr. | Initial Value | Contents |
|----------------------------------|---|---------------|--|
| Program counter | (PC) | \$0000 | Indicates program execution point from start address of ROM area |
| Status flag | (ST) | 1 | Enables conditional branching |
| Stack pointer | (SP) | \$3FF | Stack level 0 |
| Interrupt flags/mask | Interrupt enable flag (IE) | 0 | Inhibits all interrupts |
| | Interrupt request flag (IF) | 0 | Indicates there is no interrupt request |
| | Interrupt mask (IM) | 1 | Prevents (masks) interrupt requests |
| I/O | Port data register (PDR) | All bits 1 | Enables output at level 1 |
| | Data control register (DCD0) | 0000 | Turns output buffer off (to high impedance) |
| | Data control register (DCD1) | --00 | |
| | Data control register (DCD2) | 000- | |
| | Data control register (DCR0–DCR4, DCR6–DCR9) | 0000 | |
| | Data control register (DCRA) | --00 | |
| | Port mode register A (PMRA) | --00 | Refer to description of port mode register A |
| | Port mode register B (PMRB) | 0000 | Refer to description of R port |
| | Port mode register C bits 3, 1, 0 (PMRC3, PMRC1, PMRC0) | 00- | Refer to description of port mode register C |
| | Detection Edge select registers 1 and 2 (ESR1, 2) | 0000 | Refer to description of interrupts |
| Timer/counters, serial interface | Timer mode register A (TMA) | 0000 | Refer to description of timer mode register A section |
| | Timer mode register C1 (TMC1) | 0000 | Refer to description of timer mode register C1 |
| | Timer mode register C2 (TMC2) | -000 | Refer to description of timer mode register C2 |
| | Timer mode register D1 (TMD1) | 0000 | Refer to description of timer mode register D1 |
| | Timer mode register D2 (TMD2) | 0000 | Refer to description of timer mode register D2 |
| | Serial mode register 1A (SM1A) | 0000 | Refer to description of serial mode register 1A |
| | Serial mode register 1B (SM1B) | --X0 | Refer to description of serial mode register 1B |
| | Prescaler S (PSS) | \$000 | Refer to description of prescalers |
| | Prescaler W (PSW) | \$00 | Refer to description of prescalers |
| | Timer counter A (TCA) | \$00 | Refer to description of timer A |
| | Timer counter C (TCC) | \$00 | Refer to description of timer C |
| | Timer counter D (TCD) | \$00 | Refer to description of timer D |

HD404669 Series

| Item | | Abbr. | Initial Value | Contents |
|--|--|----------------|---------------|--|
| Timer/ counters, serial interface | Timer write register C | (TWCU, L) | \$X0 | Refer to description of timer write register C |
| | Timer write register D | (TWDU, L) | \$X0 | Refer to description of timer write register D |
| | Serial data register 1 | (SR1U, L) | \$XX | Refer to description of serial data register 1 |
| | Octal counter | (OC1) | 000 | Refer to description of serial interface |
| DTMF | Tone generator mode register | (TGM) | 0000 | Refer to description of tone generator mode register |
| | Tone generator control register | (TGC) | 000 - | Refer to description of tone generator control register |
| Comparator | Compare data register | (CDR) | --XX | Refer to description of compare data register |
| | Compare enable register | (CER) | 0-00 | Refer to description of compare enable register |
| Bit registers | Low speed on flag | (LSON) | 0 | Refer to description of operating modes |
| | Watchdog timer on flag | (WDON) | 0 | Refer to description of timer C |
| | Direct transfer on flag | (DTON) | 0 | Refer to description of operating modes |
| | Input capture status flag | (ICSF) | 0 | Refer to description of timer D |
| | Input capture error flag | (ICEF) | 0 | Refer to description of timer D |
| Others | Miscellaneous register | (MIS) | 0000 | Refer to description of operating modes and pull-up and pull-down MOS transistor control. |
| | System clock select register 1 bits 2 to 0 | (SSR12 -SSR10) | 000 | Refer to description of internal oscillator circuit and system clock select register 1 and 2 |
| | System clock select register 2 | (SSR2) | 0000 | Refer to description of internal oscillator circuit and system clock select register 1 and 2 |
| | Bank register | (V) | --0 | Refer to description of RAM memory map |

- Notes: 1. The statuses of other registers and flags after MCU reset are shown in the following table.
 2. X indicates invalid value. – indicates that the bit does not exist.

| Item | Abbr. | Status After Cancel-lation of Stop Mode by STOPC Input | Status After all Other Types of Reset |
|--------------------------------------|---------|--|--|
| Carry flag | (CA) | Pre-stop-mode values are not guaranteed; values must be initialized by program | Pre-MCU-reset values are not guaranteed; values must be initialized by program |
| Accumulator | (A) | | |
| B register | (B) | | |
| W register | (W) | | |
| X/SPX register | (X/SPX) | | |
| Y/SPY register | (Y/SPY) | | |
| RAM | | Pre-stop-mode values are retained | |
| RAM enable flag | (RAME) | 1 | 0 |
| Port mode register C bit 2 | (PMRC2) | Pre-stop-mode values are retained | 0 |
| System clock select register 1 bit 3 | (SSR13) | | |

Interrupts

The MCU has 9 interrupt sources: five external signals ($\overline{\text{INT}}_0$, $\overline{\text{INT}}_1$, INT_2 – INT_4), three timer/ counters (timers A, C, and D), serial interface (Serial 1).

An interrupt request flag (IF), interrupt mask (IM), and vector address are provided for each interrupt source, and an interrupt enable flag (IE) controls the entire interrupt process.

As vector addresses are shared by interrupt sources timer C and INT_3 , and timer D and INT_4 , so the type of request that has occurred must be checked at the beginning of interrupt processing.

Interrupt Control Bits and Interrupt Processing: Locations \$000 to \$003 and \$022 to \$023 in RAM are reserved for the interrupt control bits which can be accessed by RAM bit manipulation instructions.

The interrupt request flag (IF) cannot be set by software. MCU reset initializes the interrupt enable flag (IE) and the IF to 0 and the interrupt mask (IM) to 1.

A block diagram of the interrupt control circuit is shown in figure 9, interrupt priorities and vector addresses are listed in table 2, and interrupt processing conditions for the 9 interrupt sources are listed in table 3.

An interrupt request occurs when the IF is set to 1 and the IM is set to 0. If the IE is 1 at that point, the interrupt is processed. A priority programmable logic array (PLA) generates the vector address assigned to that interrupt source.

The interrupt processing sequence is shown in figure 10 and an interrupt processing flowchart is shown in figure 11. After an interrupt is acknowledged, the previous instruction is completed in the first cycle. The IE is reset in the second cycle, the carry, status, and program counter values are pushed onto the stack during the second and third cycles, and the program jumps to the vector address to execute the instruction in the third cycle.

Program the JMPL instruction at each vector address, to branch the program to the start address of the interrupt program, and reset the IF by a software instruction within the interrupt program.

Table 2 Vector Addresses and Interrupt Priorities

| Reset/Interrupt | Priority | Vector Address |
|------------------------------------|----------|----------------|
| RESET, $\overline{\text{STOPC}}$ * | — | \$0000 |
| $\overline{\text{INT}}_0$ | 1 | \$0002 |
| $\overline{\text{INT}}_1$ | 2 | \$0004 |
| Timer A | 3 | \$0006 |
| INT_2 | 4 | \$0008 |
| Timer C, INT_3 | 5 | \$000A |
| Timer D, INT_4 | 6 | \$000C |
| Serial 1 | 7 | \$000E |

Note: * The $\overline{\text{STOPC}}$ interrupt request is valid only in stop mode.

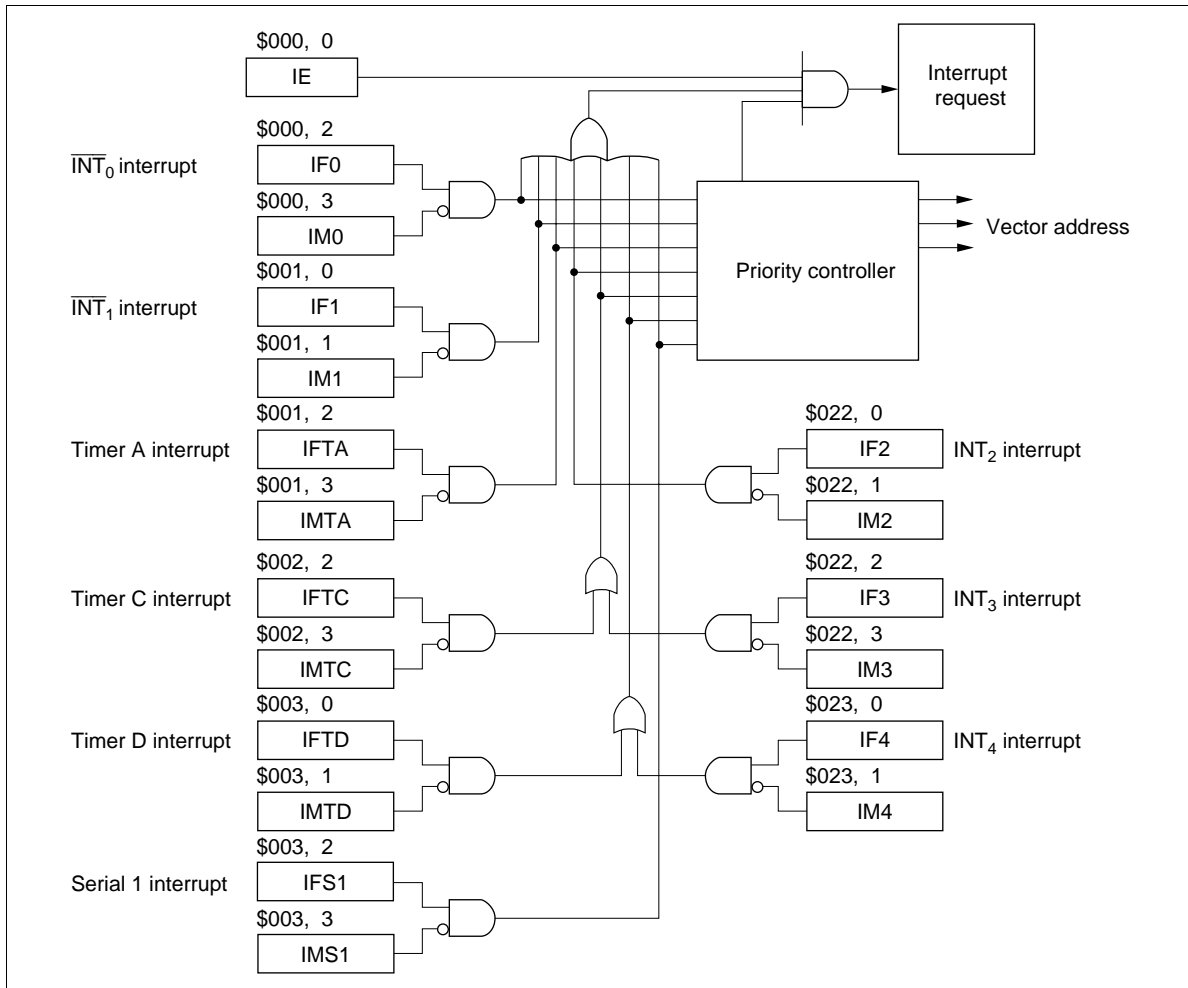


Figure 9 Interrupt Control Circuit

Table 3 Interrupt Processing and Activation Conditions

| Interrupt Control Bit | Interrupt Source | | | | | | |
|--|--------------------|--------------------|---------|---------|--------------------|--------------------|----------|
| | \overline{INT}_0 | \overline{INT}_1 | Timer A | INT_2 | Timer C or INT_3 | Timer D or INT_4 | Serial 1 |
| IE | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $IF0 \cdot \overline{IM0}$ | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| $IF1 \cdot \overline{IM1}$ | * | 1 | 0 | 0 | 0 | 0 | 0 |
| $IFTA \cdot \overline{IMTA}$ | * | * | 1 | 0 | 0 | 0 | 0 |
| $IF2 \cdot \overline{IM2}$ | * | * | * | 1 | 0 | 0 | 0 |
| $IFTC \cdot \overline{IMTC}$ + $IF3 \cdot \overline{IM3}$ | * | * | * | * | 1 | 0 | 0 |
| $IFTD \cdot \overline{IMTD}$ + $IF4 \cdot \overline{IM4}$ | * | * | * | * | * | 1 | 0 |
| $IFS1 \cdot \overline{IMS}_1$ | * | * | * | * | * | * | 1 |

Note: Bits marked * can be either 0 or 1. Their values have no effect on operation.

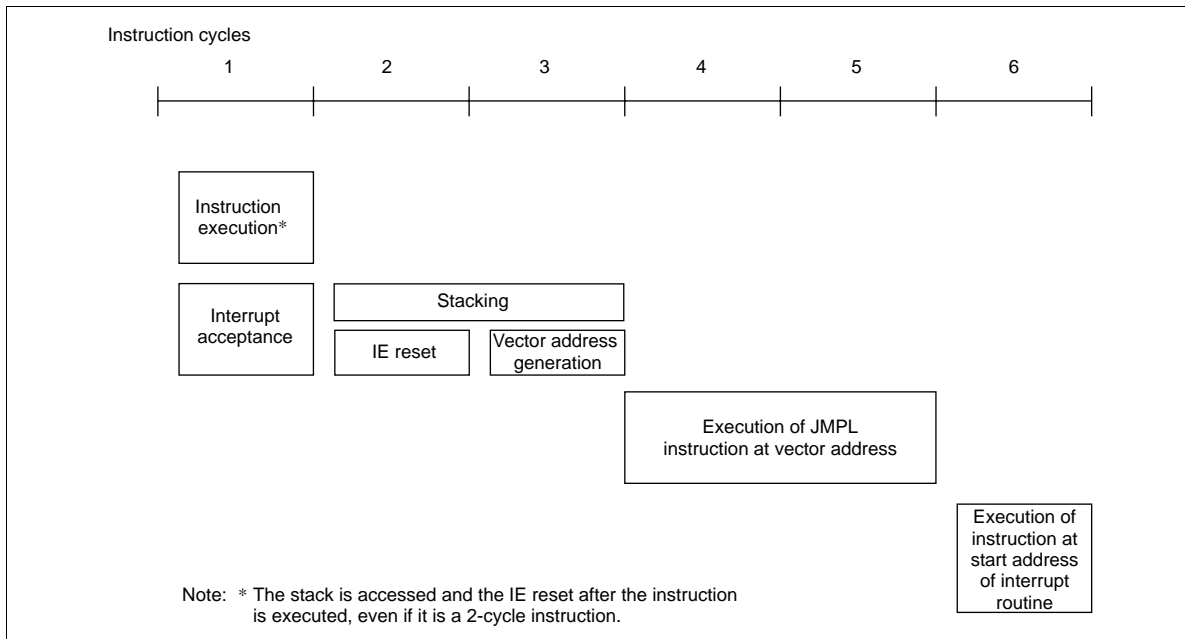


Figure 10 Interrupt Sequence

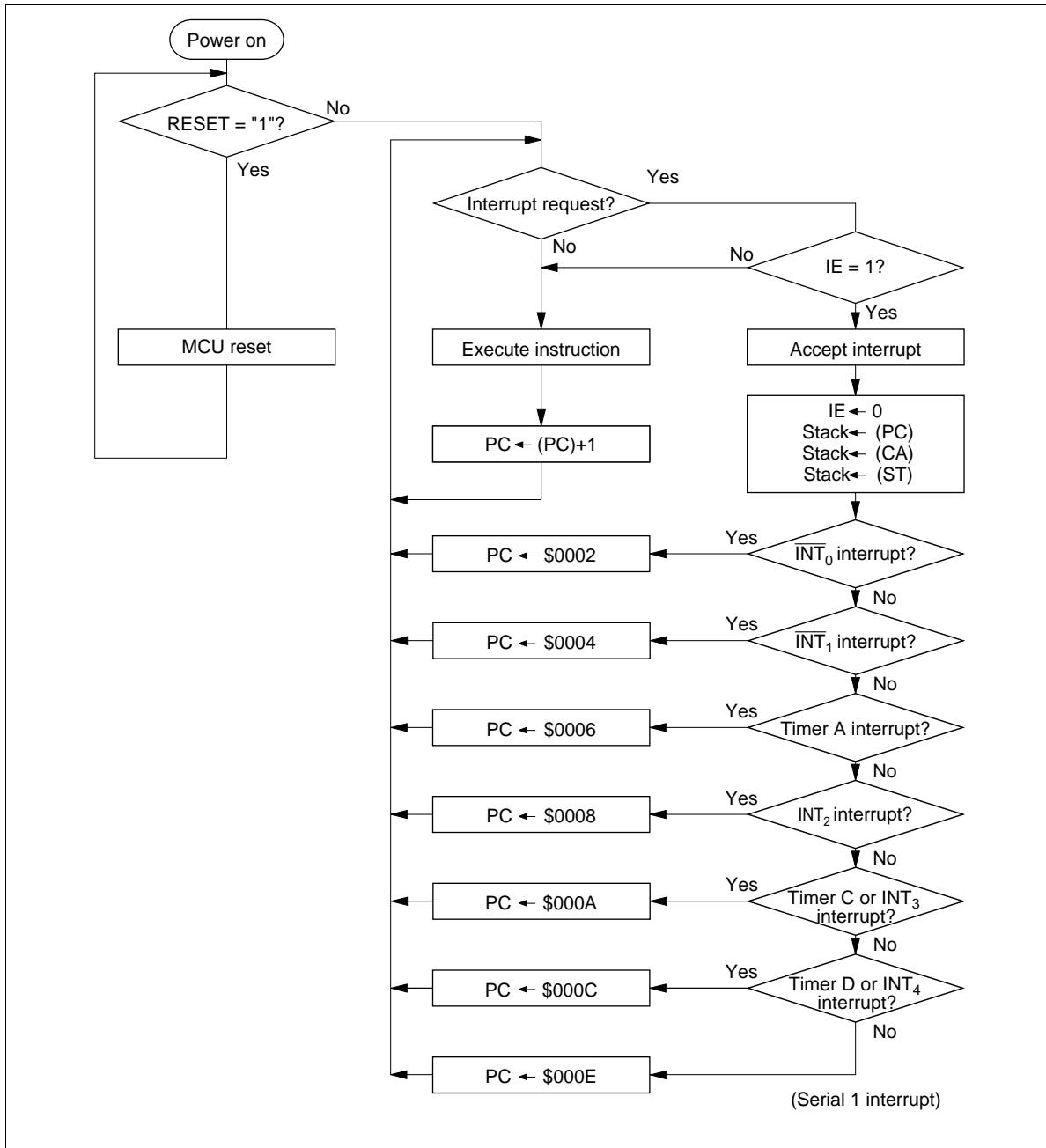


Figure 11 Interrupt Processing Flowchart

Interrupt Enable Flag (IE: \$000, Bit 0): Controls the entire interrupt process. It is reset by the interrupt processing and set by the RTNI instruction, as listed in table 4.

Table 4 Interrupt Enable Flag (IE: \$000, Bit 0)

| IE | Interrupt Enabled/Disabled |
|----|----------------------------|
| 0 | Disabled |
| 1 | Enabled |

External Interrupt Request Flags (IF0–IF4: \$000, \$001, \$022, \$023): IF0 and IF1 are set at the falling edge of signals input to \overline{INT}_0 and \overline{INT}_1 , and IF2–IF4 are set at the rising or falling edge of signals input to \overline{INT}_2 – \overline{INT}_4 , as listed in table 5. The \overline{INT}_2 – \overline{INT}_4 interrupt edges are selected by the detection edge select registers (ESR1, ESR2: \$026, \$027) as shown in figures 12 and 13.

| Detection edge selection register 1 (ESR1: \$026) | | | | | |
|---|--------------|---------------------------------------|--------------|--------------|---------------------------------------|
| Bit | 3 | 2 | 1 | 0 | |
| Initial value | 0 | 0 | 0 | 0 | |
| Read/Write | W | W | W | W | |
| Bit name | ESR13 | ESR12 | ESR11 | ESR10 | |
| ESR13 | ESR12 | INT₃ detection edge | ESR11 | ESR10 | INT₂ detection edge |
| 0 | 0 | No detection | 0 | 0 | No detection |
| | 1 | Falling-edge detection | | 1 | Falling-edge detection |
| 1 | 0 | Rising-edge detection | 1 | 0 | Rising-edge detection |
| | 1 | Falling/Rising-edge detection | | 1 | Falling/Rising-edge detection |

Figure 12 Detection Edge Selection Register 1 (ESR1)

HD404669 Series

| Detection edge selection register 2 (ESR2: \$027) | | | | | |
|---|-------|-------|-------|-------|--|
| Bit | 3 | 2 | 1 | 0 | |
| Initial value | 0 | 0 | 0 | 0 | |
| Read/Write | W | W | W | W | |
| Bit name | ESR23 | ESR22 | ESR21 | ESR20 | |

| ESR23 | ESR22 | EVND detection edge | ESR21 | ESR20 | INT ₄ detection edge |
|-------|-------|-------------------------------|-------|-------|---------------------------------|
| 0 | 0 | No detection | 0 | 0 | No detection |
| | 1 | Falling-edge detection | | 1 | Falling-edge detection |
| 1 | 0 | Rising-edge detection | 1 | 0 | Rising-edge detection |
| | 1 | Falling/Rising-edge detection | | 1 | Falling/Rising-edge detection |

Figure 13 Detection Edge Selection Register 2 (ESR2)

Table 5 External Interrupt Request Flags (IF0–IF4: \$000, \$001, \$022, \$023)

| IF0–IF4 | Interrupt Request |
|---------|-------------------|
| 0 | No |
| 1 | Yes |

External Interrupt Masks (IM0–IM4: \$000, \$001, \$022, \$023): Prevent (mask) interrupt requests caused by the corresponding external interrupt request flags, as listed in table 6.

Table 6 External Interrupt Masks (IM0–IM4: \$000, \$001, \$022, \$023)

| IM0–IM4 | Interrupt Request |
|---------|-------------------|
| 0 | Enabled |
| 1 | Disabled (masked) |

Timer A Interrupt Request Flag (IFTA: \$001, Bit 2): Set by overflow output from timer A, as listed in table 7.

Table 7 Timer A, C, D Interrupt Request Flags
(IFTA: \$001, Bit 2, IFTC: \$002, Bit 2, IFTD: \$003, Bit 0)

| Timer A, C, D Interrupt Request Flags (IFTA, IFTC, IFTD) | Interrupt Request |
|--|-------------------|
| 0 | No |
| 1 | Yes |

Timer A Interrupt Mask (IMTA: \$001, Bit 3): Prevents (masks) an interrupt request caused by the timer A interrupt request flag, as listed in table 8.

Table 8 Timer A, C, D Interrupt Masks (IMTA: \$001, Bit 3, IMTC: \$002, Bit 3, IMTD: \$003, Bit 1)

| Timer A, C, D Interrupt Masks (IMTA, IMTC, IMTD) | Interrupt Request |
|--|-------------------|
| 0 | Enabled |
| 1 | Disabled (masked) |

Timer C Interrupt Request Flag (IFTC: \$002, Bit 2): Set by overflow output from timer C, as listed in table 7.

Timer C Interrupt Mask (IMTC: \$002, Bit 3): Prevents (masks) an interrupt request caused by the timer C interrupt request flag, as listed in table 8.

Timer D Interrupt Request Flag (IFTD: \$003, Bit 0): Set by overflow output from timer D, or by the rising or falling of signals input to EVND when the input capture function is used, as listed in table 7.

Timer D Interrupt Mask (IMTD: \$003, Bit 1): Prevents (masks) an interrupt request caused by the timer D interrupt request flag, as listed in table 8.

Serial 1 Interrupt Request Flag (IFS1: \$003, Bit 2): Set when data transfer is completed or when data transfer is suspended, as listed in table 9.

Table 9 Serial 1 Interrupt Request Flag (IFS1: \$003, Bit 2)

| IFS1 | Interrupt Request |
|------|-------------------|
| 0 | No |
| 1 | Yes |

HD404669 Series

Serial 1 Interrupt Mask (IMS1: \$003, Bit 3): Prevents (masks) an interrupt request caused by the serial 1 interrupt request flag, as listed in table 10.

Table 10 Serial 1 Interrupt Mask (IMS1: \$003, Bit 3)

| IMS1 | Interrupt Request |
|-------------|--------------------------|
| 0 | Enabled |
| 1 | Disabled (masked) |

Operating Modes

The MCU has five operating modes as shown in table 11. The operations in each mode are listed in table 12. Transitions between operating modes are shown in figure 14.

Table 11 **Operating Modes and Clock Status**

| | | Mode Name | | | | |
|---------------------|----------------------|---|--------------------------------|--|---|--|
| | | Active | Standby | Stop | Watch | Subactive* ² |
| Activation method | | RESET cancellation, interrupt request, $\overline{\text{STOPC}}$ cancellation in stop mode, STOP/SBY instruction in subactive mode (when direct transfer is selected) | SBY instruction | STOP instruction when TMA3 = 0 | STOP instruction when TMA3 = 1 | $\overline{\text{INT}}_0$ or timer A interrupt request from watch mode when LSON = 1 |
| Status | System oscillator | Operation | Operation | Stopped | Stopped | Stopped |
| | Subsystem oscillator | Operation | Operation | * ¹ | Operation | Operation |
| Cancellation method | | RESET input, STOP/SBY instruction | RESET input, interrupt request | RESET input, $\overline{\text{STOPC}}$ input | RESET input, $\overline{\text{INT}}_0$ or timer A interrupt request | RESET input, STOP/SBY instruction |

Notes: 1. Operating or stopping the oscillator can be selected by setting bit 3 of the system clock select register (SSR: \$029).

2. Subactive mode is an optional function; specify it on the function option list.

HD404669 Series

Table 12 Operations in Low-Power Dissipation Modes

| Function | Stop Mode | Watch Mode | Standby Mode | Subactive Mode*2 |
|--------------------|---------------------------|------------|--------------|------------------|
| CPU | Reset | Retained | Retained | Operation |
| RAM | Retained | Retained | Retained | Operation |
| Timer A | Reset | Operation | Operation | Operation |
| Timer C | Reset | Stopped | Operation | Operation |
| Timer D | Reset | Stopped | Operation | Operation |
| Serial interface 1 | Reset | Stopped *1 | Operation | Operation |
| DTMF | Reset | Reset | Operation | Reset |
| Comparator | Reset | Stopped | Stopped | Operation |
| I/O | Reset (high-impedance) | Retained | Retained | Operation |

Notes: 1. When a clock is input in external clock mode, transmit/receive operations are performed, but interrupt operations are halted.

2. Subactive mode is a function option, and should be specified in the function option list.

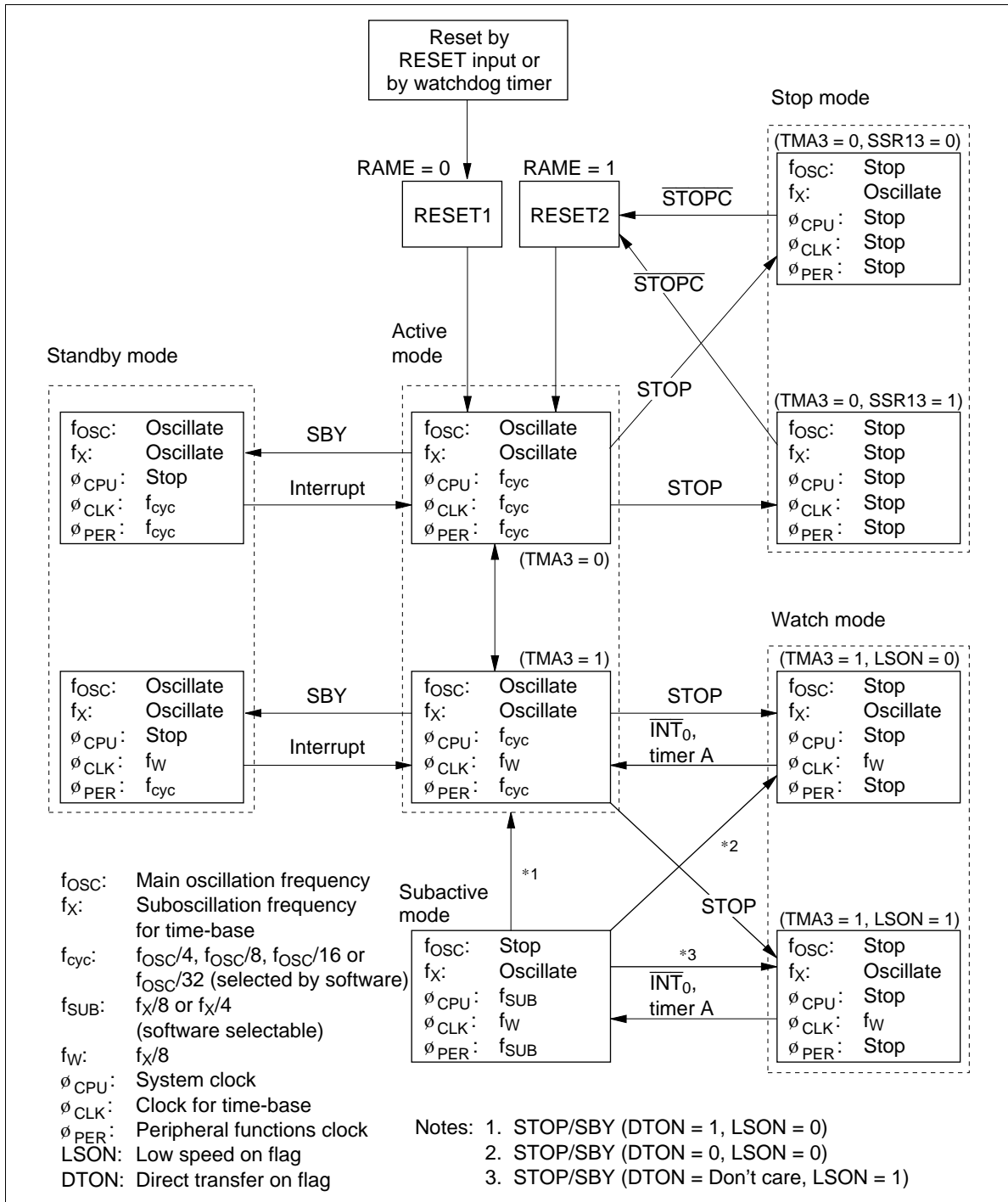


Figure 14 MCU Status Transitions

HD404669 Series

Active Mode: All MCU functions operate according to the clock generated by the system oscillator OSC₁ and OSC₂.

Standby Mode: In standby mode, the oscillators continue to operate, but the clocks related to instruction execution stop. Therefore, the CPU operation stops, but all RAM and register contents are retained, and the D or R port status, when set to output, is maintained. Peripheral functions such as interrupts, timers, and serial interface continue to operate. The power dissipation in this mode is lower than in active mode because the CPU stops. (Interrupts, timers, the serial interface, and other peripheral functions continue to operate. The exception is the comparator, which is halted.)

The MCU enters standby mode when the SBY instruction is executed in active mode.

Standby mode is terminated by a RESET input or an interrupt request. If it is terminated by RESET input, the MCU is reset as well. After an interrupt request, the MCU enters active mode and executes the next instruction after the SBY instruction. If the interrupt enable flag is 1, the interrupt is then processed; if it is 0, the interrupt request is left pending and normal instruction execution continues. Figure 15 shows a flowchart of MCU operation.

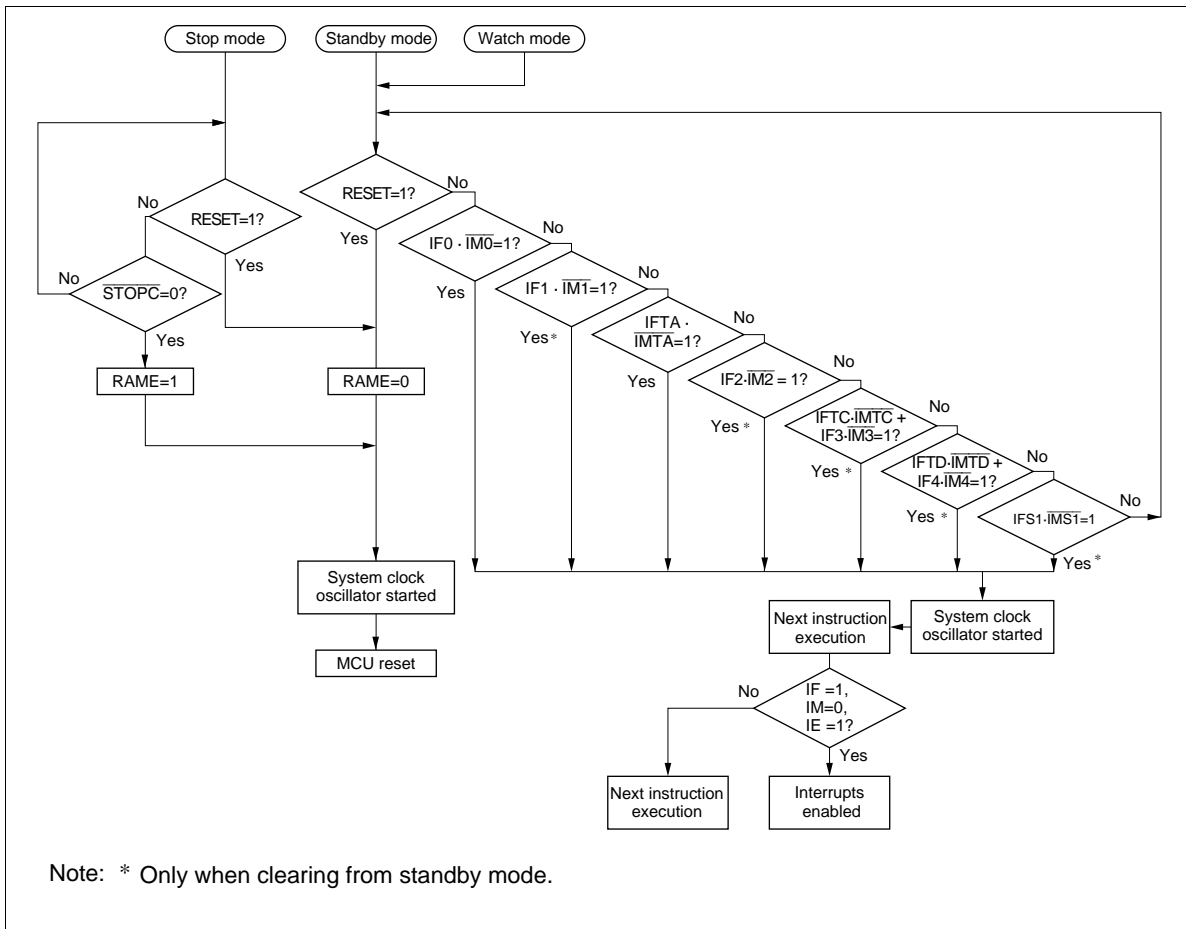


Figure 15 MCU Operation Flowchart

Stop Mode: In stop mode, all MCU operations stop and RAM data is retained. Therefore, the power dissipation in this mode is the least of all modes. The OSC₁ and OSC₂ oscillator stops. For the X1 and X2 oscillator to operate or stop can be selected by setting bit 3 of the system clock select register 1 (SSR1: \$029; operating: SSR13 = 0, stop: SSR13 = 1) (figure 24). The MCU enters stop mode if the STOP instruction is executed in active mode when bit 3 of timer mode register A (TMA: \$008) is set to 0 (TMA3 = 0) (figure 40).

Stop mode is cleared by a RESET or $\overline{\text{STOPC}}$ * input. The RESET or $\overline{\text{STOPC}}$ input must be held for at least the oscillation stabilization time (t_{RC}) as shown in figure 16. (refer to the "AC Characteristics" section.) In either of these cases, the MCU will start program execution from the program start address (location 0). However, the value of the RAM enable flag (RAME: \$021,3) will be different in these cases. In particular, RAME will be set to 0 for a RESET input and will be set to 1 for a $\overline{\text{STOPC}}$ input.

Also note that while a RESET input is effective in all MCU modes, $\overline{\text{STOPC}}$ is only effective in stop mode, and is ignored in all other modes.

If a program needs to determine if stop mode was cleared by a $\overline{\text{STOPC}}$ input (for example, if the program intends to use the contents of RAM that were stored before stop mode was entered after returning to active mode) the program should test the RAM enable flag with a TEST instruction at the start of the program.

Note: * If stop mode is to be cleared by a $\overline{\text{STOPC}}$ input, applications should set bit 2 of port mode register C (PMRC) to 1 (PMRC2 = 1) before switching to stop mode.

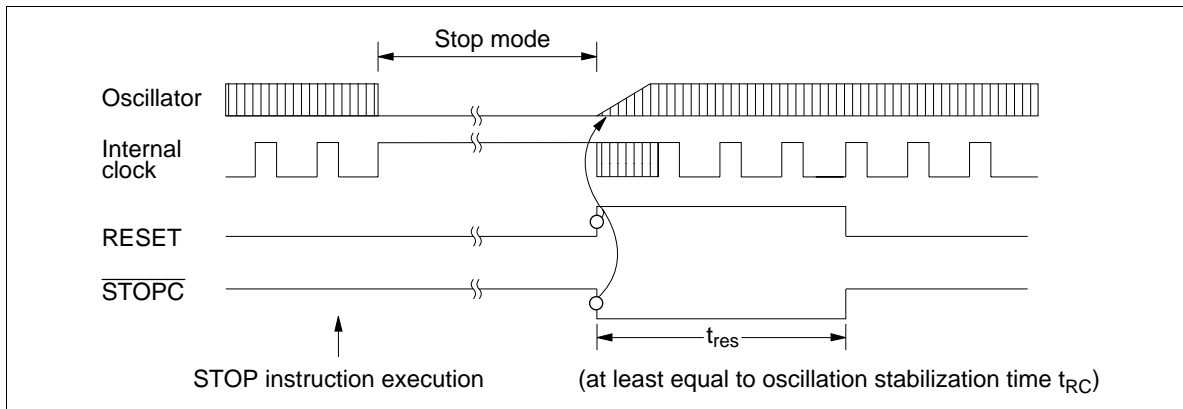


Figure 16 Timing of Stop Mode Cancellation

Watch Mode: In watch mode, the clock function (timer A) using the X1 and X2 oscillator, but other function operations stop. Therefore, the power dissipation in this mode is the second least to stop mode, and this mode is convenient when only clock display is used. In this mode, the OSC₁ and OSC₂ oscillator stops, but the X1 and X2 oscillator operates. The MCU is switched to watch mode by executing a STOP instruction while TMA3 = 1 in active mode, or by executing a STOP/SBY instruction while LSON is set to 1 or DTON is cleared to 0 in subactive mode.

Watch mode is terminated by a RESET input or a timer-A/ $\overline{\text{INT}}_0$ interrupt request. For details of RESET input, refer to the Stop Mode section. When terminated by a timer-A/ $\overline{\text{INT}}_0$ interrupt request, the MCU enters active mode if LSON = 0, or subactive mode if LSON = 1. After an interrupt request is generated, the time required to enter active mode is t_{RC} for a timer A interrupt, and T_X (where $T + t_{RC} < T_X < 2T + t_{RC}$) for an $\overline{\text{INT}}_0$ interrupt, as shown in figures 17 and 18.

HD404669 Series

Operation during mode transition is the same as that at standby mode cancellation (figure 15).

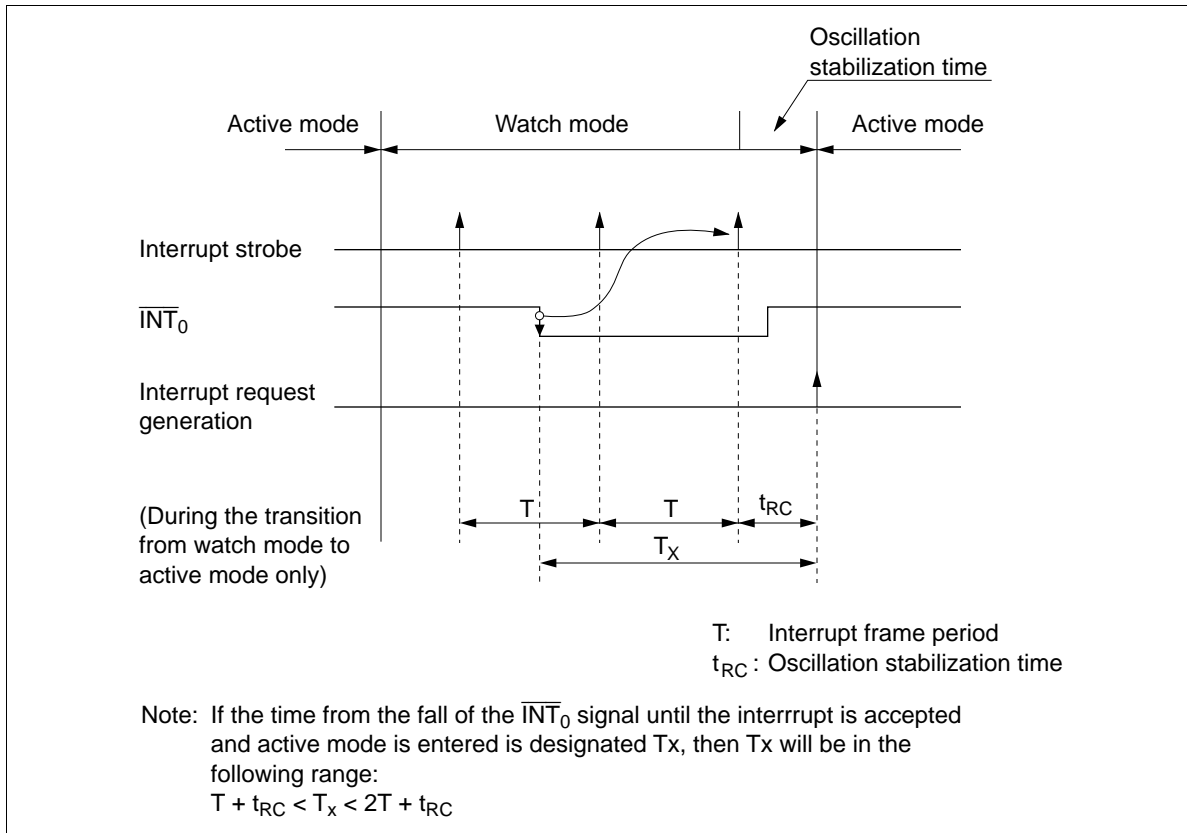


Figure 17 Interrupt Frame

Subactive Mode: The OSC₁ and OSC₂ oscillator stops and the MCU operates with a clock generated by the X1 and X2 oscillator. In this mode, functions other than the DTMF generation circuit operate, but since the operating clocks are slow, power consumption is the lowest after watch mode.

The CPU instruction execution speed can be selected as 244 μs or 122 μs by setting bit 2 (SSR12) of the system clock select register (SSR1: \$029). Note that the SSR12 value must be changed in active mode. If the value is changed in subactive mode, the MCU may malfunction.

When the STOP or SBY instruction is executed in subactive mode, the MCU enters either watch or active mode, depending on the statuses of the low speed on flag (LSON: \$020, bit 0) and the direct transfer on flag (DTON: \$020, bit 3).

Subactive mode is an optional function that the user must specify on the function option list.

Interrupt Frame: In watch and subactive modes, φ_{CLK} is applied to timer A and the $\overline{\text{INT}}_0$ circuit. Prescaler W and timer A operate as the time-base and generate the timing clock for the interrupt frame. Three interrupt frame periods (T) can be selected by setting the miscellaneous register (MIS: \$00C) (figure 18).

In watch and subactive modes, the timer-A/ $\overline{\text{INT}}_0$ interrupt is generated synchronously with the interrupt frame. The interrupt request is generated synchronously with the interrupt strobe timing except during transition to active mode. An overflow and interrupt request in timer A is generated synchronously with the interrupt strobe timing.

| Miscellaneous register (MIS: \$00C) | | | | | | |
|---|------|------|------|-----------------|--------------------------------|--------------------------------|
| Bit | 3 | 2 | 1 | 0 | | |
| Initial value | 0 | 0 | 0 | 0 | | |
| Read/Write | W | W | W | W | | |
| Bit name | MIS3 | MIS2 | MIS1 | MIS0 | | |
| MIS3 | MIS2 | MIS1 | MIS0 | T* ¹ | t _{RC} * ¹ | Oscillation circuit conditions |
| Buffer control. See figure 37 in the pull-up and pull-down MOS transistor control section | | 0 | 0 | 0.24414 ms | 0.12207 ms | External clock input |
| | | | | | 0.24414 ms* ² | |
| | | 0 | 1 | 15.625 ms | 7.8125 ms | Ceramic oscillator |
| | | 1 | 0 | 62.5 ms | 31.25 ms | Crystal oscillator |
| | | 1 | 1 | Not used | Not used | — |

Notes: 1. Values of T and t_{RC} when a 32.768-kHz crystal oscillator is used to pins x1 and x2.
2. The value is applied only when direct transfer operation is used.

Figure 18 Miscellaneous Register (MIS)

HD404669 Series

Direct Transition from Subactive Mode to Active Mode: Available by controlling the direct transfer on flag (DTON: \$020, bit 3) and the low speed on flag (LSON: \$020, bit 0). The procedures are described below:

- Set LSON to 0 and DTON to 1 in subactive mode.
- Execute the STOP or SBY instruction.
- The MCU automatically enters active mode from subactive mode after waiting for the MCU internal processing time and oscillation stabilization time (figure 19).

Notes: 1. The DTON flag can be set only in subactive mode. It is always reset in active mode.
 2. The transition time (T_D) from subactive mode to active mode:
 $t_{RC} < T_D < T + t_{RC}$

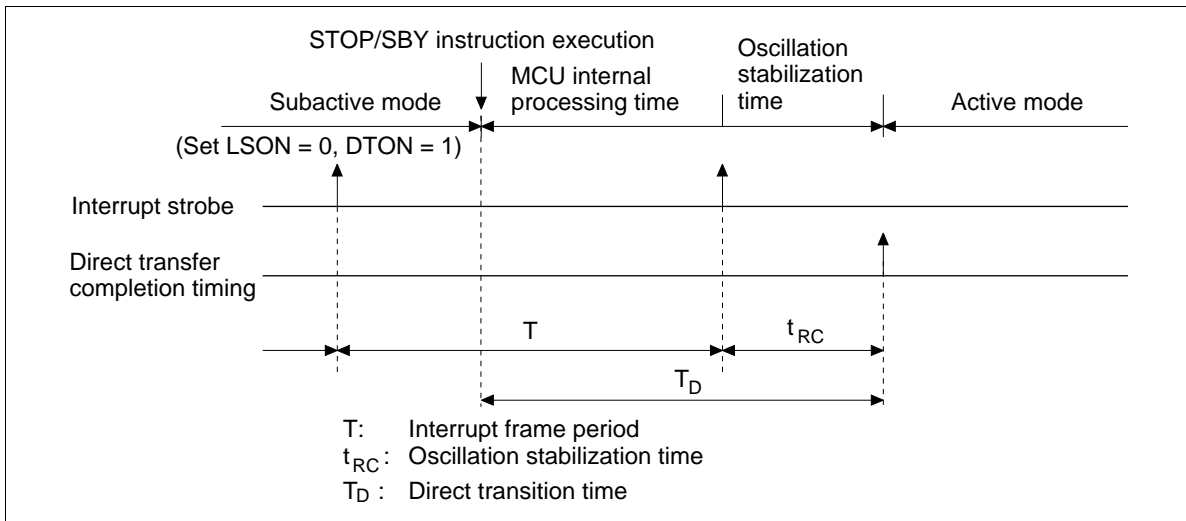


Figure 19 Direct Transition Timing

MCU Operation Sequence: The MCU operates in the sequence shown in figure 20. It is reset by an asynchronous RESET input, regardless of its status.

With the IE flag cleared and an interrupt request flag set together with its interrupt mask cleared, if a STOP/SBY instruction is executed, the instruction is cancelled (regarded as a NOP) and the following instruction is executed. Before executing a STOP/SBY instruction, make sure all interrupt request flags are cleared or all interrupts are masked.

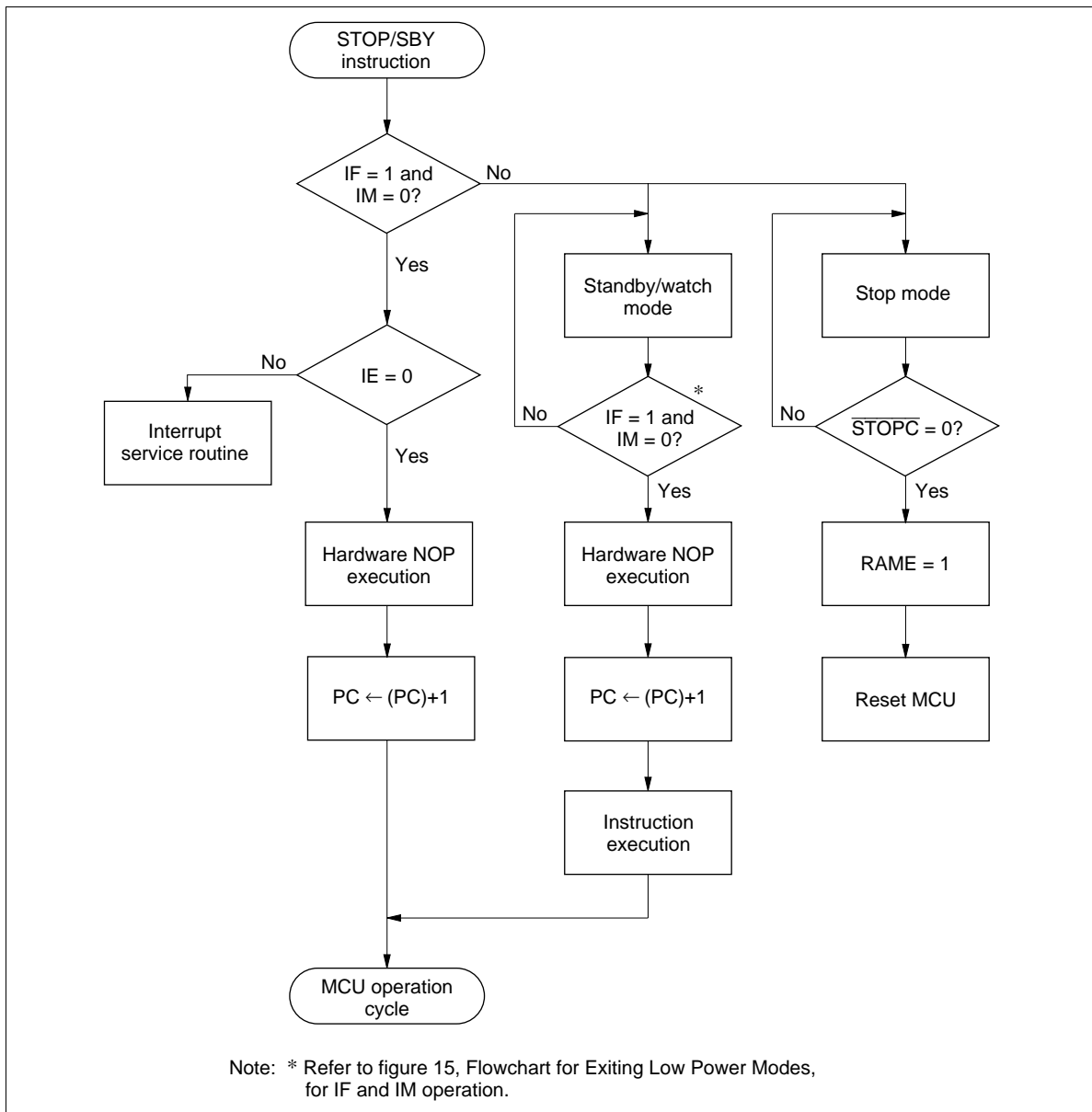


Figure 20 MCU Operating (Low-Power Mode Operation)

Notes: When the MCU is in watch mode or subactive mode, if the high level period before the falling edge of \overline{INT}_0 is shorter than the interrupt frame, \overline{INT}_0 is not detected. Also, if the low level period after the falling edge of \overline{INT}_0 is shorter than the interrupt frame, \overline{INT}_0 is not detected.

Edge detection is shown in figure 21. The level of the \overline{INT}_0 signal is sampled by a sampling clock. When this sampled value changes to low from high, a falling edge is detected.

HD404669 Series

In figure 22(a), the level of the $\overline{\text{INT}}_0$ signal is sampled by an interrupt frame. In (a) the sampled value is low at point A, and also low at point B. Therefore, a falling edge is not detected. In (b), the sampled value is high at point A, and also high at point B. A falling edge is not detected in this case either.

When the MCU is in watch mode or subactive mode, keep the high level and low level period of $\overline{\text{INT}}_0$ longer than interrupt frame.

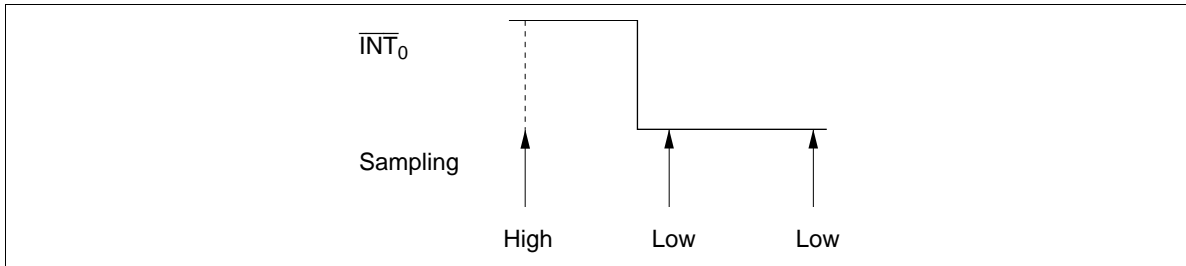


Figure 21 Edge Detection

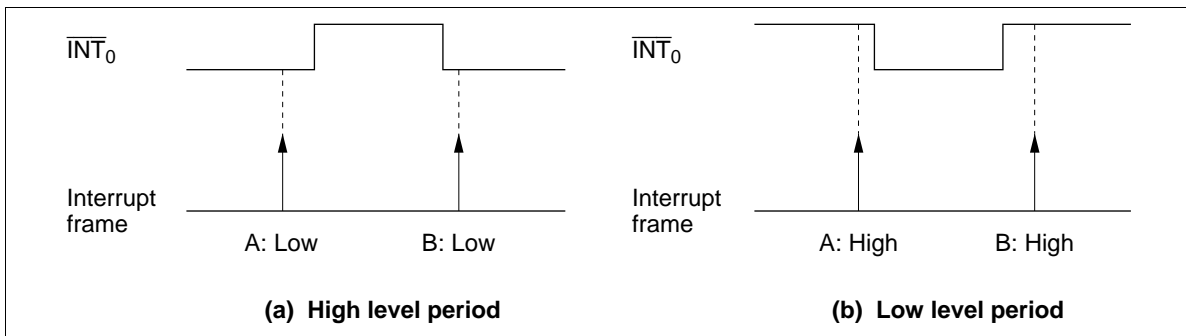


Figure 22 Sampling Example

Internal Oscillator Circuit

A block diagram of the clock generation circuit is shown in figure 23. As shown in table 13, a ceramic oscillator or crystal oscillator can be connected to OSC₁ and OSC₂, and a 32.768-kHz oscillator can be connected to X1 and X2. The system oscillator can also be operated by an external clock. Set bits 0 and 1 (SSR10, SSR11) of system clock select register 1 (SSR1: \$029) and bits 2 and 3 (SSR22, SSR23) of system clock select register 2 (SSR2: \$02A) according to the frequency of the oscillator connected to OSC₁ and OSC₂ (figures 24 and 25).

The system clock division ratio can be set with bits 0 and 1 (SSR20, SSR21) of system clock select register 2 (SSR2: \$02A). The value set in these bits does not become valid until watch mode is entered. Therefore, the system clock must be halted temporarily when changing the division ratio.

The system clock division ratio immediately after a reset or when stop mode is cleared can be selected by means of the SEL pin level, division-by-4 being selected when the SEL pin is at V_{cc} potential, and division-by-32 when at GND potential.

Note: If the system clock select register 1 and 2 (SSR1, SSR2: \$029, \$02A) setting does not match the oscillator frequency, DTMF generation circuit and subsystems using the 32.768-kHz oscillation will malfunction.

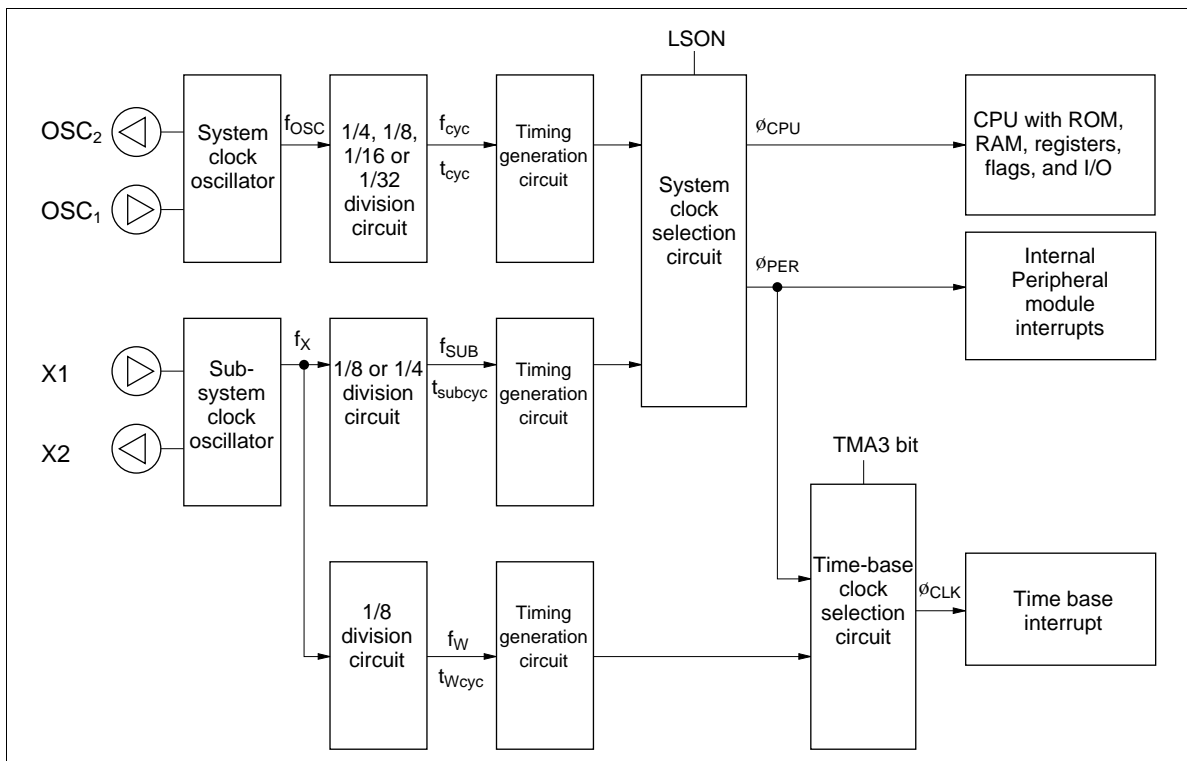


Figure 23 Clock Generation Circuit

HD404669 Series

| System clock select register 1 (SSR1: \$029) | | | | | | | |
|--|--|--------------|--------------|--------------|--------------|-------------------------------|--|
| Bit | 3 | 2 | 1 | 0 | | | |
| Initial value | 0 | 0 | 0 | 0 | | | |
| Read/Write | W | W | W | W | | | |
| Bit name | SSR13 | SSR12 | SSR11 | SSR10 | | | |
| SSR13 | 32-kHz oscillation stop | SSR23 | SSR22 | SSR11 | SSR10 | System clock selection | |
| 0 | Oscillation operates in stop mode | 0 | 0 | 0 | 0 | 400 kHz | |
| 1 | Oscillation stops in stop mode | | | | 1 | 800 kHz | |
| | | | | 1 | 0 | 2 MHz | |
| SSR12 | 32-kHz oscillation division ratio selection | | | | 1 | 4 MHz | |
| 0 | $f_{SUB} = f_x/8$ | | 1 | × | × | 3.58 MHz | |
| 1 | $f_{SUB} = f_x/4$ | 1 | 0 | 1 | 1 | 8 MHz | |
| | | | 1 | × | × | 7.16 MHz | |

Note: SSR13 is cleared only by a RESET input. SSR13 will not be cleared by a \overline{STOPC} input during stop mode, and will retain its value.
SSR13 will also not be cleared upon entering stop mode.

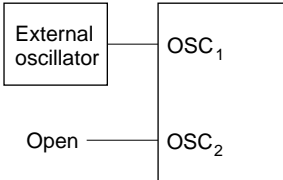
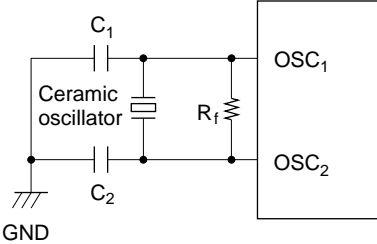
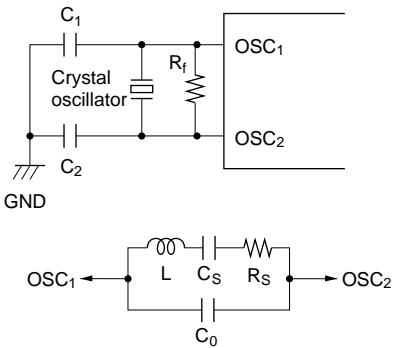
Figure 24 System Clock Select Register 1 (SSR1)

| System clock select register 2 (SSR2: \$02A) | | | | | | |
|--|--------------|--|--------------|--------------|--|--|
| Bit | 3 | 2 | 1 | 0 | | |
| Initial value | 0 | 0 | 0 | 0 | | |
| Read/Write | W | W | W | W | | |
| Bit name | SSR23 | SSR22 | SSR21 | SSR20 | | |
| SSR23 | SSR22 | System clock selection*2 | SSR21 | SSR20 | System clock division ratio selection*1 | |
| 0 | 0 | Selected from 400 kHz, 800 kHz, 2 MHz, 4 MHz | 0 | 0 | Division by 4 | |
| | 1 | 3.58MHz | | 1 | Division by 8 | |
| 1 | 0 | 8MHz | 1 | 0 | Division by 16 | |
| | 1 | 7.16MHz | | 1 | Division by 32 | |

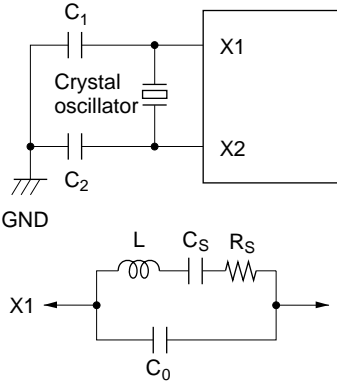
Notes : *1 The DTMF generation circuit frequencies are not affected by the system clock division ratio setting.
*2 See system clock select register 1 (SSR1).

Figure 25 System Clock Select Register 2 (SSR2)

Table 13 Oscillator Circuit Examples

| | Circuit Configuration | Circuit Constants |
|---|---|---|
| External clock operation |  | — |
| Ceramic oscillator (OSC ₁ , OSC ₂) |  | <p>Ceramic oscillator: CSB400P22 (Murata) CSB400P (Murata)</p> <p>$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 220\text{ pF} \pm 5\%$</p> <hr/> <p>Ceramic oscillator: CSB800J122 (Murata), CSB800J (Murata)</p> <p>$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 220\text{ pF} \pm 5\%$</p> <hr/> <p>Ceramic oscillator: CSA2.00MG (Murata)</p> <p>$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 30\text{ pF} \pm 20\%$</p> <hr/> <p>Ceramic oscillator: CSA4.00MG (Murata)</p> <p>$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 30\text{ pF} \pm 20\%$</p> <hr/> <p>Ceramic oscillator: CSA3.58MG (Murata)</p> <p>$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 30\text{ pF} \pm 20\%$</p> <hr/> <p>Ceramic oscillator: CSA8.00MT (Murata)</p> <p>$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 30\text{ pF} \pm 20\%$</p> |
| Crystal oscillator (OSC ₁ , OSC ₂) |  | <p>$R_f = 1\text{ M}\Omega \pm 20\%$ $C_1 = C_2 = 10\text{ to }22\text{ pF} \pm 20\%$</p> <p>Crystal oscillator: Equivalent circuit at left $C_0 = 7\text{ pF max}$ $R_s = 100\Omega\text{ max}$ $f = 400\text{ kHz, } 800\text{ kHz, } 2\text{ MHz, } 3.58\text{ MHz, } 4\text{ MHz, } 7.16\text{ MHz, } 8\text{ MHz}$</p> |

HD404669 Series

| Circuit Configuration | Circuit Constants |
|--|--|
| <p>Crystal oscillator (X1, X2)</p>  | <p>Crystal oscillator: 32.768 kHz: MX38T (Nippon Denpa) $C_1 = C_2 = 20 \text{ pF} \pm 20\%$ $R_S = 14 \text{ k}\Omega$ $C_0 = 1.5 \text{ pF}$</p> |

- Notes:
1. Circuit constants differ by the different types of crystal oscillators, ceramic oscillators, and with the stray capacitance of the board, so consult the manufacturer of the oscillator to determine the circuit parameters.
 2. The wiring between the OSC₁, OSC₂ (X1 and X2 pins), and the other elements should be as short as possible, and must not cross other wiring. Refer to figure 26.
 3. If not using a 32.768-kHz crystal oscillator, fix the X1 pin to V_{CC} and leave the X2 pin open.

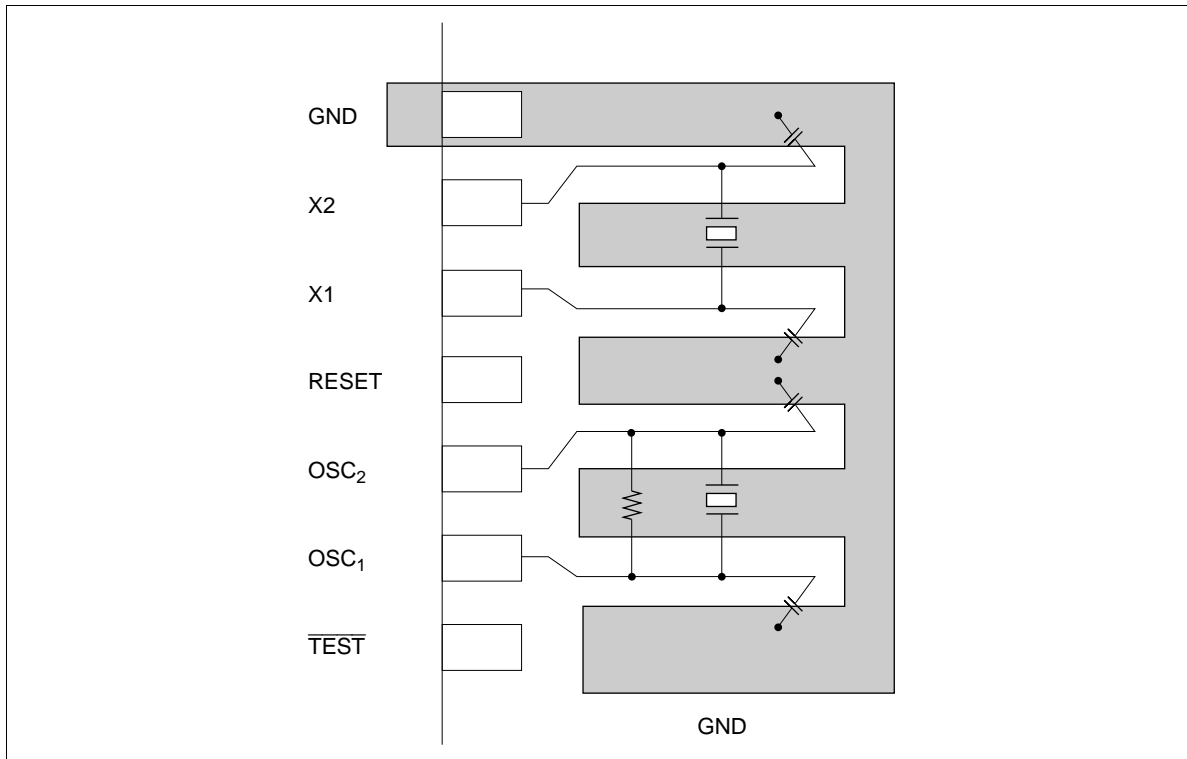


Figure 26 Typical Layouts of Crystal and Ceramic Oscillator

Input/Output

The MCU has 47 input/output pins (D_0 to D_5 , D_9 to D_{11} , $R0_0$ to $R4_3$ and $R6_0$ to RA_1) and 5 input pins (D_{12} , D_{13} , RD_0 , RD_1 and RE_0). The features are described below.

- Four pins D_0 to D_3 are high source current (10 mA maximum) input/output pins.
- Five pins D_4 , D_5 , and D_9 to D_{11} are high sink current (15 mA maximum) input/output pins.
- Certain of these input and output pins have shared functions with timers, the serial interface, and other peripheral functions. The D_{12} , D_{13} , $R0_0$, $R3_0$, $R3_2$, $R4$, RD_0 , RD_1 and RE_0 pins are shared function pins. The use of these pins as peripheral function pins takes precedence over their use as the D and R port pins. Pins that are set to function as peripheral function pins are switched automatically between their various functions and between the input and output directions according to their specifications under the peripheral function setting.
- Input or output selection for input/output pins and port or peripheral function selection for multiplexed pins are set by software.
- Peripheral function output pins are all CMOS outputs. However, the SO_1 pin and the $R4_3$ port pin can be set to function as NMOS open drain outputs by software.
- Since the MCU goes to the reset state internally after a reset and in stop mode, the peripheral function settings for these pins are cleared. Furthermore, since the data control registers (DCD and DCR) are also reset, the input/output pins go to the high-impedance state.
- The D_0 to D_3 pin circuits include pull-down MOS transistors, and all the other pin circuits include pull-up MOS transistors. Note that the on/off states of the pull-up and pull-down MOS transistors can be set independently of the setting for use as peripheral function pins.

I/O buffer configurations are shown in figures 27 and 28, and I/O pin circuit structures are listed in tables 14 and 15.

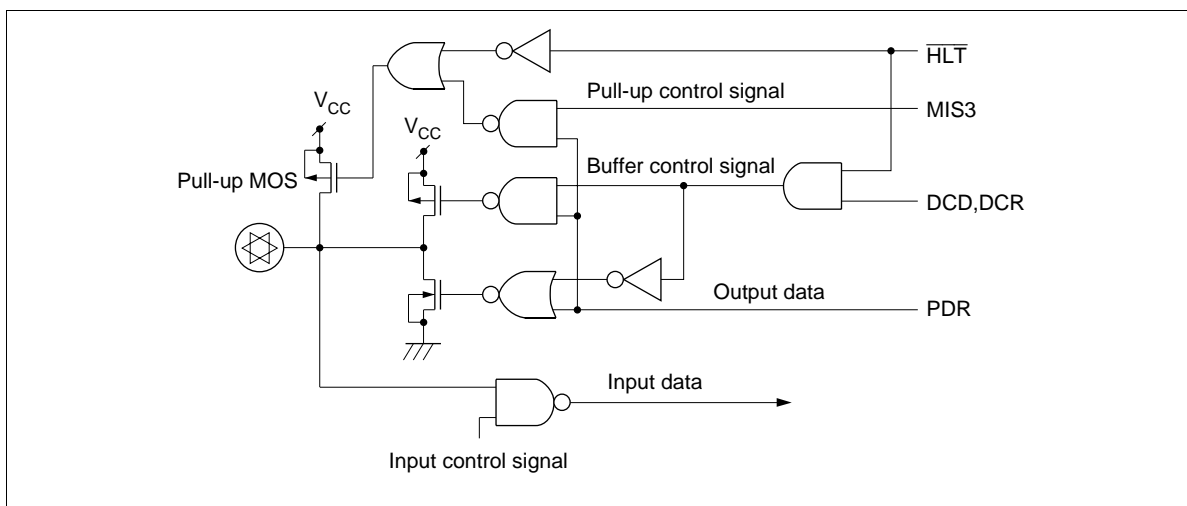


Figure 27 I/O Buffer Configuration (with Pull-Up MOS)

Table 16 Input/Output Pin Circuit Configurations

| I/O Pin Type | Circuit Configuration | Relevant Pins |
|-------------------|-----------------------|--|
| Input/output pins | | <p>D₄, D₅, D₉-D₁₁ R₀-R₃ R₁₀-R₁₃ R₂₀-R₂₃ R₃₀-R₃₃ R₄₀-R₄₂ R₆₀-R₆₃ R₇₀-R₇₃ R₈₀-R₈₃ R₉₀-R₉₃ RA₀, RA₁</p> |
| | | D ₀ -D ₃ |
| | | R ₄₃ |
| | | |
| Input pins | | <p>D₁₂, D₁₃ RD₀, RD₁, RE₀</p> |

HD404669 Series

Table 16 Input/Output Pin Circuit Configurations (cont)

| I/O Pin Type | Circuit Configuration | Relevant Pins |
|--|-----------------------|---|
| Peripheral function Input/output pins | | \overline{SCK}_1 |
| Output pins | | \overline{SO}_1 |
| | | TOC, TOD |
| Input pins | | $SI_1, \overline{INT}_1, INT_2, INT_3, INT_4, EVND$ |
| | | $\overline{INT}_0, \overline{STOPC}, RESET$ |

Note: In a reset and in stop mode, since the I/O control registers are reset, input/output pins go to the high-impedance state and peripheral function selections are cleared.

D Port

The D port consists of 9 input/output pins and 2 input-only pins that can be addressed individually on a per-bit basis. The D₀ to D₃ pins are high source current input/output pins and the D₄, D₅, and D₉ to D₁₁ pins are high sink current input/output pins. The D₁₂ and D₁₃ pins are input-only pins.

The D₀ to D₅ and D₉ to D₁₁ pins can be set or reset by the SED/RED and SEDD/REDD instructions. The output data is stored in the port data register for the pin. All the D port pins can be tested using the TD and TDD instructions.

The D port data control registers (DCD0 to DCD2: \$02C to \$02E) are used to turn the D₀ to D₅ and D₉ to D₁₁ pin output buffers on and off. The DCD registers are mapped to addresses in the RAM area. (figure 29.)

The D₁₂ and D₁₃ pins have shared functions as internal peripheral function pins and the $\overline{\text{STOPC}}$ and $\overline{\text{INT}}_0$ pins. Port mode register C (PMRC: \$025) bits 2 and 3 (PMRC2 and PMRC3) are used to switch the functions of these pins. (figure 32.)

HD404669 Series

**Data control register (DCD0 to 2: \$02C to \$02E)
(DCR0 to 4, DCR6 to A: \$030 to \$034, \$036 to \$03A)**

DCD0 to DCD2

| | | | | |
|---------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | DCD03, DCD23 | DCD02, DCD22 | DCD01– DCD21 | DCD00– DCD10 |

DCR0 to DCR4 DCR6 to DCRA

| | | | | |
|---------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | DCR03– DCR43 | DCR02– DCR42 | DCR01– DCR41 | DCR00– DCR40 |
| | DCR63– DCR93 | DCR62– DCR92 | DCR61– DCRA1 | DCR60– DCRA0 |

Note: Other bits are not used.

All Bits CMOS Buffer Control

| | |
|---|----------------------------------|
| 0 | CMOS buffer Off (high-impedance) |
| 1 | CMOS buffer active |

Correspondence between ports and DCD/DCR bits

| Register Name | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------------|-----------------|-----------------|-----------------|-----------------|
| DCD0 | D ₃ | D ₂ | D ₁ | D ₀ |
| DCD1 | — | — | D ₅ | D ₄ |
| DCD2 | D ₁₁ | D ₁₀ | D ₉ | — |
| DCR0 | R0 ₃ | R0 ₂ | R0 ₁ | R0 ₀ |
| DCR1 | R1 ₃ | R1 ₂ | R1 ₁ | R1 ₀ |
| DCR2 | R2 ₃ | R2 ₂ | R2 ₁ | R2 ₀ |
| DCR3 | R3 ₃ | R3 ₂ | R3 ₁ | R3 ₀ |
| DCR4 | R4 ₃ | R4 ₂ | R4 ₁ | R4 ₀ |
| DCR6 | R6 ₃ | R6 ₂ | R6 ₁ | R6 ₀ |
| DCR7 | R7 ₃ | R7 ₂ | R7 ₁ | R7 ₀ |
| DCR8 | R8 ₃ | R8 ₂ | R8 ₁ | R8 ₀ |
| DCR9 | R9 ₃ | R9 ₂ | R9 ₁ | R9 ₀ |
| DCRA | — | — | RA ₁ | RA ₀ |

Figure 29 Data Control Registers (DCD, DCR)

R Port

The R port consist of 38 input/output pins and 3 input pins that can be addressed in groups of 4 bits. Data can be input using the LAR and LBR instructions, and data can be output using the LRA and LRB instructions. Output data is stored in the port data register for the corresponding pin.

The R port data control registers (DCR0 to DCR4 and DCR6 to DCRA: \$030 to \$034, and \$036 to \$03A) are used to turn the R port output buffers on and off. The DCR registers are mapped to addresses in the RAM area. (figure 29.)

The R0₀ to R0₄ port pins have shared functions as the external interrupt input pins \overline{INT}_1 to INT₄. Port mode register B (PMRB \$024) is used to set these pins to their peripheral function usage. (figure 31.)

The R4₀ port pin has a shared function as the EVND peripheral function pin. Port mode register C (PMRC: \$025) bit 1 (PMRC1) is used to switch the function of this pin. (figure 32.)

The R3₁ and R3₂ port pins have shared functions as the TOC and TOD peripheral function pins. Timer mode register C2 (TMC2: \$014) bits 0 to 2 (TMC20 to TMC22) and timer mode register D2 (TMD2: \$015) are used to set these pins to their peripheral function usage. (figures 33 and 34.)

The R4₁ to R4₃ port pins have shared functions as the \overline{SCK}_1 , SI₁, and SO₁ peripheral function pins. Serial mode register 1A (SM1A: \$005) bit 3 (SM1A3) and port mode register A (PMRA: \$004) bits 0 and 1 (PMRA0 and PMRA1) are used to set these pins to their peripheral function usage. (figures 30 and 35.)

The R4₃/SO₁ pin can be set to function as an NMOS open drain output with the output buffer off. Miscellaneous register (MIS: \$00C) bit 2 (MIS2) is used for this setting. (figure 37.)

The RD₀ and RD₁ port pins have shared functions as the COMP₀ and COMP₁ peripheral function pins. The compare enable register (CER: \$018) is used to set these pins to their comparator pin functions. (figure 36.)

| Port mode register A (PMRA: \$004) | | | | |
|------------------------------------|---|----------|--------------|---|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | — | — | 0 | 0 |
| Read/Write | — | — | W | W |
| Bit name | Not used | Not used | PMRA1 | PMRA0 |
| PMRA1 | R4₂/SI₁ mode selection | | PMRA0 | R4₃/SO₁ mode selection |
| 0 | R4 ₂ | | 0 | R4 ₃ |
| 1 | SI ₁ | | 1 | SO ₁ |

Figure 30 Port Mode Register A (PMRA)

HD404669 Series

| Port mode register B (PMRB: \$024) | | | | |
|------------------------------------|--|-------|--------------|--|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | PMRB3 | PMRB2 | PMRB1 | PMRB0 |
| PMRB3 | R0₃/INT₄ mode selection | | PMRB0 | R0₀/INT₁ mode selection |
| 0 | R0 ₃ | | 0 | R0 ₀ |
| 1 | INT ₄ | | 1 | INT ₁ |
| PMRB2 | R0₂/INT₃ mode selection | | PMRB1 | R0₁/INT₂ mode selection |
| 0 | R0 ₂ | | 0 | R0 ₁ |
| 1 | INT ₃ | | 1 | INT ₂ |

Figure 31 Port Mode Register B (PMRB)

| Port mode register C (PMRC: \$025) | | | | |
|------------------------------------|--|-------|--------------|---|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | — |
| Read/Write | W | W | W | — |
| Bit name | PMRC3 | PMRC2 | PMRC1 | Not Used |
| PMRC3 | D₁₃/INT₀ mode selection | | | |
| 0 | D ₁₃ | | | |
| 1 | INT ₀ | | | |
| PMRC2 | D₁₂/STOPC mode selection | | PMRC1 | R4₀/EVND mode selection |
| 0 | D ₁₂ | | 0 | R4 ₀ |
| 1 | STOPC | | 1 | EVND |

Figure 32 Port Mode Register C (PMRC)

Timer mode register C2 (TMC2: \$014)

| | | | | |
|---------------|----------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | — | 0 | 0 | 0 |
| Read/Write | — | R/W | R/W | R/W |
| Bit name | Not used | TMC22 | TMC21 | TMC20 |

| TMC22 | TMC21 | TMC20 | R3 ₁ /TOC mode selection | |
|-------|-------|-------|-------------------------------------|----------------------|
| 0 | 0 | 0 | R3 ₁ | R3 ₁ port |
| | | 1 | TOC | Toggle output |
| | 1 | 0 | TOC | 0 output |
| | | 1 | TOC | 1 output |
| 1 | 0 | 0 | — | Not Used |
| | | 1 | | |
| | 1 | 0 | | |
| | | 1 | TOC | PWM output |

Figure 33 Timer Mode Register C2 (TMC2)

Timer mode register D2 (TMD2: \$015)

| | | | | |
|---------------|-------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W |
| Bit name | TMD23 | TMD22 | TMD21 | TMD20 |

| TMD23 | TMD22 | TMD21 | TMD20 | R3 ₂ /TOD mode selection | |
|-------|-------|-------|-------|-------------------------------------|--------------------------------------|
| 0 | 0 | 0 | 0 | R3 ₂ | R3 ₂ port |
| | | 1 | TOD | Toggle output | |
| | 1 | 0 | TOD | 0 output | |
| | | 1 | TOD | 1 output | |
| 1 | 0 | 0 | — | Not used | |
| | | 1 | | | |
| | 1 | 0 | | | |
| | | 1 | TOD | PWM output | |
| 1 | × | × | × | R3 ₂ | Input capture (R3 ₂ port) |

× : Don't care

Figure 34 Timer Mode Register D2 (TMD2)

HD404669 Series

Serial mode register 1A (SM1A: \$005)

| | | | | |
|---------------|-------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | SM1A3 | SM1A2 | SM1A1 | SM1A0 |

| SM1A3 | R4 ₁ / $\overline{\text{SCK}}_1$ mode selection | SM1A2 | SM1A1 | SM1A0 | $\overline{\text{SCK}}_1$ | Clock source | Prescaler division ratio |
|-------|---|-------|-------|-------|---------------------------|----------------|--------------------------------|
| 0 | R4 ₁ | 0 | 0 | 0 | Output | Prescaler | ÷2048 |
| 1 | $\overline{\text{SCK}}_1$ | | | 1 | Output | Prescaler | ÷512 |
| | | | 1 | 0 | Output | Prescaler | ÷128 |
| | | | | 1 | Output | Prescaler | ÷32 |
| | | 1 | 0 | 0 | Output | Prescaler | ÷8 |
| | | | | 1 | Output | Prescaler | ÷2 |
| | | | 1 | 0 | Output | System clock | — |
| | | | | 1 | Input | External clock | — |

Figure 35 Serial Mode Register 1A (SM1A)

Compare enable register (CER: \$018)

| | | | | |
|---------------|------|----------|------|------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | — | 0 | 0 |
| Read/Write | W | — | W | W |
| Bit name | CER3 | Not Used | CER1 | CER0 |

| CER1 | CER0 | Analog input pin selection |
|------|------|----------------------------|
| 0 | 0 | COMP ₀ |
| | 1 | COMP ₁ |
| 1 | × | Not Used |

× : Don't care

CER3 Comparator operation selection

| | |
|---|--|
| 0 | Normal operation (digital input mode): RD ₀ /COMP ₀ and RD ₁ /COMP ₁ pins function as R port pins |
| 1 | Comparator operation (analog input mode): RD ₀ /COMP ₀ and RD ₁ /COMP ₁ pins function as comparator pins |

Figure 36 Compare Enable Register (CER)

Pull-up and Pull-down MOS Transistor Control

The D₄, D₅, D₉ to D₁₁, and the R port pins have built-in pull-up MOS transistors that can be controlled by software, and the D₀ to D₃ pins have built-in pull-down MOS transistors that can be controlled by software.

The on/off status of all these transistors is controlled by bit 3 (MIS3) of the miscellaneous register (MIS: \$00C), and the on/off status of an individual transistor can also be controlled by the port data register (PDR) of the corresponding pin—enabling on/off control of that pin alone (tables 14, 15 and figure 37).

The on/off status of each transistor and the peripheral function mode of each pin can be set independently.

| Miscellaneous register (MIS: \$00C) | | | | | |
|-------------------------------------|------|------|------|------|--|
| Bit | 3 | 2 | 1 | 0 | |
| Initial value | 0 | 0 | 0 | 0 | |
| Read/Write | W | W | W | W | |
| Bit name | MIS3 | MIS2 | MIS1 | MIS0 | |

| MIS3 | Pull-up/Pull-down MOS transistor control | MIS2 | CMOS buffer on/off selection for pin R4 ₃ /SO ₁ | MIS1 | MIS0 |
|------|--|------|---|---|------|
| 0 | Off | 0 | Active | t _{RC} selection. Refer to figure 18 in the operation modes section. | |
| 1 | Active | 1 | Off | | |

Figure 37 Miscellaneous Register (MIS)

How to Deal with Unused I/O Pins: I/O pins that are not needed by the user system (floating) must be connected to V_{CC} to prevent LSI malfunctions due to noise. These pins must either be pulled up to V_{CC} by their pull-up MOS transistors or by resistors of about 100 kΩ. Pins provided with pull-down MOS should be pulled down to GND potential with the built-in pull-down MOS or connected to GND.

HD404669 Series

Prescalers

The MCU has the following two prescalers, S and W.

The prescalers operating conditions are listed in table 17, and the prescalers output supply is shown in figure 38. The timers A, C, D input clocks except external events, the serial transmit clock except the external clock, are selected from the prescaler outputs, depending on corresponding mode registers.

Table 17 Prescaler Operating Conditions

| Prescaler | Input Clock | Reset Conditions | Stop Conditions |
|-------------|---|-------------------------|--|
| Prescaler S | System clock (in active and standby mode), Subsystem clock (in subactive mode) | MCU reset | MCU reset, stop mode, watch mode |
| Prescaler W | Clock derived by dividing subsystem clock 32.768 kHz oscillation by 8 | MCU reset, software* | MCU reset, stop mode |

Note: * If bits TMA3 to TMA1 in timer mode register A (TMA) are all set to 1, PSW is cleared to \$00.

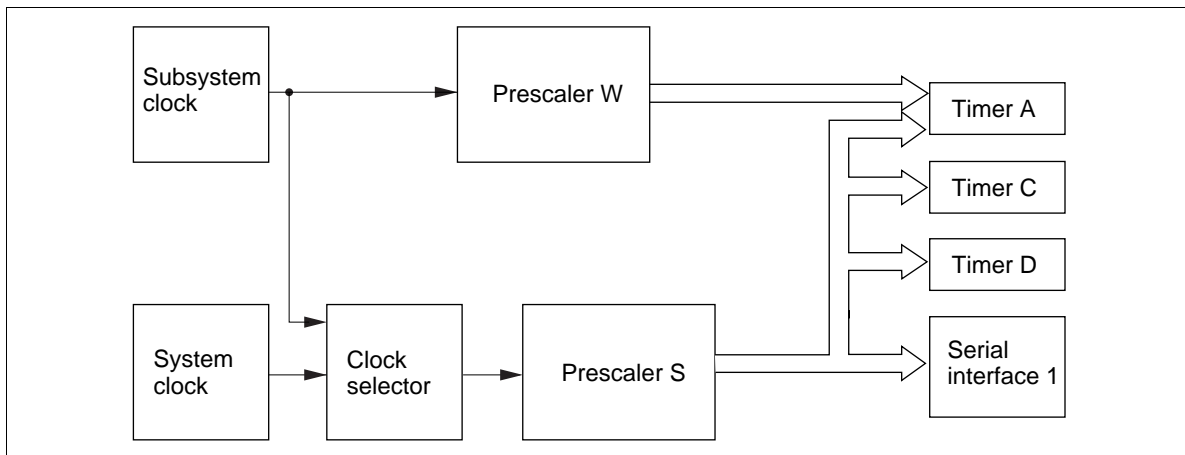


Figure 38 Prescaler Output Supply

Prescaler Operation

Prescaler S: 11-bit counter that inputs the system clock signal. After being reset to \$000 by MCU reset, prescaler S divides the system clock. Prescaler S keeps counting, except in watch and stop modes and at MCU reset.

Prescaler W: Five-bit counter that inputs the X1 input clock signal (32-kHz crystal oscillation) divided by eight. After being reset to \$00 by MCU reset, prescaler W divides the input clock. Prescaler W can be reset by software.

Timers

The MCU has three timer/counters (A, C, D).

- Timer A: Free-running timer
- Timer C: Multifunction timer
- Timer D: Multifunction timer

Timer A is an 8-bit free-running timer. Timers C, D are 8-bit multifunction timers, whose functions are listed in table 18. The operating modes are selected by software.

Table 18 Timer Functions

| Functions | | Timer A | Timer C | Timer D |
|-----------------|----------------|-----------|-----------|-----------|
| Clock source | Prescaler S | Available | Available | Available |
| | Prescaler W | Available | — | — |
| | External event | — | — | Available |
| Timer functions | Free-running | Available | Available | Available |
| | Time-base | Available | — | — |
| | Event counter | — | — | Available |
| | Reload | — | Available | Available |
| | Watchdog | — | Available | — |
| | Input capture | — | — | Available |
| Timer outputs | Toggle | — | Available | Available |
| | 0 output | — | Available | Available |
| | 1 output | — | Available | Available |
| | PWM | — | Available | Available |

Note: — implies not available.

Timer A

Timer A Functions: Timer A has the following functions.

- Free-running timer
- Clock time-base

The block diagram of timer A is shown in figure 39.

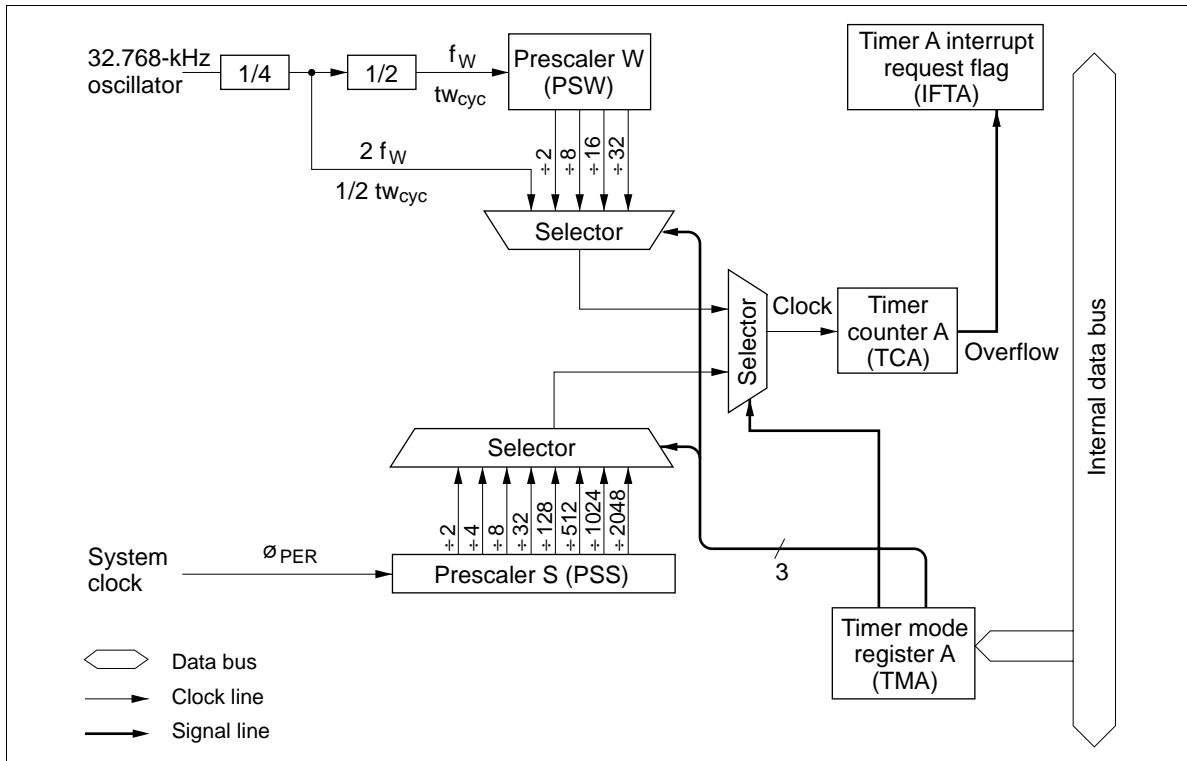


Figure 39 Block Diagram of Timer A

Timer A Operations

Free-running timer operation: The timer A input clock is selected by timer mode register A (TMA: \$008). Timer A is reset to \$00 by an MCU reset, and counts up each time the input clock is input. When the input clock is input after the timer A value reaches \$FF, overflow output is generated, and the timer A value becomes \$00. The generated overflow output sets the timer A interrupt request flag (IFTA: \$001, 2). Timer A continues counting up after the count value returns to \$00, so that an interrupt is generated regularly every 256 input clock cycles.

Realtime clock time base operation: Timer A can be used as the realtime clock time base by setting bit 3 (TMA3) of timer mode register A to 1. As the prescaler W output is input to timer counter A (TCA), interrupts are generated with accurate timing using the 32.768 kHz crystal oscillator as the basic clock. When timer A is used as the realtime clock time base, prescaler W and timer counter A (TCA) can be reset to \$00 by the program.

Registers for Timer A Operation

Timer A operating modes are set by the following registers.

Timer mode register A (TMA: \$008): Four-bit write-only register that selects timer A's operating mode and input clock source as shown in figure 40.

Timer mode register A (TMA: \$008)

| | | | | |
|---------------|------|------|------|------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TMA3 | TMA2 | TMA1 | TMA0 |

| TMA3 | TMA2 | TMA1 | TMA0 | Source prescaler | Input clock frequency | Operating mode |
|------|------|------|------|------------------|-----------------------|----------------|
| 0 | 0 | 0 | 0 | PSS | $2048t_{cyc}$ | Timer A mode |
| | | | 1 | PSS | $1024t_{cyc}$ | |
| | | 1 | 0 | PSS | $512t_{cyc}$ | |
| | | | 1 | PSS | $128t_{cyc}$ | |
| | 1 | 0 | 0 | PSS | $32t_{cyc}$ | |
| | | | 1 | PSS | $8t_{cyc}$ | |
| | | 1 | 0 | PSS | $4t_{cyc}$ | |
| | | | 1 | PSS | $2t_{cyc}$ | |
| 1 | 0 | 0 | 0 | PSW | $32t_{Wcyc}$ | Time-base mode |
| | | | 1 | PSW | $16t_{Wcyc}$ | |
| | | 1 | 0 | PSW | $8t_{Wcyc}$ | |
| | | | 1 | PSW | $2t_{Wcyc}$ | |
| | 1 | 0 | 0 | — | $1/2t_{Wcyc}$ | |
| | | | 1 | — | Not used | |
| | | 1 | × | — | Reset PSW and TCA | |

× : Don't care

- Note:
- $t_{Wcyc} = 244.14 \mu s$ (when a 32.768-kHz crystal oscillator is used)
 - Timer counter overflow output period (seconds) = input clock period (seconds) \times 256.
 - The division ratio must not be modified during time-base mode operation, otherwise an overflow cycle error will occur.

Figure 40 Timer Mode Register A (TMA)

HD404669 Series

Timer C

Timer C Functions: Timer C has the following functions.

- Free-running/reload timer
- Watchdog timer
- Timer output operation (toggle, 0, 1, and PWM outputs)

The block diagram of timer C is shown in figure 41.

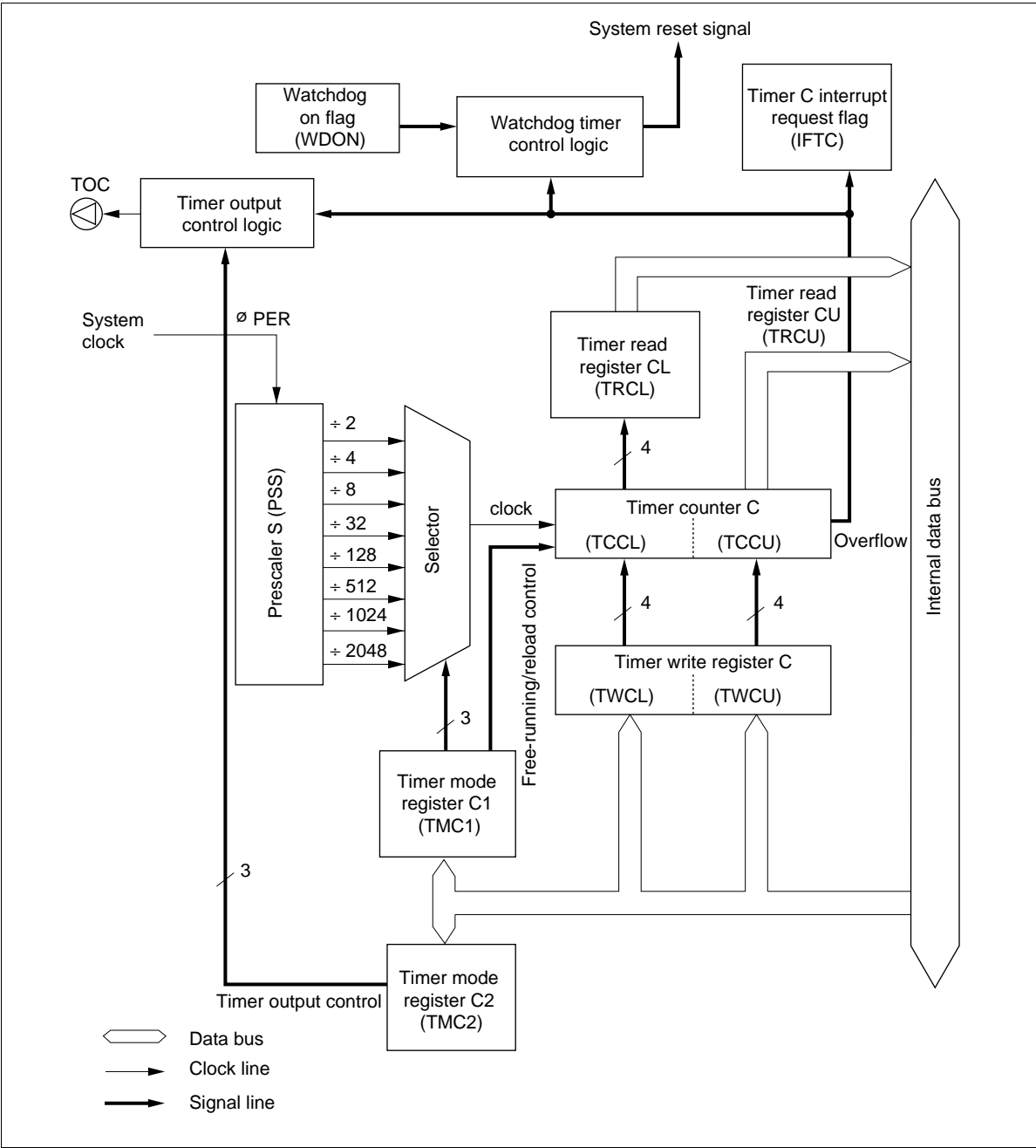


Figure 41 Block Diagram of Timer C

Timer C Operations

Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register C1 (TMC1: \$00D).

Timer C is initialized to the value set in timer write register C (TWCL: \$00E, TWCU: \$00F) by software and incremented by one at each clock input. If an input clock is applied to timer C after it has reached \$FF, an overflow is generated. In this case, if the reload timer function is enabled, timer C is initialized to its initial value set in timer write register C (TWCL: \$00E, TWCU: \$00F); if the free-running timer function is enabled, the timer is initialized to \$00 and then incremented again.

The overflow sets the timer C interrupt request flag (IFTC: \$002, bit 2). The timer C interrupt request flag is reset by the program, an MCU reset or a transition to stop mode. For details, see figure 3, Configuration of Interrupt Control Bits and Register Flag Area, and table 1, Initial Values after MCU Reset.

Watchdog timer operation: Timer C is used as a watchdog timer for detecting out-of-control program routines by setting the watchdog on flag (WDON: \$020, bit 1) to 1. If a program routine runs out of control and an overflow is generated, the MCU is reset. Program run can be controlled by initializing timer C by software before it reaches \$FF.

Timer output operation: The following four output modes can be selected for timer C by setting timer mode register C2 (TMC2: \$014). With timer C, the R3₁/TOC pin is designated as the TOC pin, and toggle waveform output, low-level output, high-level output, or PWM waveform output can be selected, by timer mode register C2 (TMC2: \$014). TOC pin output is initialized to the low level by an MCU reset.

- Toggle output

With toggle output, the output level is changed upon input of the next clock pulse after the timer C value reaches \$FF. Use of this function in combination with the reload timer allows a clock signal with any period to be output, enabling it to be used as buzzer output. The output waveform is shown in figure 42.

- Low-level output

With low-level output, the output is changed to the low level when timer C overflows. This function should be used when the output is high.

- High-level output

With high-level output, the output is changed to the high level when timer C overflows. This function should be used when the output is low.

- PWM output

With PWM output, variable-duty pulses are output. The output waveform is as shown in figure 42, according to the contents of timer mode register C1 (TMC1: \$00D) and timer write register C (TWCL: \$00E, TWCU: \$00F).

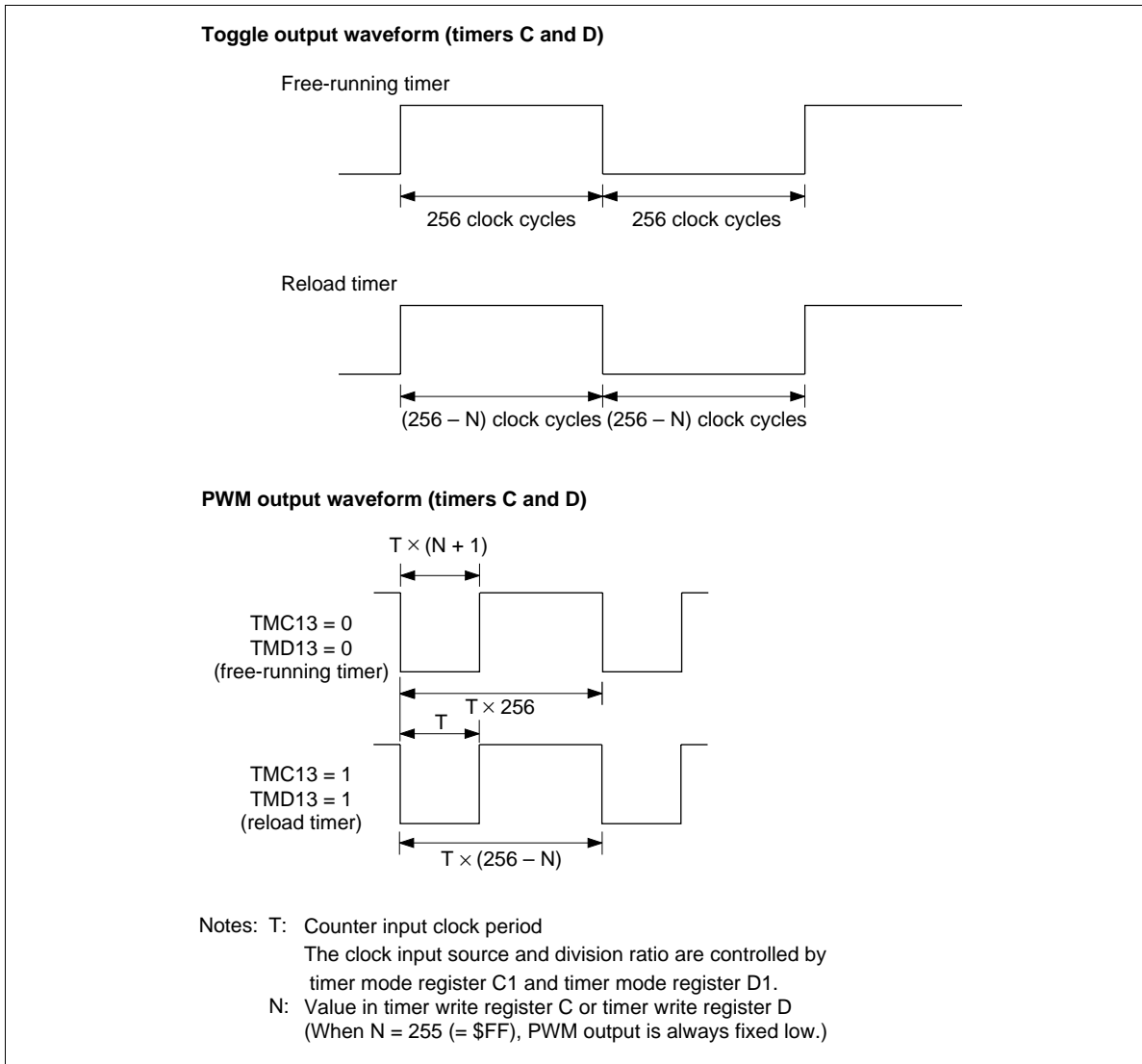


Figure 42 Timer Output Waveforms

HD404669 Series

Registers for Timer C Operation

By using the following registers, timer C operation modes are selected and the timer C count is read and written.

- Timer mode register C1 (TMC1: \$00D)
- Timer mode register C2 (TMC2: \$014)
- Timer write register C (TWCL: \$00E, TWCU: \$00F)
- Timer read register C (TRCL: \$00E, TRCU: \$00F)

Timer mode register C1 (TMC1: \$00D): Four-bit write-only register that selects the free-running/reload timer function, and the prescaler division ratio as shown in figure 43. It is reset to \$0 by MCU reset or in stop mode.

Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register C1 write instruction. Setting timer C's initialization by writing to timer write register C (TWCL: \$00E, TWCU: \$00F) must be done after a mode change becomes valid.

| Timer mode register C1 (TMC1: \$00D) | | | | | |
|--------------------------------------|-------|-------|-------|-------|--|
| Bit | 3 | 2 | 1 | 0 | |
| Initial value | 0 | 0 | 0 | 0 | |
| Read/Write | W | W | W | W | |
| Bit name | TMC13 | TMC12 | TMC11 | TMC10 | |

| TMC13 | Free-running/reload timer selection | TMC12 | TMC11 | TMC10 | Input clock period |
|-------|-------------------------------------|-------|-------|-------|--------------------|
| 0 | Free-running timer | 0 | 0 | 0 | 2048 t_{cyc} |
| 1 | Reload timer | | | 1 | 1024 t_{cyc} |
| | | | 1 | 0 | 512 t_{cyc} |
| | | | | 1 | 128 t_{cyc} |
| | | 1 | 0 | 0 | 32 t_{cyc} |
| | | | | 1 | 8 t_{cyc} |
| | | | 1 | 0 | 4 t_{cyc} |
| | | | | 1 | 2 t_{cyc} |

Figure 43 Timer Mode Register C1 (TMC1)

Timer mode register C2 (TMC2: \$014): Timer mode register C2 (TMC2: \$014) is a 3-bit read/write register, used to switch the function of the R31/TOC pin and select the timer C output mode as shown in figure 44.

Timer mode register C2 (TMC2: \$014) is reset to \$0 by an MCU reset or in stop mode.

| Timer mode register C2 (TMC2: \$014) | | | | |
|--------------------------------------|----------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | — | 0 | 0 | 0 |
| Read/Write | — | R/W | R/W | R/W |
| Bit name | Not used | TMC22 | TMC21 | TMC20 |

| TMC22 | TMC21 | TMC20 | R3 ₁ /TOC mode selection | |
|-------|-------|-------|-------------------------------------|----------------------|
| 0 | 0 | 0 | R3 ₁ | R3 ₁ port |
| | | 1 | TOC | Toggle output |
| | 1 | 0 | TOC | 0 output |
| | | 1 | TOC | 1 output |
| 1 | 0 | 0 | — | Not used |
| | | 1 | | |
| | 1 | 0 | | |
| | | 1 | TOC | PWM output |

Figure 44 Timer Mode Register C2 (TMC2)

Timer write register C (TWCL: \$00E, TWCU: \$00F): Timer write register C (TWCL: \$00E, TWCU: \$00F) is a write-only register composed of a lower digit (TWCL: \$00E) and an upper digit (TWCU: \$00F).

The lower digit (TWCL) of timer write register C is reset to \$0 by an MCU reset or in stop mode, while the upper digit (TWCU) is undetermined.

Timer C can be initialized by writing to timer write register C (TWCL, TWCU). To write the data, first write the lower digit (TWCL). The lower digit write does not change the timer C value. Next, write the upper digit (TWCU). Timer C is then initialized to the timer write register C (TWCL, TWCU) value. When writing to timer write register C (TWCL, TWCU) from the second time onward, if it is not necessary to change the lower digit (TWCL) reload value, timer C initialization is completed by the upper digit write alone.

HD404669 Series

| Timer write register C (lower digit) (TWCL: \$00E) | | | | |
|--|-------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TWCL3 | TWCL2 | TWCL1 | TWCL0 |

Figure 45 Timer Write Register C Lower Digit (TWCL)

| Timer write register C (upper digit) (TWCU: \$00F) | | | | |
|--|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | W | W | W | W |
| Bit name | TWCU3 | TWCU2 | TWCU1 | TWCU0 |

Figure 46 Timer Write Register C Upper Digit (TWCU)

Timer read register C (TRCL: \$00E, TRCU: \$00F): Timer read register C (TRCL: \$00E, TRCU: \$00F) is a read-only register composed of a lower digit (TRCL: \$00E), and an upper digit (TRCU: \$00F) from which the value of the upper digit of timer C is read directly.

First, read the upper digit (TRCU) of timer read register C. The current value of the timer C upper digit is read and, at the same time, the value of the timer C lower digit is latched in the lower digit (TRCL) of timer read register C. The timer C value is obtained when the upper digit (TRCU) of timer read register C is read by reading the lower digit (TRCL) of timer read register C.

| Timer read register C (lower digit) (TRCL: \$00E) | | | | |
|---|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | R | R | R | R |
| Bit name | TRCL3 | TRCL2 | TRCL1 | TRCL0 |

Figure 47 Timer Read Register C Lower Digit (TRCL)

| Timer read register C (upper digit) (TRCU: \$00F) | | | | |
|---|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | R | R | R | R |
| Bit name | TRCU3 | TRCU2 | TRCU1 | TRCU0 |

Figure 48 Timer Read Register C Upper Digit (TRCU)

Timer D

Timer D Functions: Timer D has the following functions.

- Free-running/reload timer
- External event counter
- Timer output operation (toggle, low-level, high-level, and PWM outputs)
- Input capture timer

The block diagram for each operation mode of timer D is shown in figures 49(1) and 49(2).

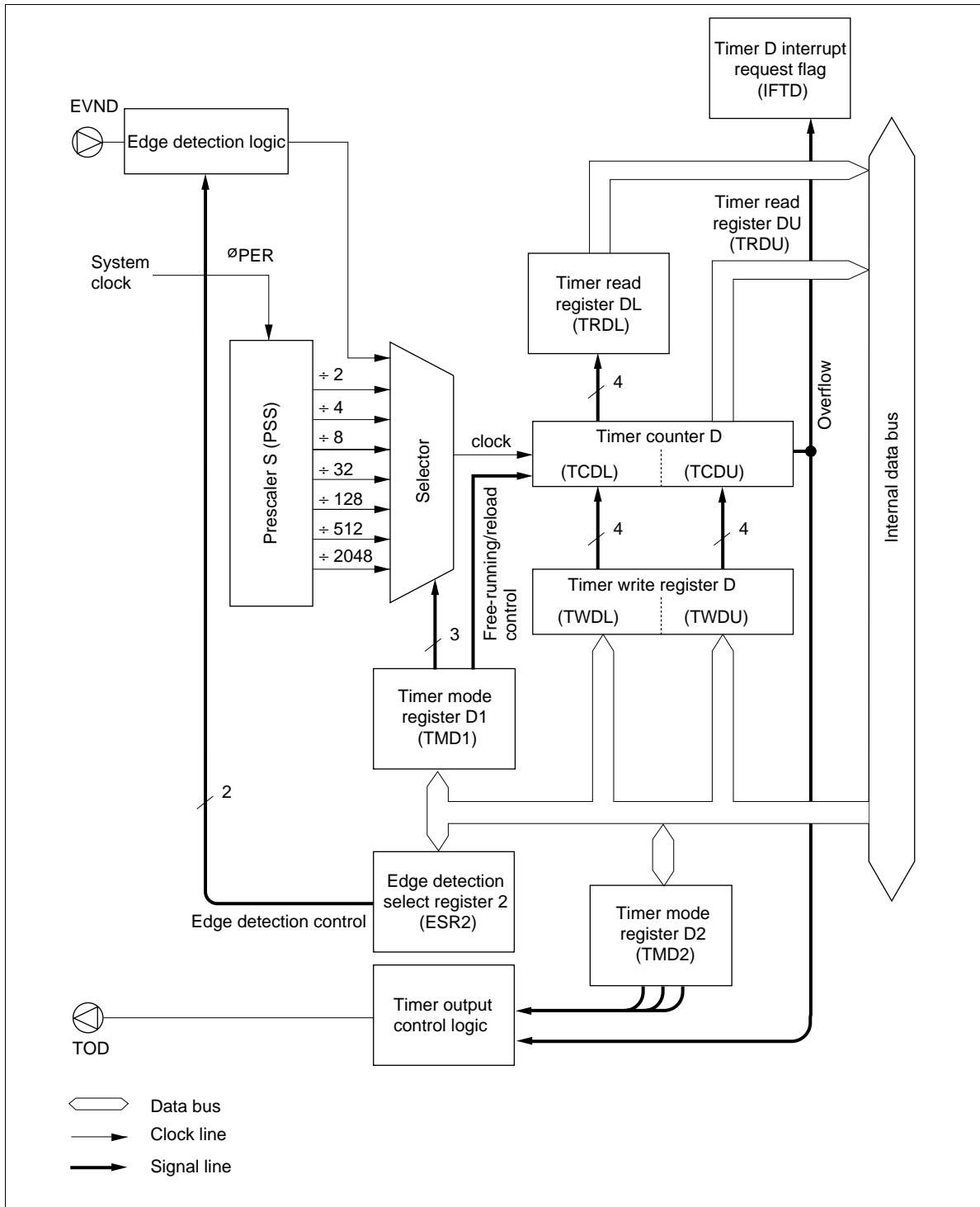


Figure 49(1) Block Diagram of Timer D (Free-Running/Reload Timer/Event Counter Modes)

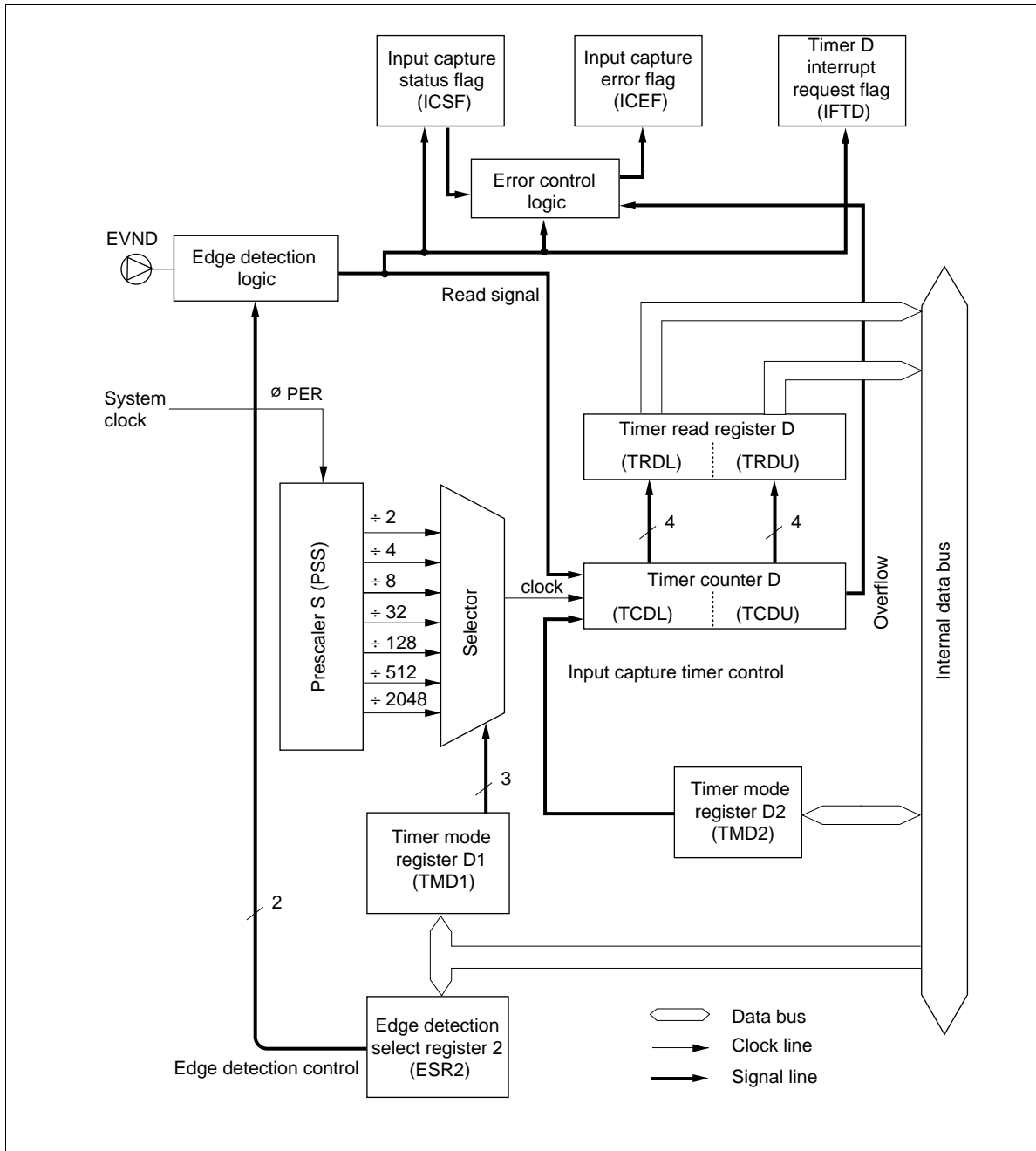


Figure 49(2) Block Diagram of Timer D (Input Capture Timer)

HD404669 Series

Timer D Operations:

- Free-running/reload timer operation: The free-running/reload operation, input clock source, and prescaler division ratio are selected by timer mode register D1 (TMD1: \$010).

Timer D is initialized to the value set in timer write register D (TWDL: \$011, TWDU: \$012) by software and incremented by one at each clock input. If an input clock is applied to timer D after it has reached \$FF, an overflow is generated. In this case, if the reload timer function is enabled, timer D is initialized to its initial value set in timer write register D (TWDL: \$011, TWDU: \$012); if the free-running timer function is enabled, the timer is initialized to \$00 and then incremented again.

The timer D interrupt request flag (IFTD: \$003, 0) is reset by the program, and by an MCU reset or a transition to stop mode. For details, see figure 3, Configuration of Interrupt Control Bits and Register Flag Areas, and table 1, Initial Values after MCU Reset.

- External event counter operation: When external event input is designated for the input clock by timer mode register D1 (TMD1), timer D operates as an external event counter. In this case, pin R4₀/EVND must be set to EVND by port mode register C (PMRC: \$025).

Either falling or rising edge, or both falling and rising edges of input signals can be selected as the external event detection edge by detection edge select register 2 (ESR2: \$027). When both rising and falling edges detection is selected, the time between the falling edge and rising edge of input signals must be $2t_{cyc}$ or longer.

Timer D is incremented by one at each detection edge selected by detection edge select register 2 (ESR2: \$027). The other operation is basically the same as the free-running/reload timer operation.

- Timer output operation: The following four output modes can be selected for timer D by setting timer mode register D2 (TMD2: \$015).

- Toggle
- Low-level output
- High-level output
- PWM output

Pin R3₂/TOD is set to TOD.

- Toggle output: The operation is basically the same as that of timer-C's toggle output.
- 0 output: The operation is basically the same as that of timer-C's 0 output.
- 1 output: The operation is basically the same as that of timer-C's 1 output.
- PWM output: The operation is basically the same as that of timer-C's PWM output.

- Input capture timer operation: The input capture timer counts the clock cycles between trigger edges input to pin EVND.

Either falling or rising edge, or both falling and rising edges of input signals can be selected as the trigger input edge by detection edge select register 2 (ESR2: \$027).

When a trigger edge is input to EVND, the count of timer D is written to timer read register D (TRDL: \$011, TRDU: \$012), and the timer D interrupt request flag (IFTD: \$003, bit 0) and the input capture status flag (ICSF: \$021, bit 0) are set. Timer D is reset to \$00, and then incremented again. While ICSF is set, if a trigger input edge is applied to timer D, or if timer D generates an overflow, the input capture error flag (ICEF: \$021, bit 0) is set. ICSF and ICEF are reset to 0 by MCU reset or by writing 0.

By selecting the input capture operation, pin R3₂/TOD is set to R3₂ and timer D is reset to \$00.

Registers for Timer D Operation: By using the following registers, timer D operation modes are selected and the timer D count is read and written.

- Timer mode register D1 (TMD1: \$010)
- Timer mode register D2 (TMD2: \$015)
- Timer write register D (TWDL: \$011, TWDU: \$012)
- Timer read register D (TRDL: \$011, TRDU: \$012)
- Port mode register C (PMRC: \$025)
- Detection edge select register 2 (ESR2: \$027)

Timer mode register D1 (TMD1: \$010): Four-bit write-only register that selects the free-running/reload timer function, input clock source, and the prescaler division ratio as shown in figure 50. Timer mode register D1 (TMD1: \$010) is reset to \$0 by an MCU reset or in stop mode.

- Writing to this register is valid from the second instruction execution cycle after the execution of the previous timer mode register D1 (TMD1: \$010) write instruction. Setting timer D's initialization by writing to timer write register D (TWDL: \$011, TWDU: \$012) must be done after a mode change becomes valid.
- When selecting the input capture timer operation, select the internal clock as the input clock source. When designating external event input for the input clock, set bit 1 (PMRC1) of port mode register C (PMRC) to 1.

HD404669 Series

Timer mode register D1 (TMD1: \$010)

| | | | | |
|---------------|-------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TMD13 | TMD12 | TMD11 | TMD10 |

| TMD13 | Free-running/reload timer selection | TMD12 | TMD11 | TMD10 | Input clock period and input clock source |
|-------|-------------------------------------|-------|-------|-------|---|
| 0 | Free-running timer | 0 | 0 | 0 | $2048t_{cyc}$ |
| 1 | Reload timer | | | 1 | $512t_{cyc}$ |
| | | | 1 | 0 | $128t_{cyc}$ |
| | | | | 1 | $32t_{cyc}$ |
| | | 1 | 0 | 0 | $8t_{cyc}$ |
| | | | | 1 | $4t_{cyc}$ |
| | | | 1 | 0 | $2t_{cyc}$ |
| | | | | 1 | EVND (external event input) |

Figure 50 Timer Mode Register D1 (TMD1)

Timer mode register D2 (TMD2: \$015): Timer mode register D2 (TMD2: \$015) is a 4-bit read/write register, used to switch the function of the R3₂/TOD pin and select the timer D output mode as shown in figure 51. Timer mode register D2 (TMD2: \$015) is reset to \$0 by an MCU reset and in stop mode.

| Timer mode register D2 (TMD2: \$015) | | | | |
|--------------------------------------|-------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | R/W | R/W | R/W | R/W |
| Bit name | TMD23 | TMD22 | TMD21 | TMD20 |

| TMD23 | TMD22 | TMD21 | TMD20 | R3 ₂ /TOD mode selection | |
|-------|-------|-------|-------|-------------------------------------|--------------------------------------|
| 0 | 0 | 0 | 0 | R3 ₂ | R3 ₂ port |
| | | | 1 | TOD | Toggle output |
| | | 1 | 0 | TOD | 0 output |
| | | | 1 | TOD | 1 output |
| | 1 | 0 | 0 | — | Not used |
| | | | 1 | | |
| | | 1 | 0 | | |
| | | | 1 | TOD | PWM output |
| 1 | × | × | × | R3 ₂ | Input capture (R3 ₂ port) |

× : Don't care

Figure 51 Timer Mode Register D2 (TMD2)

Timer write register D (TWDL: \$011, TWDU: \$012): Write-only register consisting of the lower digit (TWDL: \$011) and the upper digit (TWDU: \$012). The operation of timer write register D is basically the same as that of timer write register C (TWCL: \$00E, TWCU: \$00F).

| Timer write register D (lower digit) (TWDL: \$011) | | | | |
|--|-------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TWDL3 | TWDL2 | TWDL1 | TWDL0 |

Figure 52 Timer Write Register D Lower Digit (TWDL)

HD404669 Series

Timer write register D (upper digit) (TWDU: \$012)

| | | | | |
|---------------|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | W | W | W | W |
| Bit name | TWDU3 | TWDU2 | TWDU1 | TWDU0 |

Figure 53 Timer Write Register D Upper Digit (TWDU)

Timer read register D (TRDL: \$011, TRDU: \$012): Read-only register consisting of the lower digit (TRDL) and the upper digit (TRDU). The operation of timer read register D is basically the same as that of timer read registerC (TRCL: \$00E, TRCU: \$00F).

When the input capture timer operation is selected and if the count of timer D is read after a trigger is input, either the lower or upper digit can be read first.

Timer read register D (lower digit) (TRDL: \$011)

| | | | | |
|---------------|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | R | R | R | R |
| Bit name | TRDL3 | TRDL2 | TRDL1 | TRDL0 |

Figure 54 Timer Read Register D Lower Digit (TRDL)

Timer read register D (upper digit) (TRDU: \$012)

| | | | | |
|---------------|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | R | R | R | R |
| Bit name | TRDU3 | TRDU2 | TRDU1 | TRDU0 |

Figure 55 Timer Read Register D Upper Digit (TRDU)

Port mode register C (PMRC: \$025): Write-only register that selects R4₀/EVND pin function as shown in figure 56. It is reset to \$0 by MCU reset.

Port mode register C (PMRC: \$025) bits 3 and 1 (PMRC3, PMRC1) are reset to 00 by an MCU reset or in stop mode. Bit 2 (PMRC2) is reset to 0 by an MCU reset, but retains its previous setting in stop mode.

| Port mode register C (PMRC: \$025) | | | | |
|---|-------|-------|-------|----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | — |
| Read/Write | W | W | W | — |
| Bit name | PMRC3 | PMRC2 | PMRC1 | Not Used |

| PMRC2 | D ₁₂ / $\overline{\text{STOPC}}$ pin mode selection | PMRC1 | R4 ₀ /EVND pin mode selection |
|-------|--|-------|--|
| 0 | D ₁₂ | 0 | R4 ₀ |
| 1 | $\overline{\text{STOPC}}$ | 1 | EVND |

| PMRC3 | D ₁₃ / $\overline{\text{INT}}_0$ pin mode selection |
|-------|--|
| 0 | D ₁₃ |
| 1 | $\overline{\text{INT}}_0$ |

Figure 56 Port Mode Register C (PMRC)

HD404669 Series

Detection edge select register 2 (ESR2: \$027): Write-only register that selects the detection edge of signals input to pin EVND as shown in figure 57. It is reset to \$0 by an MCU reset or in stop mode.

| Detection edge select register 2 (ESR2: \$027) | | | | | |
|--|-------|-------|-------|-------|--|
| Bit | 3 | 2 | 1 | 0 | |
| Initial value | 0 | 0 | 0 | 0 | |
| Read/Write | W | W | W | W | |
| Bit name | ESR23 | ESR22 | ESR21 | ESR20 | |

| ESR23 | ESR22 | EVND detection edge | ESR21 | ESR20 | INT ₄ detection edge |
|-------|-------|------------------------|-------|-------|---------------------------------|
| 0 | 0 | No detection | 0 | 0 | No detection |
| | 1 | Falling-edge detection | | 1 | Falling-edge detection |
| 1 | 0 | Rising-edge detection | 1 | 0 | Rising-edge detection |
| | 1 | Double-edge detection* | | 1 | Double-edge detection* |

Note: * Both falling and rising edges are detected.

Figure 57 Detection Edge Select Register 2 (ESR2)

Serial Interface

Serial Interface Overview

Function

- 8-bit serial data transmission/reception

Features

- Multiple transmit clock sources
 - External clock
 - Internal prescaler output clock
 - System clock
- High/low control in idle states

Configuration

- Serial data register 1 (SR1L: \$006, SR1U: \$007)
- Serial mode register 1 A (SM1A: \$005)
- Serial mode register 1 B (SM1B: \$028)
- Port mode register A (PMRA: \$004)
- Miscellaneous register (MIS: \$00C)
- Octal counter (OC1)
- Selector

The block diagram of the serial interface is shown in figure 58.

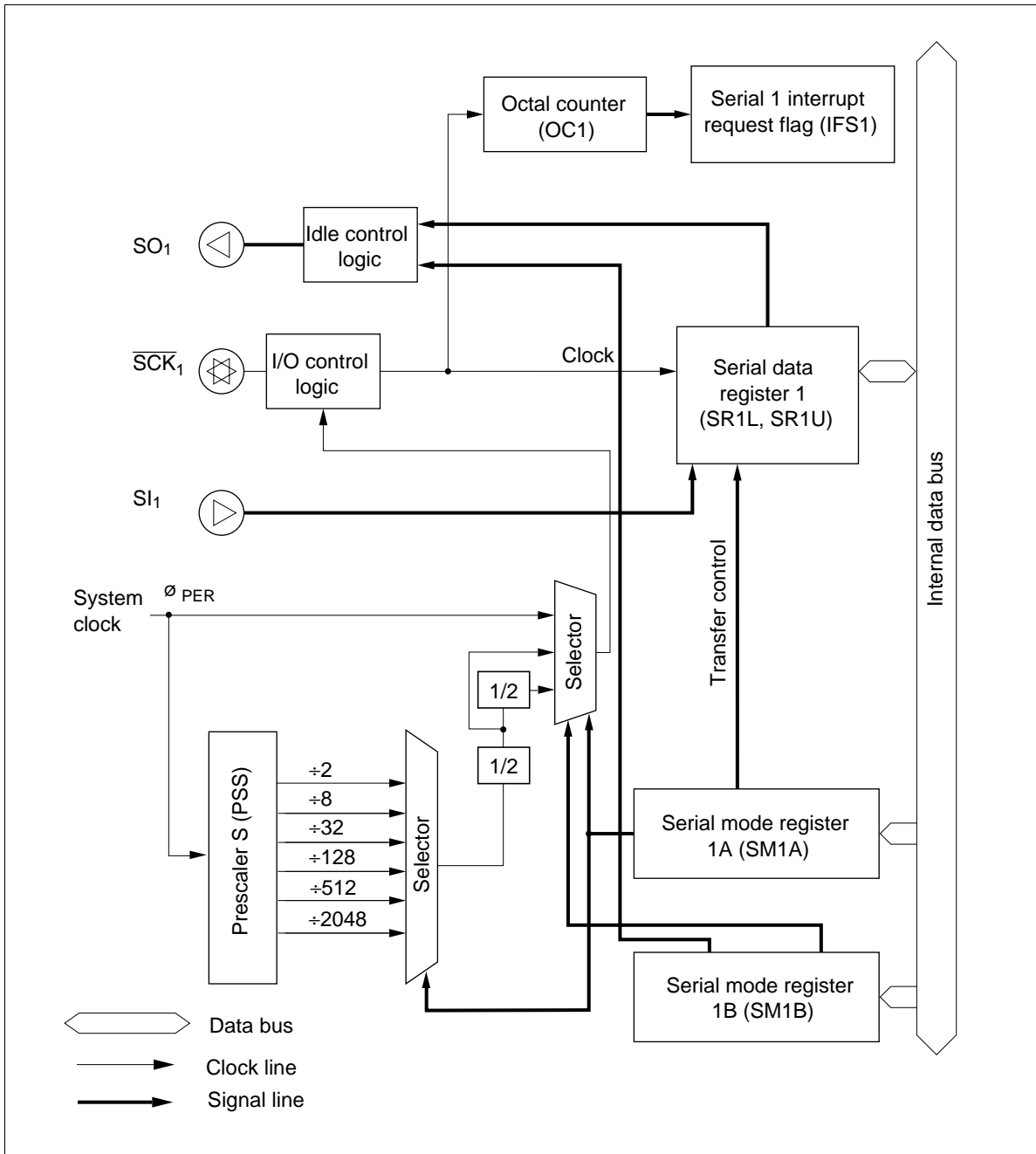


Figure 58 Block Diagram of Serial Interface

Serial Interface Operation

Selecting and Changing the Operating Mode: Table 19 lists the serial interface's operating modes. To select an operating mode, use one of these combinations of port mode register A (PMRA: \$004) and serial mode register 1A (SM1A: \$005) settings; to change the operating mode, always initialize the serial interface internally by writing data to serial mode register 1A (SM1A: \$005). Note that the serial interface is initialized by writing data to serial mode register 1A (SM1A: \$005). Refer to the following Serial Mode Register 1A section for details.

Pin Setting: The $R4_1/\overline{SCK}_1$ pin is controlled by writing data to serial mode register 1A (SM1A: \$005). The $R4_2/SI_1$ and $R4_3/SO_1$ pins are controlled by writing data to port mode register A (PMRA: \$004). Refer to the following Registers for Serial Interface section for details.

Transmit Clock Source Setting: The transmit clock source is set by writing data to serial mode register 1A (SM1A: \$005) and serial mode register 1B (SM1B: \$028). Refer to the following Registers for Serial Interface section for details.

Data Setting: Transmit data is set by writing data to the serial data register 1 (SR1L: \$006, SR1U: \$007). Receive data is obtained by reading the contents of the serial data register 1 (SR1L: \$006, SR1U: \$007). The serial data is shifted by the transmit clock and is input from or output to an external system.

The output level of the SO_1 pin is invalid until the first data is output after MCU reset, or until the High/Low level control in idle states is performed.

Table 19 Serial Interface Operating Modes

| SM1A | PMRA | | Operating Mode |
|-------|-------|-------|-------------------------------------|
| Bit 3 | Bit 1 | Bit 0 | |
| 1 | 0 | 0 | Serial clock continuous output mode |
| | | 1 | Transmit mode |
| | 1 | 0 | Receive mode |
| | | 1 | Transmit/receive mode |

Transfer Control: The serial interface is activated by the STS instruction. The octal counter is reset to 000 by this instruction, and it increments at the rising edge of the transmit clock. When the eighth transmit clock signal is input or when serial transmission/receive is discontinued, the octal counter is reset to 000, the serial 1 interrupt request flag (IFS1: \$003, bit 2) is set, and the transfer stops.

When the prescaler output is selected as the transmit clock, the transmit clock frequency is selected as $4t_{cyc}$ to $8192t_{cyc}$ by setting bits 2 to 0 (SM1A2– SM1A0) of serial mode register 1A (SM1A: \$005) and bit 0 (SM1B0) of serial mode register 1B (SM1B: \$028) as listed in table 20.

HD404669 Series

Table 20 Serial Transmit Clock (Prescaler Output)

| SM1B | | SM1A | | Transmit Clock Division Ratio | Transmit Clock Frequency |
|-------|-------|-------|----------------------------------|-----------------------------------|--------------------------|
| Bit 0 | Bit 2 | Bit 1 | Bit 0 | | |
| 0 | 0 | 0 | 0 | $(\emptyset_{PER} / 2048) \div 2$ | $4096t_{cyc}$ |
| | | | 1 | $(\emptyset_{PER} / 512) \div 2$ | $1024t_{cyc}$ |
| | | 1 | 0 | $(\emptyset_{PER} / 128) \div 2$ | $256t_{cyc}$ |
| | | | 1 | $(\emptyset_{PER} / 32) \div 2$ | $64t_{cyc}$ |
| | 1 | 0 | 0 | $(\emptyset_{PER} / 8) \div 2$ | $16t_{cyc}$ |
| | | | 1 | $(\emptyset_{PER} / 2) \div 2$ | $4t_{cyc}$ |
| | | 1 | 0 | $(\emptyset_{PER} / 2048) \div 4$ | $8192t_{cyc}$ |
| | | | 1 | $(\emptyset_{PER} / 512) \div 4$ | $2048t_{cyc}$ |
| 1 | 0 | 0 | $(\emptyset_{PER} / 128) \div 4$ | $512t_{cyc}$ | |
| | | 1 | $(\emptyset_{PER} / 32) \div 4$ | $128t_{cyc}$ | |
| | 1 | 0 | $(\emptyset_{PER} / 8) \div 4$ | $32t_{cyc}$ | |
| | | 1 | $(\emptyset_{PER} / 2) \div 4$ | $8t_{cyc}$ | |

Operating States: The serial interface has the operating states shown in figure 59 in external clock mode and internal clock mode.

STS wait state
 Transmit clock wait state
 Transfer state
 Serial clock continuous output state (internal clock mode only)

- STS wait state: The serial interface enters STS wait state by MCU reset (00, 10 in figure 59). In STS wait state, the serial interface is initialized and the transmit clock is ignored. If the STS instruction is then executed (01, 11), the serial interface enters transmit clock wait state.

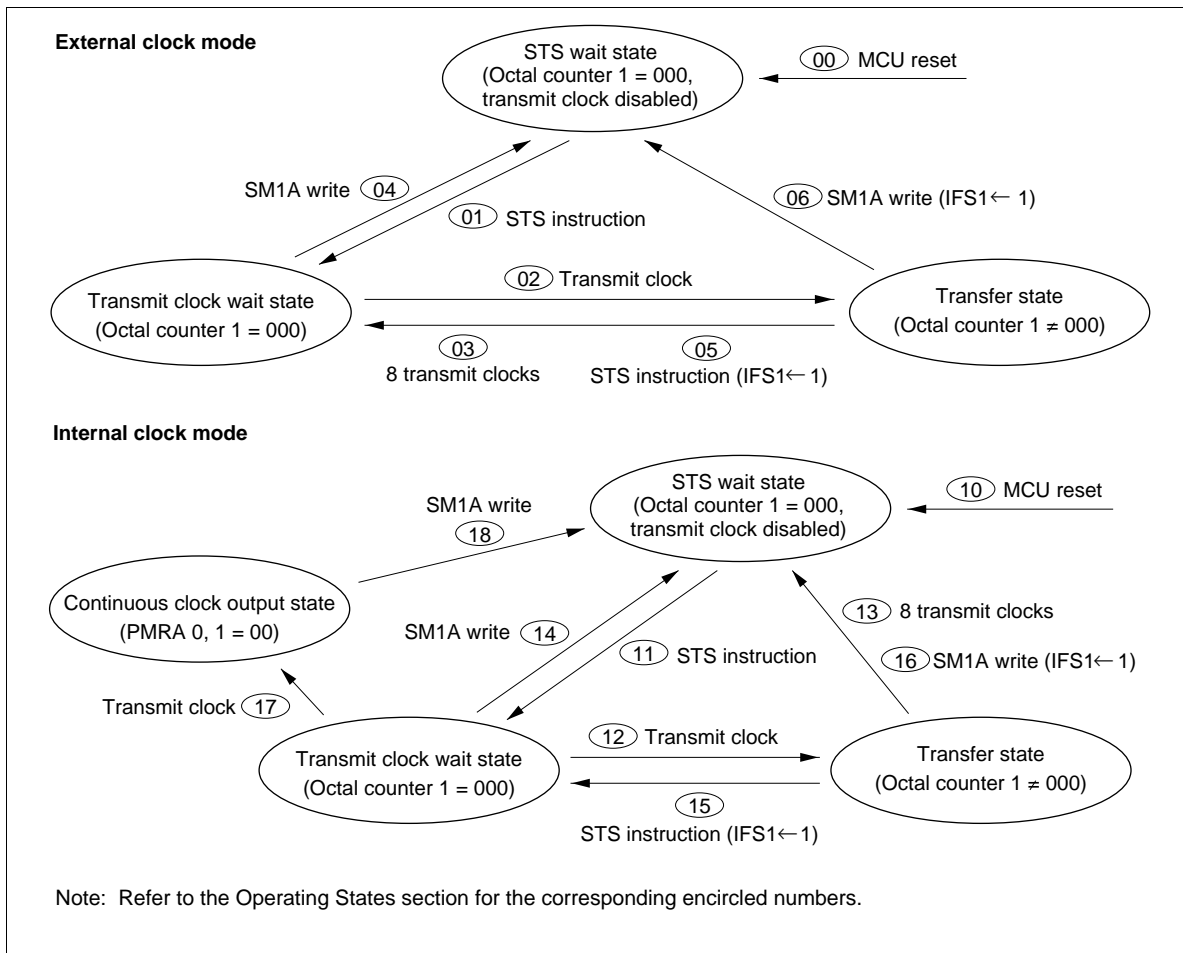


Figure 59 Serial Interface State Transitions

- **Transmit clock wait state:** Transmit clock wait state is between the STS execution and the falling edge of the first transmit clock. In transmit clock wait state, input of the transmit clock (02, 12) increments the octal counter, shifts the serial data register 1 (SR1L: \$006, SR1U: \$007), and enters the serial interface in transfer state. However, note that if continuous clock output mode is selected in internal clock mode, the serial interface does not enter transfer state but enters continuous clock output state (17).

The serial interface enters STS wait state by writing data to serial mode register 1A (SM1A: \$005) (04, 14) in transmit clock wait state.

- **Transfer state:** Transfer state is between the falling edge of the first clock and the rising edge of the eighth clock. In transfer state, the input of eight clocks or the execution of the STS instruction sets the octal counter to 000, and the serial interface enters another state. When the STS instruction is executed (05, 15), transmit clock wait state is entered. When eight clocks are input, transmit clock wait state is entered (03) in external clock mode, and STS wait state is entered (13) in internal clock mode. In internal clock mode, the transmit clock stops after outputting eight clocks.

In transfer state, writing data to serial mode register 1A (SM1A: \$005) (06, 16) initializes the serial interface, and STS wait state is entered.

HD404669 Series

If the state changes from transfer to another state, the serial 1 interrupt request flag (IFS1: \$003, bit 2) is set by the octal counter that is reset to 000.

- Continuous clock output state (only in internal clock mode): Continuous clock output state is entered only in internal clock mode. In this state, the serial interface does not transmit/receive data but only outputs the transmit clock from the \overline{SCK}_1 pin.

When bits 1 and 0 (PMRA1, PMRA0) of port mode register A (PMRA: \$004) are 00 in transmit clock wait state and if the transmit clock is input (17), the serial interface enters continuous clock output state. If serial mode register 1A (SM1A: \$005) is written to in continuous clock output mode (18), STS wait state is entered.

High/Low Control in Idle States: In idle states, that is, STS wait state and transmit clock wait state, the output level of the SO_1 pin can be controlled by setting bit 1 (SM1B1) of serial mode register 1B (SM1B: \$028) to 0 or 1. The high/low control example is shown in figure 60. Note that the high/low level cannot be controlled in transfer state.

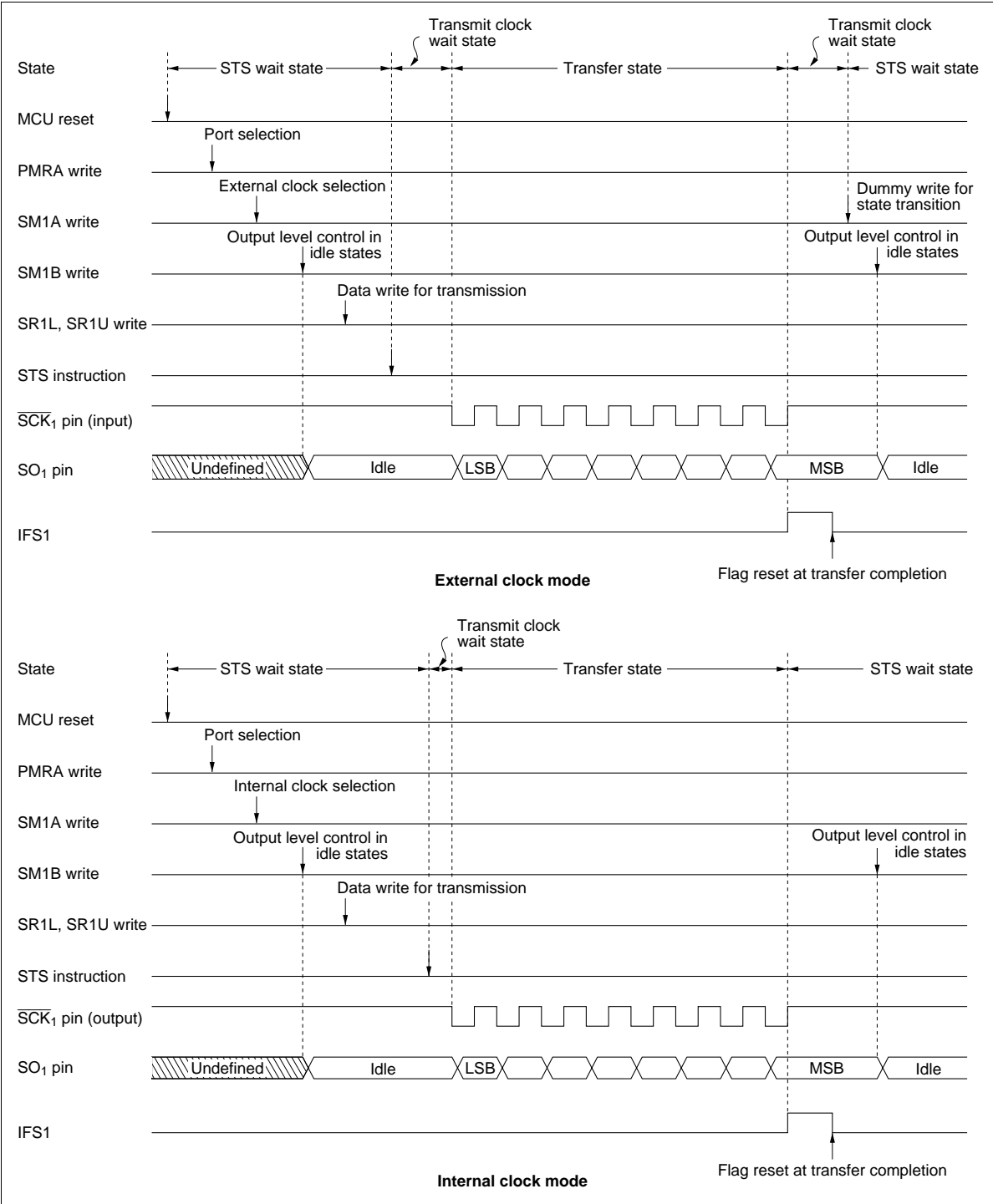


Figure 60 Example of Serial Interface Operation Sequence

HD404669 Series

Transmit Clock Error Detection (In External Clock Mode): The serial interface will malfunction if a spurious pulse caused by external noise conflicts with a normal transmit clock during transfer. A transmit clock error of this type can be detected as shown in figure 61. If more than eight transmit clocks are input in transfer state, at the eighth clock including a spurious pulse by noise, the octal counter reaches 000, the serial 1 interrupt request flag (IFS1: \$003, bit 2) is set, and transmit clock wait state is entered. At the falling edge of the next normal clock signal, the transfer state is entered.

Meanwhile, in the interrupt handling routine, transfer end processing is performed, the serial 1 interrupt request flag is reset, and a dummy write is performed to serial mode register 1A (SM1A: \$005). The serial interface then returns to the STS wait state, and the serial 1 interrupt request flag (IFS1: \$003, 2) is set again. It is therefore possible to detect a serial clock error by testing the serial 1 interrupt request flag after the dummy write to serial mode register 1A.

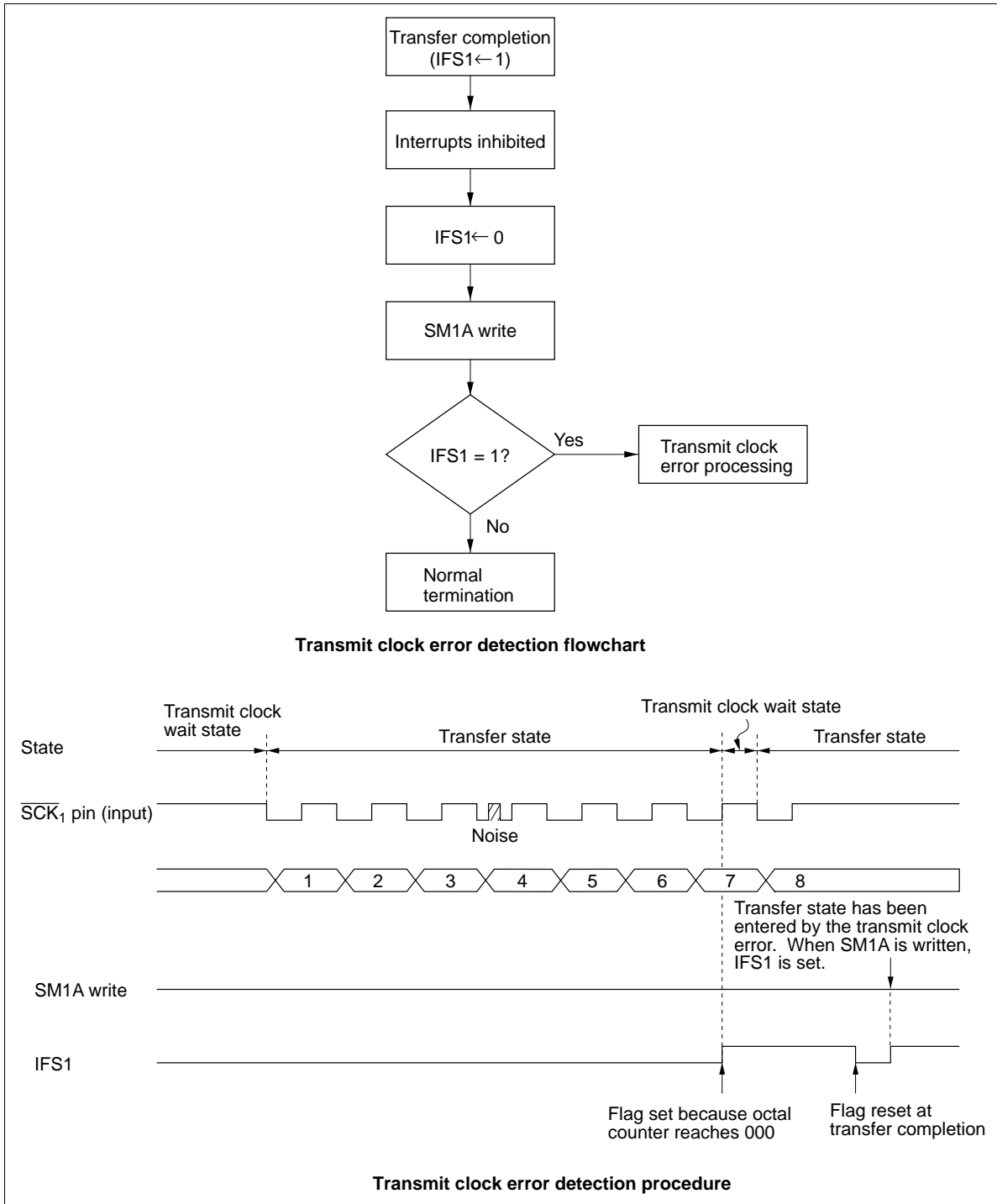


Figure 61 Transmit Clock Error Detection

HD404669 Series

Notes on Use:

- Initialization after writing to registers: If port mode register A (PMRA: \$004) is written to in transmit clock wait state or in transfer state, the serial interface must be initialized by writing to serial mode register 1A (SM1A: \$005) again.
- Serial 1 interrupt request flag (IFS1: \$003, bit 2) set: If the state is changed from transfer to another by writing to serial mode register 1A (SM1A: \$005) or executing the STS instruction during the first low pulse of the transmit clock, the serial interrupt request flag 1 (IFS1: \$003, 2) is not set. To set the serial interrupt request flag, serial mode register 1A (SM1A: \$005) write or STS instruction execution must be programmed to be executed after confirming that the \overline{SCK}_1 pin is at 1, that is, after executing the input instruction to port R4.

Registers for Serial Interface

The serial interface operation is selected, and serial data is read and written by the following registers.

Serial Mode Register 1A (SM1A: \$005)
Serial Mode Register 1B (SM1B: \$028)
Serial Data Register 1 (SR1L: \$006, SR1U: \$007)
Port Mode Register A (PMRA: \$004)
Miscellaneous Register (MIS: \$00C)

Serial Mode Register 1A (SM1A: \$005): This register has the following functions (figure 62).

- $R4_1/\overline{SCK}_1$ pin function selection
- Transfer clock selection
- Prescaler division ratio selection
- Serial interface initialization

Serial mode register 1A (SM1A: \$005) is a 4-bit write-only register. It is reset to \$0 by an MCU reset or when the MCU switches to stop mode.

A write signal input to serial mode register 1A (SM1A: \$005) discontinues the input of the transmit clock to the serial data register 1 (SR1L: \$006, SR1U: \$007) and octal counter, and the octal counter is reset to 000. Therefore, if a write is performed during data transfer, the serial 1 interrupt request flag (IFS1: \$003, bit 2) is set.

Written data is valid from the second instruction execution cycle after the write operation, so the STS instruction must be executed at least two cycles after that.

Serial mode register 1A (SM1A: \$005)

| | | | | |
|---------------|-------|-------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | SM1A3 | SM1A2 | SM1A1 | SM1A0 |

| SM1A3 | R4 ₁ / $\overline{\text{SCK}}_1$ mode selection | SM1A2 | SM1A1 | SM1A0 | $\overline{\text{SCK}}_1$ | Clock source | Prescaler division ratio |
|-------|---|-------|-------|-------|---------------------------|----------------|-----------------------------|
| 0 | R4 ₁ | 0 | 0 | 0 | Output | Prescaler | Refer to table 20 |
| 1 | $\overline{\text{SCK}}_1$ | | | 1 | | | |
| | | | 1 | 0 | | | |
| | | | | 1 | | | |
| | | 1 | 0 | 0 | | | |
| | | | | 1 | | | |
| | | | 1 | 0 | Output | System clock | — |
| | | | | 1 | Input | External clock | — |

Figure 62 Serial Mode Register 1A (SM1A)

Serial Mode Register 1B (SM1B: \$028): This register has the following functions (figure 63).

- Serial clock division ratio selection
- High/low level control in idle states

Serial mode register 1B (SM1B: \$028) is a 2-bit write-only register. It cannot be written during data transfer.

Setting bit 0 (SM1B0) of the serial mode register 1B (SM1B: \$028) selects the divisor applied to the prescaler output used for the transfer clock. Only bit 0 (SM1B0) is cleared to 0 by an MCU reset or when the MCU switches to stop mode.

Bit 1 (SM1B1) of the serial mode register (SM1B: \$028) controls the high/low state of the SO₁ pin during idle. The SO₁ pin changes state as soon as the high/low control bit is written. The value of this bit is undefined after a reset or when the MCU enters stop mode.

HD404669 Series

| Serial mode register 1B (SM1B: \$028) | | | | |
|---------------------------------------|----------|----------|-----------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | — | — | Undefined | 0 |
| Read/Write | — | — | W | W |
| Bit name | Not used | Not used | SM1B1 | SM1B0 |

| SM1B1 | Output level control in idle states | SM1B0 | Transmit clock division ratio |
|-------|-------------------------------------|-------|-------------------------------|
| 0 | Low level | 0 | Prescaler output divided by 2 |
| 1 | High level | 1 | Prescaler output divided by 4 |

Figure 63 Serial Mode Register 1B (SM1B)

Serial Data Register 1 (SR1L: \$006, SR1U: \$007): This register has the following functions (figures 64 and 65).

- Transmission data write and shift
- Receive data shift and read

Writing data in this register is output from the SO₁ pin, LSB first, synchronously with the falling edge of the transmit clock; data is input, LSB first, through the SI₁ pin at the rising edge of the transmit clock. Input/output timing is shown in figure 66.

Data cannot be read or written during serial data transfer. If a read/write occurs during transfer, the accuracy of the resultant data cannot be guaranteed.

| Serial data register 1 (lower digit) (SR1L: \$006) | | | | |
|--|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | R/W | R/W | R/W | R/W |
| Bit name | SR1L3 | SR1L2 | SR1L1 | SR1L0 |

Figure 64 Serial Data Register 1 (SR1L)

| Serial data register 1 (upper digit) (SR1U: \$007) | | | | |
|--|-----------|-----------|-----------|-----------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | Undefined | Undefined | Undefined | Undefined |
| Read/Write | R/W | R/W | R/W | R/W |
| Bit name | SR1U3 | SR1U2 | SR1U1 | SR1U0 |

Figure 65 Serial Data Register 1 (SR1U)

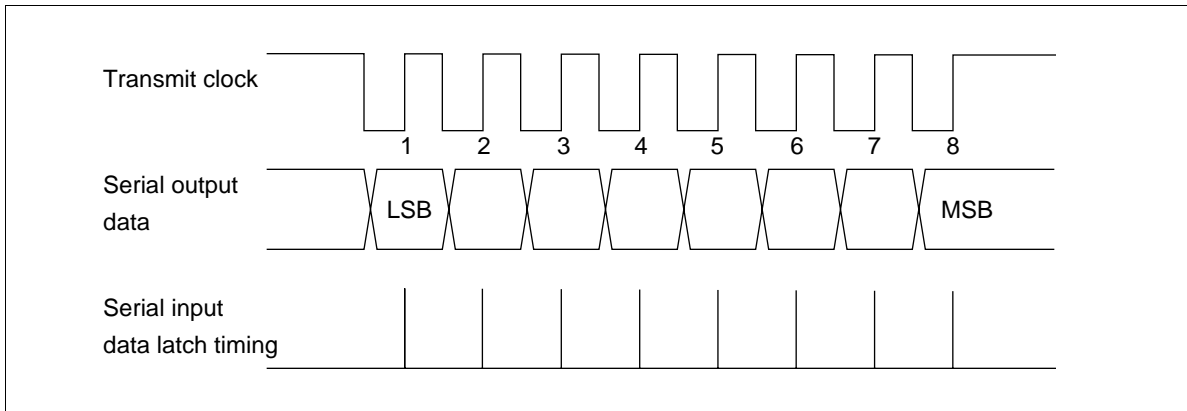


Figure 66 Serial Interface Output Timing

Port Mode Register A (PMRA: \$004): This register has the following functions (figure 67).

- R4₂/SI₁ pin function selection
- R4₃/SO₁ pin function selection

Port mode register A (PMRA: \$004) is a 2-bit write-only register. It is reset to "--00" by an MCU reset or when the MCU switches to stop mode.

Port mode register A (PMRA: \$004)

| | | | | |
|---------------|----------|----------|-------|-------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | — | — | 0 | 0 |
| Read/Write | — | — | W | W |
| Bit name | Not used | Not used | PMRA1 | PMRA0 |

| PMRA1 | R4 ₂ /SI ₁ mode selection | PMRA0 | R4 ₃ /SO ₁ mode selection |
|-------|---|-------|---|
| 0 | R4 ₂ | 0 | R4 ₃ |
| 1 | SI ₁ | 1 | SO ₁ |

Figure 67 Port Mode Register A (PMRA)

HD404669 Series

Miscellaneous Register (MIS: \$00C): This register has the following function (figure 68).

- R₄₃/SO₁ pin PMOS control

Miscellaneous register (MIS: \$00C) is a 4-bit write-only register and is reset to \$0 by an MCU reset or in stop mode.

| Miscellaneous register (MIS: \$00C) | | | | | |
|-------------------------------------|------|------|------|------|--|
| Bit | 3 | 2 | 1 | 0 | |
| Initial value | 0 | 0 | 0 | 0 | |
| Read/Write | W | W | W | W | |
| Bit name | MIS3 | MIS2 | MIS1 | MIS0 | |

| MIS3 | Pull-up/Pull-down MOS control | MIS1 | MIS0 | t _{RC} |
|------|---|------|------|-----------------|
| 0 | Off | 0 | 0 | 0.12207 ms |
| 1 | On | | | 0.24414 ms* |
| | | | 1 | 7.8125 ms |
| MIS2 | R ₄₃ /SO ₁ PMOS control | 1 | 0 | 31.25 ms |
| 0 | On | | 1 | Not used |
| 1 | Off | | | |

Note: * The value is applied only when direct transfer operation is used.

Figure 68 Miscellaneous Register (MIS)

DTMF Generation Circuit

The MCU provides a dual-tone multifrequency (DTMF) generation circuit. Figure 69 shows a block diagram of the DTMF circuit. A DTMF signal consists of two sine waves corresponding to the numbers and symbols on a telephone keypad. DTMF signals are used to access telephone switching equipment. Figure 70 shows the DTMF frequency matrix.

The OSC clock (400 kHz, 800 kHz, 2 MHz, 3.58 MHz, 4 MHz, 7.16 MHz, or 8 MHz) is changed into seven clock signals through the division circuit (1/2, 1/5, 1/9*, 1/10, 1/18*, and 1/20). The DTMF circuit uses one of the seven clock signals, which is selected by the system clock select register 1, 2 (SSR1: \$029, SSR2: \$02A) depending on the OSC clock frequency. The DTMF circuit has transformed programmable dividers, sine wave counters, and control registers.

The DTMF generation circuit is controlled by the following three registers.

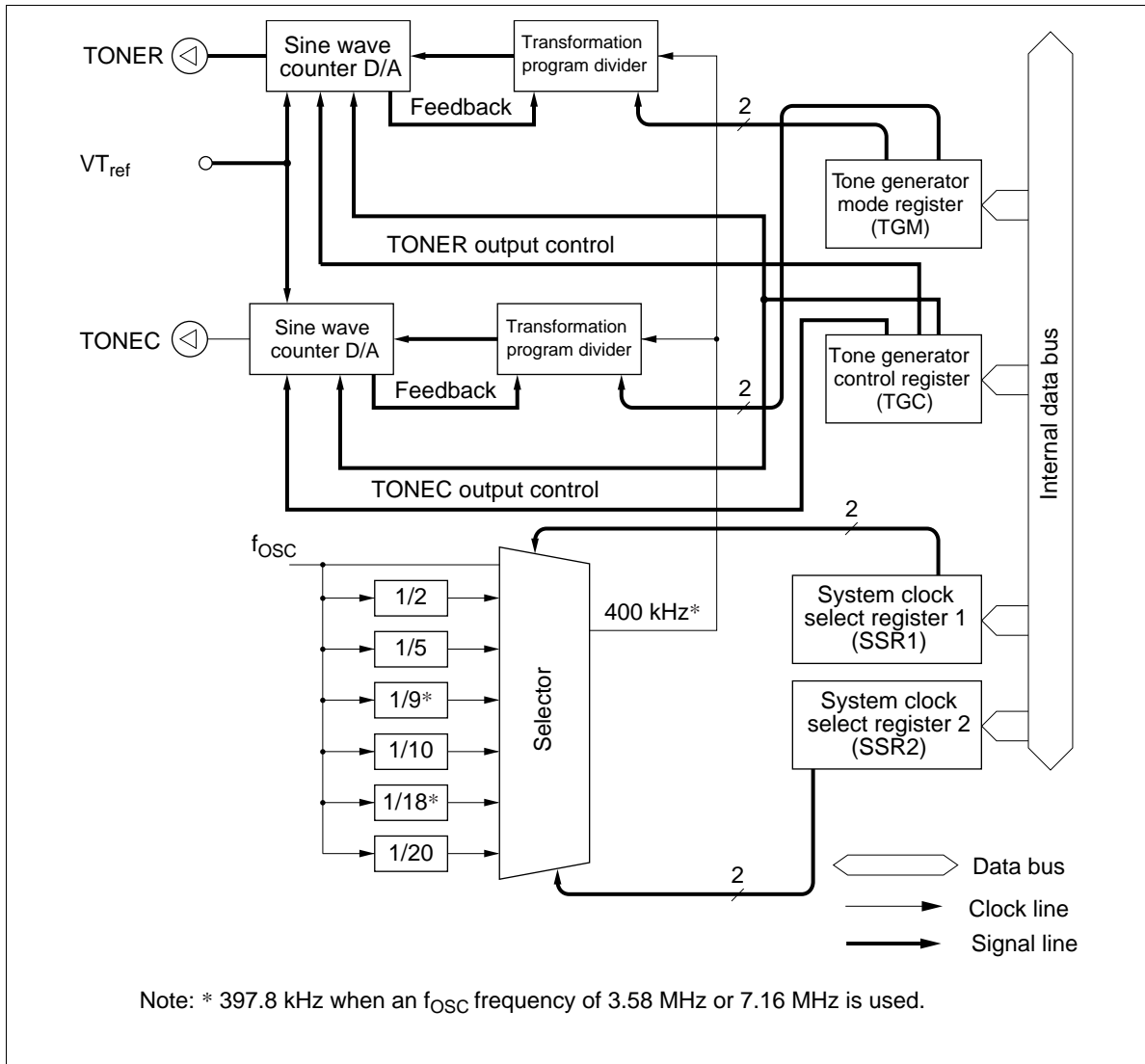


Figure 69 Block Diagram of DTMF Circuit

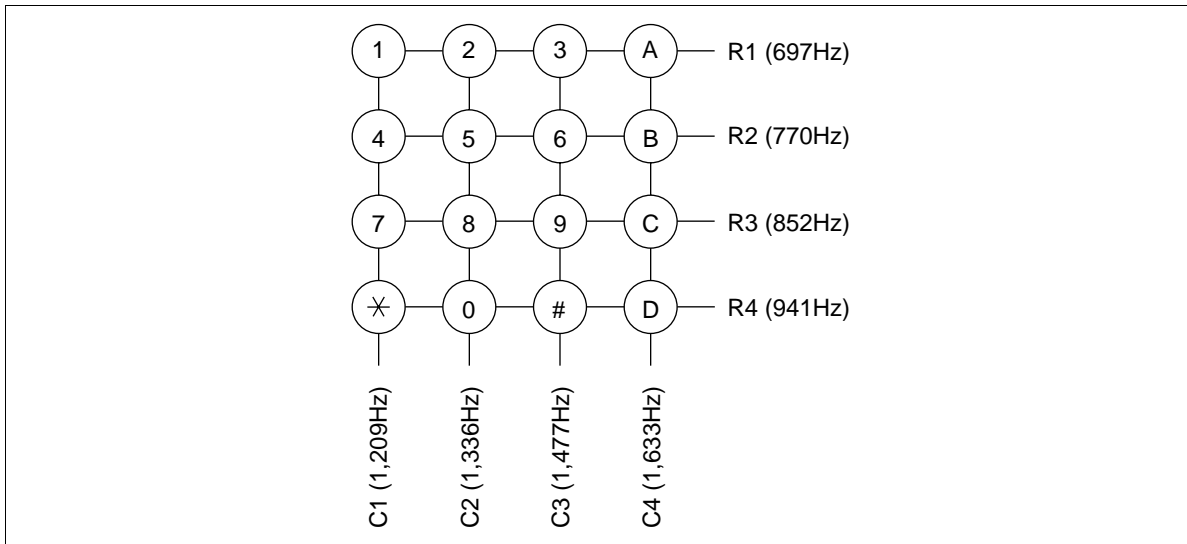


Figure 70 DTMF Keypad and Frequencies

Tone Generator Mode Register (TGM: \$019): The tone generator mode register (TGM: \$019) is a 4-bit write-only register that controls the generated DTMF frequencies as shown in figure 71. TGM is initialized to \$0 by an MCU reset or in stop mode, watch mode, and subactive mode.

Tone generator mode register (TGM: \$019)

| | | | | |
|---------------|------|------|------|------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | 0 |
| Read/Write | W | W | W | W |
| Bit name | TGM3 | TGM2 | TGM1 | TGM0 |

| TGM3 | TGM2 | TONEC output frequencies | TGM1 | TGM0 | TONER output frequencies |
|------|------|--------------------------|------|------|--------------------------|
| 0 | 0 | C1 (1,209 Hz) | 0 | 0 | R1 (697 Hz) |
| 0 | 1 | C2 (1,336 Hz) | 0 | 1 | R2 (770 Hz) |
| 1 | 0 | C3 (1,477 Hz) | 1 | 0 | R3 (852 Hz) |
| 1 | 1 | C4 (1,633 Hz) | 1 | 1 | R4 (941 Hz) |

Figure 71 Tone Generator Mode Register (TGM)

HD404669 Series

Tone Generator Control Register (TGC: \$01A): The tone generator control register (TGC: \$01A) is a 3-bit write-only register that controls starting and stopping of DTMF signal generation as shown in figure 72. TGC is initialized to 000- by an MCU reset or in stop mode, watch mode, or subactive mode. TONEC output and TONER output are controlled individually by TGC3 and TGC2, and overall DTMF control is performed by TGC1.

| Tone generator control register (TGC: \$01A) | | | | |
|--|--------------------------------------|------|-------------|------------------------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | 0 | 0 | — |
| Read/Write | W | W | W | — |
| Bit name | TGC3 | TGC2 | TGC1 | Not used |
| <hr/> | | | | |
| TGC3 | TONEC output control (column) | | TGC1 | DTMF enable bit |
| 0 | No output | | 0 | DTMF disable |
| 1 | TONEC output (active) | | 1 | DTMF enable |
| <hr/> | | | | |
| TGC2 | TONER output control (row) | | | |
| 0 | No output | | | |
| 1 | TONER output (active) | | | |

Figure 72 Tone Generator Control Register (TGC)

System Clock Select Registers 1 and 2 (SSR1: \$029 and SSR2: \$02A): The system clock select registers 1 and 2 (SSR1: \$029 and SSR2: \$02A) are 4-bit write-only registers. Applications must set these registers to the values shown in figure 73 that correspond to the frequency of the oscillator circuit connected to the OSC₁ and OSC₂ pins. If the oscillator frequency and the system clock select register settings differ from the combination shown in figure 73, the DTMF output frequencies will not have the correct values as shown in figure 71.

Except for the SSR13 bit, the system clock select registers 1 and 2 (SSR1: \$029 and SSR2: \$02A) are initialized to \$0 by an MCU reset or when the MCU switches to stop mode.

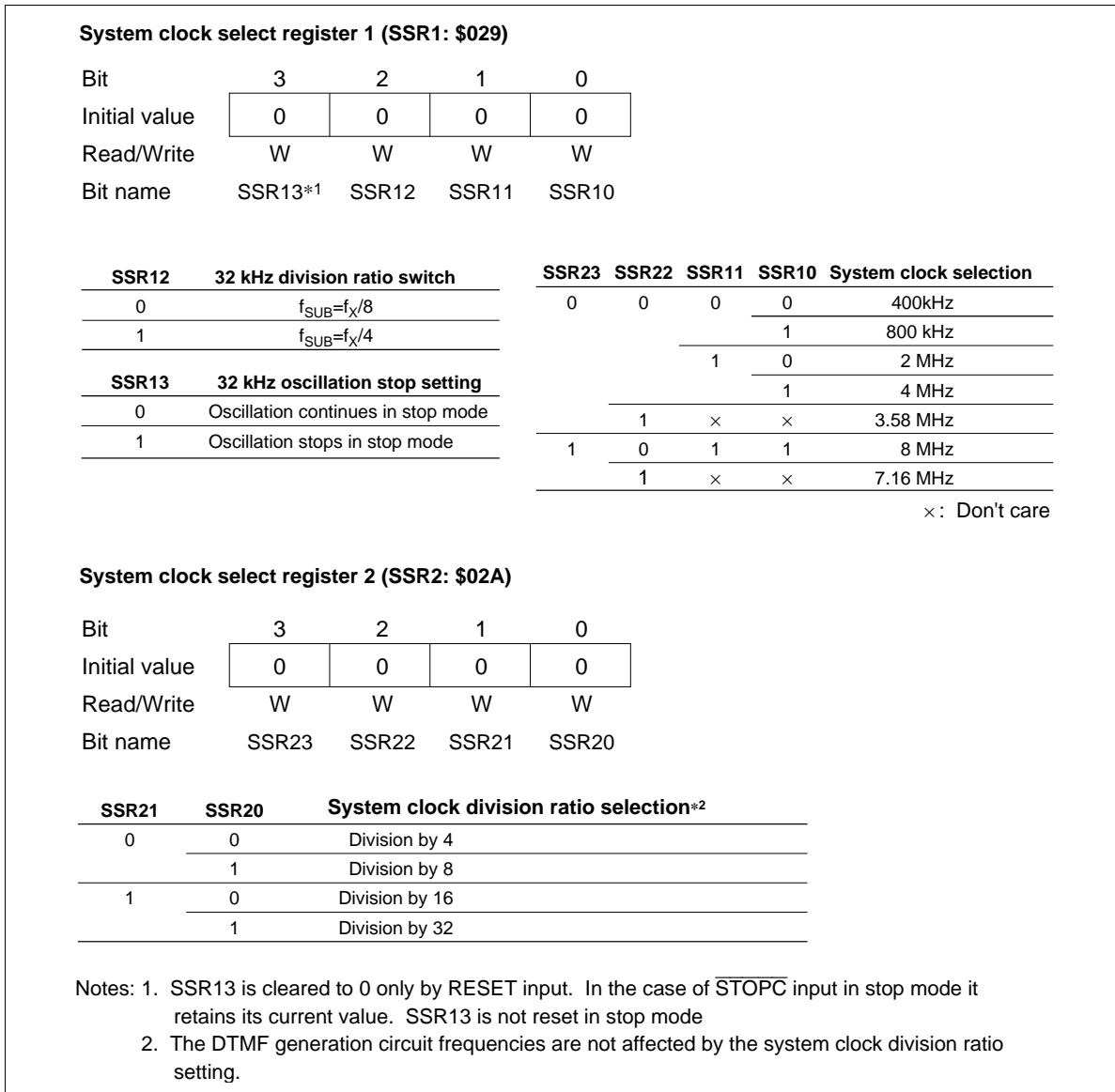


Figure 73 System Clock Select Register 1 and 2 (SSR1, SSR2)

HD404669 Series

DTMF Output: The sine waves of the row-group and column-group are output from the DTMF output pins (TONER and TONEC). These are output by a high-precision resistance-ladder type D/A converter. Figure 74 shows the TONE output pin equivalent circuit, and figure 75 shows the output waveform. One output waveform cycle is composed of 32 slots, giving stable output with a low distortion factor. Table 21 shows the deviation of the output frequencies with respect to the standard DTMF signals.

Table 21 Frequency Deviation of the MCU from Standard DTMF
($f_{osc}=400\text{kHz}, 800\text{kHz}, 2\text{MHz}, 4\text{MHz}, 8\text{MHz}$)

| | Standard DTMF (Hz) | MCU (Hz) | Deviation from Standard (%) |
|----|--------------------|----------|-----------------------------|
| R1 | 697 | 694.44 | -0.37 |
| R2 | 770 | 769.23 | -0.10 |
| R3 | 852 | 851.06 | -0.11 |
| R4 | 941 | 938.97 | -0.22 |
| C1 | 1,209 | 1,212.12 | 0.26 |
| C2 | 1,336 | 1,333.33 | -0.20 |
| C3 | 1,477 | 1,481.48 | 0.30 |
| C4 | 1,633 | 1,639.34 | 0.39 |

Table 22 Frequency Deviation of the MCU from Standard DTMF ($f_{osc}=3.58\text{kHz}, 7.16\text{MHz}$)

| | Standard DTMF (Hz) | MCU (Hz) | Deviation from Standard (%) |
|----|--------------------|----------|-----------------------------|
| R1 | 697 | 690.58 | -0.92 |
| R2 | 770 | 764.96 | -0.65 |
| R3 | 852 | 846.33 | -0.67 |
| R4 | 941 | 933.75 | -0.77 |
| C1 | 1,209 | 1,205.39 | -0.30 |
| C2 | 1,336 | 1,325.92 | -0.75 |
| C3 | 1,477 | 1,473.25 | -0.25 |
| C4 | 1,633 | 1,630.23 | -0.17 |

- Notes: 1. The DTMF signal frequency deviation must be within $\pm 1.5\%$, totaling the values in tables 21 and 22 and the precision of the oscillator used. When an f_{osc} frequency of 3.58 MHz or 7.16 MHz is used, in particular, the frequency deviation is greater (max - 0.92%) than with an f_{osc} frequency of 400 kHz, 800 kHz, 2 MHz, 4 MHz, or 8 MHz, and thorough consultation with the oscillator manufacturer is essential before deciding on the oscillator to be used.
2. This frequency deviation does not include the frequency deviation of the oscillator. Also, the ratio of oscillator waveform high-level width and low-level width in this case is 50% : 50%.

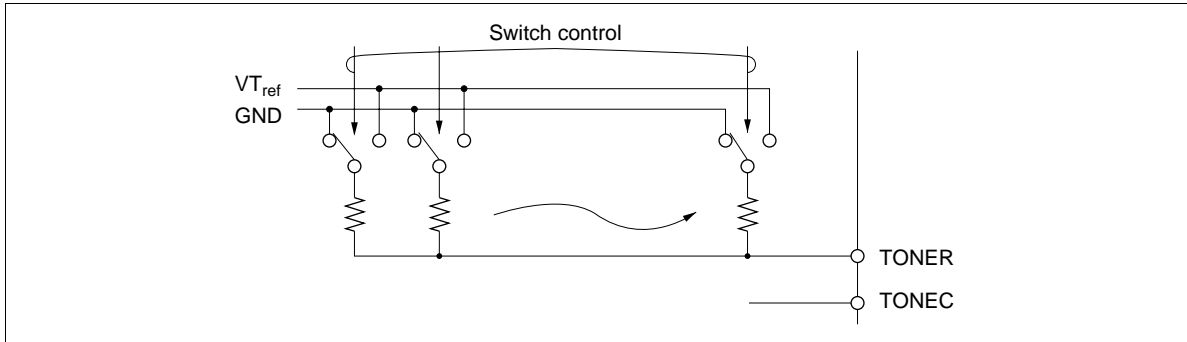


Figure 74 Tone Output Equivalent Circuit

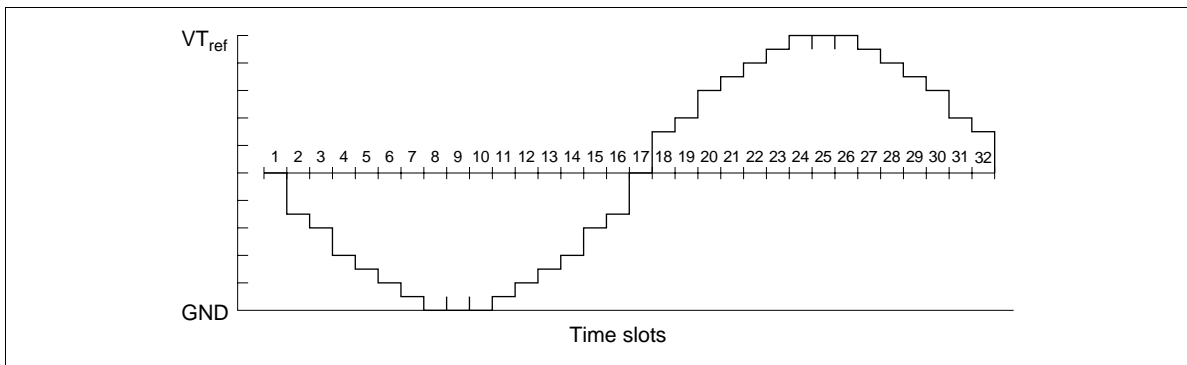


Figure 75 Waveform of Tone Output

Comparator

The MCU has a built-in comparator that compare an input voltage with the reference voltage (V_{Cref}). The comparator block diagram is shown in figure 76.

The comparator can operate in active mode and subactive mode. They are halted in other modes.

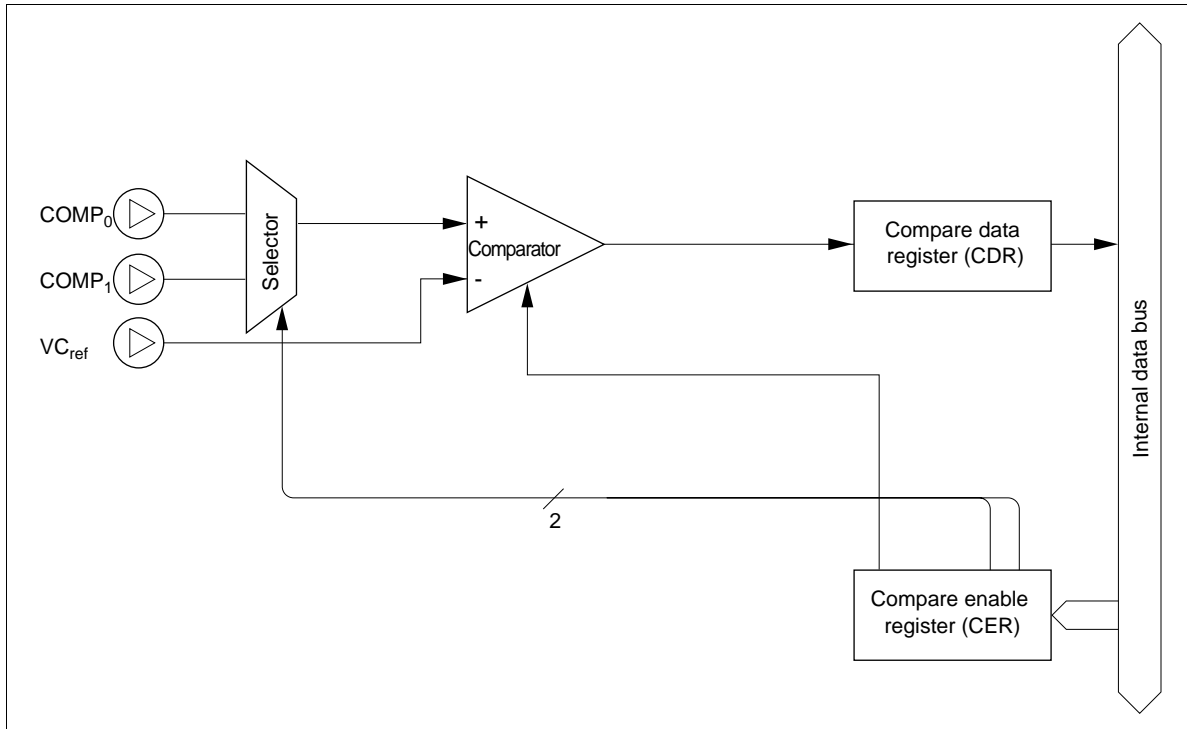


Figure 76 Comparator Block Diagram

Comparator Operation

- (1) Analog input pin selection is performed by bits 0 and 1 (CER0, CER1) of the compare enable register (CER). Setting bit 3 (CER3) to 1 places the $RD_0/COMP_0$ and $RD_1/COMP_1$ pins in analog input mode and starts comparator operation. While comparator operation is in progress, none of these pins (including pins not used for comparison) can be used as R port pins.
- (2) The compare result can be read by means of a bit test instruction (TM or TMD) on the compare data register (CDR) bit corresponding to the selected analog input pin.

Registers Used by Comparator

- Compare enable register (CER: \$018)
- Compare data register (CDR: \$017)

Compare enable register (CER: \$018): The compare enable register (CER) is a 3-bit write-only register that selects comparator operation and the analog input pin (figure 77).

CER is reset by an MCU reset or in stop mode.

| Compare enable register (CER: \$018) | | | | |
|--------------------------------------|------|----------|------|------|
| Bit | 3 | 2 | 1 | 0 |
| Initial value | 0 | — | 0 | 0 |
| Read/Write | W | — | W | W |
| Bit name | CER3 | Not Used | CER1 | CER0 |

| CER1 | CER0 | Analog input pin selection |
|------|------|----------------------------|
| 0 | 0 | COMP ₀ |
| | 1 | COMP ₁ |
| 1 | × | Not Used |

| CER3 | Comparator operation selection |
|------|--|
| 0 | Comparator operation not selected: Digital input mode RD ₀ /COMP ₀ and RD ₁ /COMP ₁ pins function as R port pins |
| 1 | Comparator operation selected: Analog input mode RD ₀ /COMP ₀ and RD ₁ /COMP ₁ pins function as comparator pins |

× : Don't care

Figure 77 Compare Enable Register (CER)

Compare data register (CDR: \$017): The compare data register (CDR) is a 2-bit read-only register that holds the result of the comparison between the analog input pin and the reference voltage (figure 78).

When comparator operation is started (CER3 is set to 1), the result of the comparison between the analog input pin selected by the compare enable register (CER) and the reference voltage is read into the corresponding bit of the compare data register (CDR). The value of the other bits in CDR is undetermined. The CDR value is not retained after the comparator operation (when CER3 = 0), and is undetermined except during comparator operation.

HD404669 Series

Compare data register (CDR: \$017)

| Bit | 3 | 2 | 1 | 0 |
|---------------|----------|----------|--------------|--------------|
| Initial value | — | — | Undetermined | Undetermined |
| Read/Write | — | — | R | R |
| Bit name | Not Used | Not Used | CDR1 | CDR0 |

CDR0 Result of comparison between COMP₀ pin and reference voltage

| | |
|---|---|
| 0 | COMP ₀ pin < reference voltage |
| 1 | COMP ₀ pin > reference voltage |

CDR1 Result of comparison between COMP₁ pin and reference voltage

| | |
|---|---|
| 0 | COMP ₁ pin < reference voltage |
| 1 | COMP ₁ pin > reference voltage |

Figure 78 Compare Data Register (CDR)

ZTAT™ Microcomputer with Built-in Programmable ROM

1. Precautions for use of ZTAT™ microcomputer with built-in programmable ROM

(1) Precautions for writing to programmable ROM built in ZTAT™ microcomputer

In the ZTAT™ microcomputer with built-in plastic mold one-time programmable ROM, incomplete electrical connection between the PROM writer and socket adapter causes writing errors and, makes the computer unoperatable. To enhance the writing efficiency, attention should be paid to the following points:

- (a) Make sure that the socket adapter is firmly fixed to the PROM writer and connected electrically with each other (neither opened nor shorted), before starting the writing process.
- (b) To secure the electrical connection between the contact pin and IC lead, make sure that there is no foreign substance on the contact pin of the socket adapter, which may cause improper electrical connection.
- (c) When inserting the IC, be careful to protect the IC lead from bending in order to secure the electrical connection between the contact pin and IC lead. If the lead is bent, correct the bending and insert it again.
- (d) If any trouble is noticed during a blank check to be performed to prevent erroneous writing due to improper electrical connection, carry out the writing process again according to above steps (a), (b), and (c).
- (e) During the writing process, do not touch the socket adapter and IC to prevent erroneous writing.
- (f) To write continuously in the IC, follow steps (a), (b), (c), (d) and (e).
- (g) If a writing error recurs, or the rate of writing errors occur frequently, stop writing and check the PROM writer, socket adapter, etc. for defects.
- (h) If any problem is noticed in the written program or in the program after being left at a high temperature, consult our technical staff.

(2) Precautions when new PROM writer, socket adapter or IC is used

When a new PROM writer, socket adapter or IC is employed, breakdown of the IC may occur or its writing may become impossible because the noise, overshoot, timing or other electrical characteristics may be inconsistent with the assured IC writing characteristics. To avoid such troubles, check the following points before starting the writing process.

- (a) To ensure stable writing operation, check that the V_{CC} of the power supplied to the PROM writer, power source current capacity of V_{PP} , and current consumption at the time of writing to IC are provided with sufficient margin.
- (b) To prevent breakdown of the IC, check that the power source voltage between GND- V_{CC} and GND- V_{PP} , and overshoot or undershoot of the power source at the connecting terminal of the socket adapter are within the ratings. Particularly, if the overshoot or undershoot exceeds the maximum rating, the pin connection may be damaged, leading to permanent breakdown. If overshoot or undershoot occurs, recheck the power source damping resistance of capacity.
- (c) To prevent breakdown of the IC and for stable writing and reading operation, insert the IC into the socket adapter and check the power noise between the GND- V_{CC} and GND- V_{PP} near the IC connecting

HD404669 Series

terminal. If power source noise is noticed, insert an appropriate capacitor between the GND power sources depending on the noise generated. In case of high frequency noise, insert a capacitor of low inductance.

- (d) For stable writing and reading operation, insert the IC into the socket adapter and check the input waveform, timing and noise near the R/W, CS, address and data terminals. Particularly, since recent ICs have increased in speed, caution should be exercised against the noise to the power source or address due to crosstalk from the output data terminal. To avoid these problems, inserting a low inductance capacitor between the GND and power source or inserting a damping resistance to the output data terminal is effective.
- (e) Particularly, when a multiple PROM writer is used, perform above items (a), (b), (c), and (d) assuming all ICs inserted into the socket adapter.
- (f) In the case of a multiple PROM writer, when an unacceptable result is noticed during a blank check performed to prevent erroneous writing due to improper electrical connection of the power source, etc., rewriting is impossible unless every writing process can be stopped. Therefore, the potential increases due to erroneous writing because of improper connection. Be sure to check the electrical connection between the PROM writer and socket adapter and IC.
- (g) If any abnormality is noticed while checking a written program, consult our technical staff.

2. Programming of Built-in programmable ROM

The MCU can stop its function as an MCU in PROM mode for programming the built-in PROM.

PROM mode is set up by setting the $\overline{\text{TEST}}$, $\overline{\text{M}}_0$, and $\overline{\text{M}}_1$ terminals to “Low” level and the RESET terminal to “High” level.

Writing and reading specifications of the PROM are the same as those for the commercial EPROM27256. Using a socket adapter for specific use of each product, programming is possible with a general-purpose PROM writer.

Since an instruction of the HMCS400 series is 10 bits long, a conversion circuit is incorporated to adapt the general-purpose PROM writer. This circuit splits each instruction into five lower bits and five higher bits to write from or read to two addresses. This enables use of a general-purpose PROM. For instance, to write to a 16kword of built-in PROM with a general-purpose PROM writer, specify 32kbyte address (\$0000-\$7FFF). An example of PROM memory map is shown in figure 80.

Notes:

1. When programming with a PROM writer, set up each ROM size to the address given in table 24. If it is programmed erroneously to an address given in Table 24 or later, check of writing of PROM may become impossible. Particularly, caution should be exercised in the case of a plastic package since reprogramming is impossible with it. Set the data in unused addresses to \$FF.
2. If the indexes of the PROM writer socket, socket adapter and product are not aligned precisely, the product may break down due to overcurrent. Be sure to check that they are properly set to the writer before starting the writing process.

3. Two levels of program voltages (V_{PP}) are available for the PROM: 12.5 V and 21 V. Our product employs a V_{PP} of 12.5 V. If a voltage of 21 V is applied, permanent breakdown of the product will result. The V_{PP} of 12.5 V is obtained for the PROM writer by setting it according to the Intel 27256 specifications.

Writing/verification

Programming of the built-in program ROM employs a high speed programming method. With this method, high speed writing is effected without voltage stress to the device or without damaging the reliability of the written data.

A basic programming flow chart is shown in figure81 and a timing chart in figure82.

For precautions for PROM writing procedure, refer to "ZTAT™ Microcomputer On-chip Programmable ROM Characteristics and Usage Notes."

Table 23 Selection of Mode

| Mode | Pins | | | |
|----------------------------|-----------------|-----------------|----------|----------------|
| | \overline{CE} | \overline{OE} | V_{PP} | O_0-O_4 |
| Writing | "Low" | "High" | V_{PP} | Data input |
| Verification | "High" | "Low" | V_{PP} | Data output |
| Prohibition of programming | "High" | "High" | V_{PP} | High impedance |

Table 24 PROM Writer Program Address

| ROM size | Address |
|----------|---------------|
| 8k | \$0000~\$3FFF |
| 12k | \$0000~\$5FFF |
| 16k | \$0000~\$7FFF |

HD404669 Series

Programmable ROM (HD407A4669)

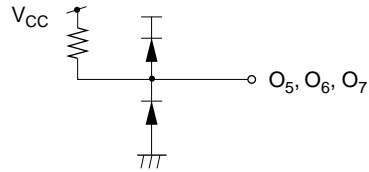
The HD407A4669 is a ZTAT™ microcomputer with built-in PROM that can be programmed in PROM mode.

PROM Mode Pin Description

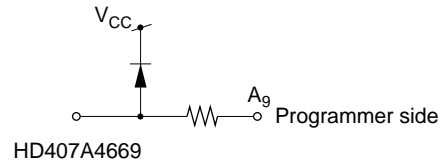
| Pin No. | MCU Mode | PROM Mode | | Pin No. | MCU Mode | PROM Mode | | | |
|---------|---|-----------|------------------------|---------|----------|-----------------------------------|-----|-----------------|-----|
| FP-64A | Pin Name | I/O | Pin Name | I/O | FP-64A | Pin Name | I/O | Pin Name | I/O |
| 1 | RE ₀ /VC _{ref} | I | | | 33 | R3 ₃ | I/O | | |
| 2 | $\overline{\text{TEST}}$ | I | GND | – | 34 | R3 ₂ /TOD | I/O | | |
| 3 | OSC ₁ | I | V _{CC} | – | 35 | R3 ₁ /TOC | I/O | | |
| 4 | OSC ₂ | O | | | 36 | R4 ₀ /EVND | I/O | | |
| 5 | RESET | I | V _{CC} | – | 37 | R4 ₁ /SCK ₁ | I/O | | |
| 6 | X1 | I | GND | – | 38 | R4 ₂ /SI ₁ | I/O | | |
| 7 | X2 | O | | | 39 | R4 ₃ /SO ₁ | I/O | | |
| 8 | GND | – | GND | – | 40 | R6 ₀ | I/O | A ₁ | I |
| 9 | D ₀ | I/O | $\overline{\text{CE}}$ | I | 41 | R6 ₁ | I/O | A ₂ | I |
| 10 | D ₁ | I/O | $\overline{\text{OE}}$ | I | 42 | R6 ₂ | I/O | A ₃ | I |
| 11 | D ₂ | I/O | V _{CC} | – | 43 | R6 ₃ | I/O | A ₄ | I |
| 12 | D ₃ | I/O | V _{CC} | – | 44 | R7 ₀ | I/O | O ₀ | I/O |
| 13 | D ₄ | I/O | | | 45 | R7 ₁ | I/O | O ₁ | I/O |
| 14 | D ₅ | I/O | | | 46 | R7 ₂ | I/O | O ₂ | I/O |
| 15 | D ₉ | I/O | | | 47 | R7 ₃ | I/O | O ₃ | I/O |
| 16 | D ₁₀ | I/O | A ₁₃ | I | 48 | R8 ₀ | I/O | O ₄ | I/O |
| 17 | D ₁₁ | I/O | A ₁₄ | I | 49 | R8 ₁ | I/O | | |
| 18 | D ₁₂ / $\overline{\text{STOPC}}$ | I | A ₉ | I | 50 | R8 ₂ | I/O | | |
| 19 | D ₁₃ / $\overline{\text{INT}}_0$ | I | V _{PP} | – | 51 | R8 ₃ | I/O | | |
| 20 | R0 ₀ / $\overline{\text{INT}}_1$ | I/O | GND | – | 52 | R9 ₀ | I/O | O ₄ | I/O |
| 21 | R0 ₁ / $\overline{\text{INT}}_2$ | I/O | GND | – | 53 | R9 ₁ | I/O | O ₃ | I/O |
| 22 | R0 ₂ / $\overline{\text{INT}}_3$ | I/O | | | 54 | R9 ₂ | I/O | O ₂ | I/O |
| 23 | R0 ₃ / $\overline{\text{INT}}_4$ | I/O | | | 55 | R9 ₃ | I/O | O ₁ | I/O |
| 24 | R1 ₀ | I/O | A ₅ | I | 56 | RA ₀ | I/O | O ₀ | I/O |
| 25 | R1 ₁ | I/O | A ₆ | I | 57 | RA ₁ | I/O | V _{CC} | – |
| 26 | R1 ₂ | I/O | A ₇ | I | 58 | SEL | I | | |
| 27 | R1 ₃ | I/O | A ₈ | I | 59 | V _{CC} | – | V _{CC} | – |
| 28 | R2 ₀ | I/O | A ₀ | I | 60 | TONEC | O | | |
| 29 | R2 ₁ | I/O | A ₁₀ | I | 61 | TONER | O | | |
| 30 | R2 ₂ | I/O | A ₁₁ | I | 62 | VT _{ref} | I | | |
| 31 | R2 ₃ | I/O | A ₁₂ | I | 63 | RD0/COMP ₀ | I | | |
| 32 | R3 ₀ | I/O | | | 64 | RD1/COMP ₁ | I | | |

HD404669 Series

- Notes:
1. I/O: I/O pin, I: Input pin, O: Output pin
 2. As there are two each of pins O_0 to O_4 , the respective pairs should be shorted.
 3. Unused data pins (O_5 to O_7) on the PROM programmer side should be handled as shown below on the socket side.



4. Pin A_9 should be handled as shown below on the socket side.



HD404669 Series

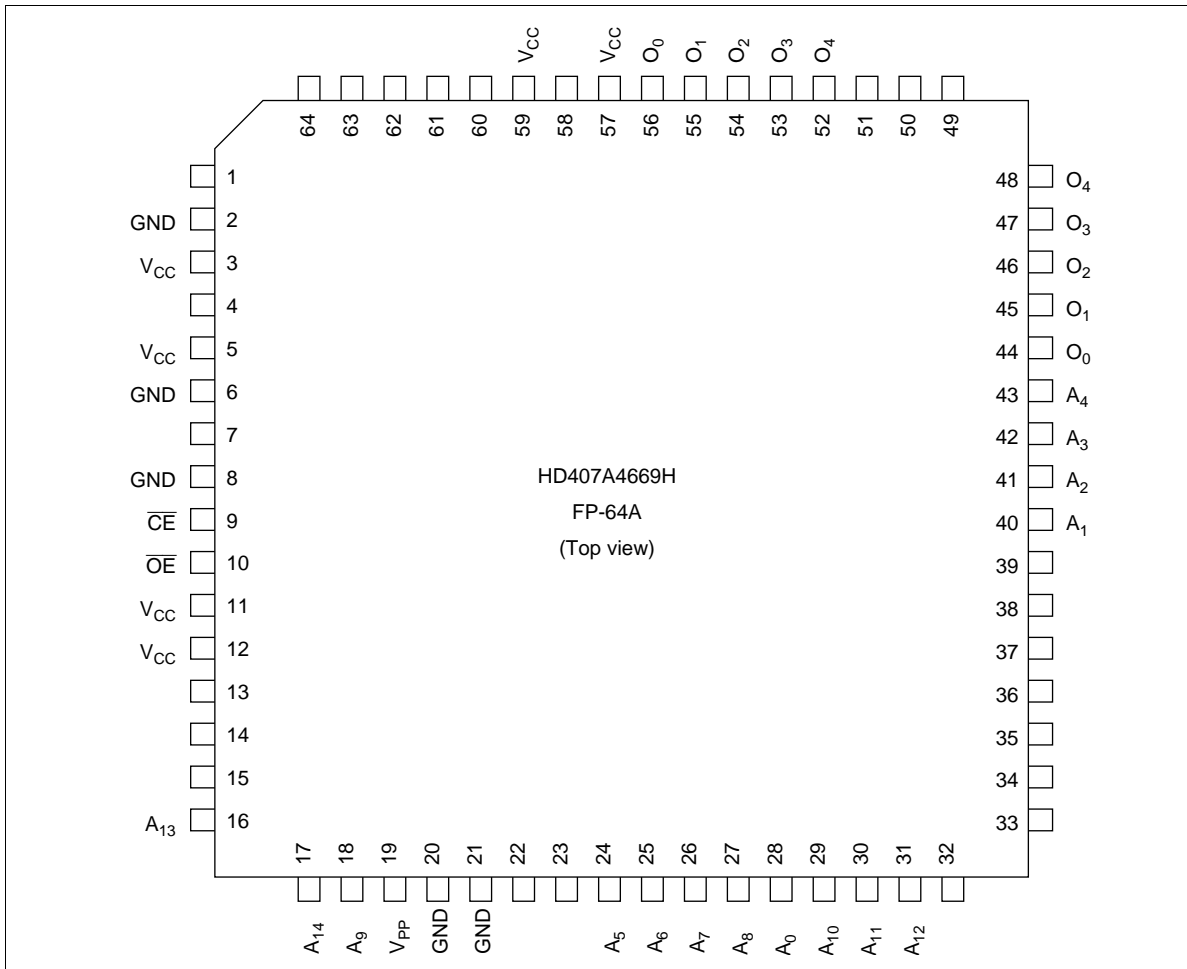


Figure 79 Pin Arrangement in PROM Mode

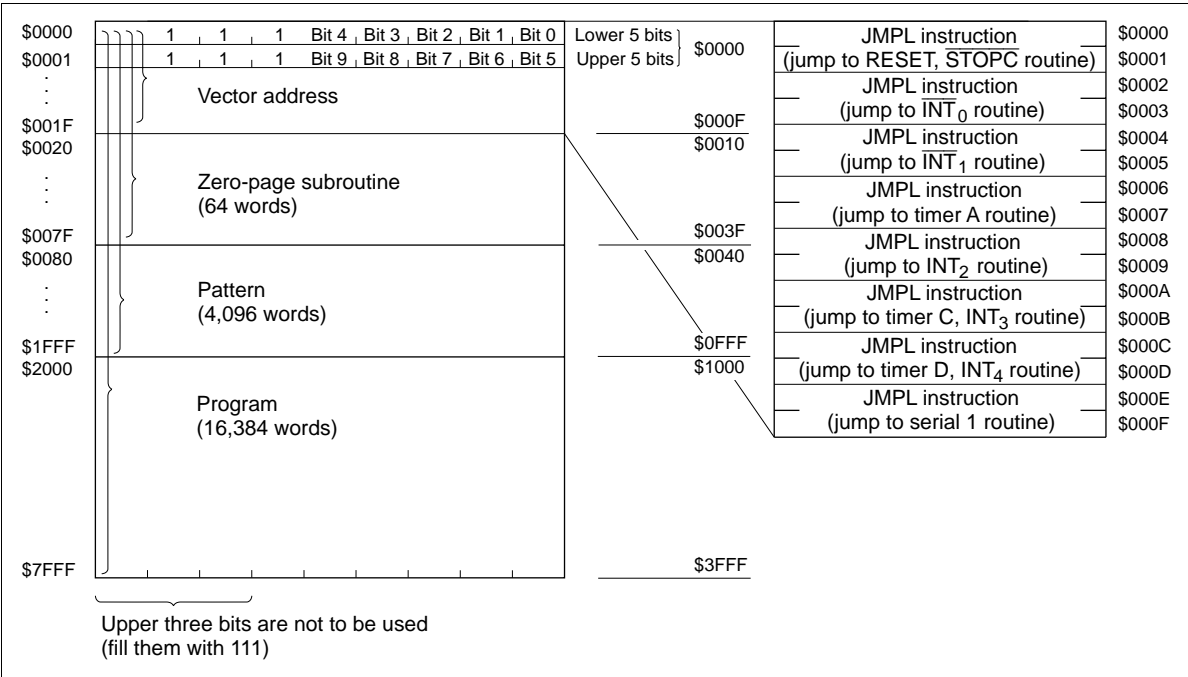


Figure 80 Memory Map in PROM Mode

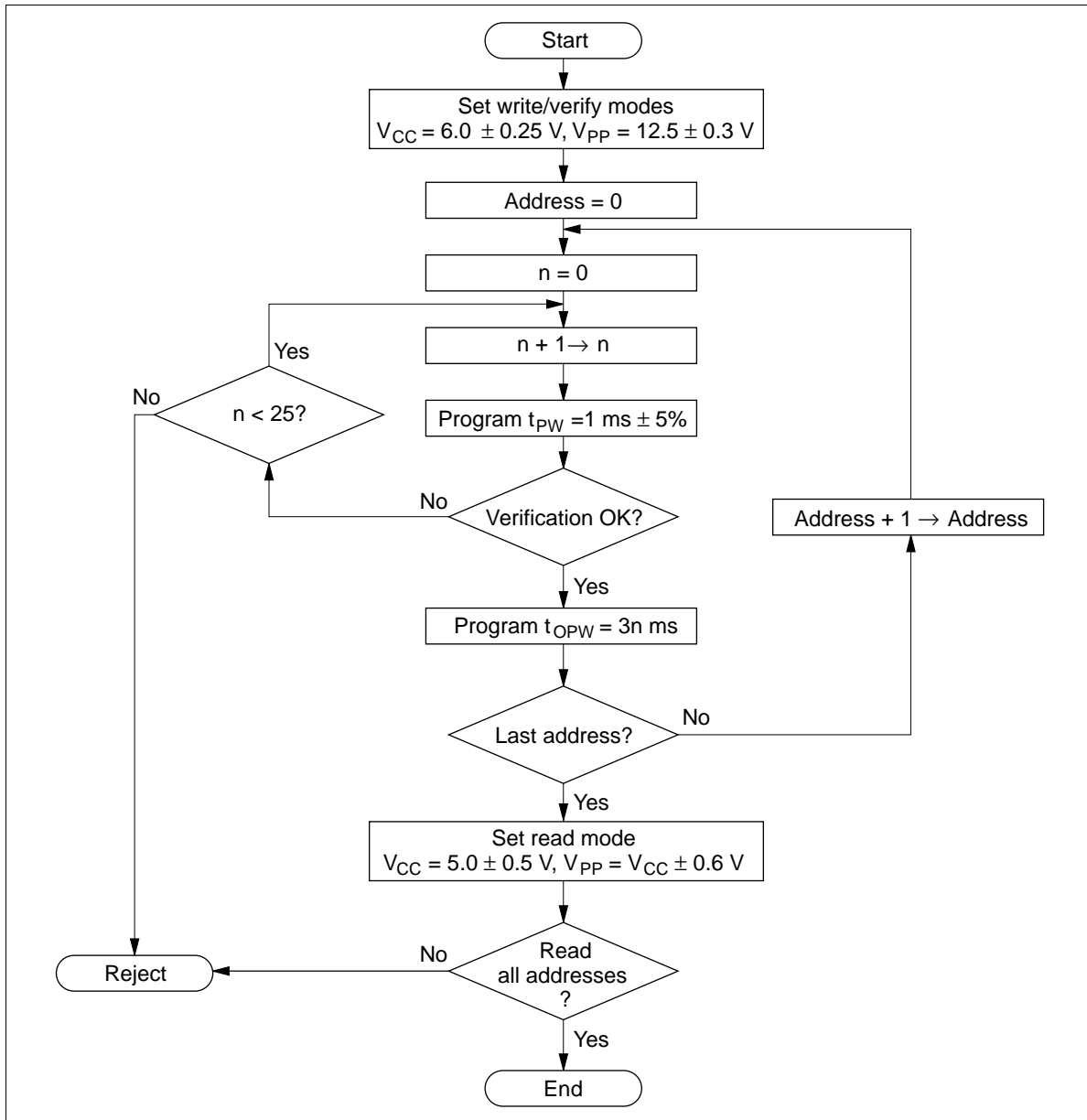


Figure 81 Flowchart of High-Speed Programming

Programming Electrical Characteristics

DC Characteristics ($V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $GND = 0\text{V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise specified)

| Item | Pin(s) | Symbol | Min | Typ | Max | Unit | Test Condition |
|---------------------------|--|------------|------|-----|----------------|---------------|---|
| Input high voltage level | $O_0-O_4, A_0-A_{14},$ $\overline{OE}, \overline{CE}$ | V_{IH} | 2.2 | — | $V_{CC} + 0.3$ | V | |
| Input low voltage level | $O_0-O_4, A_0-A_{14},$ $\overline{OE}, \overline{CE}$ | V_{IL} | -0.3 | — | 0.8 | V | |
| Output high voltage level | O_0-O_4 | V_{OH} | 2.4 | — | — | V | $I_{OH} = -200 \mu\text{A}$ |
| Output low voltage level | O_0-O_4 | V_{OL} | — | — | 0.4 | V | $I_{OL} = 1.6 \text{ mA}$ |
| Input leakage current | $O_0-O_4, A_0-A_{14},$ $\overline{OE}, \overline{CE}$ | $ I_{IL} $ | — | — | 2 | μA | $V_{in} = 5.25 \text{ V}/0.5 \text{ V}$ |
| V_{CC} current | | I_{CC} | — | — | 30 | mA | |
| V_{PP} current | | I_{PP} | — | — | 40 | mA | |

AC Characteristics ($V_{CC} = 6.0 \text{ V} \pm 0.25 \text{ V}$, $V_{PP} = 12.5 \text{ V} \pm 0.3 \text{ V}$, $GND = 0\text{V}$, $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, unless otherwise specified)

| Item | Symbol | Min | Typ | Max | Unit | Test Condition |
|--|-----------|------|-----|-------|---------------|----------------|
| Address setup time | t_{AS} | 2 | — | — | μs | See figure 82 |
| \overline{OE} setup time | t_{OES} | 2 | — | — | μs | |
| Data setup time | t_{DS} | 2 | — | — | μs | |
| Address hold time | t_{AH} | 0 | — | — | μs | |
| Data hold time | t_{DH} | 2 | — | — | μs | |
| Data output disable time | t_{DF} | — | — | 130 | ns | |
| V_{PP} setup time | t_{VPS} | 2 | — | — | μs | |
| Program pulse width | t_{PW} | 0.95 | 1.0 | 1.05 | ms | |
| \overline{CE} pulse width during overprogramming | t_{OPW} | 2.85 | — | 78.75 | ms | |
| V_{CC} setup time | t_{VCS} | 2 | — | — | μs | |
| Data output delay time | t_{OE} | 0 | — | 500 | ns | |

Note: Input pulse level: 0.8 V to 2.2 V

Input rise/fall time: $\leq 20 \text{ ns}$

Input timing reference levels: 1.0 V, 2.0 V

Output timing reference levels: 0.8 V, 2.0 V

HD404669 Series

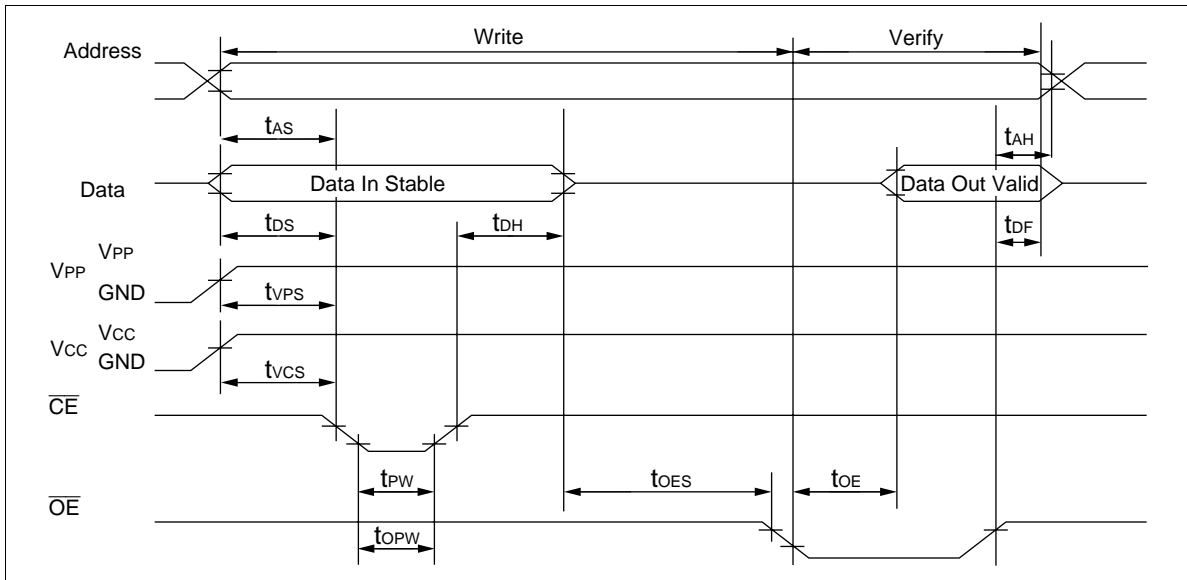


Figure 82 PROM Write/Verify Timing

ZTAT™ Microcomputer Usage Notes

ZTAT™ Microcomputer On-Chip Programmable ROM Characteristics and Usage Notes

Principles of Programming/Erase: A memory cell in a ZTAT™ microcomputer is the same as an EPROM cell; it is programmed by applying a high voltage between its control gate and drain to inject hot electrons into its floating gate. These electrons are stable, surrounded by an energy barrier formed by an SiO₂ film. The change in threshold voltage of a memory cell with a charged floating gate makes the corresponding bit appear as 0.

The charge in a memory cell may decrease with time. This decrease is usually due to one of the following causes:

- Ultraviolet light excites electrons, allowing them to escape. This effect is the basis of the erasure principle.
- Heat excites trapped electrons, allowing them to escape.
- High voltages between the control gate and drain may erase electrons.

If the oxide film covering a floating gate is defective, the electron erasure rate will be greater. However, electron erasure does not often occur because defective devices are detected and removed at the testing stage.

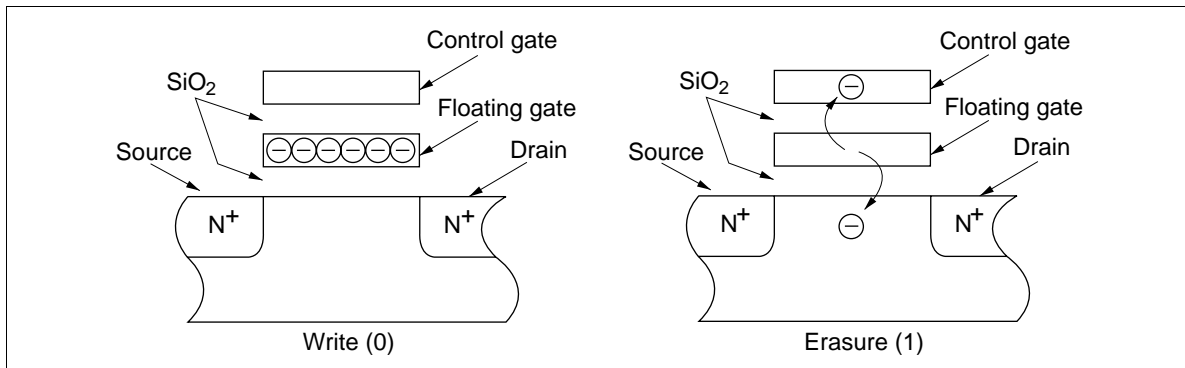


Figure 83 Cross-Sections of a PROM Cell

PROM Programming: PROM memory cells must be programmed under specific voltage and timing conditions. The higher the programming voltage V_{pp} and the longer the programming pulse t_{pw} is applied, the more electrons are injected into the floating gates. However, if V_{pp} exceeds specifications, the pn junctions may be permanently damaged. Pay particular attention to overshooting in the PROM programmer. In addition, note that negative voltage noise will produce a parasitic transistor effect that may reduce breakdown voltages.

The ZTAT™ microcomputer is electrically connected to the PROM programmer by a socket adapter. Therefore, note the following points:

HD404669 Series

- Check that the socket adapter is firmly mounted on the PROM programmer.
- Do not touch the socket adapter or the LSI during the programming. Touching them may affect the quality of the contacts, which will cause programming errors.

PROM Reliability after Programming: In general, semiconductor devices retain their reliability, provided that some initial defects can be excluded. These initial defects can be detected and rejected by screening. Baking devices under high-temperature conditions is one method of screening that can rapidly eliminate data-hold defects in memory cells. (Refer to the previous Principles of Programming/Erase section.)

ZTAT™ microcomputer devices are extremely reliable because they have been subjected to such a screening method during the wafer fabrication process, but Hitachi recommends that each device be exposed to 150°C at one atmosphere after it is programmed, to ensure its best performance. The recommended screening procedure is shown in figure 84.

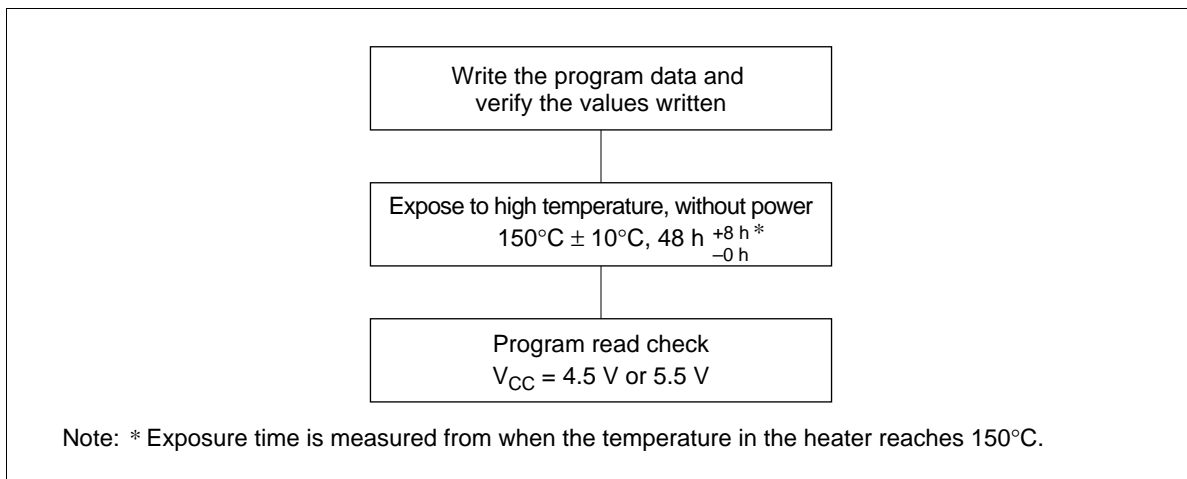


Figure 84 Recommended Screening Procedure

Note: If programming errors occur continuously during PROM programming, suspend programming and check for problems in the PROM programmer or socket adapter, using a windowed-package microcomputer with on-chip EPROM, etc. If programming verification indicates errors in programming or after high-temperature exposure, please inform Hitachi.

Write rate: A write rate of 95% or above is guaranteed.

Addressing Modes

RAM Addressing Modes

The MCU has three RAM addressing modes, as shown in figure 85 and described below.

Register Indirect Addressing Mode: The contents of the W, X, and Y registers (10 bits in total) are used as a RAM address. For \$090 to \$25F, a bank setting must be made in the bank register (V: \$03F).

Direct Addressing Mode: A direct addressing instruction consists of two words. The first word contains the opcode, and the contents of the second word (10 bits) are used as a RAM address.

Memory Register Addressing Mode: The memory registers (MR), which are located in 16 addresses from \$040 to \$04F, are accessed with the LAMR and XMRA instructions.

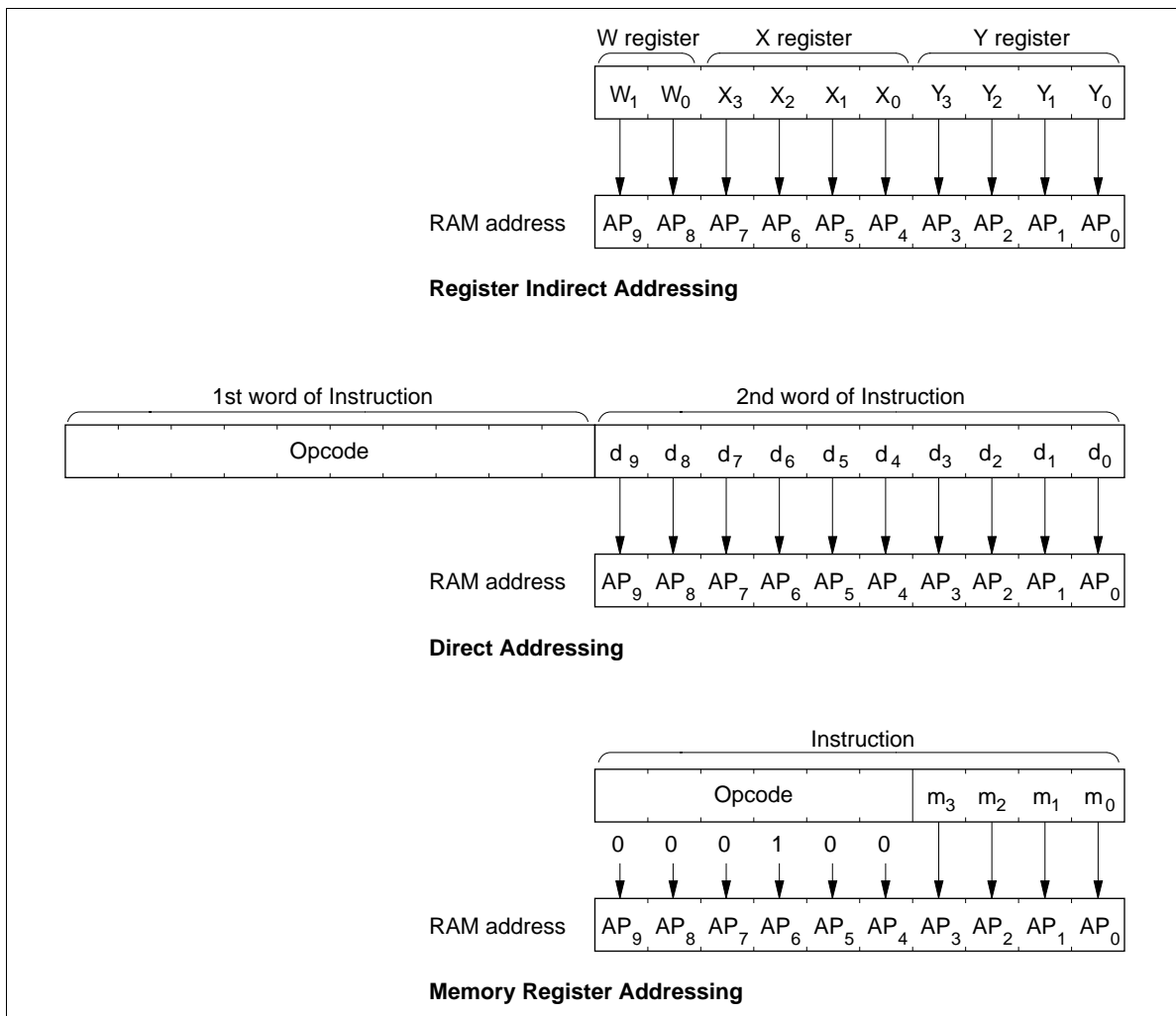


Figure 85 RAM Addressing Modes

HD404669 Series

ROM Addressing Modes and the P Instruction

The MCU has four ROM addressing modes, as shown in figure 86 and described below.

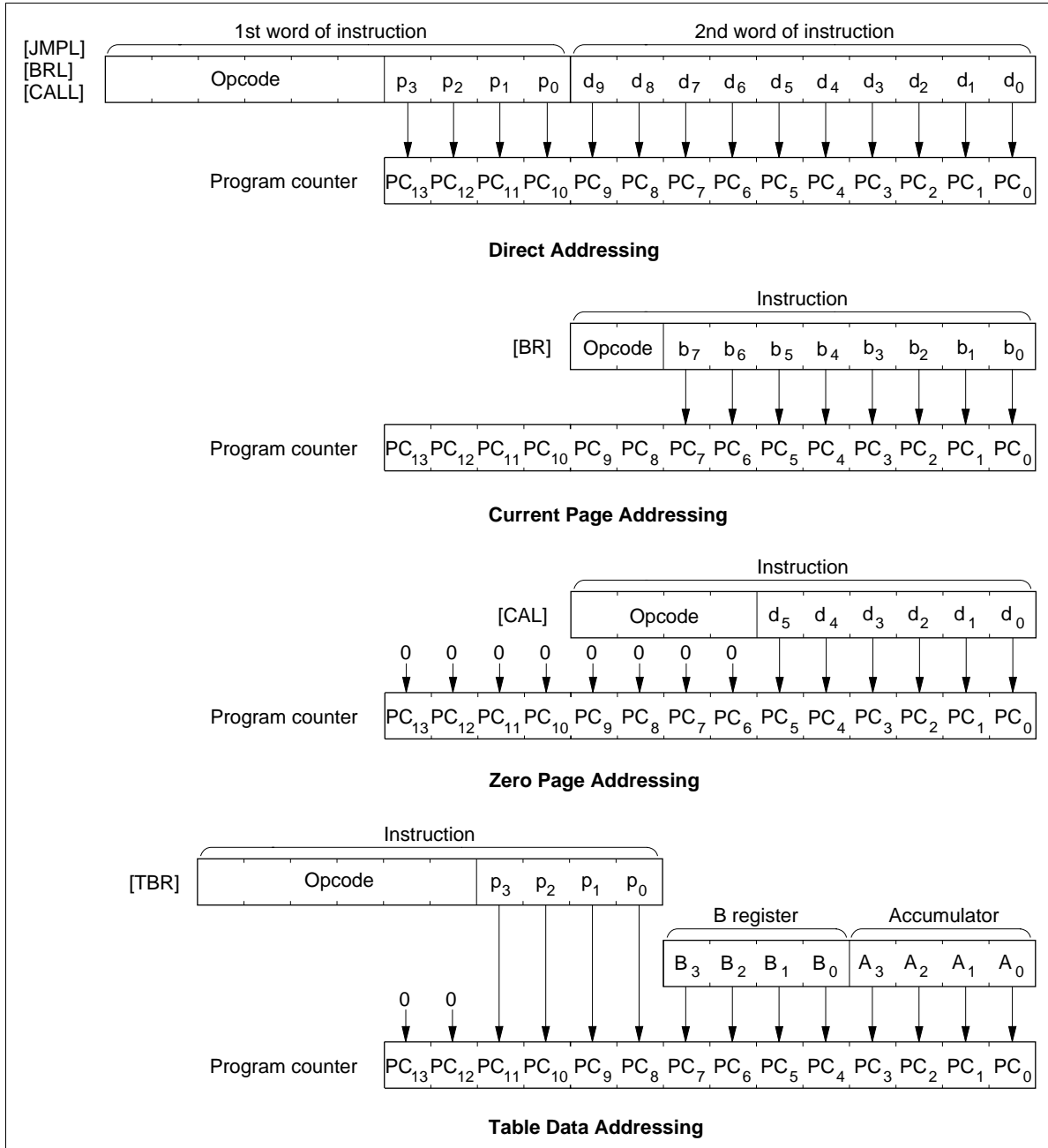


Figure 86 ROM Addressing Modes

Direct Addressing Mode: A program can branch to any address in the ROM memory space by executing the JMPL, BRL, or CALL instruction. Each of these instructions replaces the 14 program counter bits (PC_{13} – PC_0) with 14-bit immediate data.

Current Page Addressing Mode: The MCU has 64 pages of ROM with 256 words per page. A program can branch to any address in the current page by executing the BR instruction. This instruction replaces the eight low-order bits of the program counter (PC_7 – PC_0) with eight-bit immediate data. A branch by a BR instruction located at a page boundary differs from other cases: see figure 88.

Zero-Page Addressing Mode: A program can branch to the zero-page subroutine area located at \$0000–\$003F by executing the CAL instruction. When the CAL instruction is executed, 6 bits of immediate data are placed in the six low-order bits of the program counter (PC_5 – PC_0), and 0s are placed in the eight high-order bits (PC_{13} – PC_6).

Table Data Addressing Mode: A program can branch to an address determined by the contents of four-bit immediate data, the accumulator, and the B register by executing the TBR instruction.

P Instruction: ROM data addressed in table data addressing mode can be referenced with the P instruction as shown in figure 88. If bit 8 of the ROM data is 1, the lower eight bits of ROM data are written to the accumulator and the B register. If bit 9 is 1, the lower eight bits of ROM data are written to the R1 and R2 port output registers. If both bits 8 and 9 are 1, ROM data is written to the accumulator and the B register, and also to the R1 and R2 port output registers at the same time.

The P instruction has no effect on the program counter.

Branch destination of a BR instruction on a page boundary: When a BR instruction is on a page boundary ($256n + 255$), the program counter will advance to the next page because of the hardware architecture. Therefore, when using a BR instruction on a page boundary, the branch destination should be set in the next page (see figure 88).

HMCS400 Series cross assemblers are provided with an automatic paging function that automatically turns the ROM page, irrespective of the model.

HD404669 Series

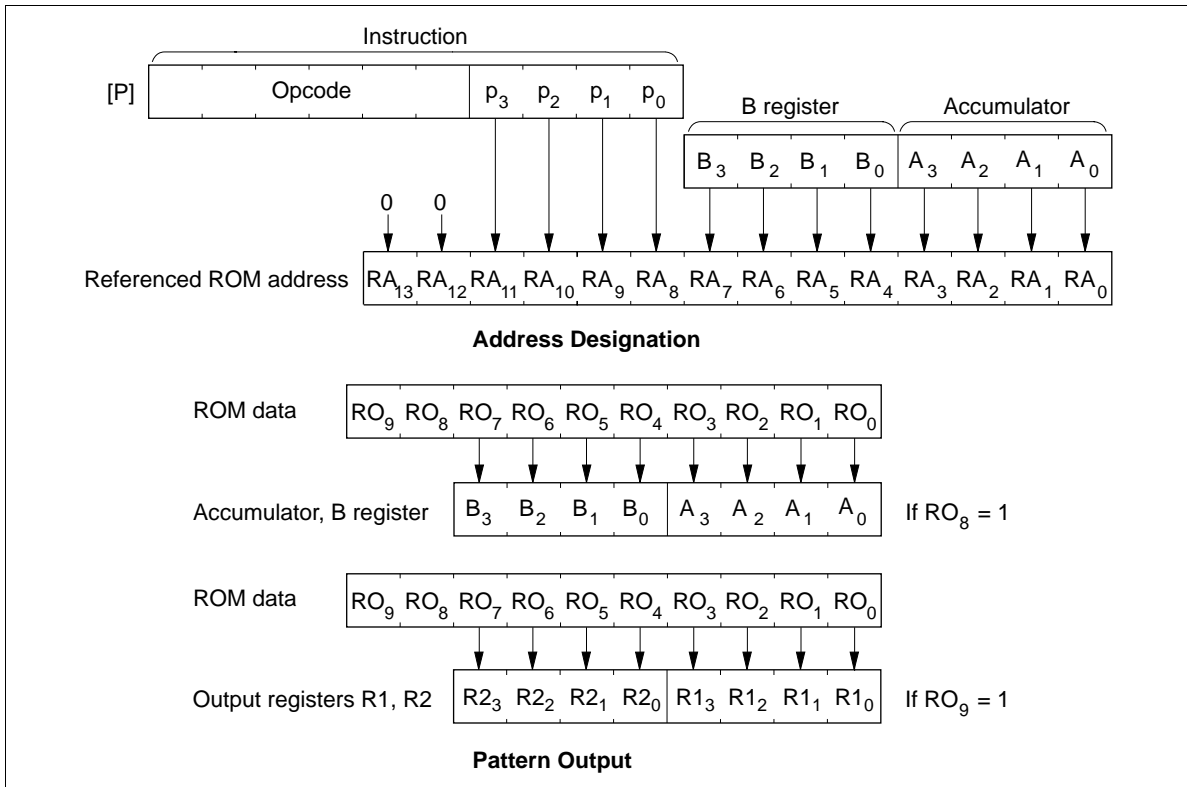


Figure 87 P Instruction

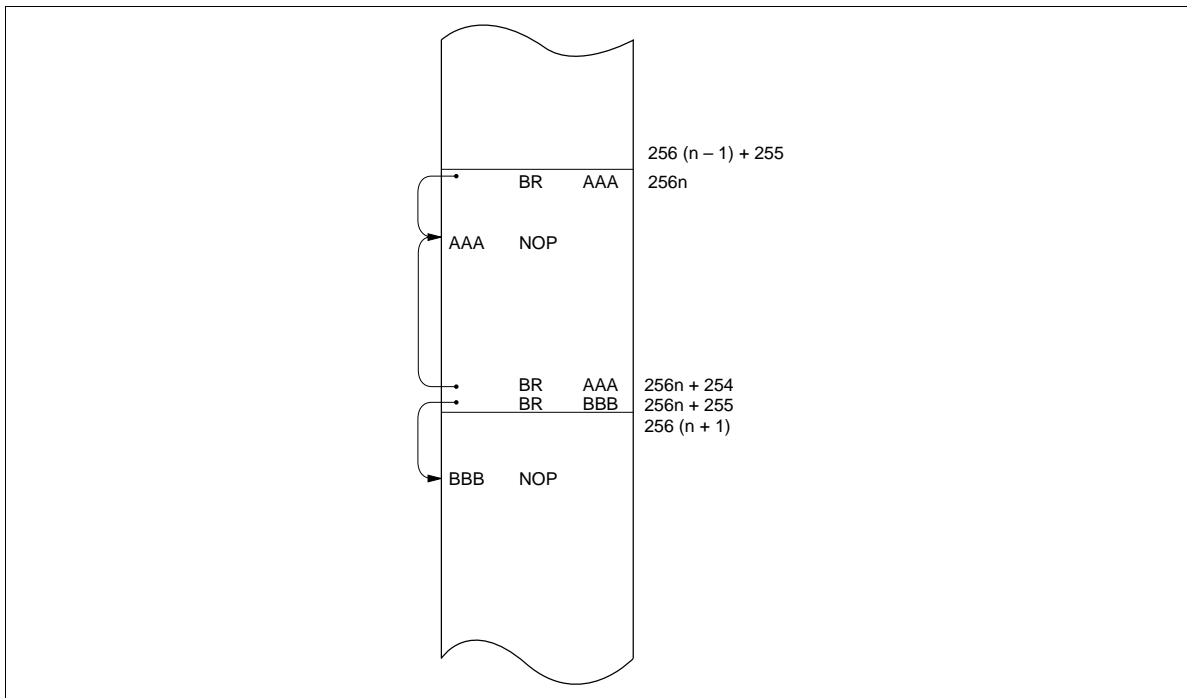


Figure 88 Branching when the Branch Destination is on a Page Boundary

Instruction Set

The MCU has 101 instructions, classified into the following 10 groups:

- Immediate instructions
- Register-to-register instructions
- RAM addressing instructions
- RAM register instructions
- Arithmetic instructions
- Compare instructions
- RAM bit manipulation instructions
- ROM addressing instructions
- Input/output instructions
- Control instructions

The functions of these instructions are listed in tables 25 to 34, and an opcode map is shown in table 35.

Table 25 Immediate Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---|----------|--|--|--------|------------------|
| Load A from immediate | LAI i | 1 0 0 0 1 1 i_3 i_2 i_1 i_0 | $i \rightarrow A$ | | 1/1 |
| Load B from immediate | LBI i | 1 0 0 0 0 0 i_3 i_2 i_1 i_0 | $i \rightarrow B$ | | 1/1 |
| Load memory from immediate | LMID i,d | 0 1 1 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $i \rightarrow M$ | | 2/2 |
| Load memory from immediate, increment Y | LMIIY i | 1 0 1 0 0 1 i_3 i_2 i_1 i_0 | $i \rightarrow M, Y + 1 \rightarrow Y$ | NZ | 1/1 |

HD404669 Series

Table 26 Register-Register Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|-------------------|----------|---|------------|--------|------------------|
| Load A from B | LAB | 0 0 0 1 0 0 1 0 0 0 | B → A | | 1/1 |
| Load B from A | LBA | 0 0 1 1 0 0 1 0 0 0 | A → B | | 1/1 |
| Load A from W | LAW | 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | W → A | | 2/2* |
| Load A from Y | LAY | 0 0 1 0 1 0 1 1 1 1 | Y → A | | 1/1 |
| Load A from SPX | LASPX | 0 0 0 1 1 0 1 0 0 0 | SPX → A | | 1/1 |
| Load A from SPY | LASPY | 0 0 0 1 0 1 1 0 0 0 | SPY → A | | 1/1 |
| Load A from MR | LAMR m | 1 0 0 1 1 1 m ₃ m ₂ m ₁ m ₀ | MR (m) → A | | 1/1 |
| Exchange MR and A | XMRA m | 1 0 1 1 1 1 m ₃ m ₂ m ₁ m ₀ | MR (m) ↔ A | | 1/1 |

Note: * The assembler automatically provides an operand for the second word of the LAW instruction.

Table 27 RAM Address Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|----------------------------------|----------|---|------------------|--------|------------------|
| Load W from immediate | LWI i | 0 0 1 1 1 1 0 0 i ₁ i ₀ | i → W | | 1/1 |
| Load X from immediate | LXI i | 1 0 0 0 1 0 i ₃ i ₂ i ₁ i ₀ | i → X | | 1/1 |
| Load Y from immediate | LYI i | 1 0 0 0 0 1 i ₃ i ₂ i ₁ i ₀ | i → Y | | 1/1 |
| Load W from A | LWA | 0 1 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 | A → W | | 2/2* |
| Load X from A | LXA | 0 0 1 1 1 0 1 0 0 0 | A → X | | 1/1 |
| Load Y from A | LYA | 0 0 1 1 0 1 1 0 0 0 | A → Y | | 1/1 |
| Increment Y | IY | 0 0 0 1 0 1 1 1 0 0 | Y + 1 → Y | NZ | 1/1 |
| Decrement Y | DY | 0 0 1 1 0 1 1 1 1 1 | Y - 1 → Y | NB | 1/1 |
| Add A to Y | AYY | 0 0 0 1 0 1 0 1 0 0 | Y + A → Y | OVF | 1/1 |
| Subtract A from Y | SY Y | 0 0 1 1 0 1 0 1 0 0 | Y - A → Y | NB | 1/1 |
| Exchange X and SPX | XSPX | 0 0 0 0 0 0 0 0 0 1 | X ↔ SPX | | 1/1 |
| Exchange Y and SPY | XSPY | 0 0 0 0 0 0 0 0 1 0 | Y ↔ SPY | | 1/1 |
| Exchange X and SPX, Y and SPY | XSPXY | 0 0 0 0 0 0 0 0 1 1 | X ↔ SPX, Y ↔ SPY | | 1/1 |

Note: * The assembler automatically provides an operand for the second word of the LWA instruction.

Table 28 RAM Register Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|------------------------------------|----------|--|-------------------------------|--------|------------------|
| Load A from memory | LAM(XY) | 0 0 1 0 0 1 0 0 y x | M → A (X ↔ SPX, Y ↔ SPY) | | 1/1 |
| Load A from memory | LAMD d | 0 1 1 0 0 1 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀ | M → A | | 2/2 |
| Load B from memory | LBM(XY) | 0 0 0 1 0 0 0 0 y x | M → B (X ↔ SPX, Y ↔ SPY) | | 1/1 |
| Load memory from A | LMA(XY) | 0 0 1 0 0 1 0 1 y x | A → M (X ↔ SPX, Y ↔ SPY) | | 1/1 |
| Load memory from A | LMAD d | 0 1 1 0 0 1 0 1 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀ | A → M | | 2/2 |
| Load memory from A, increment Y | LMAIY(X) | 0 0 0 1 0 1 0 0 0 x | A → M, Y + 1 → Y (X ↔ SPX) | NZ | 1/1 |
| Load memory from A, decrement Y | LMADY(X) | 0 0 1 1 0 1 0 0 0 x | A → M, Y - 1 → Y (X ↔ SPX) | NB | 1/1 |
| Exchange memory and A | XMA(XY) | 0 0 1 0 0 0 0 0 y x | M ↔ A (X ↔ SPX, Y ↔ SPY) | | 1/1 |
| Exchange memory and A | XMAD d | 0 1 1 0 0 0 0 0 0 0 d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀ | M ↔ A | | 2/2 |
| Exchange memory and B | XMB(XY) | 0 0 1 1 0 0 0 0 y x | M ↔ B (X ↔ SPX, Y ↔ SPY) | | 1/1 |

Note: The meanings of (XY) and (X) are as follows:

Each instruction marked with (XY) has 4 mnemonics, each with different object codes. For example, different values of x and y of the opcode of the LAM(XY) instruction are given below.

| Mnemonic | y | x | Function |
|----------|---|---|------------------|
| LAM | 0 | 0 | None |
| LAMX | 0 | 1 | X ↔ SPX |
| LAMY | 1 | 0 | Y ↔ SPY |
| LAMXY | 1 | 1 | X ↔ SPX, Y ↔ SPY |

Each instruction marked with (X) has 2 mnemonics, each with different object codes. For example, different values of x of the opcode of the LMAIY(X) instruction are given below.

| Mnemonic | x | Function |
|----------|---|----------|
| LMAIY | 0 | None |
| LMAIYX | 1 | X ↔ SPX |

HD404669 Series

Table 29 Arithmetic Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|-----------------------------------|----------|--|---|--------|------------------|
| Add immediate to A | AI i | 1 0 1 0 0 0 i_3 i_2 i_1 i_0 | $A + i \rightarrow A$ | OVF | 1/1 |
| Increment B | IB | 0 0 0 1 0 0 1 1 0 0 | $B + 1 \rightarrow B$ | NZ | 1/1 |
| Decrement B | DB | 0 0 1 1 0 0 1 1 1 1 | $B - 1 \rightarrow B$ | NB | 1/1 |
| Decimal adjust for addition | DAA | 0 0 1 0 1 0 0 1 1 0 | | | 1/1 |
| Decimal adjust for subtraction | DAS | 0 0 1 0 1 0 1 0 1 0 | | | 1/1 |
| Negate A | NEGA | 0 0 0 1 1 0 0 0 0 0 | $\bar{A} + 1 \rightarrow A$ | | 1/1 |
| Complement B | COMB | 0 1 0 1 0 0 0 0 0 0 | $\bar{B} \rightarrow B$ | | 1/1 |
| Rotate right A with carry | ROTR | 0 0 1 0 1 0 0 0 0 0 | | | 1/1 |
| Rotate left A with carry | ROTL | 0 0 1 0 1 0 0 0 0 1 | | | 1/1 |
| Set carry | SEC | 0 0 1 1 1 0 1 1 1 1 | $1 \rightarrow CA$ | | 1/1 |
| Reset carry | REC | 0 0 1 1 1 0 1 1 0 0 | $0 \rightarrow CA$ | | 1/1 |
| Test carry | TC | 0 0 0 1 1 0 1 1 1 1 | | CA | 1/1 |
| Add A to memory | AM | 0 0 0 0 0 0 1 0 0 0 | $M + A \rightarrow A$ | OVF | 1/1 |
| Add A to memory | AMD d | 0 1 0 0 0 0 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $M + A \rightarrow A$ | OVF | 2/2 |
| Add A to memory with carry | AMC | 0 0 0 0 0 0 1 1 0 0 | $M + A + CA \rightarrow A$ $OVF \rightarrow CA$ | OVF | 1/1 |
| Add A to memory with carry | AMCD d | 0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $M + A + CA \rightarrow A$ $OVF \rightarrow CA$ | OVF | 2/2 |
| Subtract A from memory with carry | SMC | 0 0 1 0 0 1 1 0 0 0 | $M - A - \bar{CA} \rightarrow A$ $NB \rightarrow CA$ | NB | 1/1 |
| Subtract A from memory with carry | SMCD d | 0 1 1 0 0 1 1 0 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $M - A - \bar{CA} \rightarrow A$ $NB \rightarrow CA$ | NB | 2/2 |
| OR A and B | OR | 0 1 0 1 0 0 0 1 0 0 | $A \cup B \rightarrow A$ | | 1/1 |
| AND memory with A | ANM | 0 0 1 0 0 1 1 1 0 0 | $A \cap M \rightarrow A$ | NZ | 1/1 |
| AND memory with A | ANMD d | 0 1 1 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $A \cap M \rightarrow A$ | NZ | 2/2 |
| OR memory with A | ORM | 0 0 0 0 0 0 1 1 0 0 | $A \cup M \rightarrow A$ | NZ | 1/1 |
| OR memory with A | ORMD d | 0 1 0 0 0 0 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $A \cup M \rightarrow A$ | NZ | 2/2 |
| EOR memory with A | EORM | 0 0 0 0 0 1 1 1 0 0 | $A \oplus M \rightarrow A$ | NZ | 1/1 |
| EOR memory with A | EORMD d | 0 1 0 0 0 1 1 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $A \oplus M \rightarrow A$ | NZ | 2/2 |

Table 30 Compare Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|--|-----------|--|------------|--------|------------------|
| Immediate not equal to memory | INEM i | 0 0 0 0 1 0 i_3 i_2 i_1 i_0 | $i \neq M$ | NZ | 1/1 |
| Immediate not equal to memory | INEMD i,d | 0 1 0 0 1 0 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $i \neq M$ | NZ | 2/2 |
| A not equal to memory | ANEM | 0 0 0 0 0 0 0 1 0 0 | $A \neq M$ | NZ | 1/1 |
| A not equal to memory | ANEMD d | 0 1 0 0 0 0 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $A \neq M$ | NZ | 2/2 |
| B not equal to memory | BNEM | 0 0 0 1 0 0 0 1 0 0 | $B \neq M$ | NZ | 1/1 |
| Y not equal to immediate | YNEI i | 0 0 0 1 1 1 i_3 i_2 i_1 i_0 | $Y \neq i$ | NZ | 1/1 |
| Immediate less than or equal to memory | ILEM i | 0 0 0 0 1 1 i_3 i_2 i_1 i_0 | $i \leq M$ | NB | 1/1 |
| Immediate less than or equal to memory | ILEMD i,d | 0 1 0 0 1 1 i_3 i_2 i_1 i_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $i \leq M$ | NB | 2/2 |
| A less than or equal to memory | ALEM | 0 0 0 0 0 1 0 1 0 0 | $A \leq M$ | NB | 1/1 |
| A less than or equal to memory | ALEMD d | 0 1 0 0 0 1 0 1 0 0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $A \leq M$ | NB | 2/2 |
| B less than or equal to memory | BLEM | 0 0 1 1 0 0 0 1 0 0 | $B \leq M$ | NB | 1/1 |
| A less than or equal to immediate | ALEI i | 1 0 1 0 1 1 i_3 i_2 i_1 i_0 | $A \leq i$ | NB | 1/1 |

Table 31 RAM Bit Manipulation Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|------------------|----------|--|----------------------|--------|------------------|
| Set memory bit | SEM n | 0 0 1 0 0 0 0 1 n_1 n_0 | $1 \rightarrow M(n)$ | | 1/1 |
| Set memory bit | SEMD n,d | 0 1 1 0 0 0 0 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $1 \rightarrow M(n)$ | | 2/2 |
| Reset memory bit | REM n | 0 0 1 0 0 0 1 0 n_1 n_0 | $0 \rightarrow M(n)$ | | 1/1 |
| Reset memory bit | REMD n,d | 0 1 1 0 0 0 1 0 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | $0 \rightarrow M(n)$ | | 2/2 |
| Test memory bit | TM n | 0 0 1 0 0 0 1 1 n_1 n_0 | | M (n) | 1/1 |
| Test memory bit | TM n,d | 0 1 1 0 0 0 1 1 n_1 n_0 d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0 | | M (n) | 2/2 |

HD404669 Series

Table 32 ROM Address Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|----------------------------------|----------|--|---------------------------|--------|------------------|
| Branch on status 1 | BR b | 1 1 b ₇ b ₆ b ₅ b ₄ b ₃ b ₂ b ₁ b ₀ | | 1 | 1/1 |
| Long branch on status 1 | BRL u | 0 1 0 1 1 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀ | | 1 | 2/2 |
| Long jump unconditionally | JMPL u | 0 1 0 1 0 1 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀ | | | 2/2 |
| Subroutine jump on status 1 | CAL a | 0 1 1 1 a ₅ a ₄ a ₃ a ₂ a ₁ a ₀ | | 1 | 1/2 |
| Long subroutine jump on status 1 | CALL u | 0 1 0 1 1 0 p ₃ p ₂ p ₁ p ₀ d ₉ d ₈ d ₇ d ₆ d ₅ d ₄ d ₃ d ₂ d ₁ d ₀ | | 1 | 2/2 |
| Table branch | TBR p | 0 0 1 0 1 1 p ₃ p ₂ p ₁ p ₀ | | 1 | 1/1 |
| Return from subroutine | RTN | 0 0 0 0 0 1 0 0 0 0 | | | 1/3 |
| Return from interrupt | RTNI | 0 0 0 0 0 1 0 0 0 1 | 1 → IE, carry restored | ST | 1/3 |

Table 33 Input/Output Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|---------------------------------|----------|---|-----------|--------|------------------|
| Set discrete I/O latch | SED | 0 0 1 1 1 0 0 1 0 0 | 1 → D (Y) | | 1/1 |
| Set discrete I/O latch direct | SEDD m | 1 0 1 1 1 0 m ₃ m ₂ m ₁ m ₀ | 1 → D (m) | | 1/1 |
| Reset discrete I/O latch | RED | 0 0 0 1 1 0 0 1 0 0 | 0 → D (Y) | | 1/1 |
| Reset discrete I/O latch direct | REDD m | 1 0 0 1 1 0 m ₃ m ₂ m ₁ m ₀ | 0 → D (m) | | 1/1 |
| Test discrete I/O latch | TD | 0 0 1 1 1 0 0 0 0 0 | | D (Y) | 1/1 |
| Test discrete I/O latch direct | TDD m | 1 0 1 0 1 0 m ₃ m ₂ m ₁ m ₀ | | D (m) | 1/1 |
| Load A from R-port register | LAR m | 1 0 0 1 0 1 m ₃ m ₂ m ₁ m ₀ | R (m) → A | | 1/1 |
| Load B from R-port register | LBR m | 1 0 0 1 0 0 m ₃ m ₂ m ₁ m ₀ | R (m) → B | | 1/1 |
| Load R-port register from A | LRA m | 1 0 1 1 0 1 m ₃ m ₂ m ₁ m ₀ | A → R (m) | | 1/1 |
| Load R-port register from B | LRB m | 1 0 1 1 0 0 m ₃ m ₂ m ₁ m ₀ | B → R (m) | | 1/1 |
| Pattern generation | P p | 0 1 1 0 1 1 p ₃ p ₂ p ₁ p ₀ | | | 1/2 |

Table 34 Control Instructions

| Operation | Mnemonic | Operation Code | Function | Status | Words/ Cycles |
|--------------------------|-----------------|-----------------------|-----------------|---------------|--------------------------|
| No operation | NOP | 0 0 0 0 0 0 0 0 0 0 | | | 1/1 |
| Start serial | STS | 0 1 0 1 0 0 1 0 0 0 | | | 1/1 |
| Standby mode/watch mode* | SBY | 0 1 0 1 0 0 1 1 0 0 | | | 1/1 |
| Stop mode/watch mode | STOP | 0 1 0 1 0 0 1 1 0 1 | | | 1/1 |

Note: * Only after a transition from subactive mode.

HD404669 Series

Table 35 Opcode Map

| R9 H | | R8 L | | | | | | | | | | | | | | | | | | |
|---------|---|------------|------|------|-------|------|----------|---|-----|-------|-----|----------|---|------|-----|---|---------|-----|--|--|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | | | |
| 0 | 0 | NOP | XSPX | XSPY | XSPXY | ANEM | | | | AM | | | | ORM | | | | | | |
| | 1 | RTN | RTNI | | | ALEM | | | | AMC | | | | EORM | | | | | | |
| | 2 | INEM i(4) | | | | | | | | | | | | | | | | | | |
| | 3 | ILEM i(4) | | | | | | | | | | | | | | | | | | |
| | 4 | LBM(XY) | | | | BNEM | | | | LAB | | | | IB | | | | | | |
| | 5 | LMAIY(X) | | | | | AYY | | | LASPY | | | | IY | | | | | | |
| | 6 | NEGA | | | | RED | | | | LASPX | | | | | | | | TC | | |
| | 7 | YNEI i(4) | | | | | | | | | | | | | | | | | | |
| | 8 | XMA(XY) | | | | | SEM n(2) | | | | | REM n(2) | | | | | TM n(2) | | | |
| | 9 | LAM(XY) | | | | | LMA(XY) | | | | SMC | | | | ANM | | | | | |
| | A | ROTR | ROTL | | | | | | DAA | | | | | DAS | | | | LAY | | |
| | B | TBR p(4) | | | | | | | | | | | | | | | | | | |
| | C | XMB(XY) | | | | BLEM | | | | LBA | | | | | | | | DB | | |
| | D | LMADY(X) | | | | | SYI | | | LYA | | | | | | | | DY | | |
| | E | TD | | | | SED | | | | LXA | | | | REC | | | | SEC | | |
| | F | LWI i(2) | | | | | | | | | | | | | | | | | | |
| 1 | 0 | LBI i(4) | | | | | | | | | | | | | | | | | | |
| | 1 | LYI i(4) | | | | | | | | | | | | | | | | | | |
| | 2 | LXI i(4) | | | | | | | | | | | | | | | | | | |
| | 3 | LAI i(4) | | | | | | | | | | | | | | | | | | |
| | 4 | LBR m(4) | | | | | | | | | | | | | | | | | | |
| | 5 | LAR m(4) | | | | | | | | | | | | | | | | | | |
| | 6 | REDD m(4) | | | | | | | | | | | | | | | | | | |
| | 7 | LAMR m(4) | | | | | | | | | | | | | | | | | | |
| | 8 | AI i(4) | | | | | | | | | | | | | | | | | | |
| | 9 | LMIIY i(4) | | | | | | | | | | | | | | | | | | |
| | A | TDD m(4) | | | | | | | | | | | | | | | | | | |
| | B | ALEI i(4) | | | | | | | | | | | | | | | | | | |
| | C | LRB m(4) | | | | | | | | | | | | | | | | | | |
| | D | LRA m(4) | | | | | | | | | | | | | | | | | | |
| | E | SEDD m(4) | | | | | | | | | | | | | | | | | | |
| | F | XMRA m(4) | | | | | | | | | | | | | | | | | | |

1-word/2-cycle instruction
 1-word/3-cycle instruction
 RAM direct address instruction (2-word/2-cycle)
 2-word/2-cycle instruction

| R8 | | 1 | | | | | | | | | | | | | | | | |
|----|---|---|------------|---|---|-----------|---|---|------|-----------|---|---|-------|----------|---|---|---|--|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | A | B | C | D | E | F | |
| 0 | H | 0 | LAW | | | ANEMD | | | AMD | | | | ORMD | | | | | |
| | | 1 | LWA | | | ALEMd | | | AMCD | | | | EORMD | | | | | |
| | | 2 | INEMD i(4) | | | | | | | | | | | | | | | |
| | | 3 | ILEMD i(4) | | | | | | | | | | | | | | | |
| | | 4 | COMB | | | OR | | | STS | | | | SBY | STOP | | | | |
| | | 5 | JMPL p(4) | | | | | | | | | | | | | | | |
| | | 6 | CALL p(4) | | | | | | | | | | | | | | | |
| | | 7 | BRL p(4) | | | | | | | | | | | | | | | |
| | | 8 | XMAD | | | SEMD n(2) | | | | REMD n(2) | | | | TMD n(2) | | | | |
| | | 9 | LAMD | | | LMAD | | | SMCD | | | | ANMD | | | | | |
| | | A | LMID i(4) | | | | | | | | | | | | | | | |
| | | B | P p(4) | | | | | | | | | | | | | | | |
| | | C | | | | | | | | | | | | | | | | |
| | | D | | | | | | | | | | | | | | | | |
| | | E | CAL a(6) | | | | | | | | | | | | | | | |
| | | F | | | | | | | | | | | | | | | | |
| 1 | H | 0 | | | | | | | | | | | | | | | | |
| | | 1 | | | | | | | | | | | | | | | | |
| | | 2 | | | | | | | | | | | | | | | | |
| | | 3 | | | | | | | | | | | | | | | | |
| | | 4 | | | | | | | | | | | | | | | | |
| | | 5 | | | | | | | | | | | | | | | | |
| | | 6 | | | | | | | | | | | | | | | | |
| | | 7 | | | | | | | | | | | | | | | | |
| | | 8 | BR b(8) | | | | | | | | | | | | | | | |
| | | 9 | | | | | | | | | | | | | | | | |
| | | A | | | | | | | | | | | | | | | | |
| | | B | | | | | | | | | | | | | | | | |
| | | C | | | | | | | | | | | | | | | | |
| | | D | | | | | | | | | | | | | | | | |
| | | E | | | | | | | | | | | | | | | | |
| | | F | | | | | | | | | | | | | | | | |

1-word/2-cycle instruction
 1-word/3-cycle instruction
 RAM direct address instruction (2-word/2-cycle)
 2-word/2-cycle instruction

HD404669 Series

Absolute Maximum Ratings

| Item | Symbol | Value | Unit | Notes |
|--|---------------|----------------------------|------|-------|
| Supply voltage | V_{CC} | -0.3 to +7.0 | V | |
| Programming voltage | V_{PP} | -0.3 to +14.0 | V | 1 |
| Pin voltage | V_T | -0.3 to ($V_{CC} + 0.3$) | V | |
| Total permissible input current (to chip) | ΣI_o | 100 | mA | 2 |
| Total permissible output current (from chip) | $-\Sigma I_o$ | 50 | mA | 3 |
| Maximum input current (to chip) | I_o | 4 | mA | 4, 5 |
| | | 30 | mA | 4, 6 |
| Maximum output current (from chip) | $-I_o$ | 4 | mA | 7, 8 |
| | | 20 | mA | 7, 9 |
| Operating temperature | T_{opr} | -20 to +75 | °C | 10 |
| Storage temperature | T_{stg} | -55 to +125 | °C | 11 |

- Notes: 1. Applies to D_{13} (V_{PP}) of the HD407A4669.
 2. The total permissible input current is the total of input currents simultaneously flowing in from all the I/O pins to ground.
 3. The total permissible output current is the total of output currents simultaneously flowing out from V_{CC} to all I/O pins.
 4. The maximum input current is the maximum current flowing from each I/O pin to ground.
 5. Applies to D_0 - D_3 , R_0 - R_4 and R_6 - RA .
 6. Applies to D_4 , D_5 and D_9 - D_{11}
 7. The maximum output current is the maximum current flowing out from V_{CC} to each I/O pin.
 8. Applies to D_4 , D_5 , D_9 - D_{11} , R_0 - R_4 and R_6 - RA .
 9. Applies to D_0 - D_3 .
 10. The operating temperature indicates the temperature range in which power can be supplied to the LSI (voltage V_{CC} shown in the electrical characteristics tables can be applied).
 11. In the case of chips, the storage specification differs from that of the package products. Please consult your Hitachi sales representative for details.

Permanent damage may occur if these absolute maximum ratings are exceeded. Normal operation must be under the conditions stated in the electrical characteristics tables. If these conditions are exceeded, the LSI may malfunction or its reliability may be affected.

Electrical Characteristics

DC Characteristics (HD404668, HD4046612, HD404669, HD40A4668, HD40A46612, HD40A4669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$; HCD404669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = +75^\circ\text{C}$; HD407A4669: $V_{CC} = 2.2$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Condition | Notes |
|--|------------|---|----------------|-----|----------------|---------------|--|-------|
| Input high voltage | V_{IH} | RESET, \overline{SCK}_1 , SI ₁ , \overline{INT}_0 , \overline{INT}_1 , INT ₂ , INT ₃ , INT ₄ , \overline{STOPC} , EVND | $0.9V_{CC}$ | — | $V_{CC} + 0.3$ | V | — | |
| | | OSC ₁ | $V_{CC} - 0.3$ | — | $V_{CC} + 0.3$ | V | External clock operation | |
| Input low voltage | V_{IL} | RESET, \overline{SCK}_1 , SI ₁ , \overline{INT}_0 , \overline{INT}_1 , INT ₂ , INT ₃ , INT ₄ , \overline{STOPC} , EVND | -0.3 | — | $0.10V_{CC}$ | V | — | |
| | | OSC ₁ | -0.3 | — | 0.3 | V | External clock operation | |
| Output high voltage | V_{OH} | \overline{SCK}_1 , SO ₁ , TOC, TOD | $V_{CC} - 0.5$ | — | — | V | $-I_{OH} = 0.3$ mA | |
| Output low voltage | V_{OL} | \overline{SCK}_1 , SO ₁ , TOC, TOD | — | — | 0.4 | V | $I_{OL} = 0.4$ mA | |
| I/O leakage current | $ I_{IL} $ | RESET, \overline{SCK}_1 , SI ₁ , \overline{INT}_0 , \overline{INT}_1 , INT ₂ , INT ₃ , INT ₄ , \overline{STOPC} , EVND, OSC ₁ , SO ₁ , TOC, TOD | — | — | 1.0 | μA | $V_{in} = 0$ V to V_{CC} | 1 |
| Active mode current dissipation (digital input mode) | I_{CC1} | V_{CC} | — | 2.5 | 5.0 | mA | $V_{CC} = 5.0$ V, $f_{OSC} = 4$ MHz | 2 |
| | I_{CC2} | V_{CC} | — | 0.3 | 1.0 | mA | $V_{CC} = 3.0$ V, $f_{OSC} = 800$ kHz | 2 |
| | I_{CC3} | V_{CC} | — | 5.0 | 9.0 | mA | HD40A4668, HD40A46612, HD40A4669, HD407A4669: $V_{CC} = 5$ V, $f_{OSC} = 8$ MHz | 2 |

4. Power supply current when the on-chip timers are operating and there are no I/O currents.

| | | |
|------------------|-------|---|
| Test conditions: | MCU: | I/O reset |
| | | Serial interface stopped |
| | | DTMF not operating |
| | | Standby mode |
| | Pins: | RESET at GND (0 V to 0.3 V) |
| | | $\overline{\text{TEST}}$ at V_{CC} ($V_{CC} - 0.3$ V to V_{CC}) |

5. These are the source currents when no I/O current is flowing.

| | | |
|------------------|-------|---|
| Test conditions: | Pins: | RESET at GND (0 V to 0.3 V) |
| | | $\overline{\text{TEST}}$ at V_{CC} ($V_{CC} - 0.3$ V to V_{CC}) |
| | | D ₁₃ at V_{CC} ($V_{CC} - 0.3$ V to V_{CC}) for the HD407A4669 |

6. The required voltage for RAM data retention.

HD404669 Series

I/O Characteristics for Standard Pins (HD404668, HD4046612, HD404669, HD40A4668, HD40A46612, HD40A4669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$; HCD404669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = +75^\circ\text{C}$; HD407A4669: $V_{CC} = 2.2$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Condition | Notes |
|---------------------|------------|---|---------------------|-----|---------------------|------|---|-------|
| Input high voltage | V_{IH} | D ₁₂ , D ₁₃ , R0 to R4, R6 to RA, RD, RE ₀ | $0.7V_{CC}$ | — | $V_{CC} + 0.3$ | V | — | |
| Input low voltage | V_{IL} | D ₁₂ , D ₁₃ , R0 to R4, R6 to RA, RD, RE ₀ | -0.3 | — | $0.3V_{CC}$ | V | — | |
| Output high voltage | V_{OH} | R0 to R4, R6 to RA | $V_{CC} - 0.5$ | — | — | V | $-I_{OH} = 0.3$ mA | |
| Output low voltage | V_{OL} | R0 to R4, R6 to RA | — | — | 0.4 | V | $I_{OL} = 0.4$ mA | |
| I/O leakage current | $ I_{IL} $ | D ₁₂ , R0 to R4, R6 to RA, RD, RE ₀ | — | — | 1 | μA | $V_{in} = 0$ V to V_{CC} | 1 |
| | | D ₁₃ | — | — | 1 | μA | HD404668, HD4046612, HD404669, HCD404669, HD40A4668, HD40A46612, HD40A4669: $V_{in} = 0$ V to V_{CC} | 1 |
| | | — | — | — | 1 | μA | HD407A4669: $V_{in} = V_{CC} - 0.3$ V to V_{CC} | 1 |
| | | — | — | — | 20 | μA | HD407A4669: $V_{in} = 0$ V to 0.3 V | 1 |
| Pull-up MOS current | $-I_{PU}$ | R0 to R4, R6 to RA | 10 | 50 | 150 | μA | $V_{CC} = 3.0$ V, $V_{in} = 0$ V | |
| Input high voltage | V_{IHA} | COMP ₀ , COMP ₁ | $V_{C_{ref}} + 0.1$ | — | — | V | Analog compare mode | |
| Input low voltage | V_{ILA} | COMP ₀ , COMP ₁ | — | — | $V_{C_{ref}} - 0.1$ | V | Analog compare mode | |

Note: 1. Output buffer current is excluded.

HD404669 Series

I/O Characteristics for High-Current (HD404668, HD4046612, HD404669, HD40A4668, HD40A46612, HD40A4669): $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$; **HCD404669:** $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = +75^{\circ}\text{C}$; **HD407A4669:** $V_{CC} = 2.2$ to 5.5 V, $GND = 0$ V, $T_a = -20^{\circ}\text{C}$ to $+75^{\circ}\text{C}$, unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Condition | Notes |
|-----------------------|------------|------------------------------------|----------------|-----|----------------|---------------|--|-------|
| Input high voltage | V_{IH} | D_0 to D_5 , D_9 to D_{11} | $0.7V_{CC}$ | — | $V_{CC} + 0.3$ | V | — | |
| Input low voltage | V_{IL} | D_0 to D_5 , D_9 to D_{11} | -0.3 | — | $0.3V_{CC}$ | V | — | |
| Output high voltage | V_{OH} | D_0 to D_5 , D_9 to D_{11} | $V_{CC} - 0.5$ | — | — | V | $-I_{OH} = 0.3$ mA | |
| | | D_0 to D_3 | $V_{CC} - 2.0$ | — | — | V | $-I_{OH} = 10$ mA $V_{CC} = 4.5\text{V to }5.5\text{V}$ | |
| Output low voltage | V_{OL} | D_0 to D_5 , D_9 to D_{11} | — | — | 0.4 | V | $I_{OL} = 0.4$ mA | |
| | | D_4 , D_5 , D_9 to D_{11} | — | — | 2.0 | V | $I_{OL} = 15$ mA, $V_{CC} = 4.5$ V to 5.5 V | |
| I/O leakage current | $ I_{IL} $ | D_0 to D_5 , D_9 to D_{11} | — | — | 1 | μA | $V_{in} = 0$ V to V_{CC} | 1 |
| Pull-up MOS current | $-I_{PU}$ | D_4 , D_5 , D_9 to D_{11} | 10 | 50 | 150 | μA | $V_{CC} = 3$ V, $V_{in} = 0$ V | |
| Pull-down MOS current | I_{PD} | D_0 to D_3 | 10 | 50 | 150 | μA | $V_{CC} = 3$ V, $V_{in} = 3$ V | |

Note: 1. Output buffer current is excluded.

HD404669 Series

DTMF Characteristics (HD404668, HD4046612, HD404669, HD40A4668, HD40A46612, HD40A4669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$; HCD404669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = +75^\circ\text{C}$; HD407A4669: $V_{CC} = 2.2$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise specified)

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|-------------------------|------------------|-------|-----|-----|-----|--------------------------|--|-------|
| Tone output voltage (1) | V_{OR} | TONER | 500 | 660 | — | mV_{rms} | $V_{T_{\text{ref}}} - GND = 2.0$ V, $R_L = 100$ k Ω , $V_{CC} = 2.2$ to 5.0 V | 1 |
| Tone output voltage (2) | V_{OC} | TONEC | 520 | 690 | — | mV_{rms} | $V_{T_{\text{ref}}} - GND = 2.0$ V, $R_L = 100$ k Ω , $V_{CC} = 2.2$ to 5.0 V | 1 |
| Tone output distortion | %DIS | — | — | 3 | 7 | % | Short circuit between TONER and TONEC, $R_L = 100$ k Ω | 2 |
| Tone output ratio | dB_{CR} | — | — | 2.5 | — | dB | Short circuit between TONER and TONEC, $R_L = 100$ k Ω | 2 |

Notes: These characteristics are guaranteed with an operating frequency, f_{OSC} , of 400 kHz, 800 kHz, 2 MHz, 3.58 MHz, 4 MHz, 7.16 MHz, or 8 MHz.

1. See figure 89.
2. See figure 90.

HD404669 Series

AC Characteristics (HD404668, HD4046612, HD404669, HD40A4668, HD40A46612, HD40A4669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$; HCD404669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = +75^\circ\text{C}$; HD407A4669: $V_{CC} = 2.2$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise specified)

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Condition | Notes |
|---|--------------|-------------------------------------|------|--------|-----|---------------|---|----------|
| Clock oscillation frequency | f_{OSC} | OSC ₁ , OSC ₂ | — | 400 | — | kHz | | 1 |
| | | | — | 800 | — | kHz | | 1 |
| | | | — | 2 | — | MHz | | 1 |
| | | | — | 3.58 | — | MHz | | 1 |
| | | | — | 4 | — | MHz | | 1 |
| | | | — | 7.16 | — | MHz | HD40A4668, HD40A46612, HD40A4669, HD407A4669: $V_{CC} = 4.0\text{V}$ to 5.5V | 1 |
| | | | — | 8 | — | MHz | | |
| | | X1, X2 | — | 32.768 | — | kHz | | |
| Instruction cycle time | t_{cyc} | — | — | 8 | — | μs | $f_{OSC} = 4$ MHz, division by 32 | 2 |
| | | | — | 4 | — | μs | $f_{OSC} = 4$ MHz, division by 16 | 2 |
| | | | — | 2 | — | μs | $f_{OSC} = 4$ MHz, division by 8 | 2 |
| | | | — | 1 | — | μs | $f_{OSC} = 4$ MHz, division by 4 | 2 |
| | t_{subcyc} | — | — | 244.14 | — | μs | 32 kHz oscillator used, division by 8 | 3 |
| | | | — | 122.07 | — | μs | 32 kHz oscillator used, division by 4 | 3 |
| Oscillation stabilization time (ceramic oscillator) | t_{RC} | OSC ₁ , OSC ₂ | — | — | 7.5 | ms | | 4, 5 |
| Oscillation stabilization time (crystal oscillator) | t_{RC} | OSC ₁ , OSC ₂ | — | — | 30 | ms | | 4, 5, 12 |
| | | X1, X2 | — | — | 2 | s | $T_a = -10^\circ\text{C}$ to $+60^\circ\text{C}$ | 4 |
| External clock high width | t_{CPH} | OSC ₁ | 1100 | — | — | ns | $f_{OSC} = 400$ kHz | 6 |
| | | | 550 | — | — | ns | $f_{OSC} = 800$ kHz | |
| | | | 215 | — | — | ns | $f_{OSC} = 2$ MHz | |
| | | | 115 | — | — | ns | $f_{OSC} = 3.58$ MHz | |
| | | | 105 | — | — | ns | $f_{OSC} = 4$ MHz | |
| | | | 57.5 | — | — | ns | $f_{OSC} = 7.16$ MHz | 6, 11 |
| | | | 52.5 | — | — | ns | $f_{OSC} = 8$ MHz | |

HD404669 Series

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Condition | Notes |
|--|------------|---|------|-----|------|----------------------------|---|-------|
| External clock low width | t_{CPL} | OSC ₁ | 1100 | — | — | ns | $f_{OSC} = 400 \text{ kHz}$ | 6 |
| | | | 550 | — | — | ns | $f_{OSC} = 800 \text{ kHz}$ | |
| | | | 215 | — | — | ns | $f_{OSC} = 2 \text{ MHz}$ | |
| | | | 115 | — | — | ns | $f_{OSC} = 3.58 \text{ MHz}$ | |
| | | | 105 | — | — | ns | $f_{OSC} = 4 \text{ MHz}$ | |
| | | | 57.5 | — | — | ns | $f_{OSC} = 7.16 \text{ MHz}$ | 6, 11 |
| | | | 52.5 | — | — | ns | $f_{OSC} = 8 \text{ MHz}$ | |
| External clock rise time | t_{CPr} | OSC ₁ | — | — | 150 | ns | $f_{OSC} = 400 \text{ kHz}$ | 6 |
| | | | — | — | 75 | ns | $f_{OSC} = 800 \text{ kHz}$ | |
| | | | — | — | 35 | ns | $f_{OSC} = 2 \text{ MHz}$ | |
| | | | — | — | 25 | ns | $f_{OSC} = 3.58 \text{ MHz}$ | |
| | | | — | — | 20 | ns | $f_{OSC} = 4 \text{ MHz}$ | |
| | | | — | — | 12.5 | ns | $f_{OSC} = 7.16 \text{ MHz}$ | 6, 11 |
| | | | — | — | 10 | ns | $f_{OSC} = 8 \text{ MHz}$ | |
| External clock fall time | t_{CPr} | OSC ₁ | — | — | 150 | ns | $f_{OSC} = 400 \text{ kHz}$ | 6 |
| | | | — | — | 75 | ns | $f_{OSC} = 800 \text{ kHz}$ | |
| | | | — | — | 35 | ns | $f_{OSC} = 2 \text{ MHz}$ | |
| | | | — | — | 25 | ns | $f_{OSC} = 3.58 \text{ MHz}$ | |
| | | | — | — | 20 | ns | $f_{OSC} = 4 \text{ MHz}$ | |
| | | | — | — | 12.5 | ns | $f_{OSC} = 7.16 \text{ MHz}$ | 6, 11 |
| | | | — | — | 10 | ns | $f_{OSC} = 8 \text{ MHz}$ | |
| \overline{INT}_0 – \overline{INT}_4 , EVND high widths | t_{tH} | \overline{INT}_0 to \overline{INT}_4 , EVND | 2 | — | — | $t_{cyc}/$ t_{subcyc} | — | 7 |
| \overline{INT}_0 – \overline{INT}_4 , EVND low widths | t_{tL} | \overline{INT}_0 to \overline{INT}_4 , EVND | 2 | — | — | $t_{cyc}/$ t_{subcyc} | — | 7 |
| RESET high width | t_{RSTH} | RESET | 2 | — | — | t_{cyc} | — | 8 |
| \overline{STOPC} low width | t_{STPL} | \overline{STOPC} | 1 | — | — | t_{RC} | — | 9 |
| RESET fall time | t_{RSTf} | RESET | — | — | 20 | ms | — | 8 |
| \overline{STOPC} rise time | t_{STPr} | \overline{STOPC} | — | — | 20 | ms | — | 9 |
| Input capacitance | C_{in} | All pins except D ₁₃ | — | — | 15 | pF | $f = 1 \text{ MHz}$ $V_{in} = 0 \text{ V}$, | |
| | | D ₁₃ | — | — | 15 | pF | HD40A4668, HD40A46612, HD40A4669, HCD404669, HD404668, HD4046612, HD404669: $f = 1 \text{ MHz}$, $V_{in} = 0 \text{ V}$ | |
| | | | — | — | 40 | pF | HD407A4669: $f = 1 \text{ MHz}$, $V_{in} = 0 \text{ V}$ | |

HD404669 Series

| Item | Symbol | Pin(s) | Min | Typ | Max | Unit | Test Condition | Notes |
|--------------------------------------|-------------------|---|-----|-----|-----|------------------|---|-------|
| Analog comparator stabilization time | t_{CSTB} | COMP ₀ to COMP ₁ | — | — | 2 | t_{cyc} | $V_{\text{CC}} = 2.2 \text{ V to } 5.5 \text{ V}$ | 10 |
| | | | — | — | 10 | t_{cyc} | $V_{\text{CC}} = 1.8 \text{ V to less than } 2.2 \text{ V}$ | |

- Notes:
1. Set bits 0 and 1 (SSR10, SSR11) of system clock select register 1 (SSR1: \$029) and bits 2 and 3 (SSR22, SSR23) of system clock select register 2 (SSR2: \$02A) according to the system clock frequency used.
 2. Set bits 0 and 1 (SSR20, SSR21) of system clock select register 2 (SSR2: \$02A) according to the system clock frequency division ratio used.
 3. Set bit 2 (SSR12) of system clock select register 1 (SSR1: \$029) according to the subsystem clock frequency division ratio used.
 4. The oscillation stabilization time is defined as follows:
 - (1) The time required for the oscillation to settle after V_{CC} has reached the minimum specification value at power-on.
 - (2) The time required for the oscillation to settle after RESET input has gone high when stop mode is cleared.
 - (3) The time required for the oscillation to settle after $\overline{\text{STOPC}}$ input has gone low when stop mode is cleared.

To ensure enough time for the oscillation to settle at power-on or when stop mode is cleared, input the RESET or $\overline{\text{STOPC}}$ signal for at least time t_{RC} . The oscillation stabilization time will depend on the circuit constants and stray capacitance. The oscillator should be determined in consultation with the oscillator manufacturer.
 5. Set bits 0 and 1 (MIS0, MIS1) in the miscellaneous register (MIS: \$00C) according to the oscillation stabilization time of the system oscillator.
 6. See figure 91.
 7. See figure 92.

Unit t_{cyc} applies when the MCU is in standby mode or active mode.

Unit t_{subcyc} applies when the MCU is in watch mode or subactive mode.
 8. See figure 93.
 9. See figure 94.
 10. This is the time required for the analog comparator to settle, ensuring that the correct data is read, after pins RD₀/COMP₀ and RD₁/COMP₁ are set to analog input mode.
 11. Applies to the HD40A4668, HD40A46612, HD40A4669, and HD407A4669. The test condition is $V_{\text{CC}} = 4.0 \text{ to } 5.5 \text{ V}$.
 12. Applies to the HD404668, HD4046612, HD404669, HCD404669, HD40A4668, HD40A46612, and HD40A4669. The test condition is $V_{\text{CC}} = 2.0 \text{ to } 5.5 \text{ V}$.

HD404669 Series

Serial Interface Timing Characteristics (HD404668, HD4046612, HD404669, HD40A4668, HD40A46612, HD40A4669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$; HCD404669: $V_{CC} = 1.8$ to 5.5 V, $GND = 0$ V, $T_a = +75^\circ\text{C}$; HD407A4669: $V_{CC} = 2.2$ to 5.5 V, $GND = 0$ V, $T_a = -20^\circ\text{C}$ to $+75^\circ\text{C}$, unless otherwise specified)

During Transmit Clock Output

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|-------------------------------|-------------------|---------------------------|-----|-----|-----|-------------------|-------------------------|-------|
| Transmit clock cycle time | t_{Scyc} | $\overline{\text{SCK}}_1$ | 1.0 | — | — | t_{cyc} | Load shown in figure 96 | 1 |
| Transmit clock high width | t_{SCKH} | $\overline{\text{SCK}}_1$ | 0.4 | — | — | t_{Scyc} | Load shown in figure 96 | 1 |
| Transmit clock low width | t_{SCKL} | $\overline{\text{SCK}}_1$ | 0.4 | — | — | t_{Scyc} | Load shown in figure 96 | 1 |
| Transmit clock rise time | t_{SCKr} | $\overline{\text{SCK}}_1$ | — | — | 100 | ns | Load shown in figure 96 | 1 |
| Transmit clock fall time | t_{SCKf} | $\overline{\text{SCK}}_1$ | — | — | 100 | ns | Load shown in figure 96 | 1 |
| Serial output data delay time | t_{DSO} | SO_1 | — | — | 300 | ns | Load shown in figure 96 | 1 |
| Serial input data setup time | t_{SSI} | SI_1 | 200 | — | — | ns | — | 1 |
| Serial input data hold time | t_{HSI} | SI_1 | 200 | — | — | ns | — | 1 |

Note: 1. Refer to figure 95.

During Transmit Clock Input

| Item | Symbol | Pin | Min | Typ | Max | Unit | Test Condition | Notes |
|-------------------------------|-------------------|---------------------------|-----|-----|-----|-------------------|-------------------------|-------|
| Transmit clock cycle time | t_{Scyc} | $\overline{\text{SCK}}_1$ | 1.0 | — | — | t_{cyc} | — | 1 |
| Transmit clock high width | t_{SCKH} | $\overline{\text{SCK}}_1$ | 0.4 | — | — | t_{Scyc} | — | 1 |
| Transmit clock low width | t_{SCKL} | $\overline{\text{SCK}}_1$ | 0.4 | — | — | t_{Scyc} | — | 1 |
| Transmit clock rise time | t_{SCKr} | $\overline{\text{SCK}}_1$ | — | — | 100 | ns | — | 1 |
| Transmit clock fall time | t_{SCKf} | $\overline{\text{SCK}}_1$ | — | — | 100 | ns | — | 1 |
| Serial output data delay time | t_{DSO} | SO_1 | — | — | 300 | ns | Load shown in figure 96 | 1 |
| Serial input data setup time | t_{SSI} | SI_1 | 200 | — | — | ns | — | 1 |
| Serial input data hold time | t_{HSI} | SI_1 | 200 | — | — | ns | — | 1 |

Note: 1. Refer to figure 95.

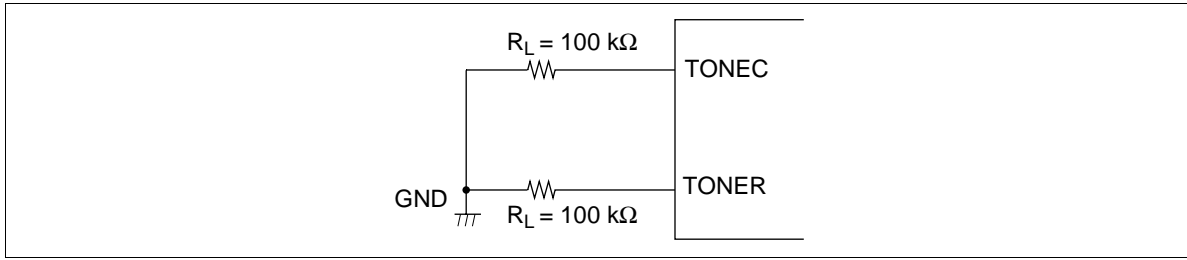


Figure 89 Tone Output Load Circuit

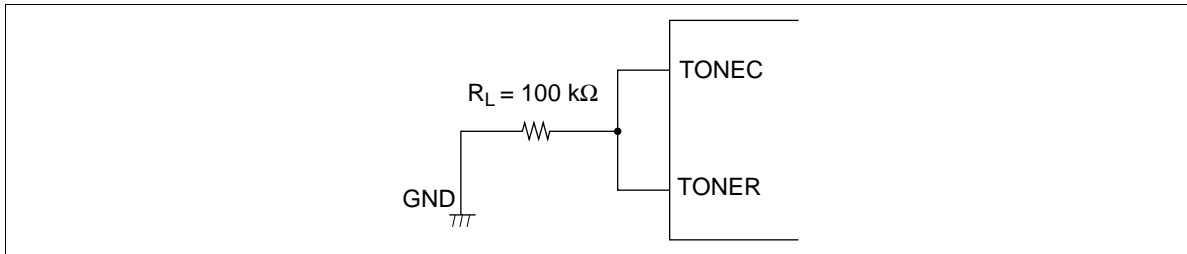


Figure 90 Distortion and dB_{CR} Load Circuit

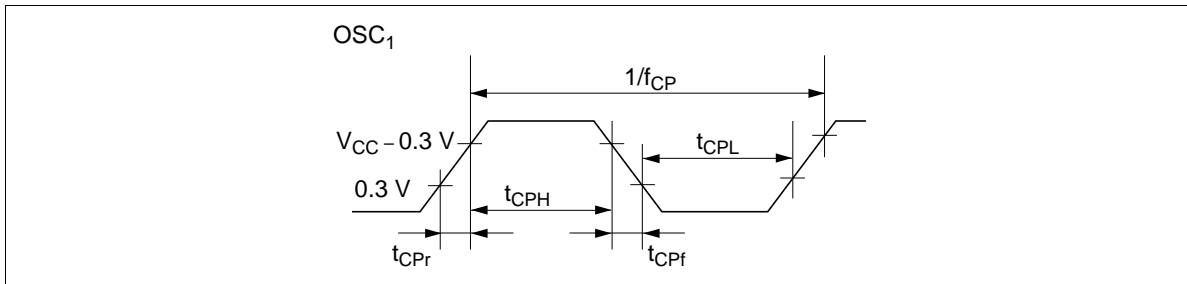


Figure 91 External Clock Timing

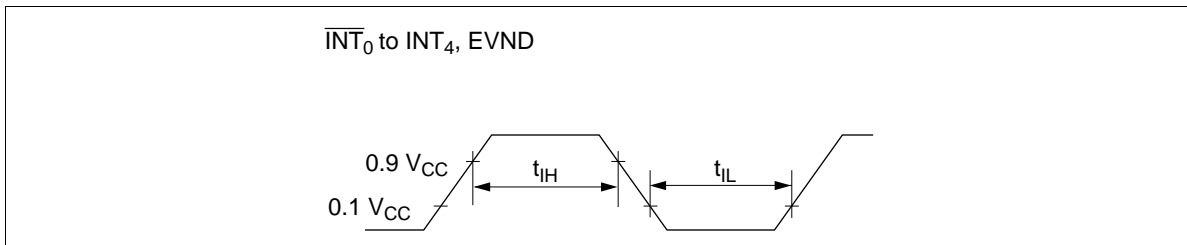


Figure 92 Interrupt Timing

HD404669 Series

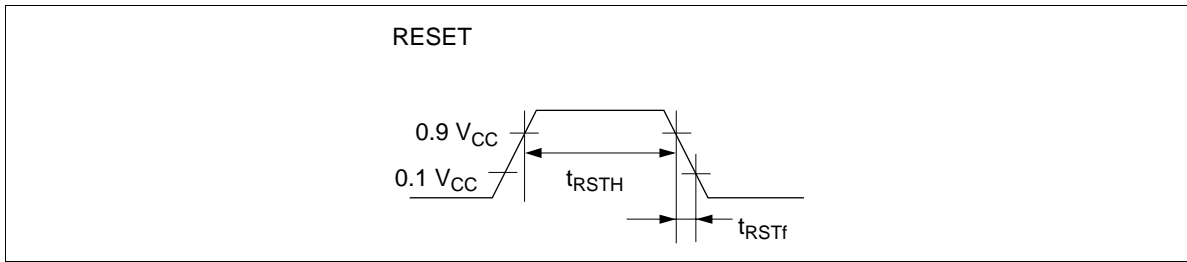


Figure 93 Reset Timing

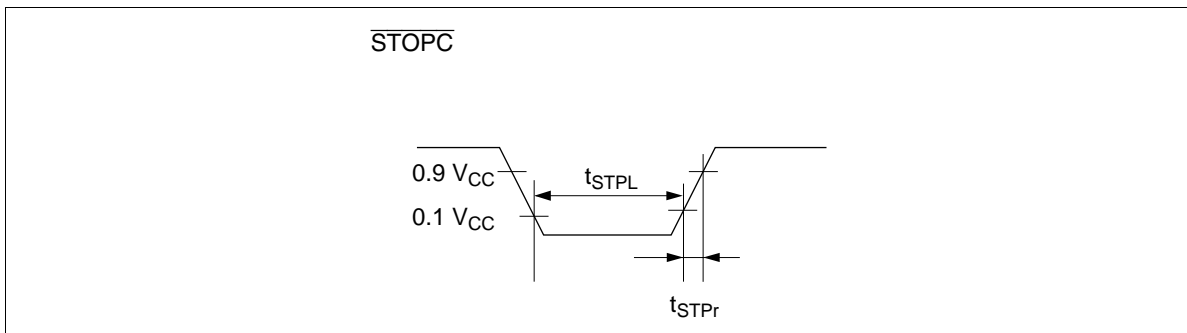


Figure 94 $\overline{\text{STOPC}}$ Timing

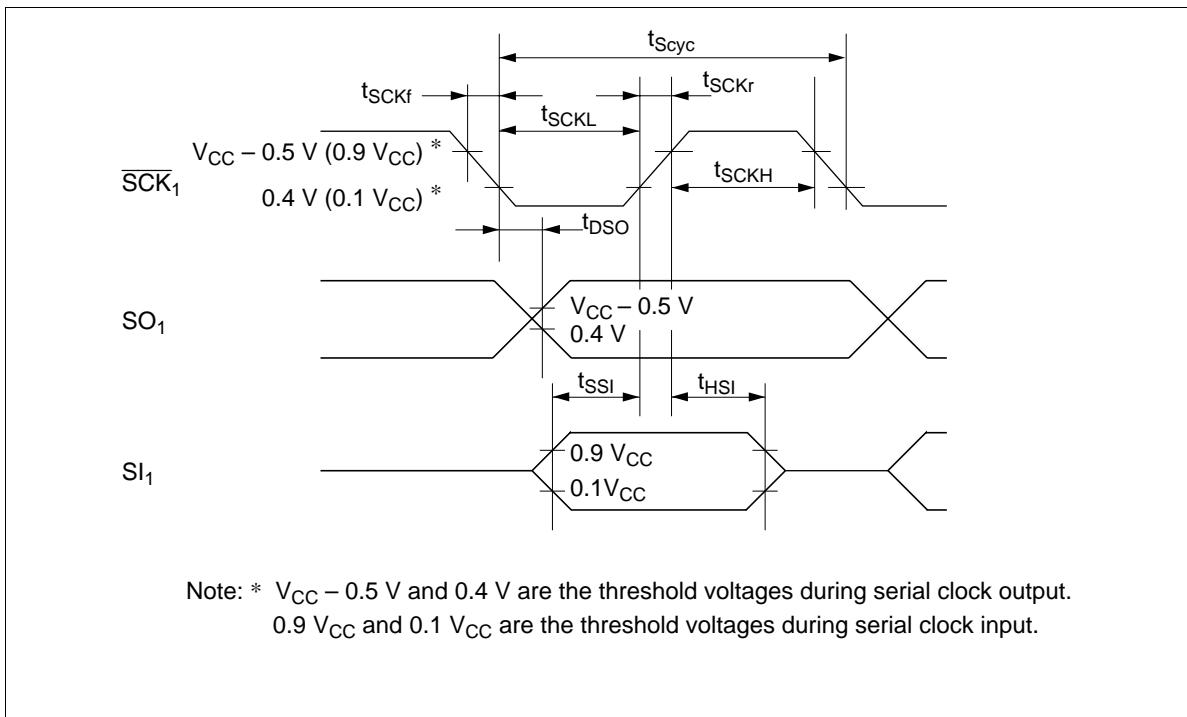


Figure 95 Serial Interface Timing

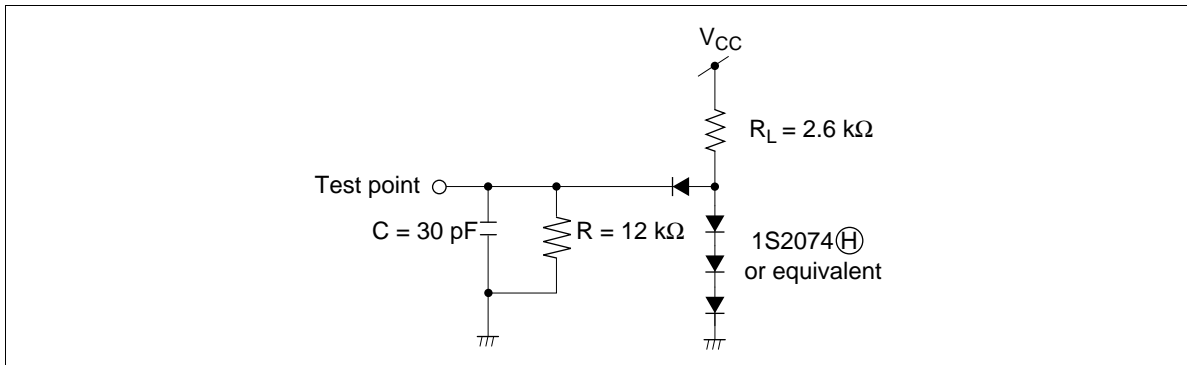


Figure 96 Timing Load Circuit

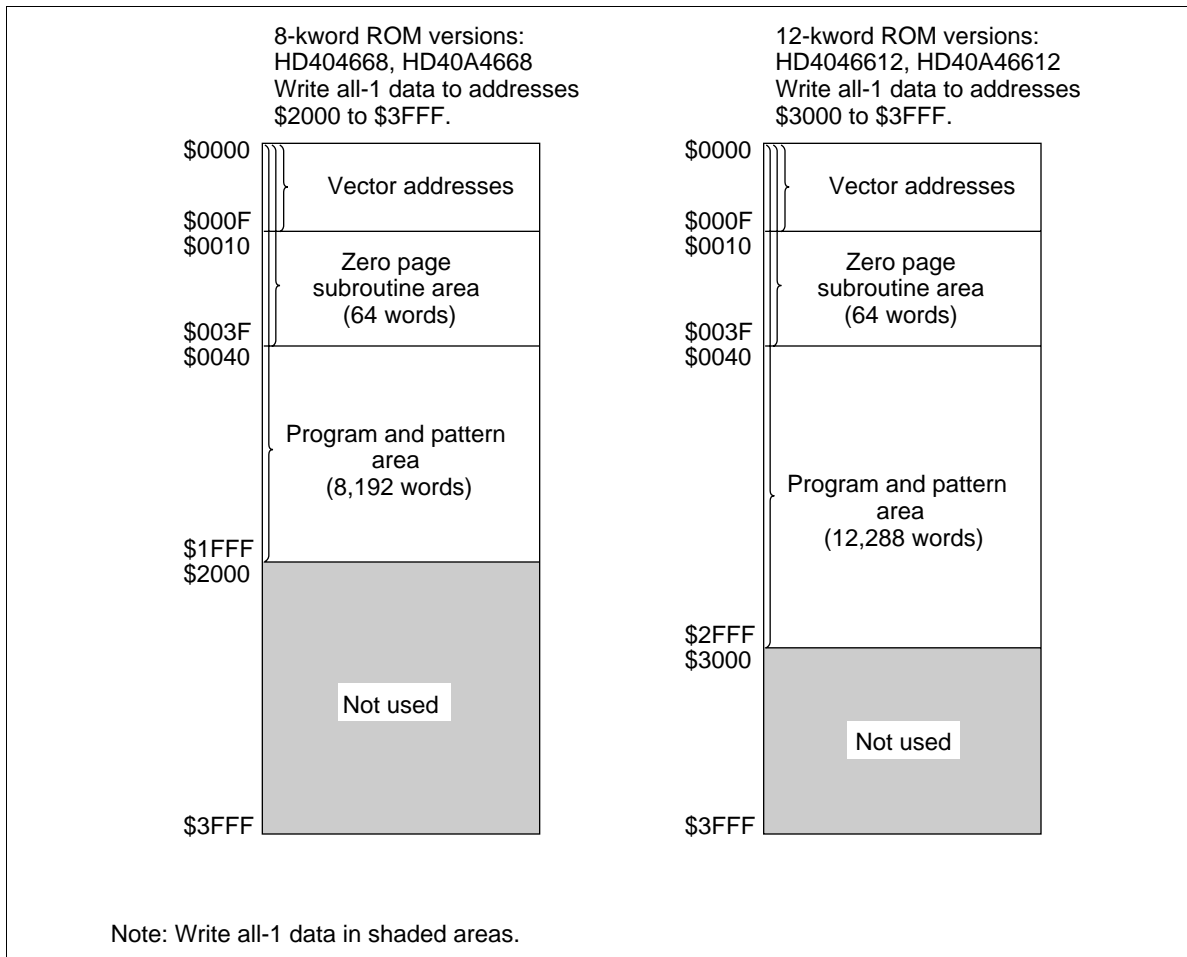
HD404669 Series

Notes on ROM Out

Please note the following when ordering HD404668, HD4046612, HD40A4668, or HD40A46612 ROM.

On ROM out, fill the ROM area indicated below with 1s to create the same data size as a 16-kword version (HD404669, HD40A4669). A 16-kword data size is required to change ROM data to mask manufacturing data since the program used is for a 16-kword version.

This limitation applies when using an EPROM or a data base.



HD404669 Series

HD404668/HD4046612/HD404669/HCD404669/HD40A4668/HD40A46612/HD40A4669 Option List

Please check off the appropriate applications and enter the necessary information.

| | | |
|-------------------------------|---|---|
| Date of order | / | / |
| Customer | | |
| Department | | |
| Name | | |
| ROM code name | | |
| LSI number (Hitachi entry) | | |

1. ROM Size

| | | |
|--------------------------|--|----------|
| <input type="checkbox"/> | Standard operation version: HD404668 | 8-kword |
| <input type="checkbox"/> | High-speed operation version: HD40A4668 | |
| <input type="checkbox"/> | Standard operation version: HD4046612 | 12-kword |
| <input type="checkbox"/> | High-speed operation version: HD40A46612 | |
| <input type="checkbox"/> | Standard operation version: HD404669 | 16-kword |
| <input type="checkbox"/> | High-speed operation version: HD40A4669 | |
| <input type="checkbox"/> | Chip version: HCD404669 | |

2. Optional Functions

| | | |
|---|--------------------------|---|
| * | <input type="checkbox"/> | With 32-kHz CPU operation, with time-base for clock |
| * | <input type="checkbox"/> | Without 32-kHz CPU operation, with time-base for clock |
| | <input type="checkbox"/> | Without 32-kHz CPU operation, without time-base for clock |

Note: * Options marked with an asterisk require a subsystem crystal oscillator (X1, X2).

3. ROM Code Data Type

Please specify the first type below (the upper bits and lower bits are mixed together), when using the EPROM on-package microcomputer type (including ZTAT™ version).

| | |
|--------------------------|--|
| <input type="checkbox"/> | The upper bits and lower bits are mixed together. The upper five bits and lower five bits are programmed to the same EPROM in alternating order (i.e., LULULU...). |
| <input type="checkbox"/> | The upper bits and lower bits are separated. The upper five bits and lower five bits are programmed to different EPROMs |

4. System Oscillator (OSC₁ and OSC₂)

| | | | |
|--------------------------|--------------------|-----|-----|
| <input type="checkbox"/> | Ceramic oscillator | f = | MHz |
| <input type="checkbox"/> | Crystal oscillator | f = | MHz |
| <input type="checkbox"/> | External clock | f = | MHz |

5. Stop Mode

| | |
|--------------------------|----------|
| <input type="checkbox"/> | Used |
| <input type="checkbox"/> | Not used |

6. Package

| | |
|--------------------------|--------|
| <input type="checkbox"/> | FP-64A |
| <input type="checkbox"/> | Chip |

Note: The specifications of shipped chips differ from of the package product. Please contact our sales staff for details.

HD404669 Series

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