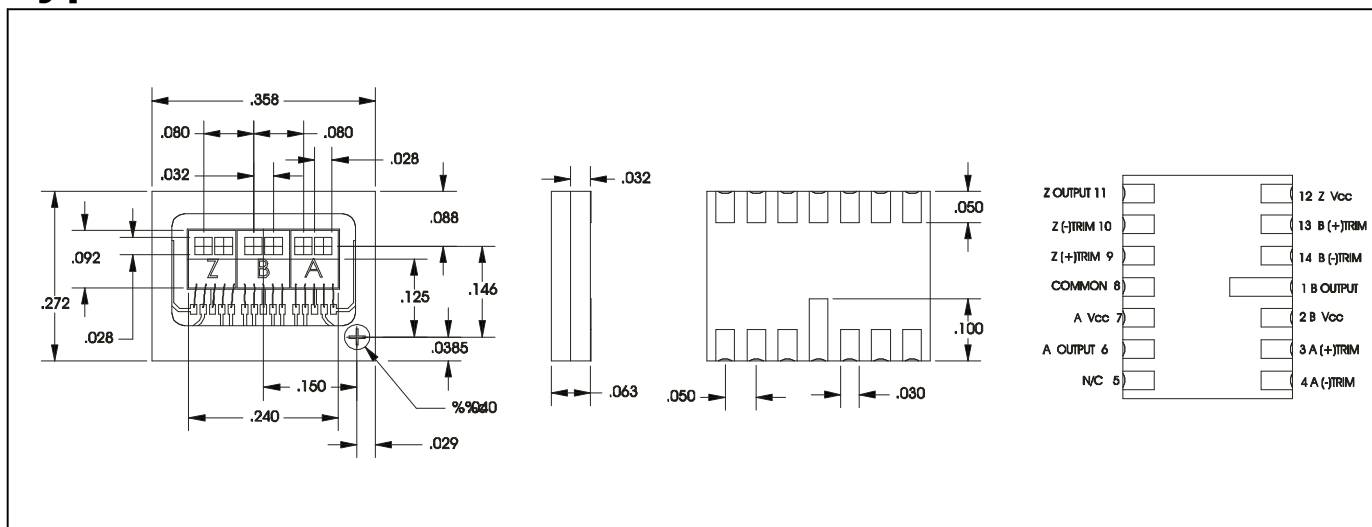


Optical Comparator Array Type OPR5011



Features

- Precise active area location
- Surface mountable
- TTL compatible output
- Wide supply voltage range
- Wide operating temperature range

Description

The OPR5011 is a hybrid sensor array consisting of three channels of the Optek OPC8332 Differential Optical Comparator, ("TRI-DOC") IC. The single chip construction ensures very tight dimensional tolerances between active areas. Specifically designed for high-speed/high resolution encoder applications, the open collector output switches based on the comparator output of input photodiode's light current levels. Logarithmic amplification of the input signals makes possible operation over a wide range of light levels.

The packages are surface mountable and made from a custom opaque polyimide which shields the active devices from stray light. The high temperature laminate can withstand multiple exposures to the most demanding soldering conditions. Wrap around contacts are gold plated for exceptional storage and wetting characteristics.

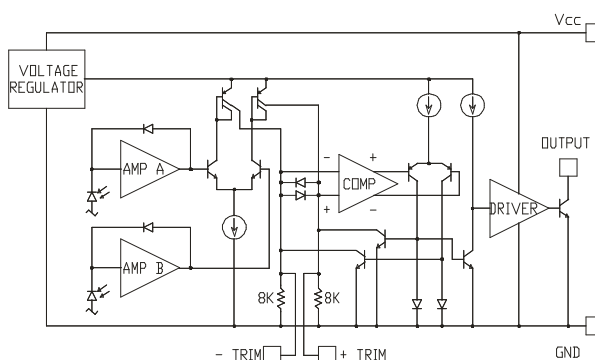
Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Storage Temperature	 -40°C to $+100^\circ\text{C}$
Operating Temperature	 -40°C to $+100^\circ\text{C}$
Supply Voltage	 24 V
Output Voltage	 24 V
Output Current	 14 mA
Power Dissipation	 500 mW
Soldering Temperature (Vapor Phase Reflow for 30 seconds)	 235°C

Replaces

OPR5003B
OPR5010

OPC8332 Block Diagram



Type OPR5011

Electrical Characteristics ($T_A = 25^\circ \text{C}$ unless otherwise noted)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS	NOTES
I_{CC}	Supply Current		9	20	mA	$V_{CC} = 24 \text{ V}$	
V_{OL}	Low Level Output Voltage		0.3	0.4	V	$I_{OL} = 14 \text{ mA}$, $V_{CC} = 4.5 \text{ V}$	2
I_{OH}	High Level Output Current		0.1	1.0	μA	$V_{CC} = V_O = 20.0 \text{ V}$	3
OPT-HYS	Optical Hysteresis		40.0		%	$V_{CC} = 5.0 \text{ V}$, $I_{OL} = 1.0 \text{ mA}$	4, 7
OPT-OFF	Optical Offset	-40	10	+40	%	$V_{CC} = 5.0 \text{ V}$, $I_{OL} = 1.0 \text{ mA}$	4, 7
$f_{\max}$	Frequency Response		1.0		MHz	$V_{CC} = 5.0 \text{ V}$	5
t_{lh}	Output Rise Time		1.0		μs		6
t_{hl}	Output Fall Time		300		ns		

NOTES:

- Pin (+) = $1.2 \mu\text{W}$ and Pin (-) = $0.8 \mu\text{W}$.
- Pin (+) = 100.0 nW and Pin (-) = $1.0 \mu\text{W}$.
- Pin (+) = $1.0 \mu\text{W}$ and Pin (-) 100.0 nW .
- Pin (-) held at $1.0 \mu\text{W}$ while Pin (+) is ramped from $0.5 \mu\text{W}$ to $1.5 \mu\text{W}$ and back to $0.5 \mu\text{W}$.
- Pin (+) modulated from $1.0 \mu\text{W}$ to $2.0 \mu\text{W}$. Pin (-) modulated from $1.0 \mu\text{W}$ to $2.0 \mu\text{W}$ with phase shifted 180° with respect to Pin (+). Use $100 \text{ k}\Omega$ trimpot to set the output signal to 50% duty cycle for maximum operating frequency.
- Measured between 10% and 90% points.
- Optical Hysteresis and Optical Offset are found by placing $1.0 \mu\text{W}$ of light on the inverting photodiode and ramping the light intensity of the noninverting input from $.5 \mu\text{W}$ up to $1.5 \mu\text{W}$ and back down. This will produce two trigger points, an upper trigger point and lower trigger point. These points are used to calculate the optical hysteresis and offset.

These are defined as:

$$\% \text{ Optical Hysteresis} = 100 \times \frac{(P_{\text{rise}} - P_{\text{fall}})}{P_{\text{in}}(-)}$$

$$\% \text{ Optical Offset} = 100 \times \frac{(P_{\text{average}} - P_{\text{in}}(-))}{P_{\text{in}}(-)}$$

Where:

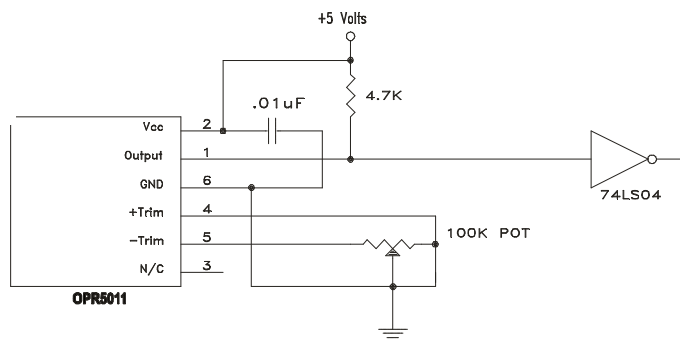
$P_{\text{in}}(-)$ = Light level incident upon the “-” photodiode on the IC chip ($P_{\text{in}}(-) = 1.0 \mu\text{W}$).

P_{rise} = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is an increasing level (rising edge).

P_{fall} = Value of light power level incident upon the “+” photodiode that is required to switch the digital output when the light level is a decreasing level (falling edge).

$$P_{\text{average}} = \frac{(P_{\text{rise}} + P_{\text{fall}})}{2}$$

Application Circuit



NOTES:

- The 74LS04 is recommended as a means of isolating the “DOC” comparator circuitry from transients induced by inductive and capacitive loads.
- It is recommended that a decoupling capacitor be placed as close as possible to the device.

Optek reserves the right to make changes at any time in order to improve design and to supply the best product possible.

Optek Technology, Inc. 1215 W. Crosby Road Carrollton, Texas 75006 (972)323-2200 Fax (972)323-2396

TBD