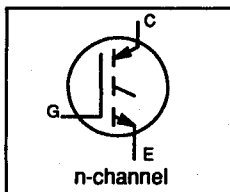


INSULATED GATE BIPOLAR TRANSISTOR

Fast-Speed IGBT

- Hermetically sealed
- Isolated
- Latch-proof
- Simple gate drive
- High operating frequency
- Switching-loss rating includes all "tail" losses
- Ceramic eyelets



$$V_{CES} = 1200 \text{ V}$$

$$f_{ic/2} \approx 7 \text{ kHz}$$

$$I_C @ f_{ic/2} = 13 \text{ A}$$

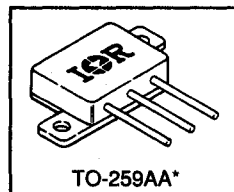
$$V_{CE(sat)} \leq 2.9 \text{ V}$$

$$@ V_{GE} = 15 \text{ V}, I_C = 25 \text{ A}$$

Description

Insulated Gate Bipolar Transistors (IGBTs) from International Rectifier have higher usable current densities than comparable bipolar transistors, while at the same time having simpler gate-drive requirements of the familiar power MOSFET. They provide substantial benefits to a host of higher-voltage, higher-current applications.

The performance of various IGBTs varies greatly with frequency. Note that IR now provides the designer with a speed benchmark ($f_{ic/2}$, or the "half-current frequency"), as well as an indication of the current handling capability of the device.



TO-259AA*

*For mechanical dimensions see page G-58

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Voltage*	1200	V
$I_C @ T_C = 25^\circ\text{C}$	Continuous Collector Current	45	A
$I_C @ T_C = 100^\circ\text{C}$	Continuous Collector Current	25	
I_{CM}	Pulsed Collector Current ①	180	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
I_{LM}	Clamped Inductive Load Current ②	90	A
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	200	W
$P_D @ T_C = 100^\circ\text{C}$	Maximum Power Dissipation	80	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
	Soldering Temperature, for 10 sec.	300 (0.063 in. (1.6mm) from case)	
	Weight	10.5	g

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	---	0.625	$^\circ\text{C/W}$
$R_{\theta CS}$	Case-to-Sink, flat, greased surface	---	0.21	---	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	---	---	30	

* User must not exceed the 1200V maximum rating, or permanent damage to the device may result.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$V_{(BR)ECS}$	Emitter-to-Collector Breakdown Volt. ④	22	---	---	V	$V_{GE}=0V, I_C=1.0A$
$V_{CE(sat)}$	Collector-to-Emitter Saturation Voltage	---	2.1	2.9	V	$V_{GE}=15V, I_C=25A$
		---	2.5	---		$V_{GE}=15V, I_C=45A$
		---	2.4	---		$V_{CE}=15V, I_C=25A, T_J=125^\circ\text{C}$
$V_{GE(th)}$	Gate Threshold Voltage	3.0	---	6.0		$V_{CE}=V_{GE}, I_C=250\mu A$
$\Delta V_{GE}(\eta)/\Delta T_J$	Temp. Coeff. of Threshold Voltage	---	-14	---	mV/°C	$V_{CE}=V_{GE}, I_C=250\mu A$
g_{fs}	Forward Transconductance ⑤	7.5	---	---	S	$V_{CE}=100V, I_C=25A$
I_{CES}	Zero Gate Voltage Collector Current	---	---	100	μA	$V_{GE}=0V, V_{CE}=960V, T_J=25^\circ\text{C}$
		---	---	1200		$V_{GE}=0V, V_{CE}=960V, T_J=125^\circ\text{C}$

Switching Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
Q_G	Total Gate Charge (turn-on)	---	---	100	nC	$I_C=25A, V_{CC}=400V$ $V_{GE}=15V$ See fig. 8. ⑥
Q_{GE}	Gate - Emitter Charge (turn-on)	---	---	21		
Q_{GC}	Gate - Collector Charge (turn-on)	---	---	43		
$t_{d(on)}$	Turn-On Delay Time	---	---	68	ns	$I_C=25A, V_{CC}=400V$ $T_J=25^\circ\text{C}$ ⑥
t_r	Rise Time	---	---	26		
$t_{d(off)}$	Turn-off Delay Time	---	---	480		
t_f	Fall Time	---	---	330	mJ	$V_{GE}=15V, R_G=2.35\Omega$ Energy losses include "tail". See fig. 10 & 14a
E_{on}	Turn-On Switching Loss	---	1.4	---		
E_{off}	Turn-Off Switching Loss	---	4.5	---		
E_{ts}	Total Switching Loss	---	5.9	8.2	mJ	$I_C=25A, V_{CC}=400V$ $T_J=125^\circ\text{C}$ ⑥
$t_{d(on)}$	Turn-On Delay Time	---	33	---		
t_r	Rise Time	---	15	---		
$t_{d(off)}$	Turn-Off Delay Time	---	590	---	ns	$V_{GE}=15V$ $R_G=2.35\Omega$ See fig. 10 & 14a
t_f	Fall Time	---	500	---		
E_{ts}	Total Switching Loss	---	13	---		
L_E	Internal Emitter Inductance	---	8.7	---	nH	Measured 5mm from package.
C_{iss}	Input Capacitance	---	2400	---	pF	$V_{GE}=0V$ $V_{CC}=30V$ $f=1.0\text{MHz}$
C_{oss}	Output Capacitance	---	140	---		
C_{res}	Reverse Transfer Capacitance	---	28	---		

Notes:

- ① Repetitive rating; $V_{GE}=20V$, pulse width limited by max. junction temperature. (See fig. 13b.)
 ② $V_{CC}=80\%(V_{CES})$, $V_{GE}=20V$, $L \geq 10\mu H$, $R_G=5.0\Omega$, (See fig. 13a.)
 ③ Pulse width $\leq 80\mu s$; duty factor $\leq 0.1\%$.
 ④ Equipment limitation
 ⑤ Pulse width $\leq 5\mu s$, single shot.

For both, power dissipation = 39.8 W

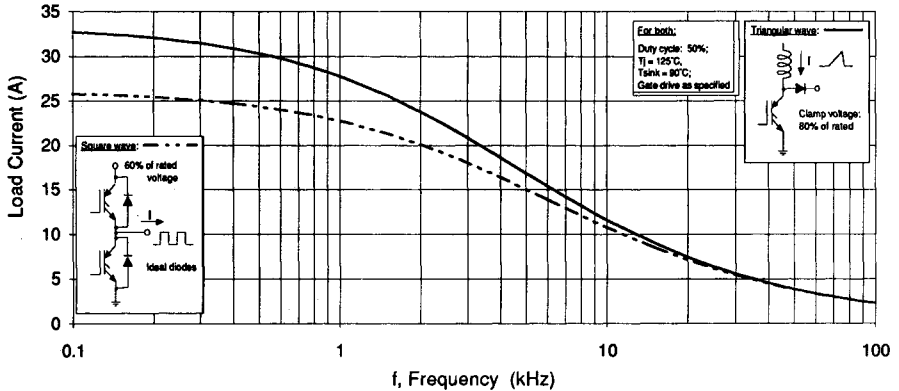


Fig. 1. Typical Load Current vs. Frequency
(For square wave, $I = I_{\text{RMS}}$ of fundamental; for triangular wave, $I = I_{\text{PK}}$)

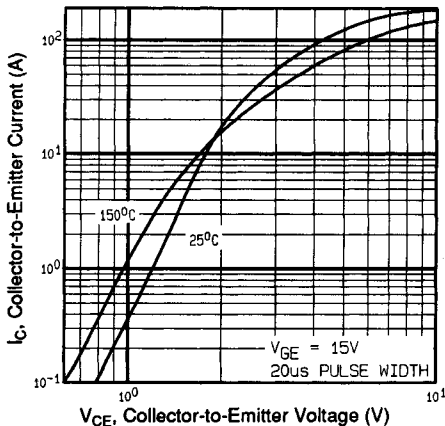


Fig. 2. Typical Output Characteristics

$T_J = 25^\circ\text{C}$
 $T_J = 150^\circ\text{C}$

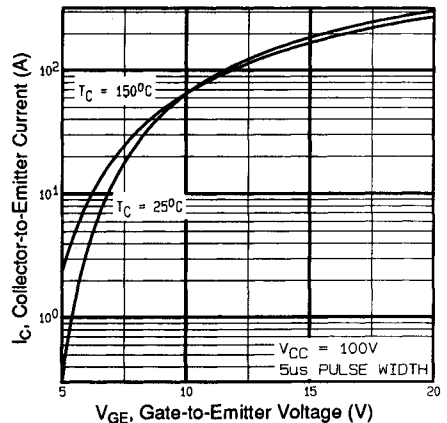


Fig. 3. Typical Transfer Characteristics

$T_J = 25^\circ\text{C}$
 $T_J = 150^\circ\text{C}$

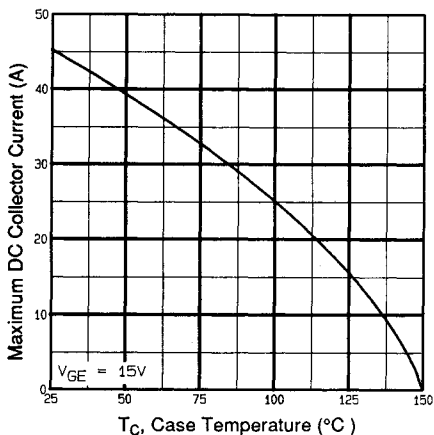


Fig. 4 Maximum Collector Current vs. Case Temperature

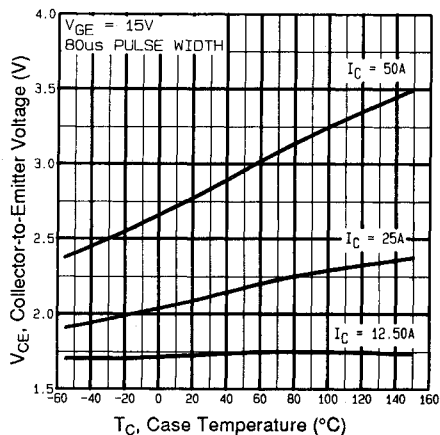


Fig. 5 Collector-to-Emitter Saturation Voltage vs. Case Temperature

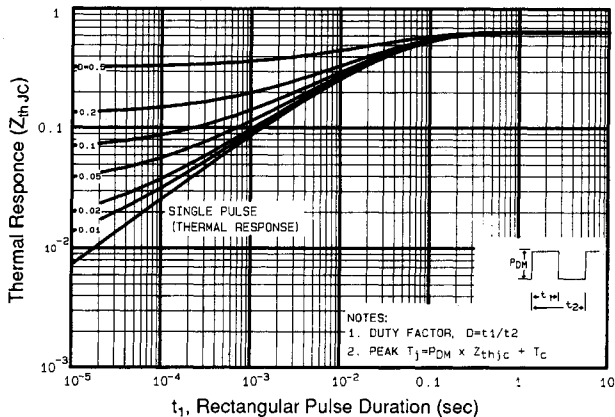


Fig. 6 Maximum Effective Transient Thermal Impedance, Junction-to-Case

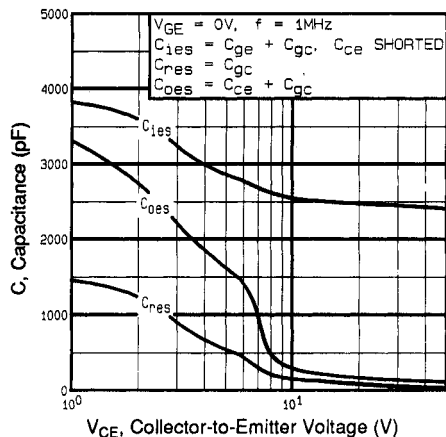


Fig. 7. Typical Capacitance vs. Collector-to-Emitter Voltage

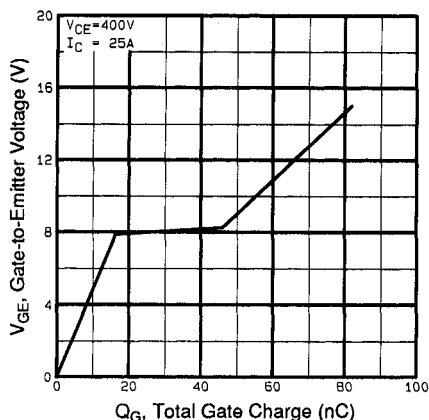


Fig. 8. Typical Gate Charge vs. Gate-to-Emitter Voltage

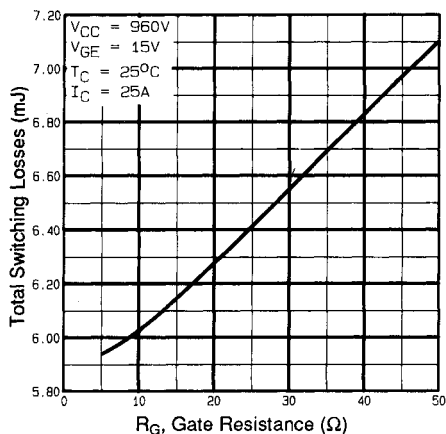


Fig. 9. Typical Switching Losses vs. Gate Resistance

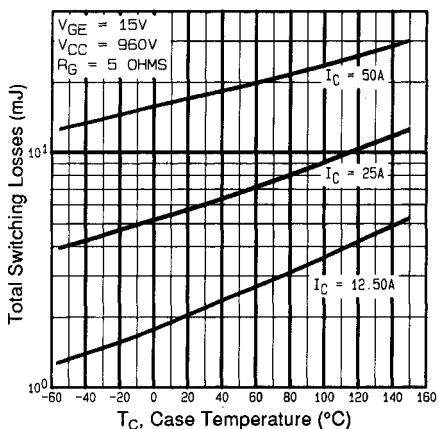


Fig. 10. Typical Switching Losses vs. Case Temperature

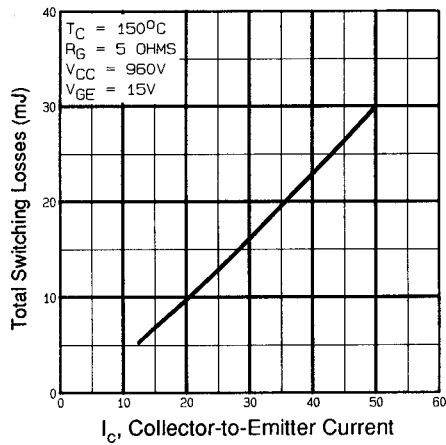


Fig. 11. Typical Switching Losses vs. Collector-to-Emitter Current

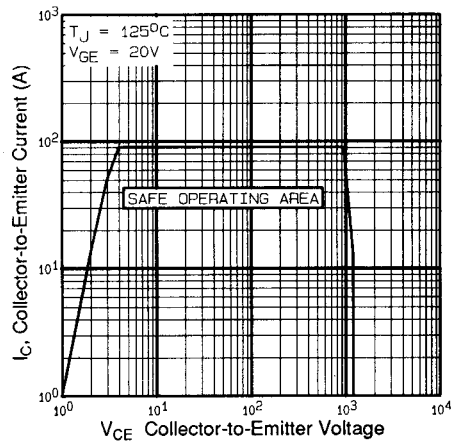
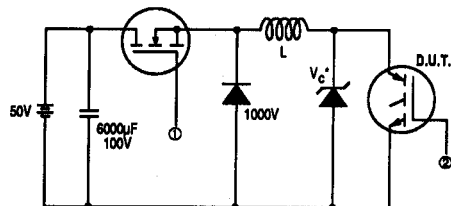


Fig. 12. Turn-Off SOA



* Driver same type as D.U.T.; $V_c = 80\%$ of $V_{ce(max)}$
 * Note: Due to the 50V power supply, pulse width and inductor will increase to obtain rated I_d .

Fig 13a. Clamped Inductive Load Test Circuit

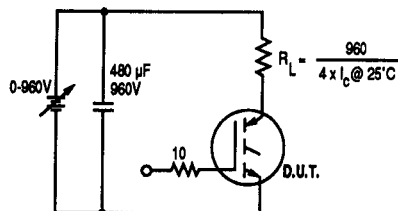


Fig 13b. Pulsed Collector Current Test Circuit

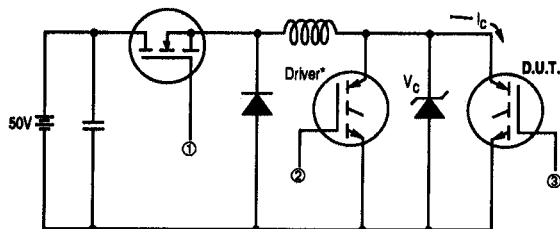


Fig 14a. Switching Loss Test Circuit

* Driver same type as D.U.T., $V_c = 960V$

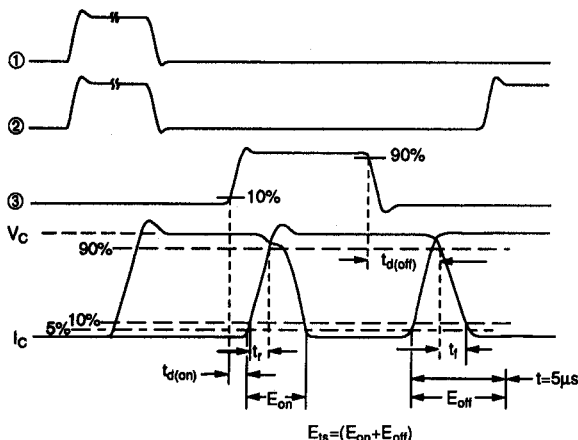
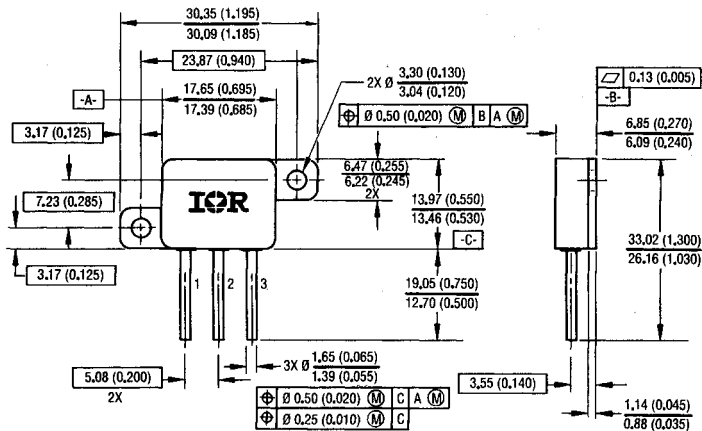


Fig 14b. Switching Loss Waveforms



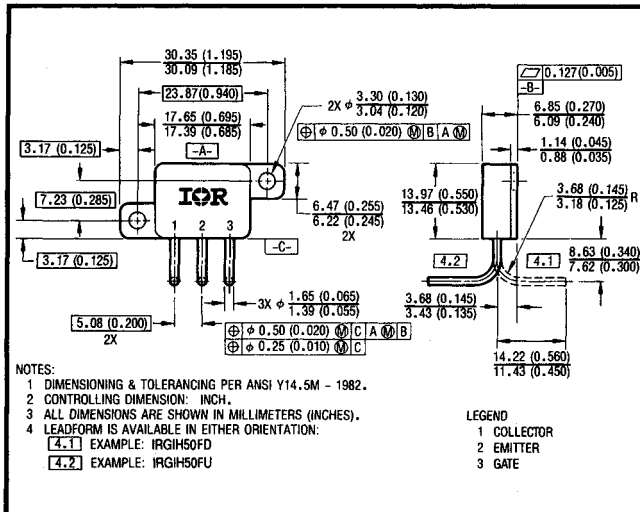
NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
- 2 DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

LEGEND

- 1 COLLECTOR
- 2 EMITTER
- 3 GATE

Fig. 15 - Conforms to JEDEC Outline TO-259AA



NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
- 2 CONTROLLING DIMENSION: INCH.
- 3 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 4 LEADFORM IS AVAILABLE IN EITHER ORIENTATION:
 [4.1] EXAMPLE: IRGIH50FD
 [4.2] EXAMPLE: IRGIH50FU

LEGEND

- 1 COLLECTOR
- 2 EMITTER
- 3 GATE

BERYLLIA WARNING PER MIL-S-19500
 Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

Fig. 16 - Optional Leadforms for Outline TO-259