UMC

T-75-07-90

UMC

UM9310

PRELIMINARY

Cordless Telephone Controller

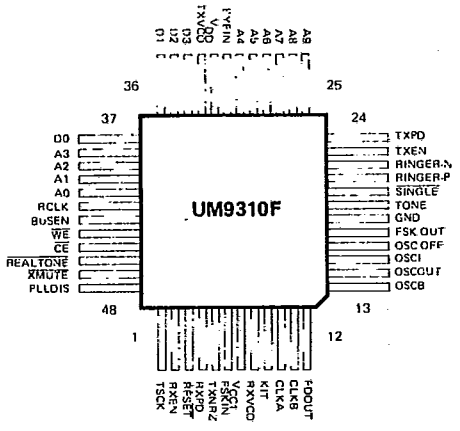
Features

- Two independent phase locked loop frequency synthesizers for transmitting and receiving
- 10 channels selectable
- Single frequency reference of 10.240 MHz
- Operating voltage of 3.3 to 5.5 volts
- On-chip 444.4 bps FSK modem
- Duplex data passage on pilot tone
- On-chip 1K SRAM expansion interface
- Microcontroller interface bus
- On-chip DTMF generator
- On-chip ringing tone output
- On-chip key-in tone output
- 48-pin flat package

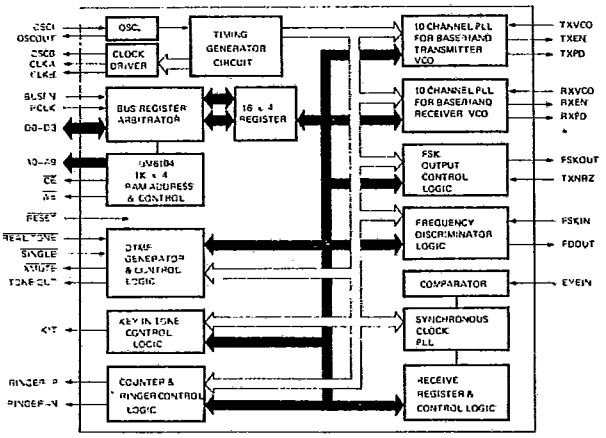
General Description

The UM9310 is a cordless telephone controller suitable for cordless telephone systems with automatic channel searching. It includes two independent PLL frequency synthesizers for the selection of communication channels. Up to ten channels can be selected. The UM9310 has a built-in modem which can be used to pass all control and status monitoring signals, such as ringing and dialing signal information between the handset unit and the base unit. For maximum flexibility in telecommunication applications, UM9310 also includes built-in DTMF tone, key-in tone, and ringing tone generators. All of the UM9310's operation can be controlled and monitored by accessing its 16 internal registers through a 4-bit data bus, which can be easily interfaced with a microprocessor or a microcontroller.

Pin Configuration



Block Diagram



Pin Description

Pin No.	Symbol	I/O	Description
1	TSCK	I	This pin is used for testing only and is internally pulled low.
2	RXEN	O	This pin functions as the receiver enable output. It follows the content of bit 1 of register 11.
3	$\overline{\text{RESET}}$	I	Chip reset. All registers are reset by this signal.
4	RXPD	O	Receiver VCO control pin. This pin sends a phase error detection signal to the receiver VCO. The frequency of the receiver VCO is controlled by the duty cycle of RXPD.
5	TXNRZ	O	Transmitter NRZ data is sent out through this pin.
6	FSKIN	I	The FSK signal is AC coupled to this input. The internal circuit of this pin is a waveshaper that converts the input FSK signal to a square wave which is sent to the frequency discriminator to determine the MARK or SPACE.
7	V_{DD2}		Positive power supply 2.
8	RXVCO	I	This input receives the receiver VCO frequency. The VCO signal is sharpened by a waveshaper and divided by two to act as the receiver PLL counter clock.
9	KIT	O	This is the KIT signal output. The KIT frequency is 1185 Hz.
10	CLKA	O	The frequency of this output is OSC/15 = 682.667 KHz. This output remains low as long as the $\overline{\text{RESET}}$ pin is low.
11	CLKB	O	The frequency of this output is OSC/3 = 3.413 MHz. This pin remains low as long as the $\overline{\text{RESET}}$ pin is low.
12	FDOUT	O	This pin is the frequency discriminator output. The FSK signal is converted to a mark or space voltage level determined by the frequency of FSK signal and output through this pin. This voltage is then filtered and sent to the EYEIN input.
13	OSCB	O	Oscillator buffer output.
14	OSCOUT	O	This is the oscillator output. A 10.24 MHz crystal and two capacitors should be connected between this pin and OSCIN to construct the oscillator circuit.
15	OSCIN	I	Oscillator input.
16	OSCOFF	I	This pin acts as the oscillator control pin. When this pin is high, the oscillator is disabled.
17	FSKOUT	O	This pin outputs the synthesized FSK signal. The synthesized waveform is a 10-time segment, 4-step sinusoid, and the data (MARK or SPACE) is controlled by TXNRZ.
18	GND		Signal ground.
19	TONE	O	This pin is the synthesized DTMF output. The row tone is a 20-time segment, 9-step sinusoid, while the column tone is 16-segment, 7-step sinusoid.

Pin Description

Pin No.	Symbol	I/O	Description
20	$\overline{\text{SINGLE}}$	I	This input controls the tone output. When this pin is low, a single tone is sent out rather than a row/column pair DTMF tone. The single tone produced for each key on the key pad is shown in the following: 1/R1 2/C2 3/R1 4/C1 5/R2 6/C3 7/R3 8/R3 9/R3 */R4 0/R4 #/R4
21	RINGERP	O	This pin is the ringer signal output.
22	RINGERN	O	Ringer signal output. This pin is the inverse of RINGERP.
23	TXEN	O	This pin functions as the transmitter enable output. It follows the content of bit 0 of register 11.
24	TXPD	O	Transmitter VCO control pin. This pin sends a phase error detection signal to the transmitter VCO. The frequency of the transmitter VCO is controlled by the duty cycle of TXPD.
25 – 30	A9 – A4	O	These pins output the external SRAM address.
38 – 41	A3 – A0	O	These pins output the external SRAM address.
31	EYEIN	I	This input receives the filtered output of FDOUT. It contains a comparator to determine the FSK signal as MARK or SPACE.
32	V_{DD}		Positive power supply.
33	TXVCO	I	This input receives the transmitter VCO frequency. The VCO signal is sharpened by a waveshaper and divided by two to act as the transmitter PLL counter clock.
34 – 37	D3 – D0	I/O	These pins are the data I/O pins of the external SRAM and registers.
42	RCLK	I	This input signal is used to count the input data nibble and acts as the clock of the data latch.
43	BUSEN	I	This input is the bus enable pin. Data access of UM9310 by external processor is enabled by activating this pin to high.
44	$\overline{\text{WE}}$	O	This output follows bit 3 of the first nibble data and is used to control read/write operation of external SRAM or internal registers.
45	$\overline{\text{CE}}$	O	During SRAM operation, this pin sends a low signal which is the inverse of the fourth clock of RCLK.
46	$\overline{\text{REALTONE}}$	I	If this pin is low during the DTMF signal output, the tone duration counter will be reset, and the DTMF signal will be sent out continuously.
47	$\overline{\text{XMUTE}}$	O	This pin is held low during the DTMF signal output.
48	PLLDIS	I	This pin is used for testing only and is pulled low internally.

Function Description

The functions and operations of UM9310 are controlled by sixteen internal 4-bit registers, which can be accessed by external microcomputer or micro-controller.

Registers R0 to R11 are used to handle the data communications performed by built-in 444.4 bps modem.

Output Registers – R0 to R3 (write-only):

These four registers can only be written by the microcomputer or micro-controller. When bit 0 of register 8 is set to 1, data written in these registers is sent out from FSKOUT according to the following format:

Start bits	R0	R1	R2	R3	Stop bits
011000	4 bits data	4 bits data	4 bits data	4 bits data	01

first bit sent out — last bit sent out

Input Registers – R4 to R7 (read-only):

These four registers are read-only registers which can be read through data buses D0 to D3. Once the start character embedded in the data stream input to the FSKIN pin is detected, these registers will start to buffer the data within the start and stop characters into R4 to R7 in the sequence of R4, R5, R6 and then R7.

Output Status Register – R8 (read/write):

Only bit 0 of this register is used. When bit 0 is set, the transmission of data within R0 to R3 is initiated. It will be cleared automatically after the data within R0 to R3 has been transmitted out.

Input Status Register – R9 (read/write):

Bit 0	Bit 1	Bit 2	Bit 3
R4 data available	R5 data available	R6 data available	R7 data available

R9 is used to indicate whether the data buffered in input registers R4 to R7 is available to be read by the microcontroller or not. The associated bit in register R9 is set as long as the data received by the corresponding registers are available. They must be reset by the microcontroller in order to receive the next set of data.

Signal Status Register – R10 (read-only):

In normal data receiving operations, bit 0 of R10 will be set only when the receiver is synchronous with the incoming data stream. It will be reset when the synchronous signal is lost or bit 2 or R11 is cleared.

Modem control Register – R11 (write-only):

Bit 0	Bit 1	Bit 2	Bit 3
Transmitter on	Demodulator on	Asynchronous receiver on	Hand/base mode select

When bit 0 is cleared, the FSK generator will be disabled and powered down, R8 will be cleared, and TXPD will be pulled low. The TXEN pin, which follows the state of bit 0, is used to control the external RF amplifier and TXVCO.

Bit 1 is used to control the operations of the data receiving circuit. When it is cleared, the discriminator will be disabled, the slice comparator will be powered down and RXPD will be pulled low. At all other times this circuit will operate normally. The RXEN pin, which follows the state of bit 1, can be used to control the external RF amplifier, mixer, IF, and RXVCO.

The data receiver for extracting the timing clock and data information from the data communications of the built-in modem can be disabled by resetting bit 2 to 0, which will in turn reset R10. Bit 2 of R11 must be set to 1 during normal receiving operation.

UM9310 can be operated in either a base or a handset unit by programming bit 3 of R11. When bit 3 is 0, base mode is selected. When bit 3 is 1, handset mode is selected.

Channel Select Register – R12 (read/write):

One of ten channels (each consisting of a pair of transmitting and receiving frequencies) can be selected by programming R11 in accordance with Table 1:

bit				Channel No.	Transmission and Reception Frequency (MHZ)			
					Base Unit (bit 3, R11 = 0)		Hand Unit (bit 3, R11 = 1)	
3	2	1	0		transmit	receive	transmit	receive
0	0	0	1	1	46.610	38.975	49.670	35.915
0	0	1	0	2	46.630	39.150	49.845	35.935
0	0	1	1	3	46.670	39.165	49.860	35.975
0	1	0	0	4	46.710	39.075	49.770	36.015
0	1	0	1	5	46.730	39.180	49.875	36.035
0	1	1	0	6	46.770	39.135	49.830	36.075
0	1	1	1	7	46.830	39.195	49.890	36.135
1	0	0	0	8	46.870	39.235	49.930	36.175
1	0	0	1	9	46.930	39.295	49.990	36.235
1	0	1	0	10	46.970	39.275	49.970	36.275

Table 1: Channel Selection

The frequencies listed in this table are synthesized by the external VCO and the built-in divider.

DTMF Dial Digit Register – R13(read/write):

The DTMF tone is sent out through the TONE pin by programming R13 in accordance with Table 2:

bit 3	bit 2	bit 1	bit 0	DTMF tone ($\overline{SINGLE}$ = 1)	Single tone ($\overline{SINGLE}$ = 0)
0	0	0	1	1	R1
0	0	1	0	2	C2
0	0	1	1	3	R1
0	1	0	0	4	C1
0	1	0	1	5	R2
0	1	1	0	6	C3
0	1	1	1	7	R3
1	0	0	0	8	R3
1	0	0	1	9	R3
1	0	1	0	0	R4
1	0	1	1	*	R4
1	1	0	0	#	R4
1	1	0	1	inhibited	inhibited
1	1	1	0	inhibited	inhibited
1	1	1	1	inhibited	inhibited
0	0	0	0	reset	reset

Table 2

	Frequency (Hz)	Deviation (%)
R1	695.65	–0.19
R2	771.08	+0.14
R3	853.33	+0.16
R4	941.18	+0.02
C1	1212.12	+0.26
C2	1333.33	+0.20
C3	1481.48	+0.3

If the $\overline{\text{REAL-TONE}}$ pin is pulled low, the tone signal will be output continuously. Otherwise, the tone output will be of minimum tone duration, t_{MFD}, and will automatically follow an interdigit pause, t_{IDP}. t_{MFD} and t_{IDP} are 101 ms in duration. R13 will reset to 0000 once the tone signal is sent out, and can only be written after cleared to zero.

Ringer and Key-in Tone Register – R14(Write-only):

Bit 3	Bit 2	Bit 1	Bit 0
—	high freq. pair/ low freq. pair	ringer output enable	key-in tone output enable

When bit 0 is set to 1, an 1185 Hz Key-in tone is sent out from the KIT pin for t_{MFD}, the minimum tone duration. If bit 0 is set repeatedly with a period less than 101 ms, the Key-in tone will be sent out continuously. Bit 0 will automatically reset to 0 once the Key-in tone has been sent out.

The ringer will be inhibited if bit 1 is reset to 0. When bit 1 is sent to 1, UM9310 will output a ringer signal if R15 contains a non-zero value. The time duration of ringing equals 270 ms times the content of R15.

The ringer signal consists of two different frequency pairs. For each pair, there are two different frequencies sent with a change rate of 19.75 Hz. The selection of frequency pair is determined by bit 2 of R14 and is described in Table 3.

Bit 2	Ringing Frequency (Hz)
0 (high air)	1896/2370
1 (low pair)	474/592.5

Ringer Time Register – R15(read/write):

The time duration for ringing can be preset by programming R15, the ringer timer. R15 will count down at a rate of about 3.7 Hz. The RINGERP and RINGERN pins will output ringer signals with the time duration determined by R15. R15 will automatically count down to zero during ringing. When R15 counts down to zero, the ringer stops. It is necessary to reload R15 with a non-zero value for another ringing.

Absolute Maximum Ratings*

Power Supply Voltage 5.5V
Input Voltage 5.8V
Maximum power dissipation . . . . . 500 mW
Operating temperature . . . . . 0°C to 70°C
Storage temperature . . . . . –55°C to 150°C
Lead temperature . . . . . 256°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{DD} = 3.3V, T_{OP} = 25°C, unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	Operating Voltage	3.3		5.5	V	
I_{OP}	Operating Current			1.5	mA	Receive only, Outputs unloaded
I_{STB}	Standby Current		3.0	5.0	μA	(1) chip reset (2) oscillator off
V_{IH}	Input High Voltage	0.8 V_{DD}	V_{DD}	V_{DD} +0.3		1 input
V_{IL}	Input Low Voltage	V_{SS}–0.3	V_{SS}	0.2 V_{DD}		0 input
I_{OL}	Output Sink Current	0.8			mA	V_{OL} = 0.5V
I_{OH}	Output Source Current	0.8			mA	V_{OH} = 2.8V
ZOUT	FSKOUT		5.0k		ohm	
	FDOUT		15.0k		ohm	
	Tone		3.0k		ohm	
	TXNRZ		10.0k		ohm	
Vref	EYEIN Pin Comparator Reference Voltage	0.625 V_{DD}			volt	
Cin	Input Capacitance			10.0	pF	
Cout	Output Capacitance			10.0	pF	
V_{OC}	Column Tone Output Amplitude	680	740	800	mV_{P-P}	V_{DD} = 2.5V R_{LOAD} = 10 KΩ
V_{OR}	Row Tone Output Amplitude	515	560	605	mV_{P-P}	V_{DD} = 2.5V R_{LOAD} = 10 KΩ
DIS %	Distortion		1	5	%	See Note
V_{VRC}	Valley of single row/ column Tone output		1.4		V	V_{DD} = 2.5V R_{LOAD} = 10 KΩ

Note: $DIS\% = \frac{100 \times (V_1^2 + V_2^2 + \ldots + V_n^2)^{1/2}}{(V_{IL}^2 + V_{IH}^2)^{1/2}}$

a. $V_1, \ldots V_n$ is the intermodulation or the harmonic frequency in 500 Hz to 3400 Hz band

b. V_{IL}, V_{IH} are the individual frequency components of the DTMF signal.

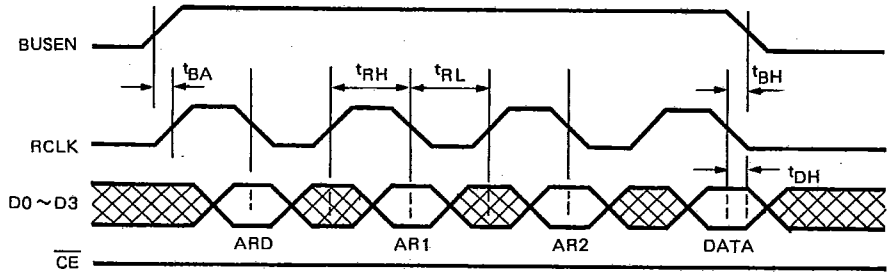
AC Electrical Characteristics (V_{DD} = 3.3V, T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
	RXVCO, TXVCO Pins Input Clock Rate			50.0	MHz	V_{P-P} > 0.3V
t_{BA}	Lead Time for Bus Enable Before Access	25			ns	
t_{BH}	Hold Time for Bus Enable After Access	25			ns	
t_{RH}	RCLK Clock High Duration	400			ns	
t_{RL}	RCLK Clock Low Duration	600			ns	
t_{DS}	Data Set Up Time	25			ns	
t_{MFD}	Minimum Tone Duration		101		ms	
t_{IDP}	Minimum Interdigit Pause		101		ns	
t_{DH}	Data Hold Time	0			ns	

Timing Waveform

(1) In order to operate properly as described previously for UM9310, the data access of internal registers and/or external SRAM should be programmed in accordance with the timing waveforms shown in Fig. 1.

(a) Microcontroller READ/WRITE data FROM/TO register:

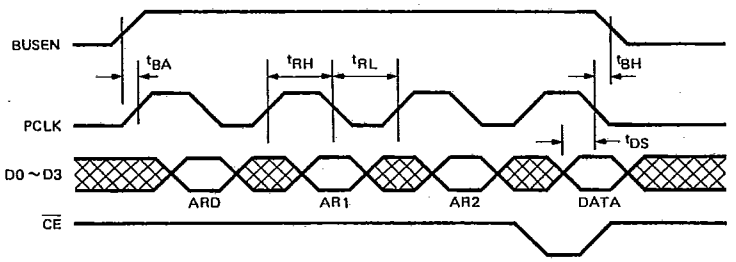


Note:

	BIT 3	BIT 2	BIT 1	BIT 0	
AR0	$\overline{WE}$	RSEL	–	–	RSEL = "1" = V_{DD}
AR1	–	–	–	–	$\overline{WE}$ = "0" (WRITE)
AR2	A3	A2	A1	A0	= "1" (READ)
DATA	D3	D2	D1	D0	

Figure 1(a)

(b) Microcontroller WRITEs to SRAM



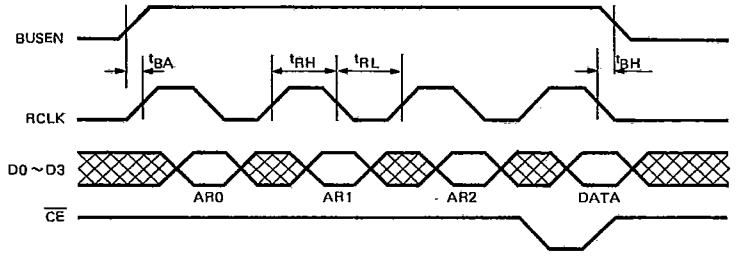
Note:
(1)

	BIT 3	BIT 2	BIT 1	BIT 0	
AR0	$\overline{WE}$	RSEL	A9	A8	RSEL = "0"
AR1	A7	A6	A5	A4	$\overline{WE}$ = "0" (WRITE)
AR2	A3	A2	A1	A0	
DATA	D3	D2	D1	D0	

(2) The SRAM interface timing is according to UM6104.

Figure 1(b)

(c) Microcontroller READs data from SRAM

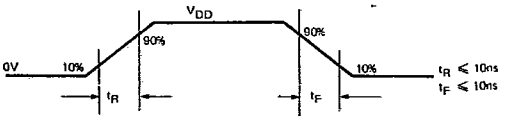


Note:

	BIT 3	BIT 2	BIT 1	BIT 0	
AR0	$\overline{WE}$	RSEL	A9	A8	RSEL = "0"
AR1	A7	A6	A5	A4	$\overline{WE}$ = "1" (READ)
AR2	A3	A2	A1	A0	
DATA	D3	D2	D1	D0	

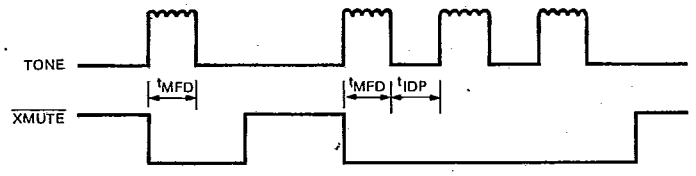
Figure 1(c)

Note: 1. Input Waveform limitations:



2. The address and/or data are latched at the falling edge of RCLK.

(2) The timing relation of TONE and $\overline{XMUTE}$ output is plotted in the following diagram.



Application Circuit

The application circuits are plotted in Figure-2, 3. Figure-2 is the overall block diagram for practical application. However, Figure-3 only contains part of the implementation circuit of Figure-2.

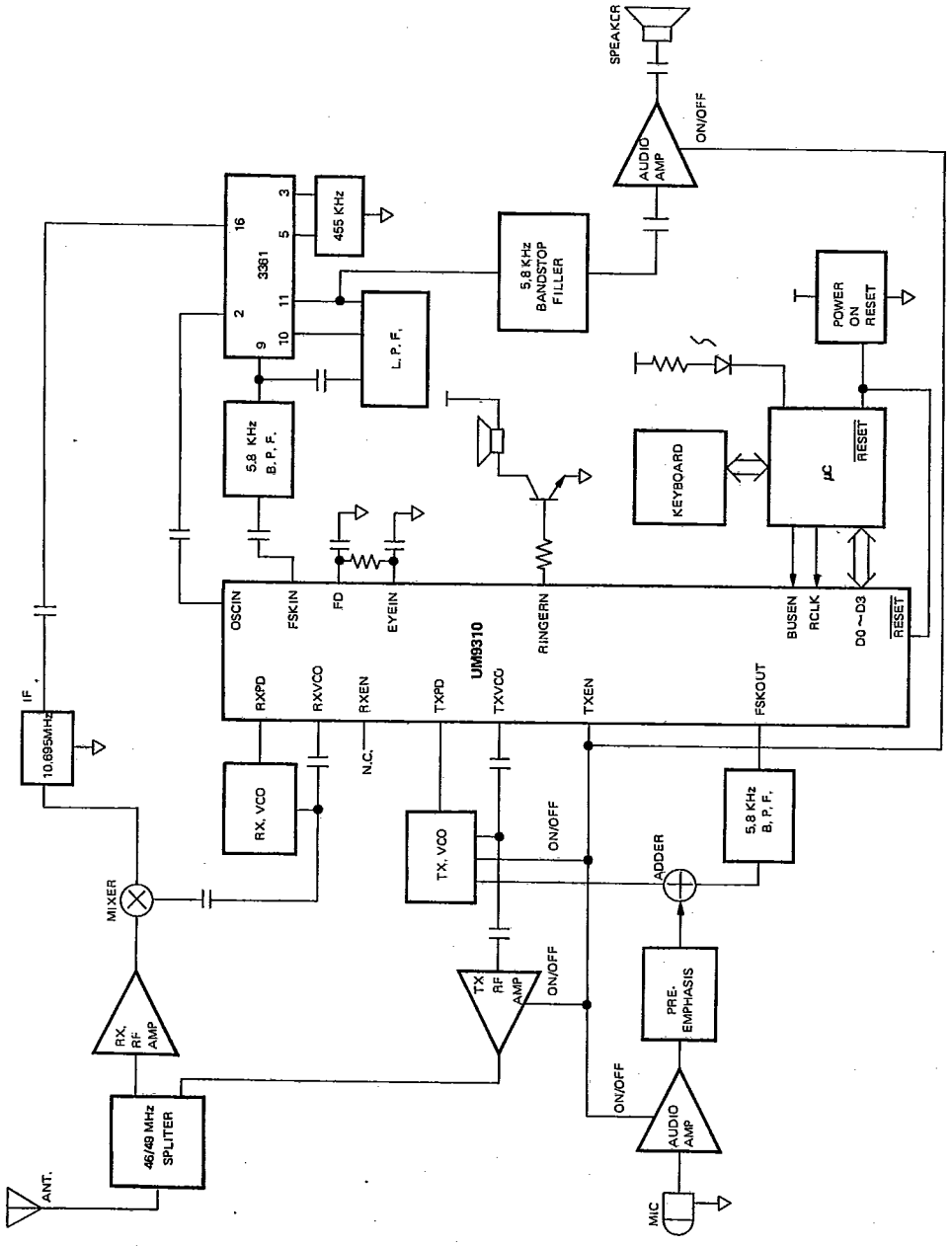


Figure-2(a) Block Diagram of the Cordless Telephone for Handset Unit

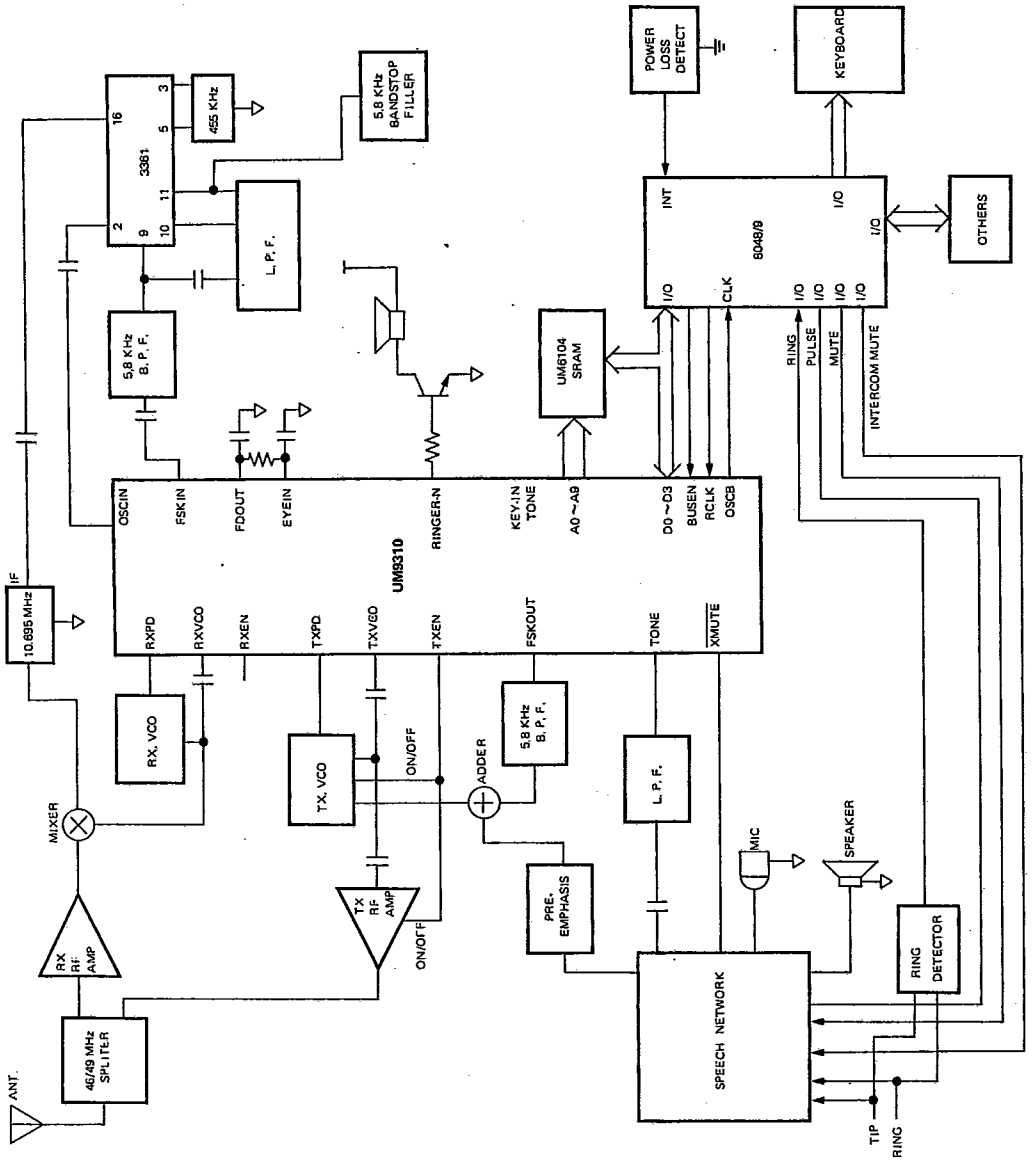


Figure-2(b) Block Diagram of the Cordless Telephone for Base Unit

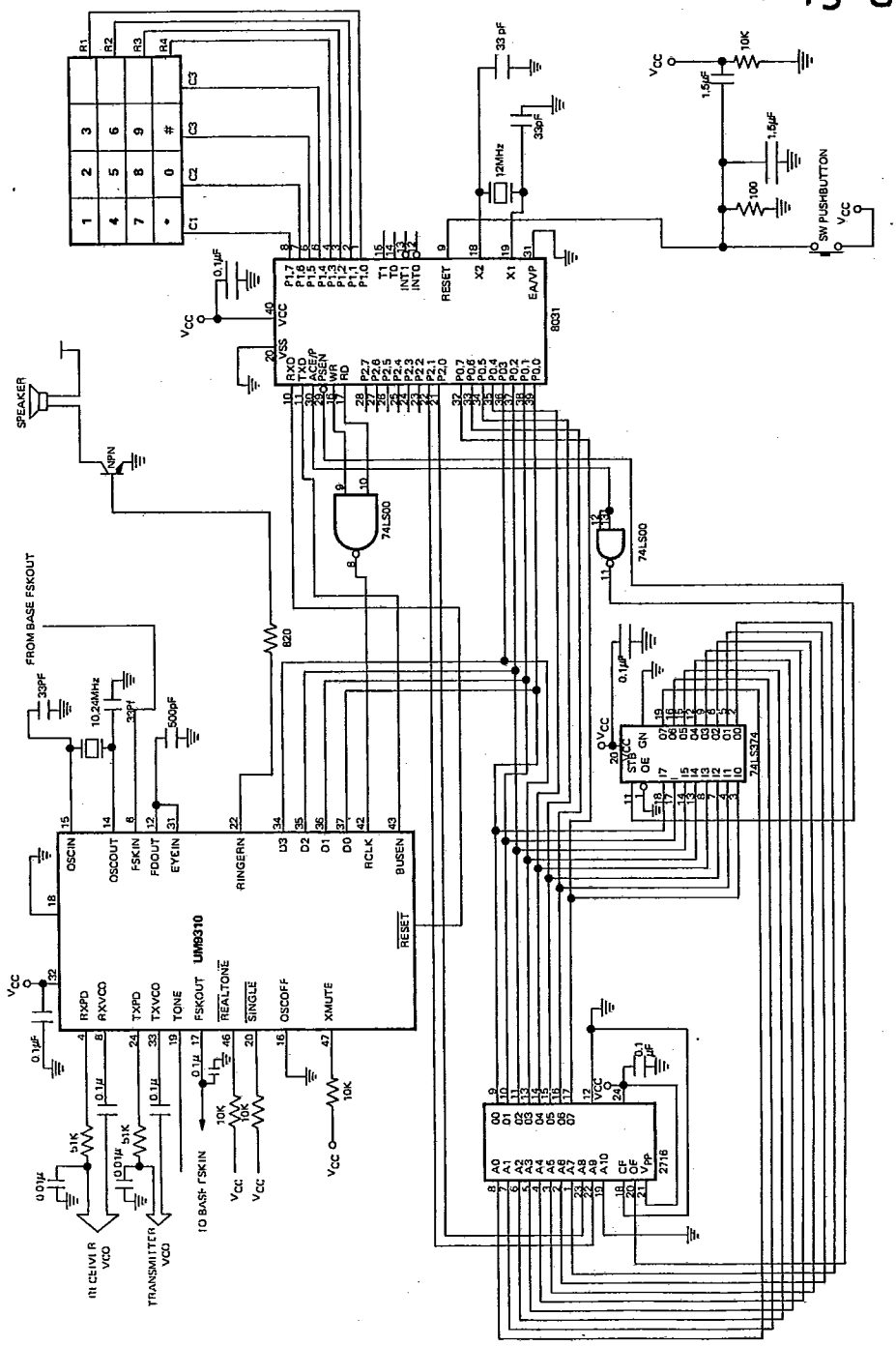


Figure-3(a) Implementation of Handset Unit (contains only part of Figure-2(a))

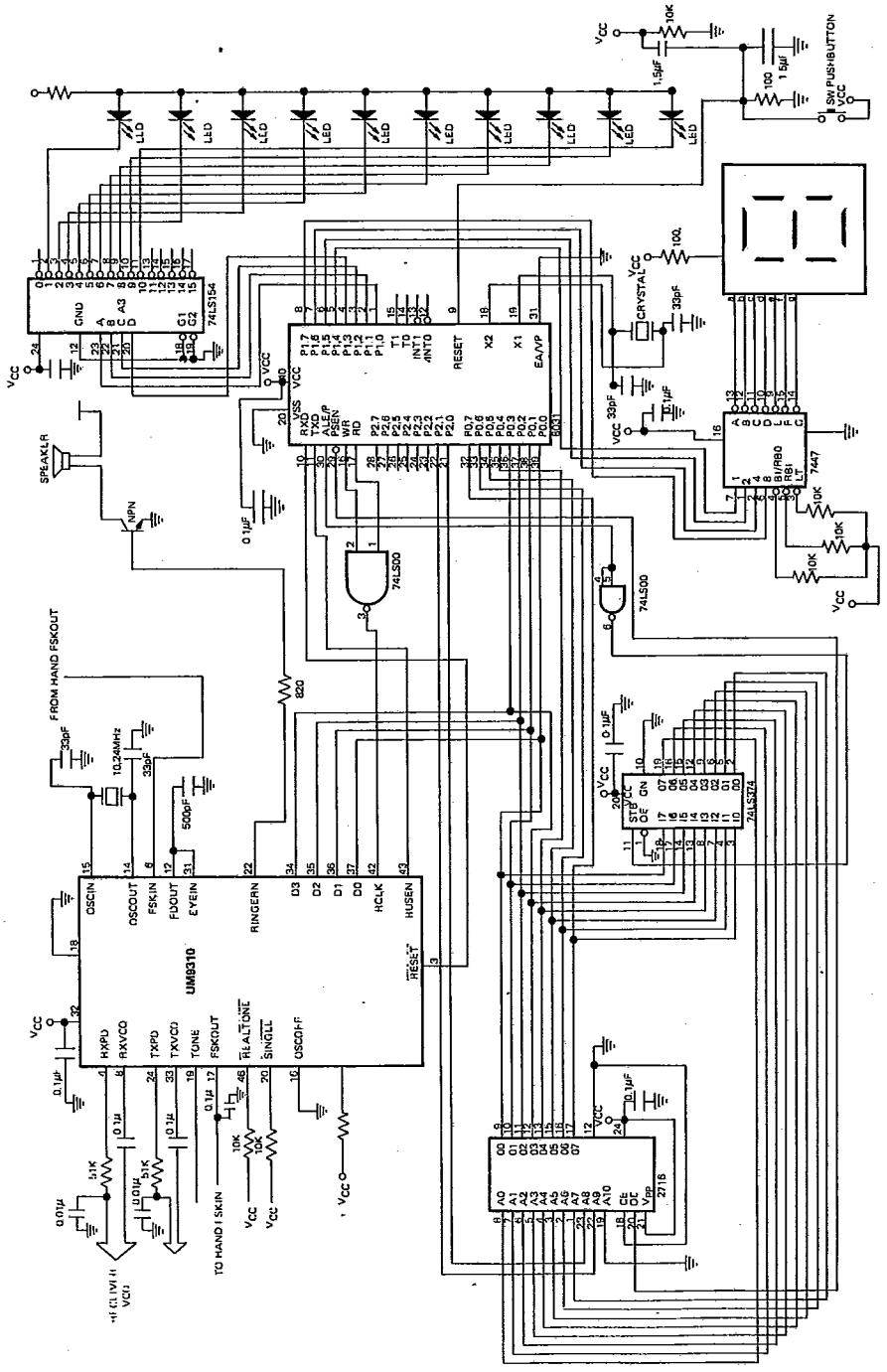


Figure-3(b) Implementation of Base Unit (contains only part of Figure-2(b))

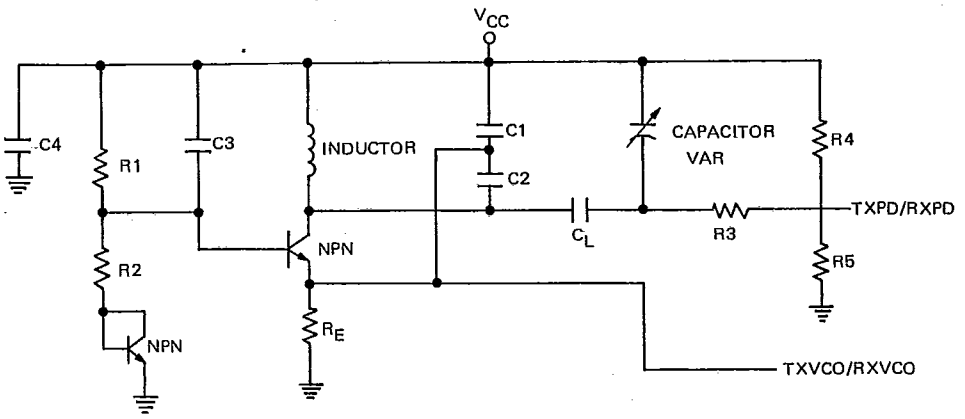


Figure-3(C) Implementation of The VCO circuit