

To all our customers

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Renesas Technology Corp.  
Customer Support Dept.  
April 1, 2003

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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# H7N0307AB

Silicon N Channel MOS FET  
High Speed Power Switching

**RENESAS**

ADE-208-1568A (Z)

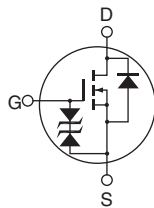
2nd. Edition  
Aug. 2002

## Features

- Low on-resistance
- $R_{DS(on)} = 4.6 \text{ m}\Omega$  typ.
- Low drive current
- 4.5 V gate drive device can be driven from 5 V source

## Outline

TO-220AB



1. Gate
2. Drain  
(Frangle)
3. Source

## Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	30	V
Gate to source voltage	$V_{GSS}$	±20	V
Drain current	$I_D$	60	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	240	A
Body-drain diode reverse drain current	$I_{DR}$	60	A
Channel dissipation	Pch <sup>Note 2</sup>	90	W
Channel to Case Thermal Impedance	$\theta_{ch-c}$	1.39	°C/W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1.  $PW \leq 10 \mu s$ , duty cycle  $\leq 1\%$

2. Value at Tc = 25°C

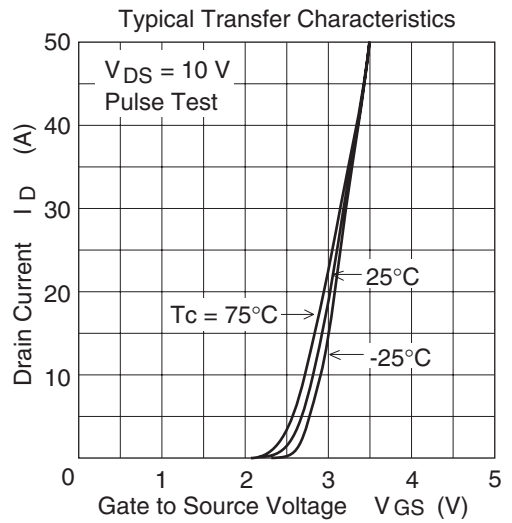
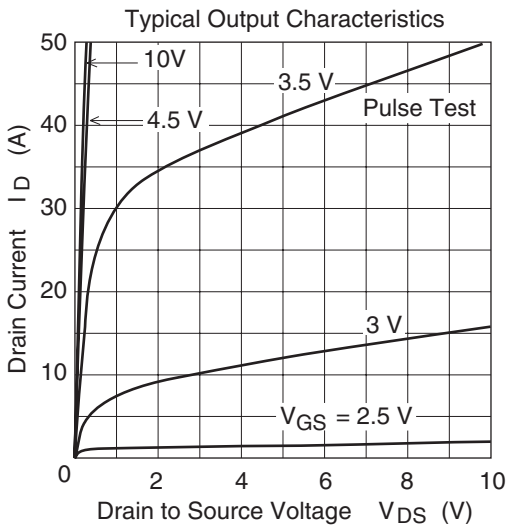
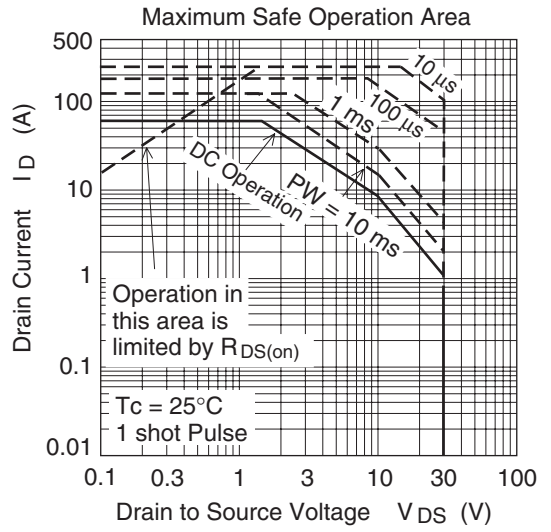
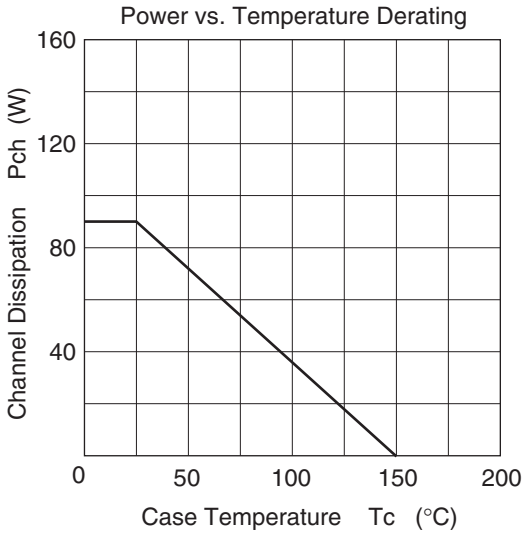
## Electrical Characteristics

(Ta = 25°C)

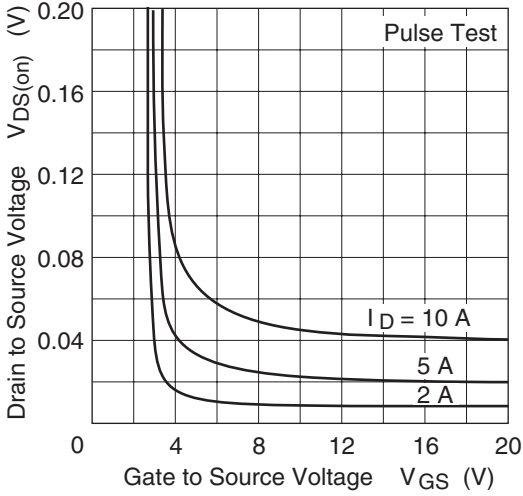
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—		$I_G = \pm 100 \text{ } \mu\text{A}$ , $V_{DS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	μA	$V_{DS} = 30 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$ , $V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Static drain to source on state resistance	$R_{DS(on)}$	—	4.6	5.8	mΩ	$I_D = 30 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note 1</sup>
		—	8.0	11.5	mΩ	$I_D = 30 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note 1</sup>
Forward transfer admittance	$ y_{fs} $	40	65	—	S	$I_D = 30 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note 1</sup>
Input capacitance	Ciss	—	2500	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	650	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	350	—	pF	f = 1 MHz
Total gate charge	Qg	—	40	—	nc	$V_{DD} = 10 \text{ V}$
Gate to source charge	Qgs	—	7	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	8	—	nc	$I_D = 60 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 30 \text{ A}$
Rise time	$t_r$	—	300	—	ns	$R_L = 0.33 \text{ } \Omega$
Turn-off delay time	$t_{d(off)}$	—	70	—	ns	$R_g = 4.7 \text{ } \Omega$
Fall time	$t_f$	—	20	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.92	—	V	$I_F = 60 \text{ A}$ , $V_{GS} = 0$
Body-drain diode reverse recovery time	$t_{rr}$	—	60	—	ns	$I_F = 60 \text{ A}$ , $V_{GS} = 0$ diF/ dt = 50 A/μs

Notes: 1. Pulse test

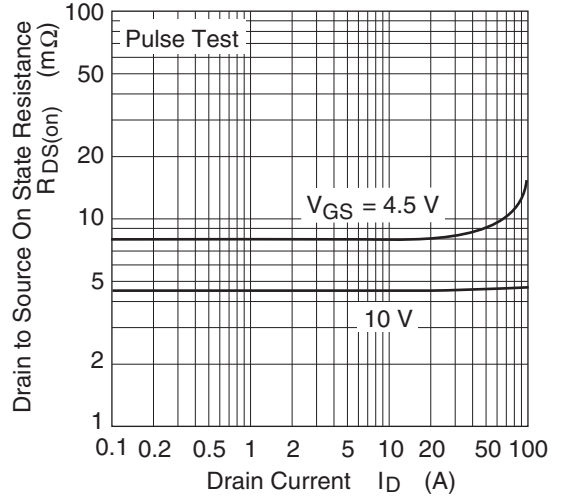
## Main Characteristics



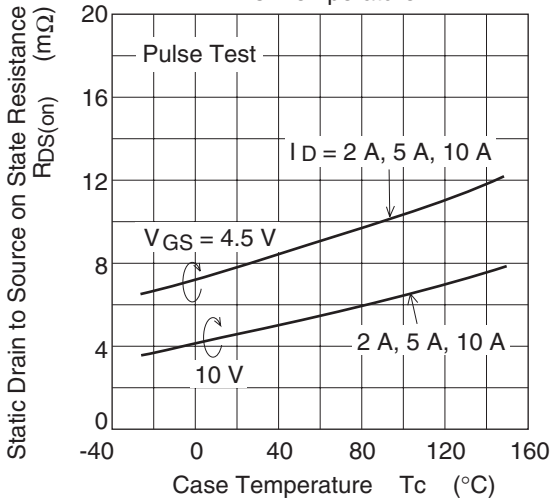
Drain to Source Saturation Voltage vs. Gate to Source Voltage



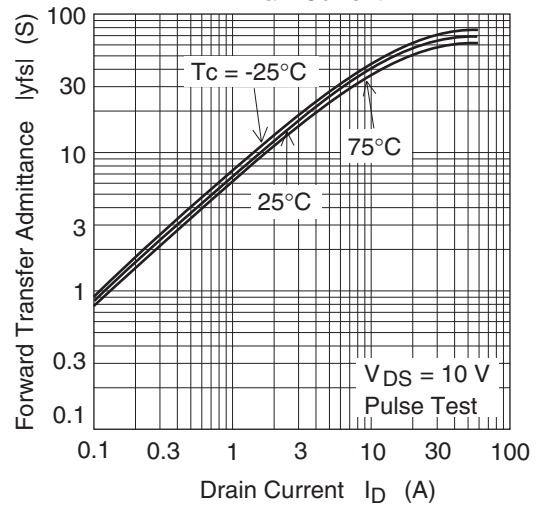
Static Drain to Source on State Resistance vs. Drain Current



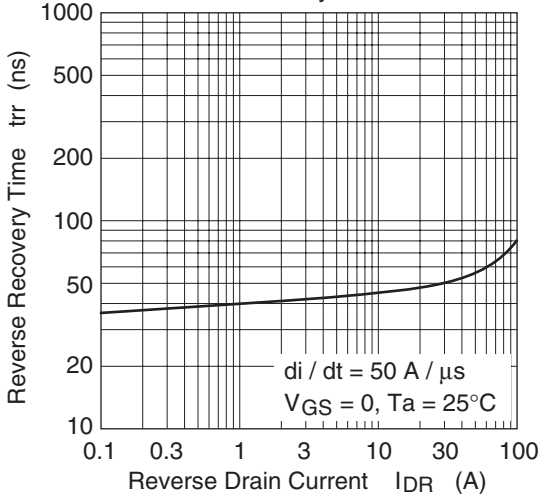
Static Drain to Source on State Resistance vs. Temperature



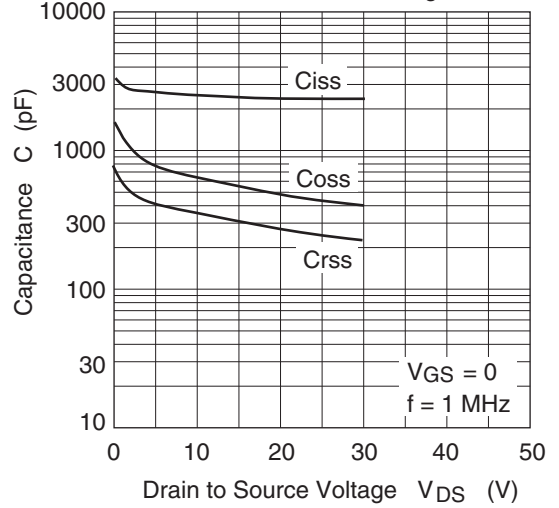
Forward Transfer Admittance vs. Drain Current



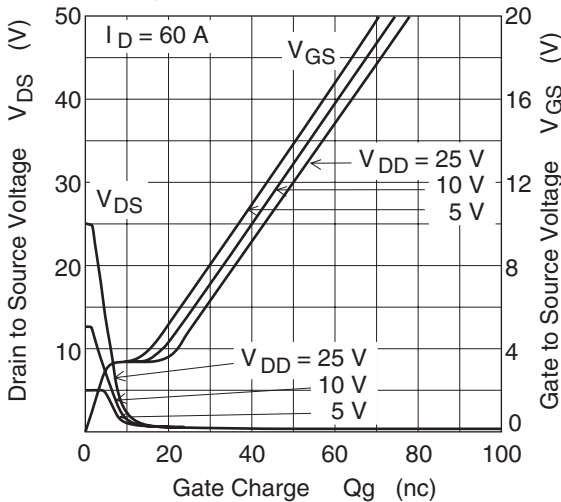
Body-Drain Diode Reverse Recovery Time



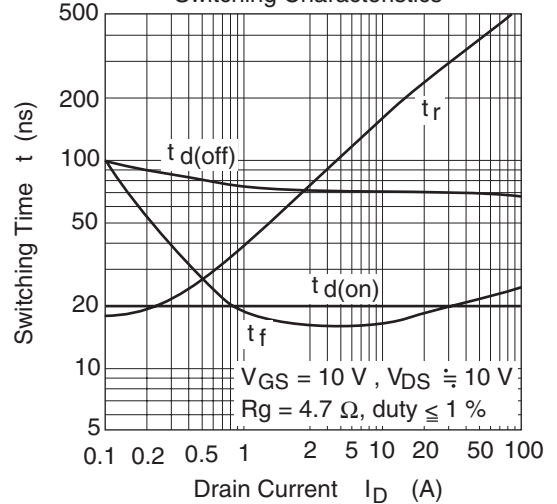
Typical Capacitance vs. Drain to Source Voltage



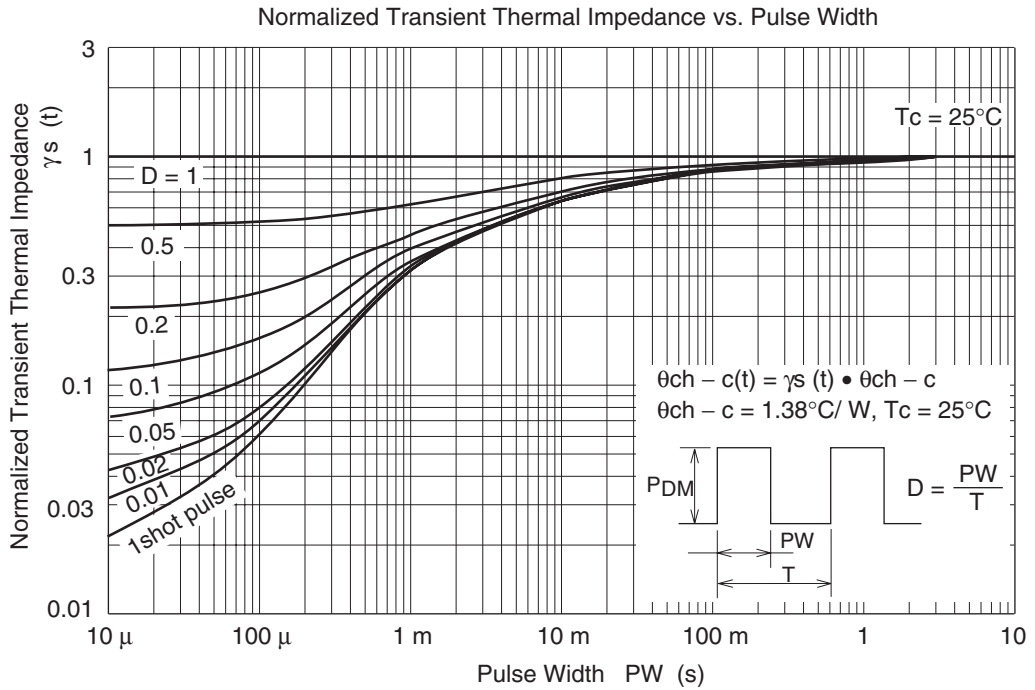
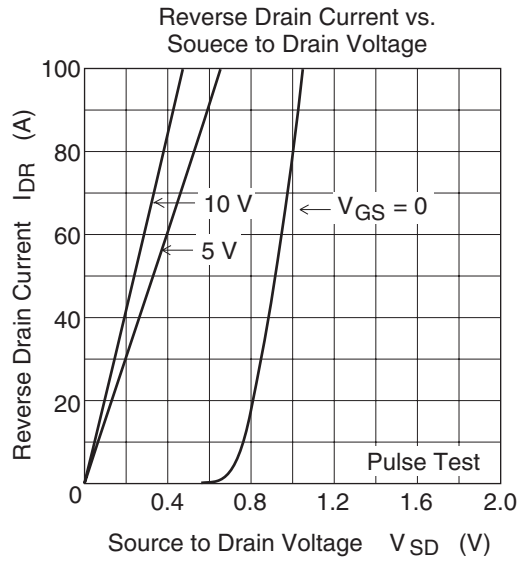
Dynamic Input Characteristics



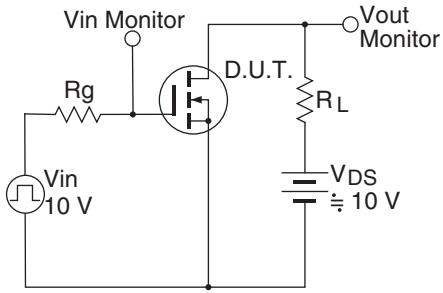
Switching Characteristics



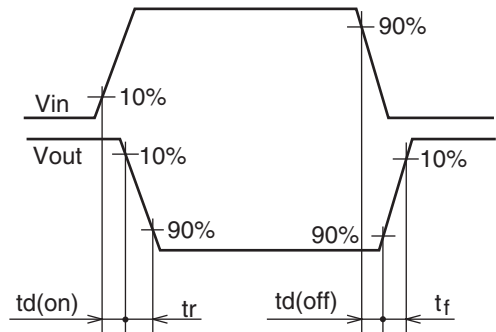




### Switching Time Test Circuit

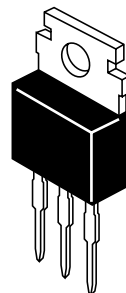
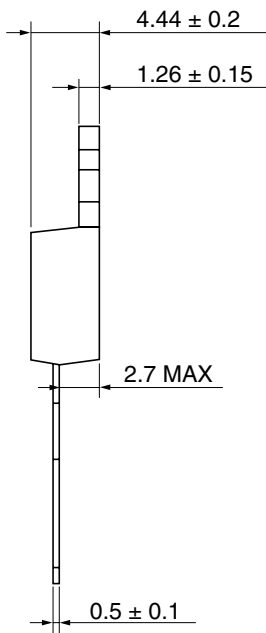
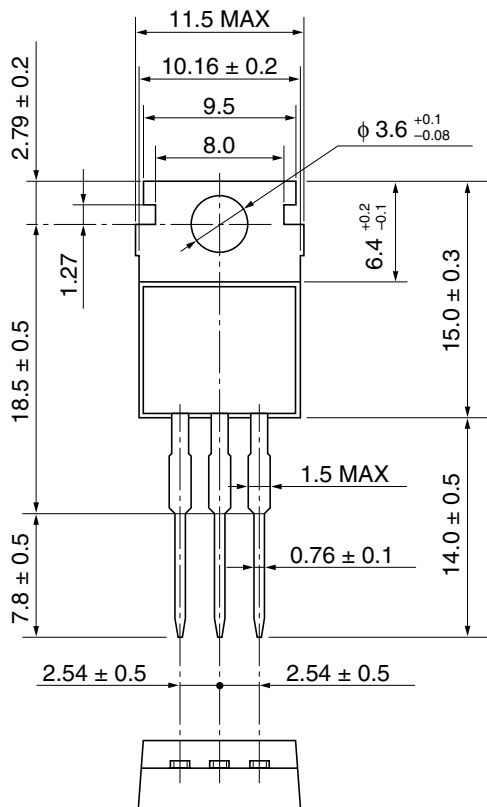


### Switching Time Waveform



Package Dimensions

As of January, 2002  
Unit: mm



Hitachi Code	TO-220AB
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	1.8 g

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