

SP8916 (MP)

5GHZ ÷**16 Fixed Modulus Divider**Preliminary Information

Ordering Information

DS4361 Issue 1.2 September 1999

The SP8916 is one of a range of very high speed low power prescalers for professional applications. The dividing elements are static D type flip flops and therefore allow operation down to DC if the drive signal is a pulse waveform with fast risetime. The output stage has internal 100 ohm pull up resistors, giving a 0.5V p-p output. If required, an external 100 ohm can be connected in parallel to give a 50 ohm output.

SP8916/KG/MP1S (tubes)

SP8916/KG/MP1T (tape and reel)

Absolute Maximum Ratings

Supply voltage, V_{CC} 6.5V Storage temperature -65°C to $+150^{\circ}\text{C}$ Maximum junction temperature $+150^{\circ}\text{C}$ Prescaler input voltage 2.5Vp-p Operating temperature $+35^{\circ}\text{C}$ T_{CASE}

Features

- Very High Operating Speed
- Operation down to DC with Square Wave Input
- Silicon Technology for Low Phase Noise (Typically better than -140dBc/Hz at 1KHz)
- 5V Single Supply Operation
- Low Power Dissipation: 340mW (Typ.)
- Surface Mount Plastic Package

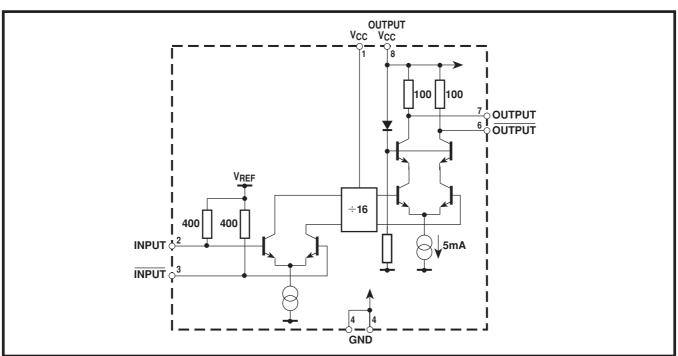


Figure 1 block diagram

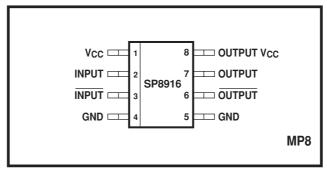


Figure 2 Pin connections - top view

Electrical Characteristics

These characteristics are guaranteed by either production test or design over the following range of operating conditions unless otherwise stated: $T_{AMB} = -40^{\circ}C$ to $+85^{\circ}C$, $V_{CC} = 4.75V$ to 5.25V

	Pin	Value					
Characteristic		Min.	Тур.	Max.	Units	Conditions	
Supply current	1, 8	-	68	92	mA		
Input frequency	2, 3	1.0	-	5∙0	GHz	RMS sinewave	
Input sensitivity	2, 3	-	-	180	mVrms	f _{IN} = 1GHz and 4.2GHz	
Input sensitivity	2, 3	-	-	570	mVrms	f _{IN} = 5GHz	
Input overload	2, 3	440	-	-	mVrms	f _{IN} = 1GHz and 3GHz	
Input overload	2, 3	700	-	-	mVrms	$f_{IN} = 5.0GHz$ and 3.8GHz	
Output voltage	6, 7	-	0.25	-	Vp-р	Into 100Ω pullup resistor	
Output power	6, 7	−18·0	-9∙0	-4·0	dBm	f _{IN} = 1GHz and 5GHz (see note 1)	

NOTE

^{1.} Measured into 50Ω measuring instrument in parallel with 100Ω pullup resistor. See Figure 5.

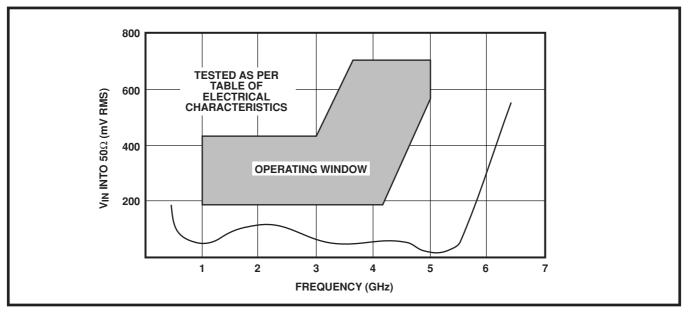


Figure 3 Typical input sensitiviy (sinewave drive)

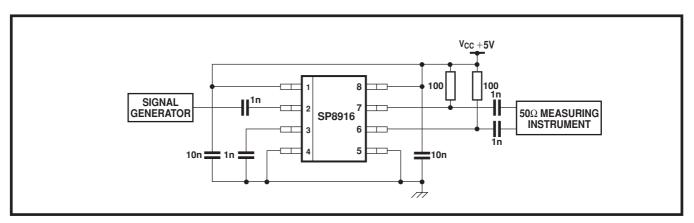


Figure 4 Typical application and test circuit

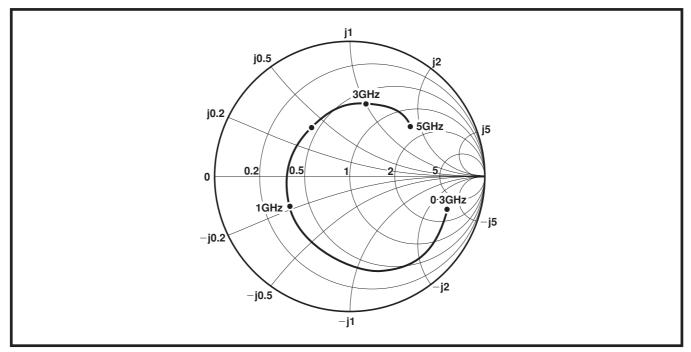


Figure 5 Typical input impedance

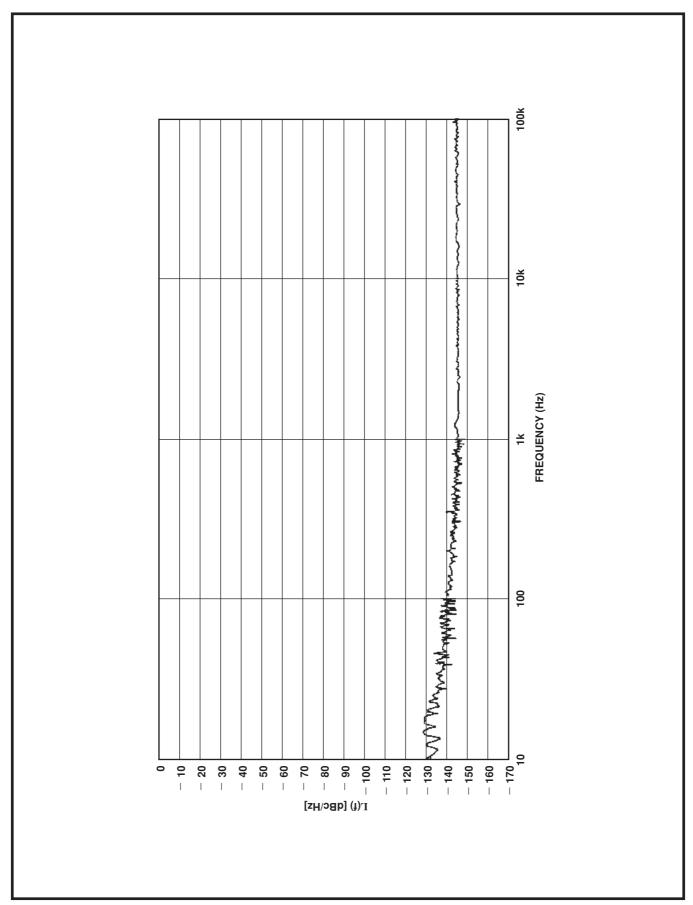
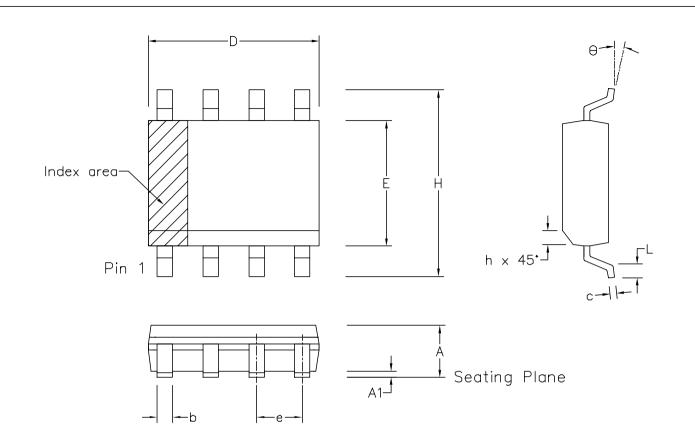


Figure 6 Typical phase noise, input frequency = 3GHz



	Min	Max	Min	Max	
	mm	mm	inch	inch	
A	1.35	1.75	0.053	0.069	
A1	0.10	0.25	0.004	0.010	
D	4.80	5.00	0.189	0.197	
Н	5.80	6.20	0.228	0.244	
E	3.80	4.00	0.150	0.157	
L	0.40	1.27	0.016	0.050	
е	1.27	BSC	0.050 BSC		
b	0.33	0.51	0.013	0.020	
С	0.19	0.25	0.008	0.010	
0	0 º	8°	0°	84	
h	0.25	0.50	0.010	0.020	
h	0.25		0.010 eatures	0.020	
h N	0.25	Pin Fe	eatures	0.020 3	

Notes:

- 1. The chamfer on the body is optional. If it not present, a visual index feature, e.g. a dot, must be located within the cross—hatched area.
- 2. Controlling dimension are in inches.

- 3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
 4. Dimension E1 do not include inter—lead flash or protusion. These shall not exceed 0.010" per side.
 5. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ISSUE	1	2	3	4			SEMICONDUCTOR	Title: Package Outline Drawing for 8 Ids SOIC(N)-0.150" Body Width (MP)
ACN	006745	201936	202595	203705		MITEL		8 Ids SOIC(N)-0.150 Body Width (MP)
DATE	5APR95	27FEB97	12JUN97	9DEC97				Drawing Number
APPROVED								GPD00010



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