Z8001®/Z8002® Military Z8000® CPU Central Processing Unit

T-49-17-07

Zilog

Military Electrical Specification

September 1988

FEATURES

- Regular, easy-to-use architecture
- Instruction set more powerful than many minicomputers
- Directly addresses 8 Mbytes
- Eight user-selectable addressing modes
- Seven data types that range from bits to 32-bit long words and byte and word strings
- System and Normal operating modes
- Separate code, data, and stack spaces
- Sophisticated interrupt structure
- Resource-shaping capabilities for multiprocessing systems
- Multi-programming support
- Compiler support
- Memory management and protection provided by Z8010™ Memory Management Unit
- 32-bit operations, including signed multiply and divide
- Z-BUS® compatible
- 4, 6, and 10 MHz clock rate

GENERAL DESCRIPTION

The Z8000 is an advanced high-end 16-bit microprocessor that spans a wide variety of applications ranging from simple stand-alone computers to complex parallel-processing systems. Essentially a monolithic minicomputer central processing unit, the Z8000 CPU is characterized by an instruction set more powerful than many minicomputers; abundant resources in registers, data types, addressing modes and addressing range, and a regular architecture that enhances throughput by avoiding critical bottlenecks such as implied or dedicated registers.

CPU resources include sixteen 16-bit general-purpose registers, seven data types that range from bits to 32-bit long words and byte and word strings, and eight user-selectable addressing modes. The 110 distinct instruction types can be combined with the various data types and addressing modes to form a powerful set of 414 instructions. Moreover, the instruction set is regular; most instructions can use any of the five main addressing modes and can operate on byte, word, and long-word data types.

The CPU can operate in either the system or normal mode. The distinction between these two modes permits privileged operations, thereby improving operating system organization and implementation. Multiprogramming is supported by the "atomic" Test and Set instruction; multiprocessing by a combination of instruction and hardware features; and compilers by multiple stacks, special instructions, and addressing modes.

The Z8000 CPU is offered in two versions: the Z8001 segmented CPU and the Z8002 nonsegmented CPU. The main difference is in addressing range. The Z8001 can directly address 8 megabytes of memory; the Z8002 directly addresses 64 kilobytes. The two operating modes—system and normal— and the distinction between code,

data, and stack spaces within each mode allows memory extension up to 48 megabytes for the Z8001 and 384 kilobytes for the Z8002.

To meet the requirements of complex, memory-intensive applications, a companion memory-management device is offered for the Z8001. The Z8010 Memory Management Unit manages the large address space by providing features such as segment relocation and memory protection.

The Z8001 can be used with or without the Z8010. If used by itself, the Z8001 still provides an 8 megabyte direct addressing range, extendable to 48 megabytes.

The Z8001, Z8002, and Z8010 are fabricated with high-density, high-performance scaled n-channel silicon-gate depletion-load technology, and are housed in dual-in-line packages (DIPS) and leadless chip carriers (LCC).

Z8000 CPU TIMING

The Z8000 CPU executes instructions by stepping through sequences of basic machine cycles, such as memory read or write, I/O device read or write, interrupt acknowledge, and internal execution. Each of these basic cycles requires three to ten clock cycles to execute. Instructions that require more clock cycles to execute are broken up into several machine cycles. Thus no machine cycle is longer than ten clock cycles and fast response to a Bus Request is guaranteed.

The instruction opcode is fetched by a normal memory read operation. A memory refresh cycle can be inserted just after the completion of any first instruction fetch (IF_1) cycle and can also be inserted while the following instructions are being executed: MULT, MULTL, DIV, DIVL, HALT, all Shift instructions, all Block Move instructions, and the Multi-Micro Request instruction (MREQ).

The following timing diagrams show the relative timing relationships of all CPU signals during each of the basic operations. When a machine cycle requires additional clock cycles for CPU internal operation, one to five clock cycles are added. Memory and I/O read and write, as well as interrupt acknowledge cycles, can be extended by activating the $\overline{\text{WAIT}}$ input. For exact timing information, refer to the composite timing diagram.

Note that the $\overline{\text{WAIT}}$ input is not synchronized in the Z8000 and that the setup and hold times for $\overline{\text{WAIT}}$, relative to the clock, must be met. If asynchronous $\overline{\text{WAIT}}$ signals are generated, they must be synchronized with the CPU clock before entering the Z8000.

MEMORY READ AND WRITE

Memory read and instruction fetch cycles are identical, except for the status information on the ST_0-ST_3 outputs. During a memory read cycle, a 16-bit address is placed on the AD_0-AD_{15} outputs early in the first clock period, as shown in Figure 1. In the Z8001, the 7-bit segment number is output on SN_0-SN_6 one clock period earlier than the 16-bit address offset.)

A valid address is indicated by the rising edge of Address Strobe. Status and mode information become valid early in the memory access cycle and remain stable throughout. The state of the $\overline{WAIT}$ input is sampled in the middle of the second clock cycle by the falling edge of Clock. If $\overline{WAIT}$ is Low, an additional clock period is added between T_2 and T_3. $\overline{WAIT}$ is sampled again in the middle of this wait cycle, and additional wait states can be inserted: this allows interfacing slow memories. No control outputs change during wait states.

Although Z8000 memory is word organized, memory is addressed as bytes. All instructions are word-aligned, using even addresses. Within a 16-bit word, the most significant byte (D_8-D_{15}) is addressed by the low-order address (A_0 = Low), and the least significant byte (D_0-D_7) is addressed by the high-order address (A_0 = High).

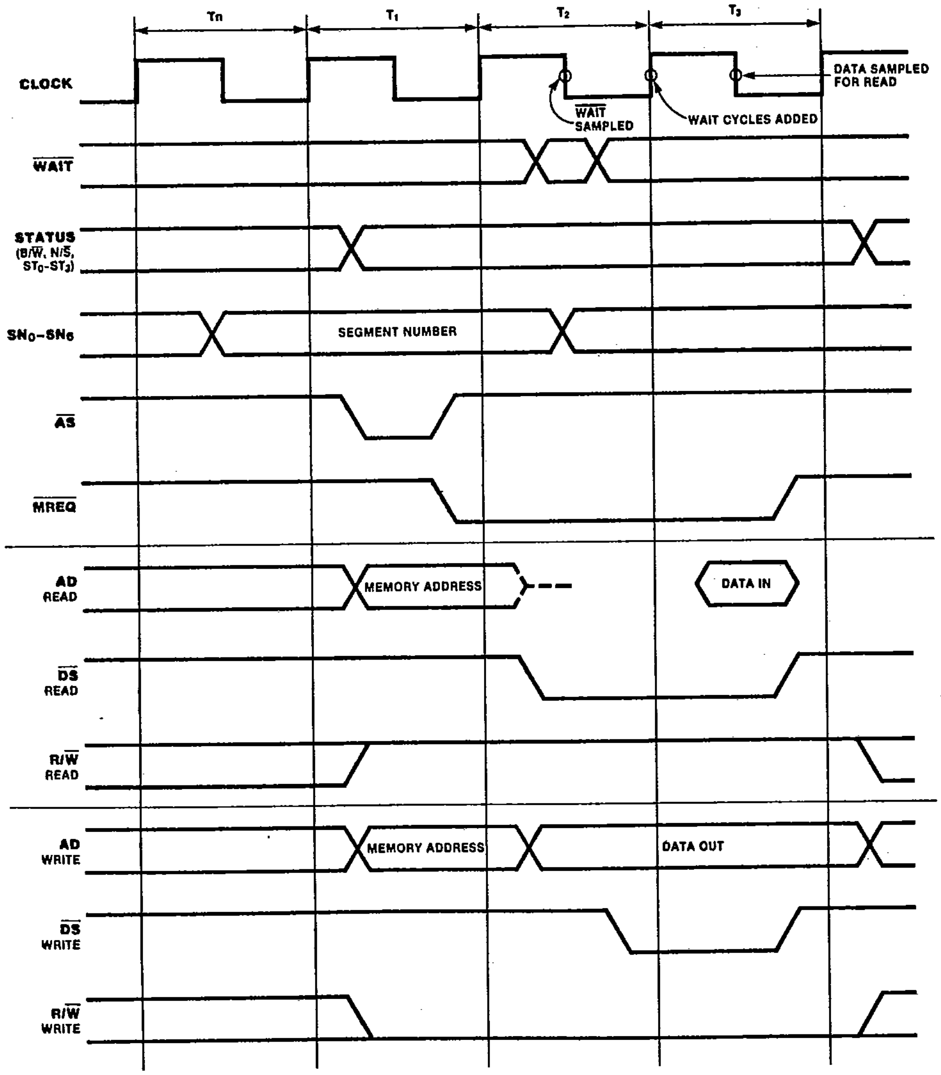

Figure 1. Memory Read and Write Timing

INPUT/OUTPUT

I/O timing is similar to memory read/write timing, except that one wait state is automatically (T_{WA}) inserted between T_2 and T_3 (Figure 2). Both the segmented Z8001 and the nonsegmented Z8002 use 16-bit I/O addresses.

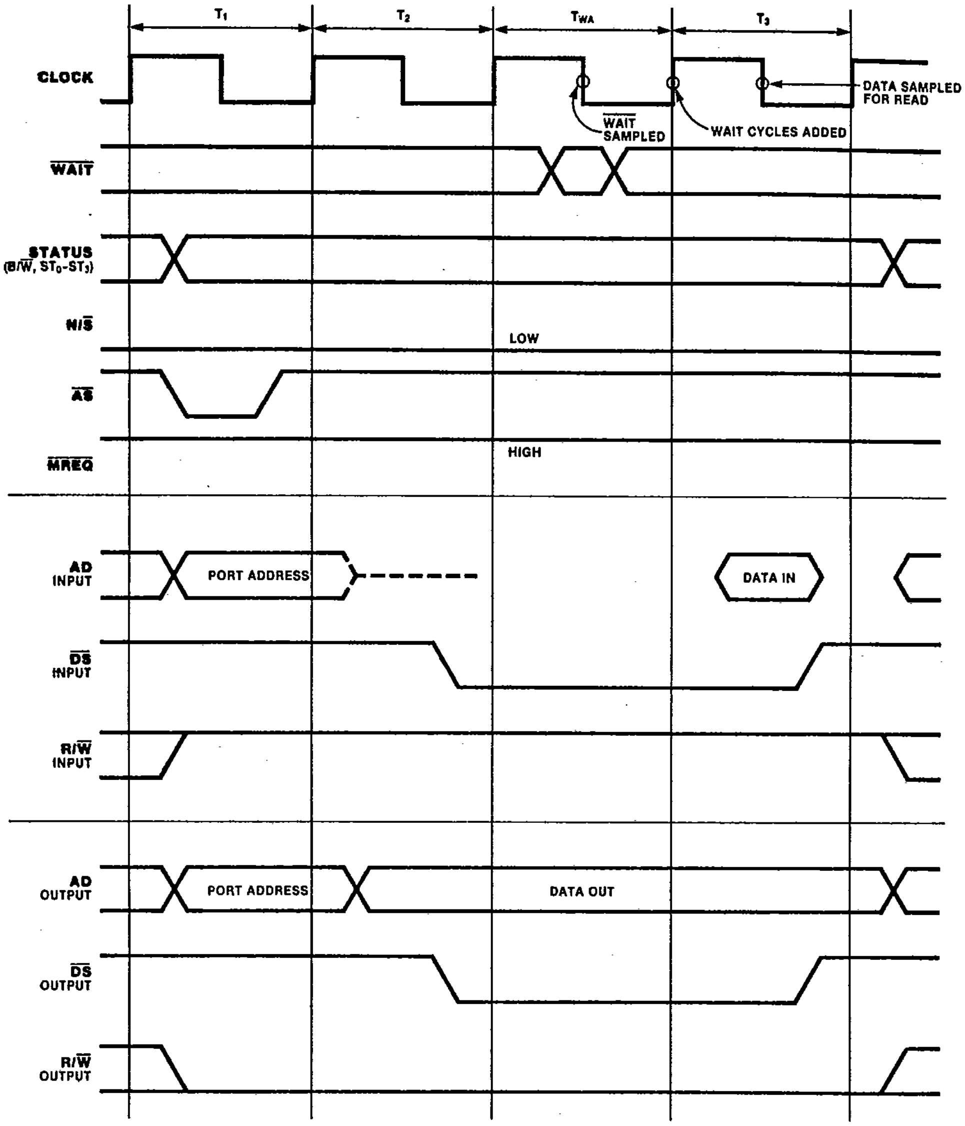

Figure 2. Input/Output Timing

INTERRUPT AND SEGMENT TRAP REQUEST AND ACKNOWLEDGE

The Z8000 CPU recognizes three interrupt inputs (non-maskable, vectored, and nonvectored) and a segmentation trap input. Any High-to-Low transition on the $\overline{NMI}$ input is asynchronously edge detected and sets the internal $\overline{NMI}$ latch. The $\overline{VI}$, $\overline{NVI}$, and $\overline{SEGT}$ inputs, as well as the state of the internal $\overline{NMI}$ latch, are sampled at the end of T_2 in the last machine cycle of any instruction.

In response to an interrupt or trap, the subsequent IF_1 cycle is exercised, but ignored. The internal state of the CPU is not altered and the instruction will be refetched and executed after the return from the interrupt routine. The program counter is not updated, but the system stack pointer is decremented in preparation for pushing starting information onto the system stack.

The next machine cycle is the interrupt acknowledge cycle. This cycle has five automatic wait states, with additional wait states possible, as shown in Figure 3.

After the last wait state, the CPU reads the information on AD_0-AD_{15} and temporarily stores it, to be saved on the stack later in the acknowledge sequence. This word identifies the source of the interrupt or trap. For the nonvectored and nonmaskable interrupts, all 16 bits can represent peripheral device status information. For the vectored interrupt, the low byte is the jump vector, and the high byte can be extra user status. For the segmentation trap, the *high* byte is the Memory Management Unit identifier and the *low* byte is undefined.

After the acknowledge cycle, the N/$\overline{S}$ output indicates the automatic change to system mode.

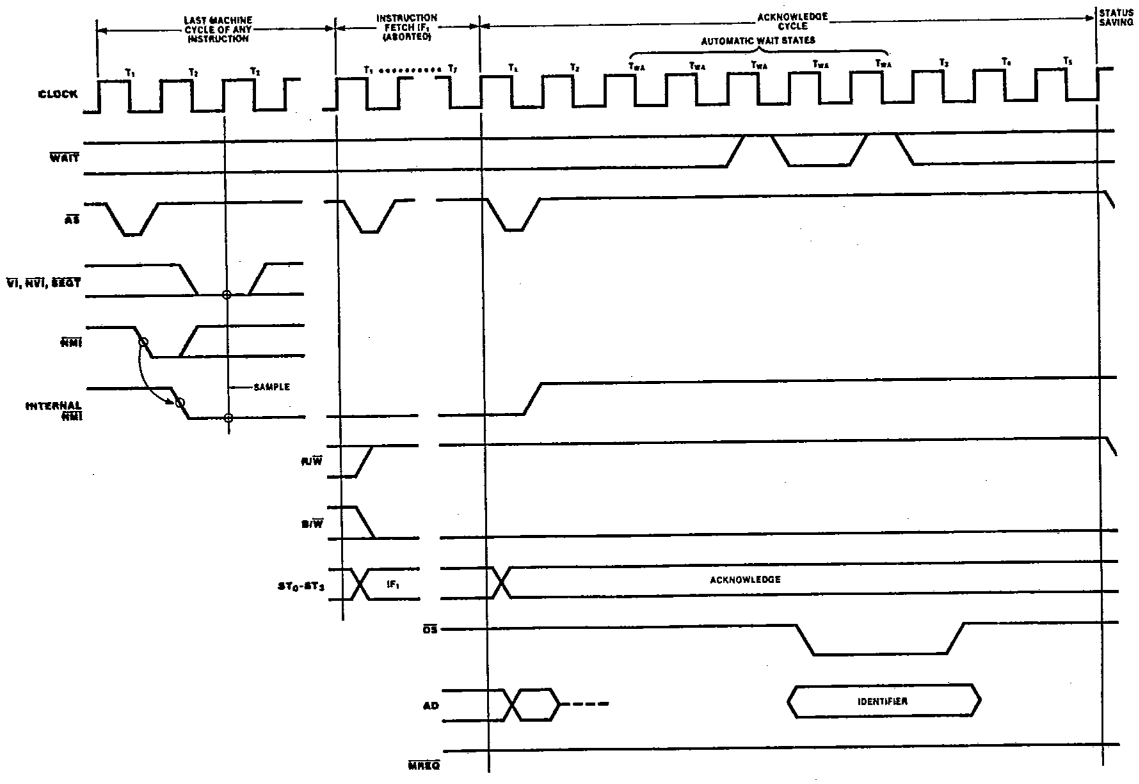

Figure 3. Interrupt and Segment Trap Request/Acknowledge Timing

STATUS SAVING SEQUENCE

The machine cycles, following the interrupt acknowledge or segmentation trap acknowledge cycle, push the old status information on the system stack in the following order: the 16-bit program counter; the 7-bit segment number (Z8001 only); the flag control word; and finally the interrupt/trap identifier. Subsequent machine cycles fetch the new program status from the program status area, and then branch to the interrupt/trap service routine.

BUS REQUEST ACKNOWLEDGE TIMING

A Low on the $\overline{BUSREQ}$ input indicates to the CPU that another device is requesting the Address/Data and control buses. The asynchronous $\overline{BUSREQ}$ input is synchronized at the beginning of any machine cycle (Figure 4). $\overline{BUSREQ}$ takes priority over $\overline{WAIT}$. If $\overline{BUSREQ}$ is Low, an internal synchronous $\overline{BUSREQ}$ signal is generated, which—after completion of the current machine cycle—causes the $\overline{BUSACK}$ output to go Low and all bus outputs to go into the high-impedance state. The requesting device—typically a DMA—can then control the bus.

When $\overline{BUSREQ}$ is released, it is synchronized with the rising clock edge; the $\overline{BUSACK}$ output goes High one clock period later, indicating that the CPU will again take control of the bus.

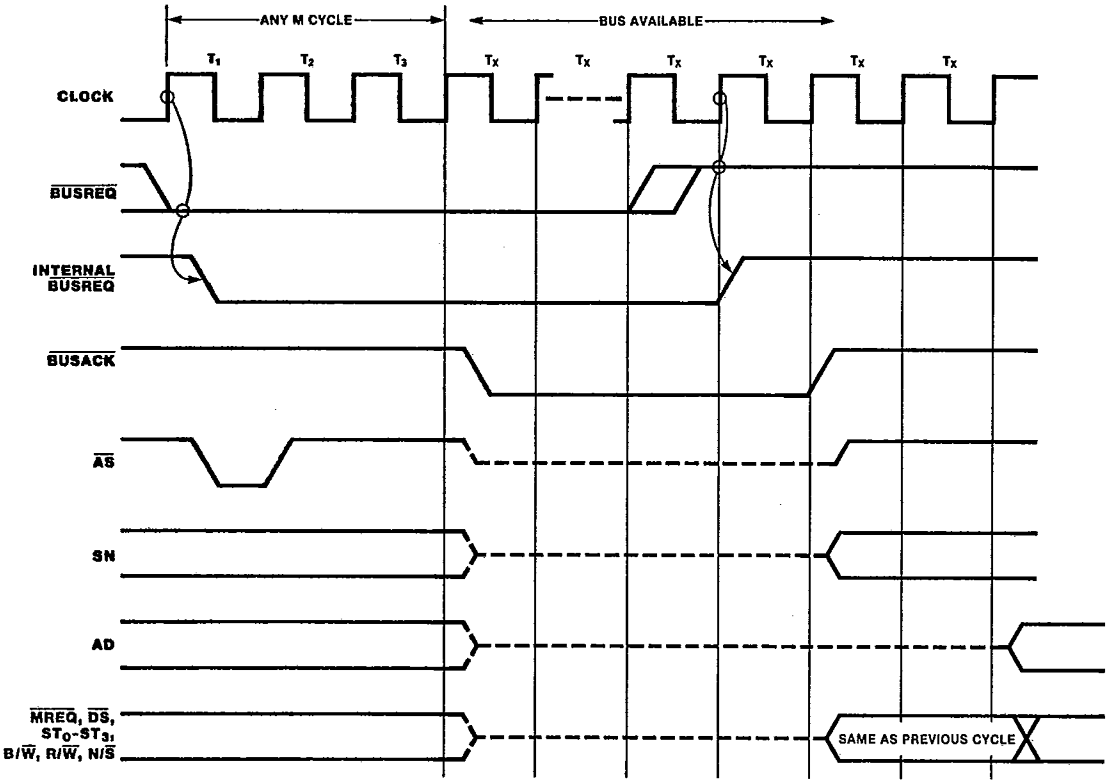

Figure 4. Bus Request/Acknowledge Timing

STOP

The $\overline{STOP}$ input is sampled by the last falling clock edge immediately preceding any IF_1 cycle (Figure 5) and before the second word of an EPA instruction is fetched. If $\overline{STOP}$ is found Low during the IF_1 cycle, a stream of memory refresh cycles is inserted after T_3, again sampling the $\overline{STOP}$ input on each falling clock edge in the middle of the T_3 states. During the EPA instruction, both EPA instruction words are fetched but any data transfer or subsequent instruction fetch is postponed until $\overline{STOP}$ is sampled High. This refresh operation does not use the refresh prescaler or its divide-by-four clock prescaler; rather, it double-increments the refresh counter every three clock cycles. When $\overline{STOP}$ is found High again, the next refresh cycle is completed, any remaining T states of the IF_1 cycle are then executed, and the CPU continues its operation.

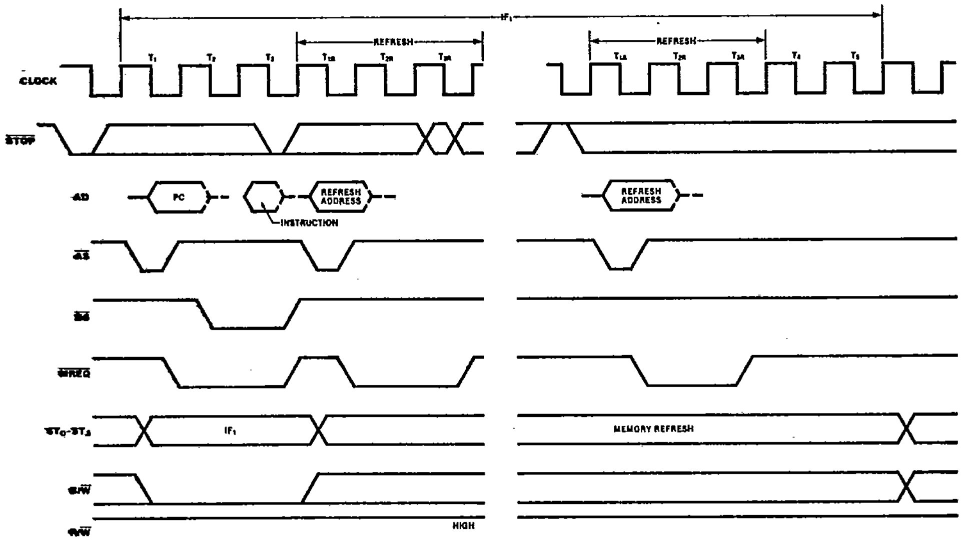

Figure 5. Stop Timing

INTERNAL OPERATION

Certain extended instructions, such as Multiply and Divide, and some special instructions need additional time for the execution of internal operations. In these cases, the CPU goes through a sequence of internal operation machine cycles, each of which is three to eight clock cycles long (Figure 6). This allows fast response to Bus Request and Refresh Request, because bus request or refresh cycles can be inserted at the end of any internal machine cycle.

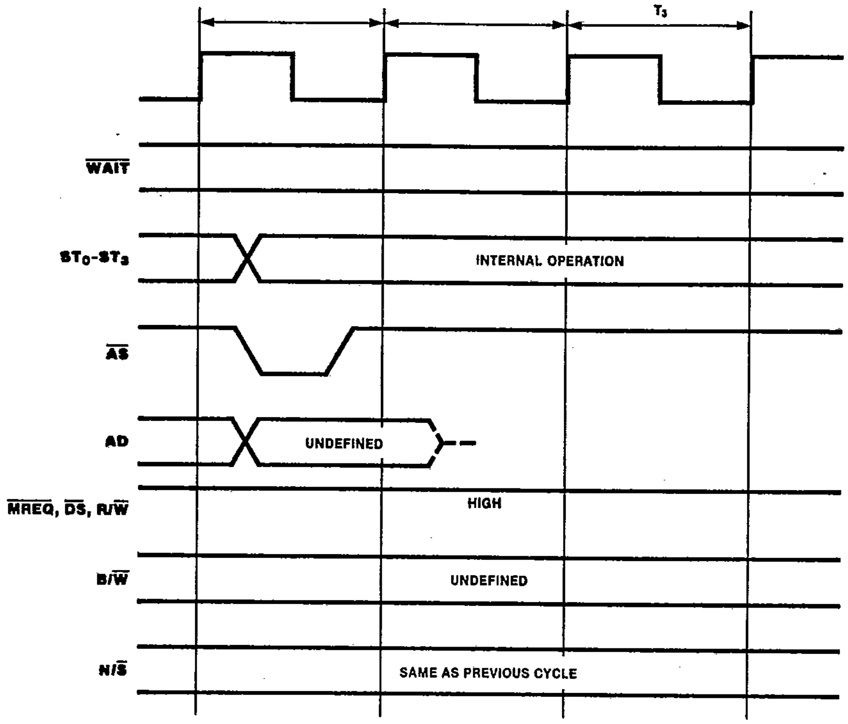

Figure 6. Internal Operation Timing

HALT

A HALT instruction executes an unlimited number of 3-cycle internal operations, interspersed with memory refresh cycles whenever requested. An interrupt, segmentation trap, or reset are the only exits from a HALT instruction.

The CPU samples the $\overline{VI}$, $\overline{NVI}$, $\overline{NMI}$, and $\overline{SEGT}$ inputs at the beginning of every T_3 cycle. If an input is found active during two consecutive samples, the subsequent IF_1 cycle is exercised, but ignored, and the normal interrupt acknowledge cycle is started.

MEMORY REFRESH

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When the 6-bit prescaler in the refresh counter has been decremented to zero, a refresh cycle consisting of three T-states is started as soon as possible (that is, after the next IF_1 cycle or Internal Operation cycle).

The 9-bit refresh counter value is put on the low-order side of the address bus (AD_0-AD_8); AD_9-AD_{15} are undefined (Figure 7). Since the memory is word-organized, A_0 is always Low during refresh and the refresh counter is always incremented by two, thus stepping through 256 consecutive refresh addresses on AD_1-AD_8. Unless disabled, the presettable prescaler runs continuously and the delay in starting a refresh cycle is therefore not cumulative.

While the $\overline{STOP}$ input is Low, a continuous stream of memory refresh cycles, each three T-states long, is executed without using the refresh prescaler.

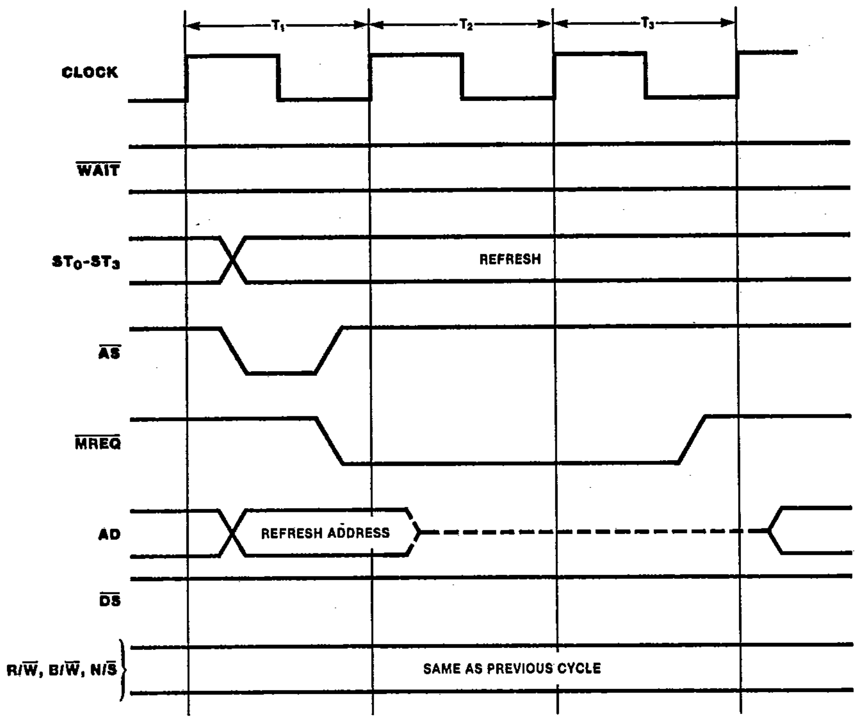

Figure 7. Memory Refresh Timing

RESET

A Low on the $\overline{RESET}$ input causes the following results within five clock cycles (Figure 8):

- AD_0-AD_{15} are 3-stated
- $\overline{AS}$, $\overline{DS}$, $\overline{MREQ}$, ST_0-ST_3, $\overline{BUSACK}$, and $\overline{MO}$ are forced High
- SN_0-SN_6 are forced Low
- Refresh is disabled
- R/$\overline{W}$, B/$\overline{W}$, and N/$\overline{S}$ are not affected

When $\overline{RESET}$ has been High for three clock periods, three consecutive memory read cycles are executed in the system mode for the Z8001. The Z8002 has two consecutive read cycles. In the Z8001 the first cycle reads the flag and control word from location 0002, the next reads the 7-bit program counter segment number from location 0004, the next reads the 16-bit PC offset from location0006, and the following IF_1 cycle starts the program. In the Z8002, the first cycle reads the flag and control word from location 0002, the next reads the PC from location 0004, and the following IF_1 cycle starts the program.

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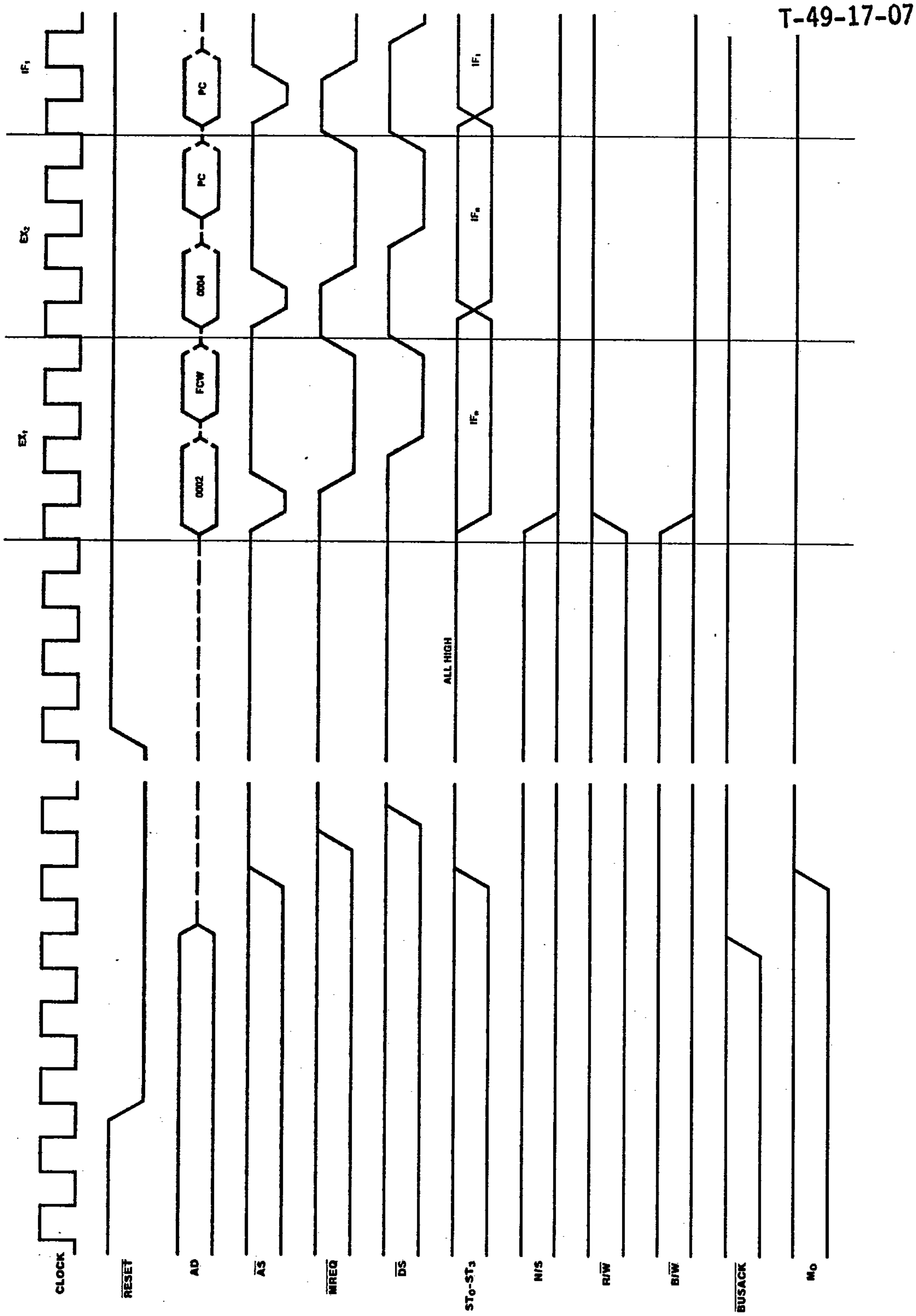
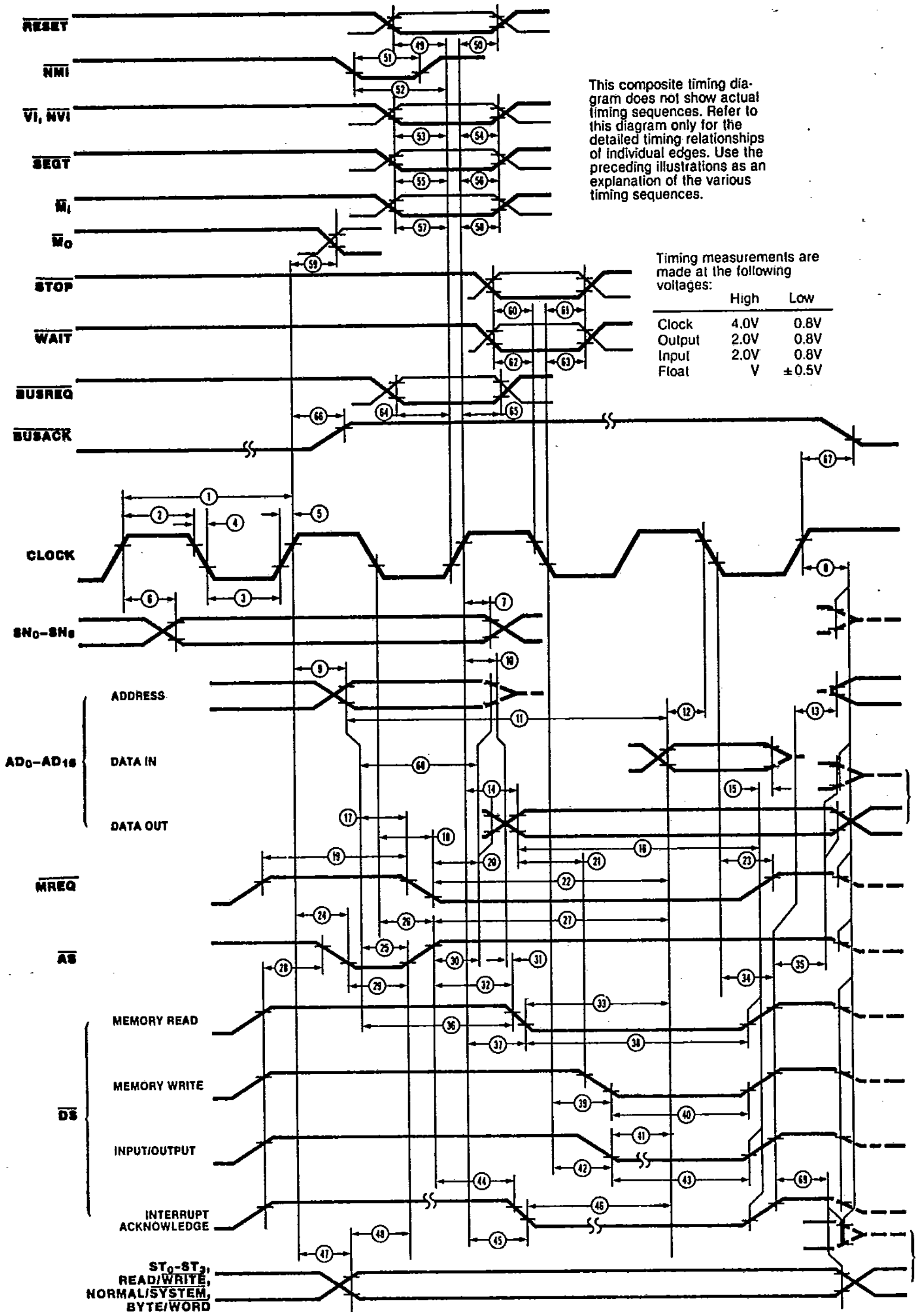

CLOCK
RESET
AD
AS
MREQ
DS
ST0–ST3
N/S
R/W
B/W
BUSACK
M0
ALL HIGH
EX1
EX2
IF1
0002
FCW
0004
PC
PC

COMPOSITE AC TIMING DIAGRAM



This composite timing diagram does not show actual timing sequences. Refer to this diagram only for the detailed timing relationships of individual edges. Use the preceding illustrations as an explanation of the various timing sequences.

Timing measurements are made at the following voltages:

	High	Low
Clock	4.0V	0.8V
Output	2.0V	0.8V
Input	2.0V	0.8V
Float	V	±0.5V

ABSOLUTE MAXIMUM RATINGS

Guaranteed by characterization/design.

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Voltages on all pins with respect to GND . . . . −0.3V to +7.0V
Operating Case Temperature . . . . −55°C to +125°C
Storage Temperature . . . . −65°C to +150°C
Absolute Maximum Power Dissipation. 2.25W
Solder Temperature .... 270°C for 5 sec.

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

STANDARD TEST CONDITIONS

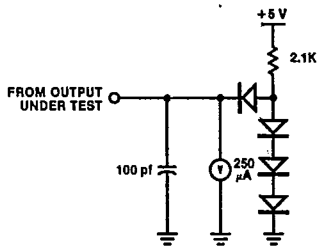
The DC Characteristics section listed below applies for the following standard test conditions, unless otherwise noted.

Military Operating Temperature Range (T_C)
−55°C to +125°C

Standard Military Test Condition
$+4.5V \leqslant V_{CC} \leqslant +5.5V$

All voltages are referenced to GND (0V). Positive current flows into the referenced pin.

All AC parameters assume a total load capacitance (including parasitic capacitances) or 100 pf max, except for parameter 6 (50 pf max). Timing references between two output signals assume a load difference of 50 pf max.



DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Unit	Condition
V_{CH}	Clock Input High Voltage	$V_{CC}-0.4$[a]	$V_{CC}+0.3$[c]	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	−0.3[c]	0.45[a]	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2.2[a]	$V_{CC}+0.3$[c]	V	
$V_{IH\ RESET}$	Input High Voltage on RESET pin	2.4[a]	$V_{CC}+0.3$[c]	V	
$V_{IH\ NMI}$	Input High Voltage on NMI pin	2.4[a]	$V_{CC}+0.3$[c]	V	
V_{IL}	Input Low Voltage	−0.3[c]	0.8[a]	V	
V_{OH}	Output High Voltage	2.4[a]		V	$I_{OH} = -250\,\mu A$
V_{OL}	Output Low Voltage		0.4[a]	V	$I_{OL} = +2.0$ mA
I_{IL}	Input Leakage		±10[a]	µA	$0.4 \leqslant V_{IN} \leqslant +2.4V$
$I_{IL\ SEGT}$	Max Input Current on SEGT pin (8001 only)		200[a]	µA	
I_{OL}	Output Leakage		±10[a]	µA	$0.4 \leqslant V_{IN} \leqslant +2.4V$
I_{CC}	V_{CC} Power Supply Current		400[a]	mA	**4,6 and 10 MHz**

Parameter Test Status:
[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design

AC CHARACTERISTICS†

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Number	Symbol	Parameter	Z8001/2 4 MHz Min	Z8001/2 4 MHz Max	Z8001/2 6 MHz Min	Z8001/2 6 MHz Max	Z8001/2 10 MHz Min	Z8001/2 10 MHz Max
1	TcC	Clock Cycle Time	250[a]	2000[a]	165[a]	2000[a]	100[a]	2000[a]
2	TwCh	Clock Width (High)	105[a]		70[a]		40[a]	
3	TwCl	Clock Width (Low)	105[a]		70[a]		40[a]	
4	TfC	Clock Fall Time		20[a]		15[a]		10[a]
5	TrC	Clock Rise Time		20[a]		15[a]		10[a]
6	TdC(SNv)	Clock ↑ to Segment Number Valid (50 pf load) (8001 only)		130[a]		110[a]		80[a]
7	TdC(SNn)	Clock ↑ to Segment Number Not Valid (8001 only)	20[a]		10[a]		0[a]	
8	TdC(Bz)	Clock ↑ to Bus Float		65[c]		55[c]		50[c]
9	TdC(A)	Clock ↑ to Address Valid		100[a]		75[a]		55[a]
10	TdC(Az)	Clock ↑ to Address Float		65[c]		55[c]		50[c]
11	TdA(DR)	Address Valid to Read Data Required Valid		475[d]*		305[d]*		180[d]*
12	TsDR(C)	Read Data to Clock ↓ Setup time	30[a]		20[a]		10[a]	
13	TdDS(A)	$\overline{DS}$ ↑ to Address Active	80[d]*		45[d]*		20[d]*	
14	TdC(DW)	Clock ↑ to Write Data Valid		100[a]		75[a]		60[a]
15	ThDR(DS)	Read Data to $\overline{DS}$ ↑ Hold Time	0[a]		0[a]		0[a]	
16	TdDW(DS)	Write Data Valid to $\overline{DS}$ ↑ Delay	295[d]*		195[d]*		110[d]*	
17	TdA(MR)	Address Valid to $\overline{MREQ}$ ↓ Delay	55[d]*		35[d]*		20[d]*	
18	TdC(MR)	Clock ↓ to $\overline{MREQ}$ ↓ Delay		80[a]		70[a]		40[a]
19	TwMRh	$\overline{MREQ}$ Width (High)	210[d]*		135[d]*		80[d]*	
20	TdMR(A)	$\overline{MREQ}$ ↓ to Address Not Active	70[d]*		35[d]*		20[d]*	
21	TdDW(DSW)	Write Data Valid to $\overline{DS}$ ↓ (Write) Delay	55[d]*		35[d]*		15[d]*	
22	TdMR(DR)	$\overline{MREQ}$ ↓ to Read Data Required Valid		370[d]*		230[d]*		140[d]*
23	TdC(MR)	Clock ↓ $\overline{MREQ}$ ↑ Delay		80[a]		60[a]		45[a]
24	TdC(ASf)	Clock ↑ to $\overline{AS}$ ↓ Delay		80[a]		60[a]		40[a]
25	TdA(AS)	Address Valid to $\overline{AS}$ ↑ Delay	55[d]*		35[d]*		20[d]*	
26	TdC(ASr)	Clock ↓ to $\overline{AS}$ ↑ Delay		90[a]		80[a]		40[a]
27	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid		360[d]*		220[d]*		140[d]*
28	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	70[d]*		35[d]*		15[d]*	
29	TwAS	$\overline{AS}$ Width (Low)	85[d]*		55[d]*		30[d]*	
30	TdAS(A)	$\overline{AS}$ ↑ to Address Not Active Delay	70[d]*		45[d]*		20[d]*	
31	TdAz(DSR)	Address Float to $\overline{DS}$ (Read) ↓ Delay	0[c]		0[c]		0[c]	
32	TdAS(DSR)	$\overline{AS}$ ↑ to $\overline{DS}$ (Read) ↓ Delay	80[d]*		55[d]*		30[d]*	
33	TdDSR(DR)	$\overline{DS}$ (Read) ↓ to Read Data Required Valid		205[d]*		130[d]*		70[d]*
34	TdC(DSr)	Clock ↓ to $\overline{DS}$ ↑ Delay		70[a]		65[a]		45[a]
35	TdDS(DW)	$\overline{DS}$ ↑ to Write Data Not Valid	75[d]*		45[d]*		25[d]*	

*Clock-cycle time-dependent characteristics. See Footnotes to AC Characteristics.
†Units in nanoseconds (ns).

Parameter Test Status:

[a] Tested
[b] Guaranteed
[c] Guaranteed by Characterization/Design
[d] Calculated Parameter—Not Directly Tested

AC CHARACTERISTICS† (Continued)

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Number	Symbol	Parameter	Z8001/2 4 MHz Min	Z8001/2 4 MHz Max	Z8001/2 6 MHz Min	Z8001/2 6 MHz Max	Z8001/2 10 MHz Min	Z8001/2 10 MHz Max
36	TdA(DSR)	Address Valid to $\overline{DS}$ (Read) ↓ Delay	180d*		110d*		65d*	
37	TdC(DSR)	Clock ↑ to $\overline{DS}$ (Read) ↓ Delay		120a		85a		60a
38	TwDSR	$\overline{DS}$ (Read) Width (Low)	275d*		185d*		110d*	
39	TdC(DSW)	Clock ↓ to $\overline{DS}$ (Write) ↓ Delay		95a		80a		60a
40	TwDSW	$\overline{DS}$ (Write) Width (Low)	185d*		110d*		75d*	
41	TdDSI(DR)	$\overline{DS}$ (I/O) ↓ to Read Data Required Valid		330d*		210d*		120d*
42	TdC(DSf)	Clock ↓ to $\overline{DS}$ (I/O) ↓ Delay		120a		90a		60a
43	TwDS	$\overline{DS}$ (I/O) Width (Low)	410d*		255d*		160d*	
44	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay	1065d*		690d*		410d*	
45	TdC(DSA)	Clock ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay		120a		85a		65a
46	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Required Delay		455d*		295d*		165d*
47	TdC(S)	Clock ↑ to Status Valid Delay		110a		85a		65a
48	TdS(AS)	Status Valid to $\overline{AS}$ ↑ Delay	50d*		30d*		20d*	
49	TsR(C)	$\overline{RESET}$ to Clock ↑ Setup Time	180a		70a		50a	
50	ThR(C)	$\overline{RESET}$ to Clock ↑ Hold Time	0a		0a		0a	
51	TwNMI	$\overline{NMI}$ Width (Low)	100a		70a		50a	
52	TsNMI(C)	$\overline{NMI}$ to Clock ↑ Setup Time	140a		70a		50a	
53	TsVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Setup Time	110a		50a		40a	
54	ThVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Hold Time	20a		20a		10a	
55	TsSGT(C)	$\overline{SEGT}$ to Clock ↑ Setup Time (8001 only)	70a		55a		40a	
56	ThSGT(C)	$\overline{SEGT}$ to Clock ↑ Hold Time (8001 only)	0a		0a		0a	
57	TsMI(C)	$\overline{MI}$ to Clock ↑ Setup Time	180a		140a		80a	
58	ThMI(C)	$\overline{MI}$ to Clock ↑ Hold Time	0a		0a		0a	
59	TdC(MO)	Clock ↑ to $\overline{MO}$ Delay		120a		85a		65a
60	TsSTP(C)	$\overline{STOP}$ to Clock ↓ Setup Time	140a		100a		50a	
61	ThSTP(C)	$\overline{STOP}$ to Clock ↓ Hold Time	0a		0a		0a	
62	TsW(C)	$\overline{WAIT}$ to Clock ↓ Setup Time	50a		30a		20a	
63	ThW(C)	$\overline{WAIT}$ to Clock ↓ Hold Time	10a		10a		5a	
64	TsBRQ(C)	$\overline{BUSREQ}$ to Clock ↑ Setup Time	90a		80a		60a	
65	ThBRQ(C)	$\overline{BUSREQ}$ to Clock ↑ Hold Time	10a		10a		5a	
66	TdC(BAKr)	Clock ↑ to $\overline{BUSACK}$ ↑ Delay		100a		75a		60a
67	TdC(BAKf)	Clock ↑ to $\overline{BUSACK}$ ↓ Delay		100a		75a		60a
68	TwA	Address Valid Width	150d*		95d*		50d*	
69	TdDS(S)	$\overline{DS}$ ↑ to STATUS Not Valid	80d*		55d*		30d*	

*Clock-cycle time-dependent characteristics. See Footnotes to AC Characteristics.
†Units in nanoseconds (ns).

Parameter Test Status:

a Tested
b Guaranteed
c Guaranteed by Characterization/Design
d Calculated Parameter—Not Directly Tested

FOOTNOTES TO AC CHARACTERISTICS

Number	Symbol	Z8001/2 4 MHz Equation	Z8001/2 6 MHz Equation	Z8001/2 10 MHz Equation
11	TdA(DR)	2TcC + TwCh − 130 ns	2TcC + TwCh − 95 ns	2TcC + TwCh − 60 ns
13	TdDS(A)	TwCl − 25 ns	TwCl − 25 ns	TwCl − 20 ns
16	TdDW(DS)	TcC + TwCh − 60 ns	TcC + TwCh − 40 ns	TcC + TwCh − 30 ns
17	TdA(MR)	TwCh − 50 ns	TwCh − 35 ns	TwCh − 20 ns
19	TwMRh	TcC − 40 ns	TcC − 30 ns	TcC − 20 ns
20	TdMR(A)	TwCl − 35 ns	TwCl − 35 ns	TwCl − 20 ns
21	TdDW(DSW)	TwCh − 50 ns	TwCh − 35 ns	TwCh − 25 ns
22	TdMR(DR)	2TcC − 130 ns	2TcC − 100 ns	2TcC − 60 ns
25	TdA(AS)	TwCh − 50 ns	TwCh − 35 ns	TwCh − 20 ns
27	TdAS(DR)	2TcC − 140 ns	2TcC − 110 ns	2TcC − 60 ns
28	TdDS(AS)	TwCl − 35 ns	TwCl − 35 ns	TwCl − 25 ns
29	TwAS	TwCh − 20 ns	TwCh − 15 ns	TwCh − 10 ns
30	TdAS(A)	TwCl − 35 ns	TwCl − 25 ns	TwCl − 20 ns
32	TdAS(DSR)	TwCl − 25 ns	TwCl − 15 ns	TwCl − 10 ns
33	TdDSR(DR)	TcC + TwCh − 150 ns	TcC + TwCh − 105 ns	TcC + TwCh − 70 ns
35	TdDS(DW)	TwCl − 30 ns	TwCl − 25 ns	TwCl − 15 ns
36	TdA(DSR)	TcC − 70 ns	TcC − 55 ns	TcC − 35 ns
38	TwDSR	TcC + TwCh − 80 ns	TcC + TwCh − 50 ns	TcC + TwCh − 30 ns
40	TwDSW	TcC − 65 ns	TcC − 55 ns	TcC − 25 ns
41	TdDSI(DR)	2TcC − 170 ns	2TcC − 120 ns	2TcC − 80 ns
43	TwDS	2TcC − 90 ns	2TcC − 75 ns	2TcC − 40 ns
44	TdAS(DSA)	4TcC + TwCl − 40 ns	4TcC + TwCl − 40 ns	4TcC + TwCl − 30 ns
46	TdDSA(DR)	2TcC + TwCh − 150 ns	2TcC + TwCh − 105 ns	2TcC + TwCh − 75 ns
48	TdS(AS)	TwCh − 55 ns	TwCh − 40 ns	TwCh − 20 ns
68	TwA	TcC − 90 ns	TcC − 70 ns	TcC − 50 ns
69	TdDS(s)	TwCl − 25 ns	TwCl − 15 ns	TwCl − 10 ns

AC Timing Test Conditions

V_{OL} = 0.8V
V_{OH} = 2.0V
V_{IL} = 0.8V
V_{IH} = 2.4V
V_{ILC} = 0.45V
V_{IHC} = V_{CC}−0.4V

PIN DESCRIPTION

AD_0-AD_{15}. *Address/Data* (inputs/outputs, active High, 3-state). These multiplexed address and data lines are used for I/O and to address memory.

$\overline{\text{AS}}$. *Address Strobe* (output, active Low, 3-state). The rising edge of $\overline{\text{AS}}$ indicates addresses are valid.

$\overline{\text{BUSACK}}$. *Bus Acknowledge* (output active Low). A Low on this line indicates the CPU has relinquished control of the bus.

$\overline{\text{BUSREQ}}$. *Bus Request* (input, active Low). This line must be driven Low to request the bus from the CPU.

B/$\overline{\text{W}}$. *Byte/Word* (output, Low = Word, 3-state). This signal defines the type of memory reference on the 16-bit address/data bus.

CLK. *System Clock* (input). CLK is a 5V single-phase time-base input.

$\overline{\text{DS}}$. *Data Strobe* (output, active Low, 3-state). This line times the data in and out of the CPU.

$\overline{\text{MREQ}}$. *Memory Request* (output, active Low, 3-state). A Low on this line indicates that the address/data bus holds a memory address.

$\overline{\text{MI}}$, $\overline{\text{MO}}$. *Multi-Micro In, Multi-Micro Out* (input and output, active Low). These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource.

$\overline{\text{NMI}}$. *Non-Maskable Interrupt* (edge triggered, input, active Low). A high-to-low transition on $\overline{\text{NMI}}$ requests a non-maskable interrupt. The $\overline{\text{NMI}}$ interrupt has the highest priority of the three types of interrupts.

N/$\overline{\text{S}}$. *Normal/System Mode* (output, Low = System Mode, 3-state). N/$\overline{\text{S}}$ indicates the CPU is in the normal or system mode.

$\overline{\text{NVI}}$. *Non-Vectored Interrupt* (input, active Low). A Low on this line requests a non-vectored interrupt.

$\overline{\text{RESET}}$. *Reset* (input, active Low). A Low on this line resets the CPU.

R/$\overline{\text{W}}$. *Read/Write* (output, Low = Write, 3-state). R/$\overline{\text{W}}$ indicates that the CPU is reading from or writing to memory or I/O.

$\overline{\text{SEGT}}$. *Segment Trap* (input, active Low). The Memory Management Unit interrupts the CPU with a Low on this line when the MMU detects a segmentation trap. Input on Z8001 only.

SN_0-SN_6. *Segment Number* (outputs, active High, 3-state). These lines provide the 7-bit segment number used to address one of 128 segments by the Z8010 memory Management Unit. **Output by the Z8001 only.**

ST_0-ST_3. *Status* (outputs, active High, 3-state). These lines specify the CPU status.

$\overline{\text{STOP}}$. *Stop* (input, active Low). This input can be used to single-step instruction execution.

$\overline{\text{VI}}$. *Vectored Interrupt* (input, active Low). A Low on this line requests a vectored interrupt.

$\overline{\text{WAIT}}$. *Wait* (input, active Low). This line indicates to the CPU that the memory or I/O device is not ready for data transfer.

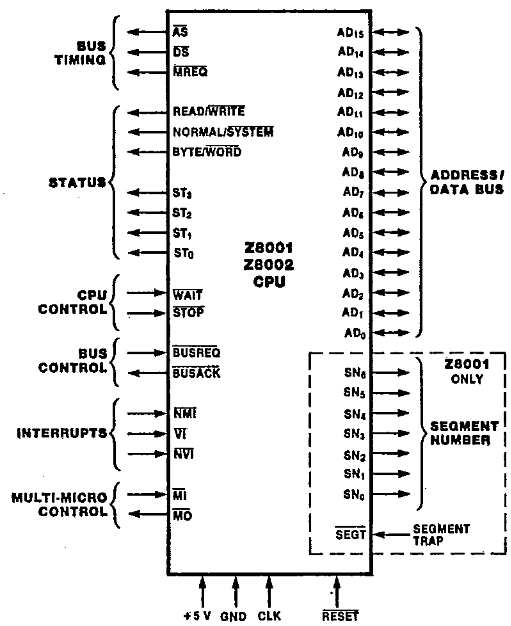


Figure 9. Z8000 CPU Pin Functions

PACKAGE PINOUTS

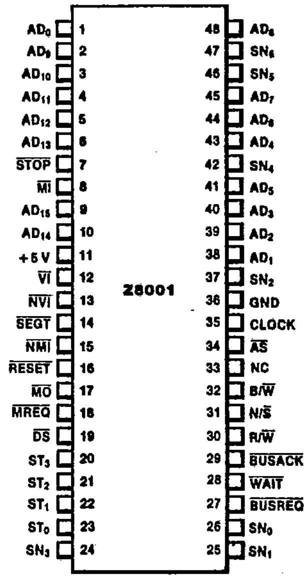


Figure 10a. 48-pin Dual-In-Line Package (DIP), Pin Assignments

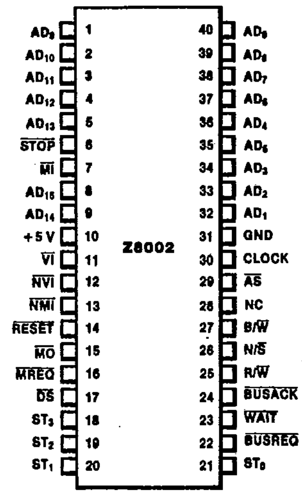
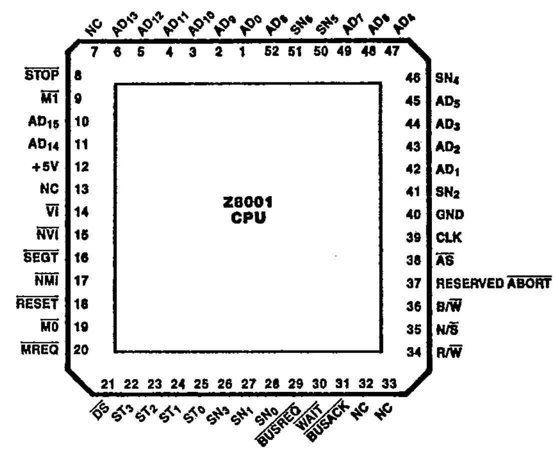


Figure 11a. 40-pin Dual-In-Line Package (DIP), Pin Assignments



NC = No connection

Figure 10b. 52-pin Chip Carrier, Pin Assignments

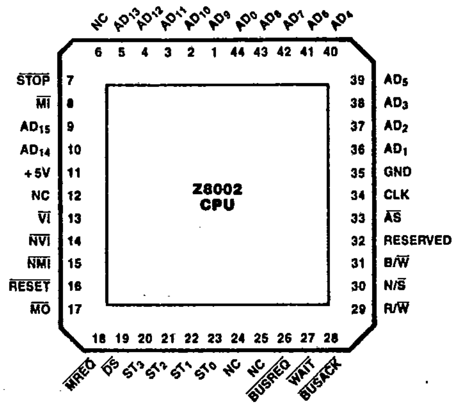


Figure 11b. 44-pin Chip Carrier, Pin Assignments

MIL-STD-883 MILITARY PROCESSED PRODUCT

T-49-17-07

- Mil-Std-883 establishes uniform methods and procedures for testing microelectronic devices to insure the electrical, mechanical, and environmental integrity and reliability that is required for military applications.
- Mil-Std-883 Class B is the industry standard product assurance level for military ground and aircraft application.
- Compliant to 883 Class B, Revision C process requirements.
- The total reliability of a system depends upon tests that are designed to stress specific quality and reliability concerns that affect microelectronic products.
- The following tables detail the 100% screening and electrical tests, sample electrical tests, and Qualification/Quality Conformance testing required.

Zilog Military Product Flow

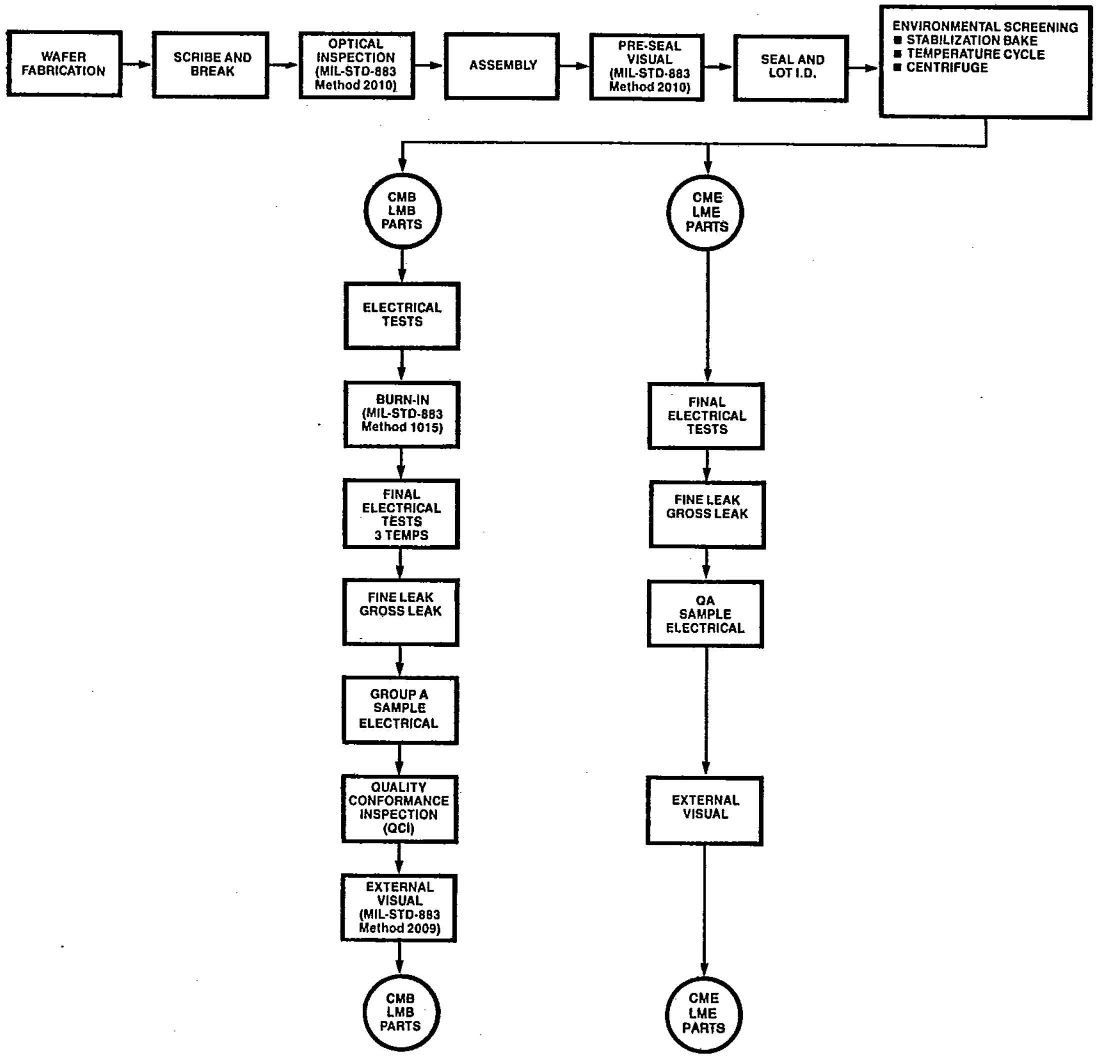


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Table I
MIL-STD-883 Class B Screening Requirements
Method 5004 (Note 4)

Test		Mil-Std-883 Method	Test Condition	Requirement
Internal Visual		2010	Condition B	100%
Stabilization Bake		1008	Condition C	100%
Temperature Cycle		1010	Condition C	100%
Constant Acceleration (Centrifuge)		2001	Condition E or D(Note 1), Y_1 Axis Only	100%
Initial Electrical Tests			Zilog Military Electrical Specification Static/DC $T_C = +25°C$	100%
Burn-In		1015	Condition D(Note 2), 160 hours, $T_A = +125°C$	100%
Interim Electrical Tests			Zilog Military Electrical Specification Static/DC $T_C = +25°C$	100%
PDA Calculation			PDA = 5%	100%
Final Electrical Tests			Zilog Military Electrical Specification Static/DC $T_C = +125°C, -55°C$ Functional, Switching/AC $T_C = +25°C$	100%
Fine Leak		1014	Condition B	100%
Gross Leak		1014	Condition C	100%
Quality Conformance Inspection (QCI)				
Group A	Each Inspection Lot	5005	(See Table II)	Sample
Group B	Every Week	5005	(See Table III)	Sample
Group C	Periodically(Note 3)	5005	(See Table IV)	Sample
Group D	Periodically(Note 3)	5005	(See Table V)	Sample
External Visual		2009		100%
QA—Ship				100%

NOTES:
1. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
2. In process of fully implementing of Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.
3. Performed periodically as required by Mil-Std-883, paragraph 1.2.1 b(17).
4. **Processing fully compliant to Mil-Std-883 Revision C requirements.**

Table II Group A
Sample Electrical Tests
MIL-STD-883 Method 5005

T-49-17-07

Subgroup	Tests	Temperature (T_C)	Sample Size
Subgroup 1	Static/DC	+25°C	100%
Subgroup 2	Static/DC	+125°C	116/0
Subgroup 3	Static/DC	−55°C	116/0
Subgroup 7	Functional	+25°C	100%
Subgroup 8	Functional	−55°C and +125°C	116/0
Subgroup 9	Switching/AC	+25°C	100%
Subgroup 10	Switching/AC	+125°C	116/0
Subgroup 11	Switching/AC	−55°C	116/0

NOTES:
- The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail electrical specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no Group A testing is required for that subgroup or test.
- Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.
- **If any failure occurs during sample testing of any subgroup then the lot is 100% tested at the failed subgroup only.**

Table III Group B

T-49-17-07

Sample Test Performed Every Week to Test Construction and Insure Integrity of Assembly Process. MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 2			
Resistance to Solvents	2015		4/0
Subgroup 3			
Solderability	2003	Solder Temperature +245°C ± 5°C	15(Note 1)
Subgroup 5			
Bond Strength	2011	C	15(Note 2)

NOTES:
1. Number of leads inspected selected from a minimum of 3 devices.
2. Number of bond pulls selected from a minimum of 4 devices.

Table IV Group C

T-49-17-07

Sample Test Performed Periodically to Verify Integrity of the Die.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Steady State Operating Life	1005	Condition D(Note 1), 1000 hours at +125°C	5
End Point Electrical Tests		Zilog Military Electrical Specification T_C = +25°C, +125°C, −55°C	

NOTE:
1. In process of fully implementing Condition D Burn-In Circuits. Contact factory for copy of specific burn-in circuit available.

Table V Group D

T-49-17-07

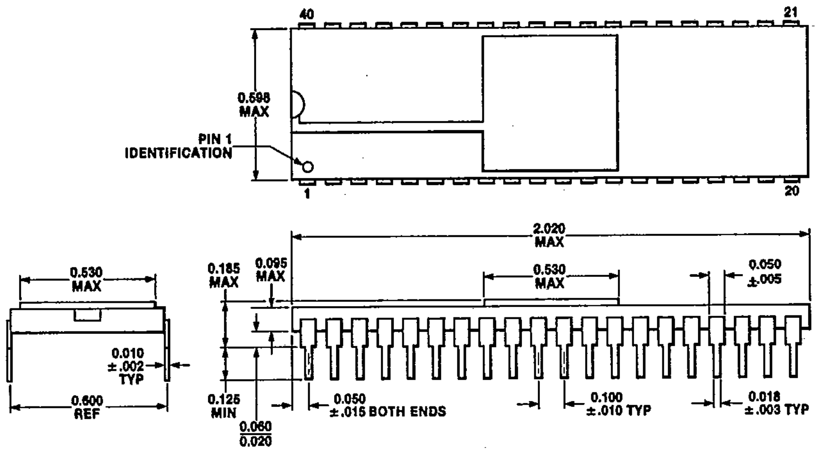
Sample Test Performed Periodically to Insure Integrity of the Package.
MIL-STD-883 Method 5005

Subgroup	Mil-Std-883 Method	Test Condition	Quantity or LTPD/Max Accept
Subgroup 1			
Physical Dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Condition B_2 or D(Note 1)	15
Subgroup 3			
Thermal Shock	1011	Condition B minimum, 15 cycles minimum	
Temperature Cycling	1010	Condition C, 100 cycles minimum	15
Moisture Resistance	1004		
Seal	1014		
3a) Fine Leak		3a) Condition B	
3b) Gross Leak		3b) Condition C	
Visual Examination	1004 or 1010		
End Point Electrical Tests	.	Zilog Military Electrical Specification $T_C = +25°C, +125°C, -55°C$	
Subgroup 4			
Mechanical Shock	2002	Condition B minimum	
Vibration Variable Frequency	2007	Condition A minimum	
Constant Acceleration (Centrifuge)	2001	Condition E or D(Note 2), Y_1 Axis Only	15
Seal	1014		
4a) Fine Leak		4a) Condition B	
4b) Gross Leak		4b) Condition C	
Visual Examination	1010 or 1011		
End Point Electrical Tests		Zilog Military Electrical Specification $T_C = +25°C, +125°C, -55°C$	
Subgroup 5			
Salt Atmosphere	1009	Condition A minimum	
Seal	1014		15
5a) Fine Leak		5a) Condition B	
5b) Gross Leak		5b) Condition C	
Visual Examination	1009		
Subgroup 6			
Internal Water Vapor Content	1018	5,000 ppm. maximum water content at +100°C	3/0 or 5/1
Subgroup 7(Note 3)			
Adhesion of Lead Finish	2025		15(Note 4)
Subgroup 8(Note 5)			
Lid Torque	2024		5/0

NOTES:
1. Lead Integrity Condition D for leadless chip carriers.
2. Applies to larger packages which have an inner seal or cavity perimeter of two inches or more in total length or have a package mass of ≥5 grams.
3. Not applicable to leadless chip carriers.
4. LTPD based on number of leads.
5. Not applicable for solder seal packages.

PACKAGE INFORMATION

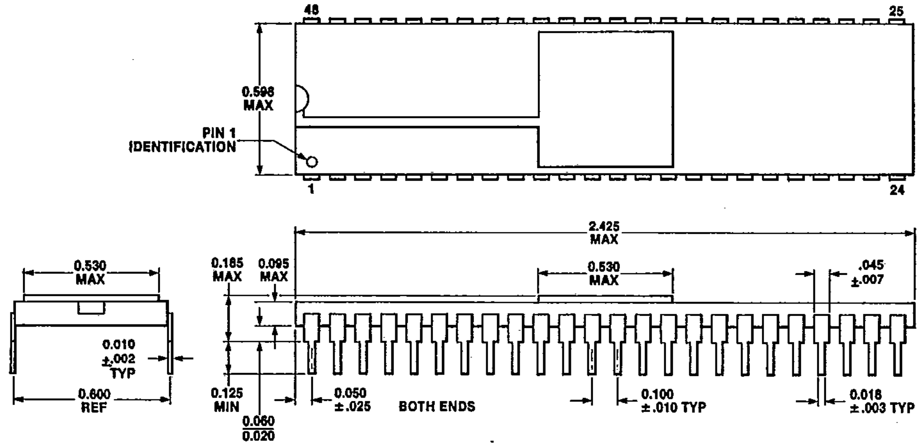
T-49-17-07



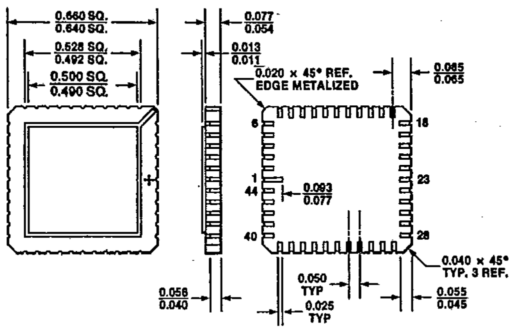
40-Pin Dual-In-Line Package (DIP), Ceramic

PACKAGE INFORMATION (Continued)

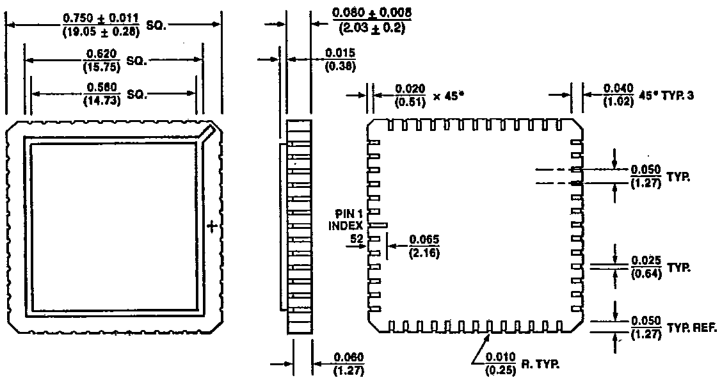
T-49-17-07



48-Pin Dual-In-Line Package (DIP), Ceramic



44-Pin Leadless Chip Carrier (LCC), Ceramic, JEDEC Type C



52-Pin Leadless Chip Carrier (LCC), Ceramic, JEDEC Type C

ORDERING INFORMATION

T-49-17-07

Z8001 Segmented CPU, 4.0 MHz

48-pin DIP	52-pin LCC
Z0800104CMB	Z0800104LMB

Z8001 Segmented CPU, 6.0 MHz

48-pin DIP	52-pin LCC
Z0800106CME	Z0800106LME
Z0800106CMB	Z0800106LMB

Z8001 Segmented CPU, 10.0 MHz

48-pin DIP	52-pin LCC
Z0800110CME	Z0800110LME
Z0800110CMB	Z0800110LMB

Z8002 Non-Segmented CPU, 4.0 MHz

40-pin DIP	44-pin LCC
Z0800204CMB	Z0800204LMB
Z0800204CMJ*	

Z8002 Non-Segmented CPU, 6.0 MHz

40-pin DIP	44-pin LCC
Z0800206CME	Z0800206LME
Z0800206CMB	Z0800206LMB
Z0800206CMJ*	

Z8002 Non-Segmented CPU, 10.0 MHz

40-pin DIP	44-pin LCC
Z0800210CME	Z0800210LME
Z0800210CMB	Z0800210LMB

Codes

PACKAGE

C = Ceramic
L = Ceramic LCC

TEMPERATURE

M = -55°C to +125°C

ENVIRONMENTAL

E = Hermetic Standard
B = 833 Class B Military
J = JAN 38510 Military

Example:
Z0800104CMB is an 8001, 4 MHz, Ceramic DIP, -55°C to +125°C, 883 Class B Military Flow (Revision C Compliant).

Z 0 8001 0 4 C M B

- B — Environmental Flow
- M — Temperature
- C — Package
- 04 — Speed
- 8001 — Product Number
- Z0 — Zilog Prefix

*See MIL-M-38510 Slash Sheet 520 for flow and electrical specifications for Z8002 (4 and 6 MHz).