

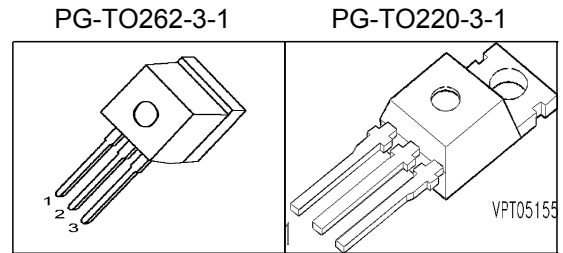
## SIPMOS® Power-Transistor

### Feature

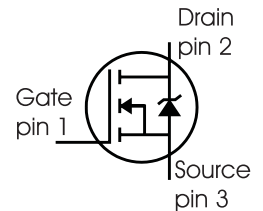
- N-Channel
- Enhancement mode
- Logic Level
- 175°C operating temperature
- Avalanche rated
- dv/dt rated
- Pb-free lead plating; RoHS compliant

### Product Summary

$V_{DS}$	100	V
$R_{DS(on)}$	154	mΩ
$I_D$	10.3	A



Type	Package	Ordering Code	Marking
SPP10N10L	PG-TO220-3-1	Q67042-S4163	10N10L
SPI10N10L	PG-TO262-3-1	Q67042-S4162	10N10L



### Maximum Ratings, at $T_j = 25\text{ °C}$ , unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	$I_D$	10.3	A
$T_C=25\text{ °C}$		10.3	
$T_C=100\text{ °C}$		8.1	
Pulsed drain current	$I_D \text{ puls}$	42.2	
$T_C=25\text{ °C}$			
Avalanche energy, single pulse	$E_{AS}$	60	mJ
$I_D=10.3\text{ A}$ , $V_{DD}=25\text{ V}$ , $R_{GS}=25\text{ Ω}$			
Reverse diode dv/dt	dv/dt	6	kV/μs
$I_S=10.3\text{ A}$ , $V_{DS}=80\text{ V}$ , $di/dt=200\text{ A/μs}$ , $T_{jmax}=175\text{ °C}$			
Gate source voltage	$V_{GS}$	±20	V
Power dissipation	$P_{tot}$	50	W
$T_C=25\text{ °C}$			
Operating and storage temperature	$T_j, T_{stg}$	-55... +175	°C
IEC climatic category; DIN IEC 68-1		55/175/56	

**Thermal Characteristics**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Characteristics</b>					
Thermal resistance, junction - case	$R_{thJC}$	-	-	3	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$	-	-	100	
SMD version, device on PCB: @ min. footprint @ 6 cm <sup>2</sup> cooling area <sup>1)</sup>	$R_{thJA}$	-	-	75 50	

**Electrical Characteristics, at  $T_j = 25^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Static Characteristics</b>					
Drain-source breakdown voltage $V_{GS}=0V, I_D=1mA$	$V_{(BR)DSS}$	100	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D = 21 \mu A$	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current $V_{DS}=100V, V_{GS}=0V, T_j=25^\circ C$ $V_{DS}=100V, V_{GS}=0V, T_j=125^\circ C$	$I_{DSS}$	-	0.01 1	1 100	$\mu A$
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	$I_{GSS}$	-	1	100	
Drain-source on-state resistance $V_{GS}=4.5V, I_D=8.1A$	$R_{DS(on)}$	-	169	210	m $\Omega$
Drain-source on-state resistance $V_{GS}=10V, I_D=8.1A$	$R_{DS(on)}$	-	124	154	

<sup>1)</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70  $\mu m$  thick) copper area for drain connection. PCB is vertical without blown air.

**Electrical Characteristics, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic Characteristics**

Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 8.1\text{A}$	4.7	9.4	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$	-	355	444	pF
Output capacitance	$C_{oss}$		-	72	90	
Reverse transfer capacitance	$C_{rss}$		-	42	63	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{V}$ , $V_{GS} = 10\text{V}$ , $I_D = 10.3\text{A}$ , $R_G = 13\Omega$	-	4.6	6.9	ns
Rise time	$t_r$		-	19.1	28.7	
Turn-off delay time	$t_{d(off)}$		-	27.8	41.7	
Fall time	$t_f$		-	17.8	26.7	

**Gate Charge Characteristics**

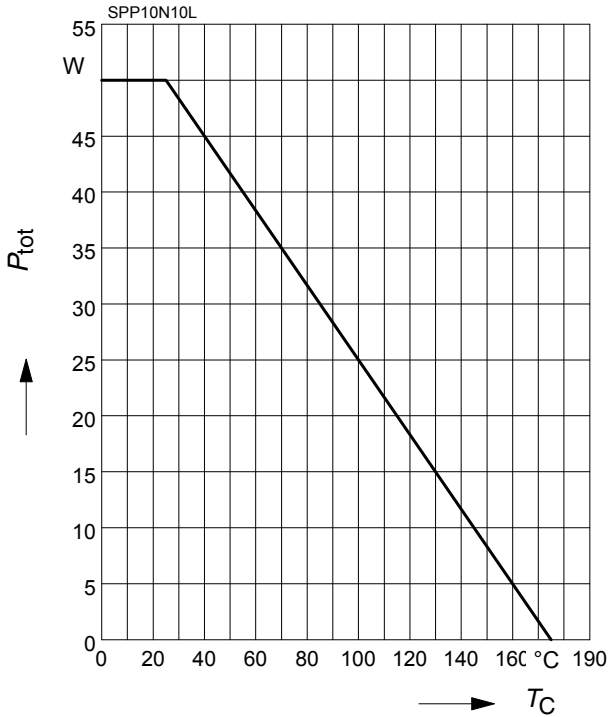
Gate to source charge	$Q_{gs}$	$V_{DD} = 80\text{V}$ , $I_D = 10.3\text{A}$	-	1.1	1.4	nC
Gate to drain charge	$Q_{gd}$		-	7.3	11	
Gate charge total	$Q_g$	$V_{DD} = 80\text{V}$ , $I_D = 10.3\text{A}$ , $V_{GS} = 0\text{ to }10\text{V}$	-	17.7	22	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 80\text{V}$ , $I_D = 10.3\text{A}$	-	3.8	-	V

**Reverse Diode**

Inverse diode continuous forward current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	10.3	A
Inv. diode direct current, pulsed	$I_{SM}$		-	-	42.2	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{V}$ , $I_F = 10.3\text{A}$	-	0.93	1.25	V
Reverse recovery time	$t_{rr}$	$V_R = 50\text{V}$ , $I_F = I_S$ , $di_F/dt = 100\text{A}/\mu\text{s}$	-	57	71	ns
Reverse recovery charge	$Q_{rr}$		-	126	158	

### 1 Power dissipation

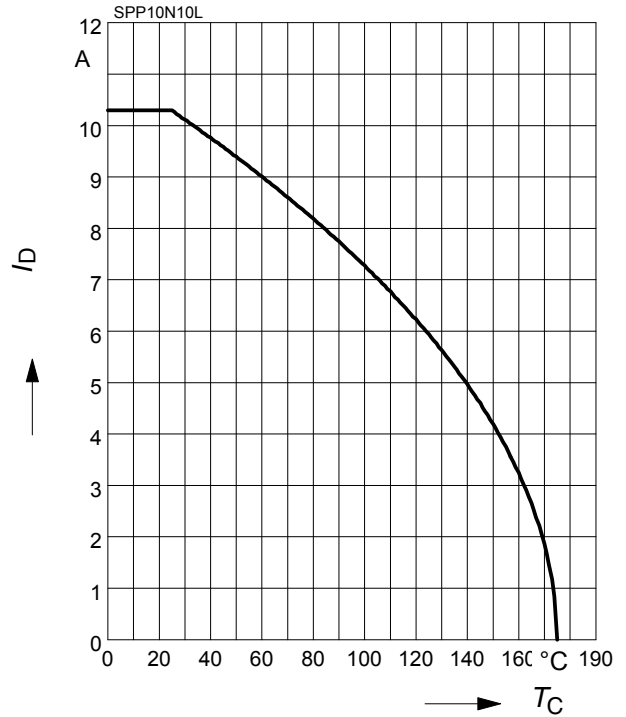
$$P_{\text{tot}} = f(T_C)$$



### 2 Drain current

$$I_D = f(T_C)$$

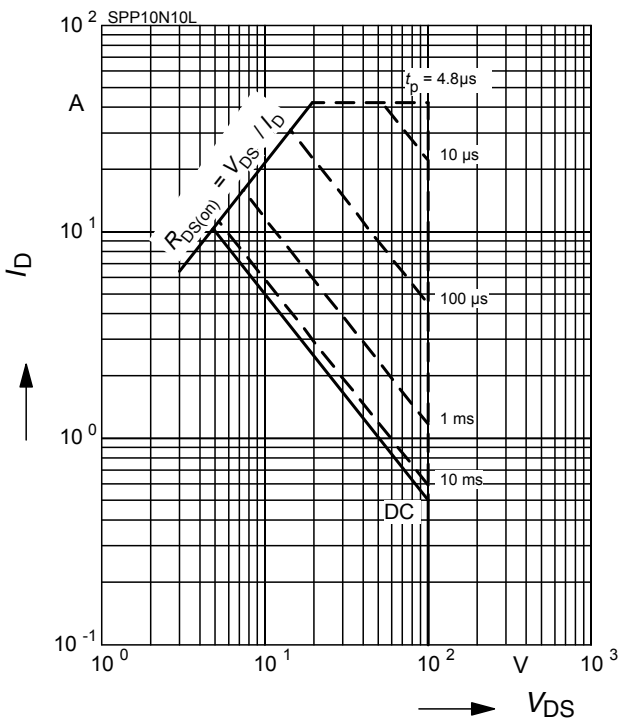
parameter:  $V_{GS} \geq 10$  V



### 3 Safe operating area

$$I_D = f(V_{DS})$$

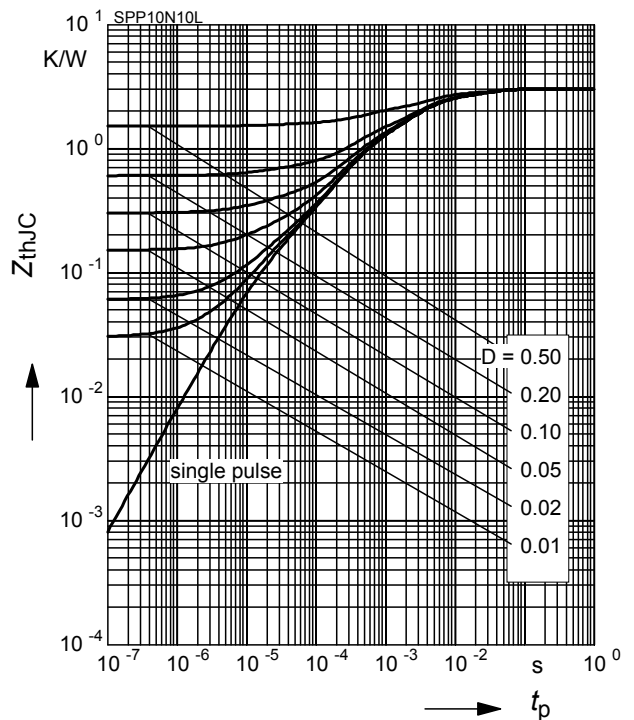
parameter:  $D = 0$ ,  $T_C = 25$  °C



### 4 Transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

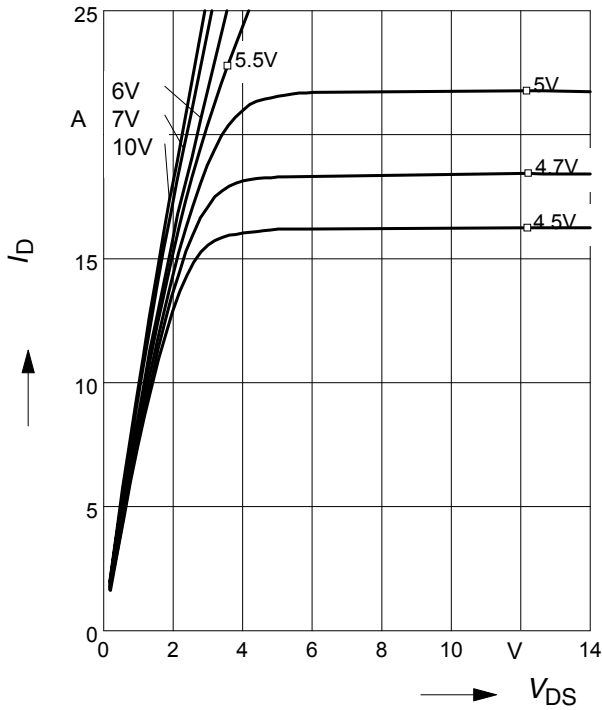
parameter:  $D = t_p / T$



**5 Typ. output characteristic**

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

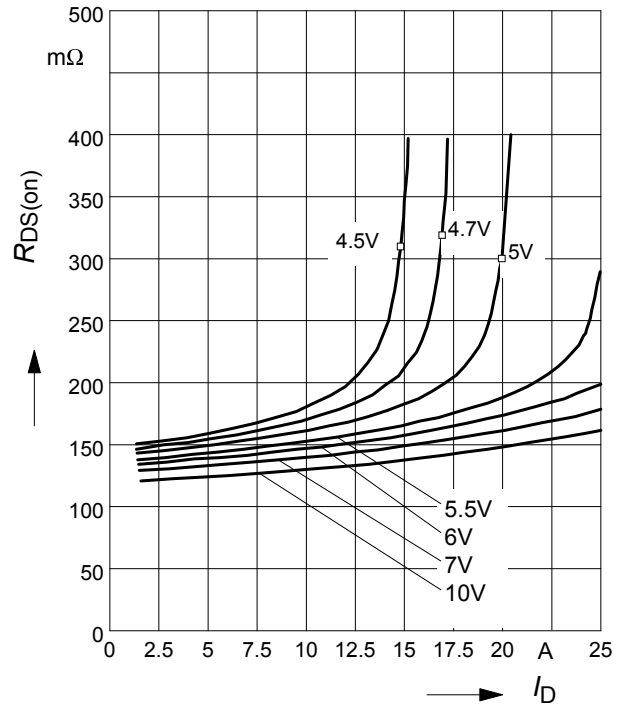
parameter:  $t_p = 80 \mu\text{s}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D)$

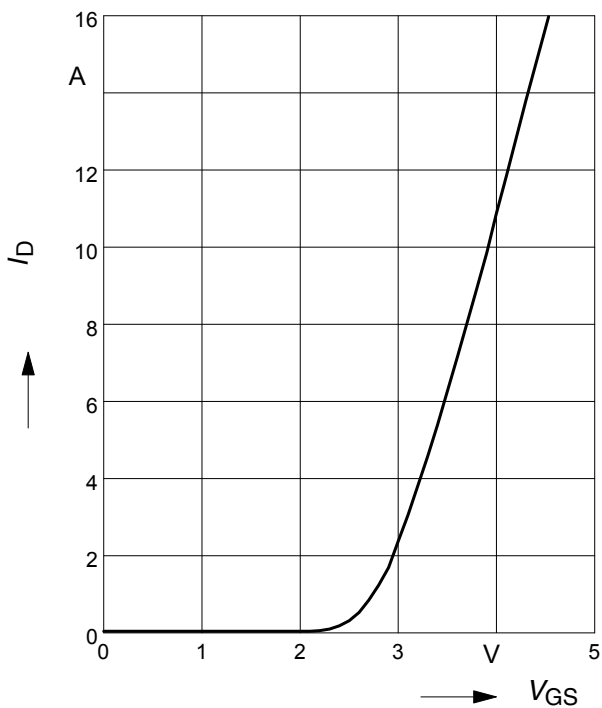
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

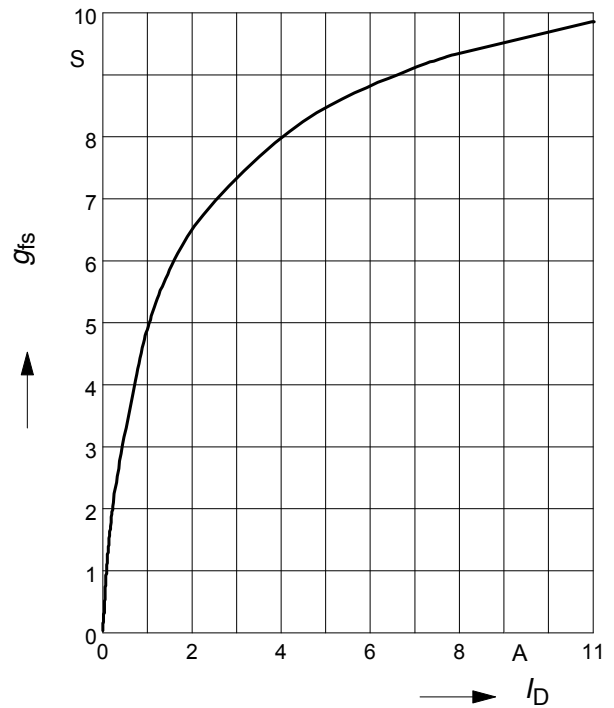
parameter:  $t_p = 80 \mu\text{s}$



**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

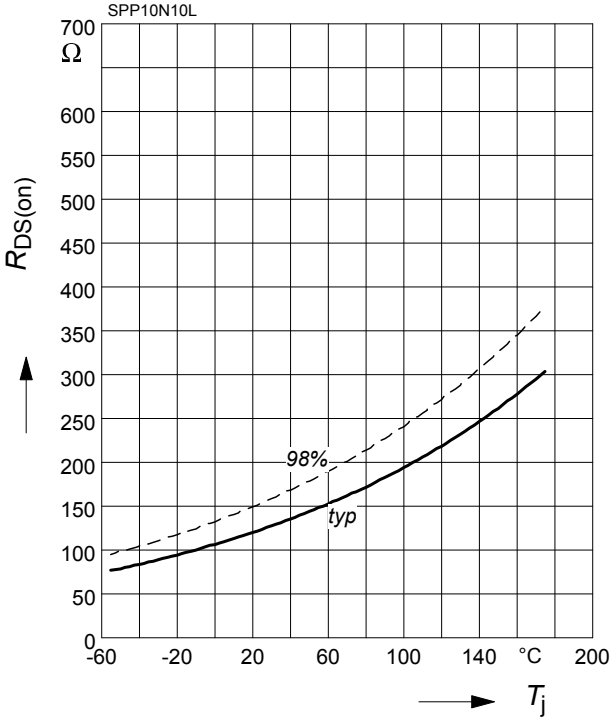
parameter:  $g_{fs}$



**9 Drain-source on-state resistance**

$R_{DS(on)} = f(T_j)$

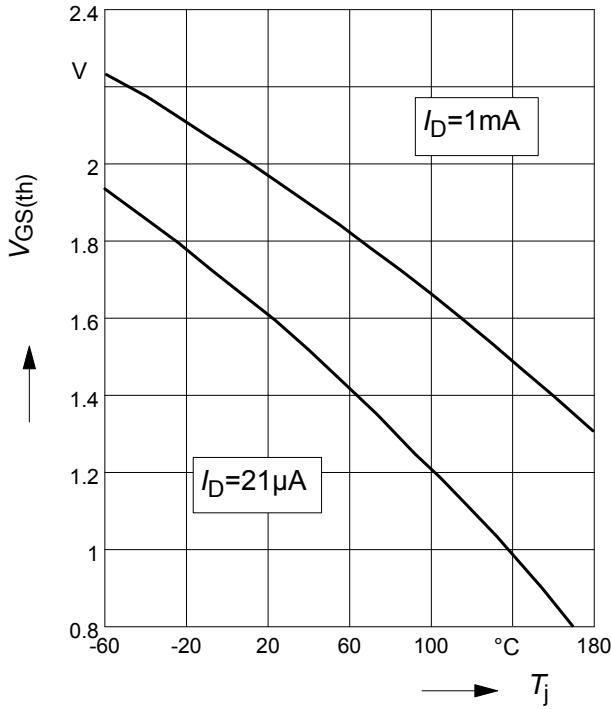
parameter :  $I_D = 8.1 \text{ A}$ ,  $V_{GS} = 10 \text{ V}$



**10 Typ. gate threshold voltage**

$V_{GS(th)} = f(T_j)$

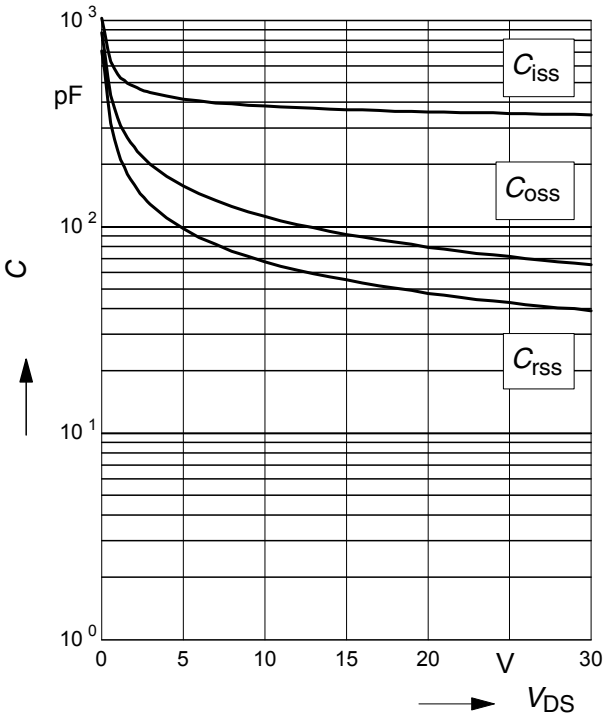
parameter:  $V_{GS} = V_{DS}$



**11 Typ. capacitances**

$C = f(V_{DS})$

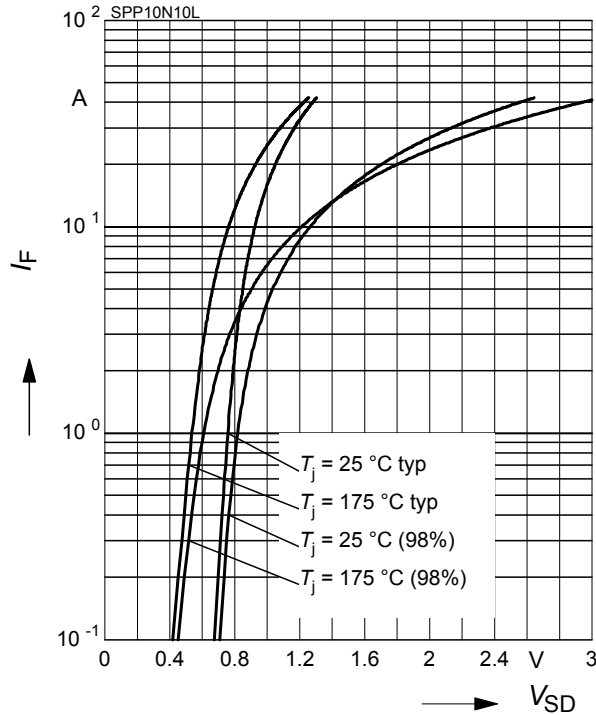
parameter:  $V_{GS}=0\text{V}$ ,  $f=1 \text{ MHz}$



**12 Forward character. of reverse diode**

$I_F = f(V_{SD})$

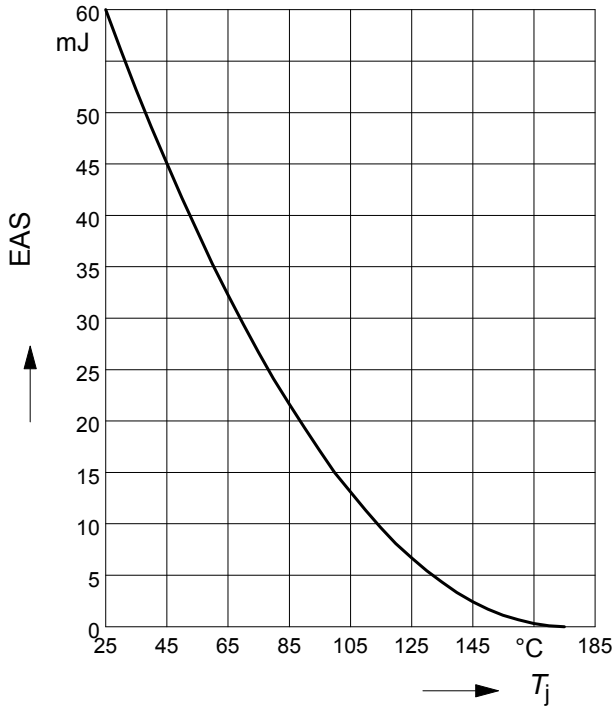
parameter:  $T_j$ ,  $t_p = 80 \mu\text{s}$



### 13 Typ. avalanche energy

$$E_{AS} = f(T_j)$$

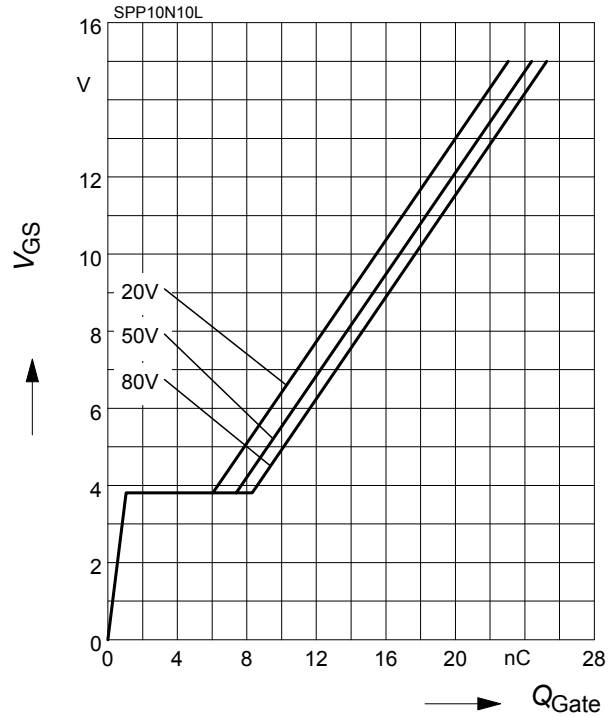
par.:  $I_D = 10.3 \text{ A}$  ,  $V_{DD} = 25 \text{ V}$  ,  $R_{GS} = 25 \Omega$



### 14 Typ. gate charge

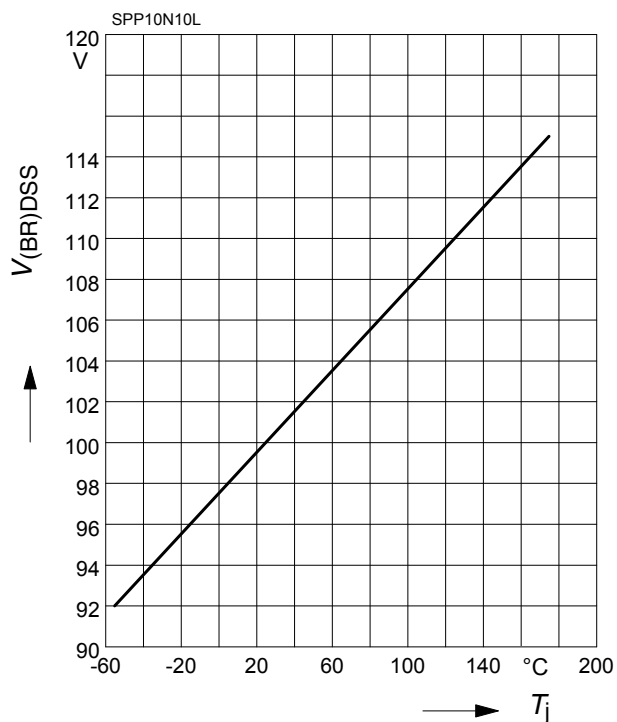
$$V_{GS} = f(Q_{Gate})$$

parameter:  $I_D = 10.3 \text{ A}$  pulsed



### 15 Drain-source breakdown voltage

$$V_{(BR)DSS} = f(T_j)$$



**Published by**  
**Infineon Technologies AG,**  
**Bereichs Kommunikation**  
**St.-Martin-Strasse 53,**  
**D-81541 München**  
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