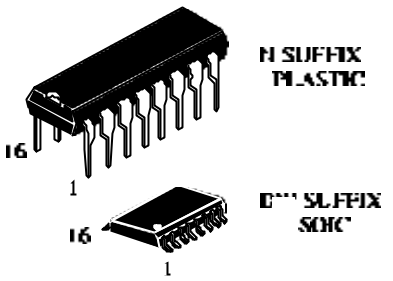
Counter/Divider

High-Voltage Silicon-Gate CMOS

The SL4017B is 5-stage Johnson counter having 10 decoded outputs. Inputs include a CLOCK, a RESET, and a CLOCK INHIBIT signal. Schmitt trigger action in the CLOCK input circuit provides pulse shaping that allows unlimited clock input pulse rise and fall times.

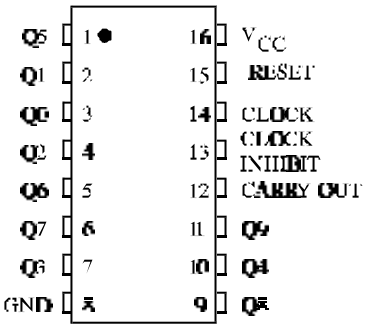
The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. A high RESET signal clears the counter to its zero count. Use of the Johnson counter configuration permits high-speed operation, 2-input decode-gating and spike-free decoded outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The decoded outputs are normally low and go high only at their respective decoded time slot. Each decoded output remains high for one full clock cycle. A CARRY-OUT signal completes one cycle every 10 clock input cycles in the SL4017B.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 µA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  1.0 V min @ 5.0 V supply
  2.0 V min @ 10.0 V supply
  2.5 V min @ 15.0 V supply

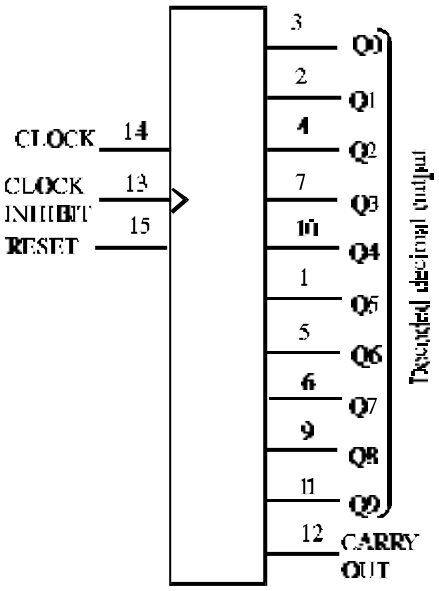


ORDERING INFORMATION
SL4017BN Plastic
SL4017BD SOIC
T_A = -55° to 125° C for all packages

PIN ASSIGNMENT

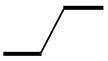


LOGIC DIAGRAM



PIN 16 =V_{CC}
PIN 8 = GND

FUNCTION TABLE

Clock	Clock Enable	Reset	Output State *
L	X	L	no change
X	H	L	no change
X	X	H	reset counter Q0=H, Q1-Q9=L, C0=H
	L	L	Advance to next state
	X	L	no change
X		L	no change
H		L	Advance to next state

* Carry Out=H for Q0,Q1,Q2,Q3 or Q4=H
Carry Out = L otherwise, X=don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS(Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				≥-55°C	25°C	≤125 °C	
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5V or V_{CC} - 0.5V V_{OUT}=1.0V or V_{CC} - 1.0V V_{OUT}=1.5V or V_{CC} - 1.5V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.5V or V_{CC} - 0.5V V_{OUT}=1.0V or V_{CC} - 1.0V V_{OUT}=1.5V or V_{CC} - 1.5V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	5 10 20 100	5 10 20 100	150 300 600 3000	μA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	 5.0 10 15	 0.64 1.6 4.2	 0.51 1.3 3.4	 0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	 5.0 5.0 10 15	 -2.0 -0.64 -1.6 -4.2	 -1.6 -0.51 -1.3 -3.4	 -1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	25°C	≤125°C	Unit
f_{max}	Maximum Clock Frequency	5.0 10 15	2.5 5 5.5	2.5 5 5.5	1.25 2.5 2.75	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Decode Output (Figure 1)	5.0 10 15	650 270 170	650 270 170	1300 540 340	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Carry Output (Figure 1)	5.0 10 15	600 250 160	600 250 160	1200 500 320	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Carry Output or Decode Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Reset to Carry Output or Decode Output (Figure 1)	5.0 10 15	530 230 170	530 230 170	1060 460 340	ns
C_{IN}	Maximum Input Capacitance	-		5		pF

TIMING REQUIREMENTS (V_{CC}=5.0V±10%, C_L=50pF, Input t_r=t_f=20 ns, R_L=200kΩ)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	25°C	≤125°C	Unit
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	200 90 60	200 90 60	400 180 120	ns
t_r, t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	5.0 10 15	UNLIMITED			μs
t_w	Minimum Pulse Width, Reset (Figure 1)	5.0 10 15	260 110 60	260 110 60	520 220 120	ns
t_{rem}	Minimum Removal Time, Reset (Figure 1)	5.0 10 15	400 280 150	400 280 150	800 560 300	ns

t_{SU}	Minimum Setup Time, Clock Inhibit to Clock (Figure 1)	5.0 10 15	230 100 70	230 100 70	460 200 140	ns

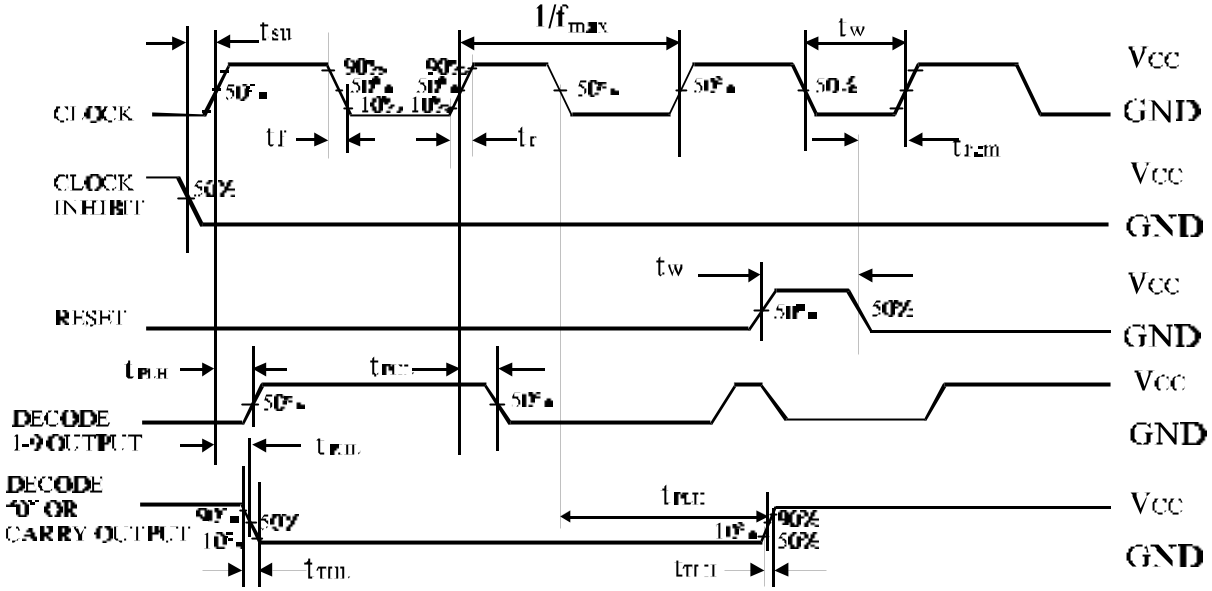
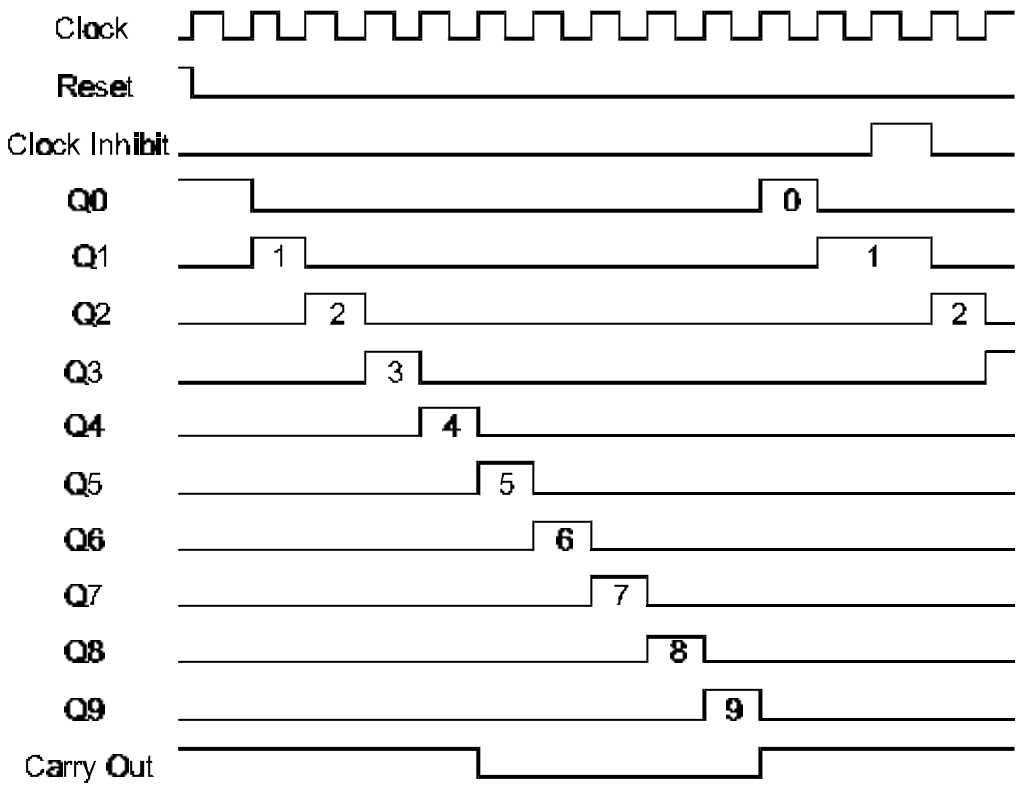


Figure 1. Switching Waveforms

Timing diagram



EXPANDED LOGIC DIAGRAM