

## Data Slicer for Teletext

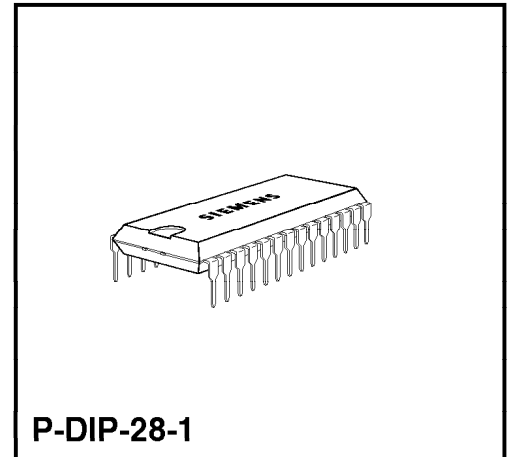
SDA 5231-5

### Preliminary Data

Bipolar IC

#### Features

- Crystal-stable data clock regeneration for a bit rate of 6.9375 MHz
- Separation and regeneration of teletext information
- Separation of the horizontal and vertical synchronization signals
- Phase-locked coupling of 6-MHz oscillator with comp. video
- Optional adjustment to 1 V or 2.5 V comp. video level
- Processing of externally separated teletext data
- Output of negative and positive synchronous signals to television set



Type	Ordering Code	Package
SDA 5231-5	Q 67000-A5162	P-DIP-28-1

The SDA 5231-5 has been designed to separate teletext signals from TV signals for a microcontroller-operated I<sup>2</sup>C bus concept. The video processor meets the requirements for teletext data clock regeneration and synchronization of the TV set during teletext operation. At the same time, the video signals (CVBS) provided by the television set are evaluated for the teletext decoder.

#### Functional Description

The SDA 5231-5 is used in an I<sup>2</sup>C bus controlled teletext system. Its function is the processing of the teletext informations, the system clock generation and the switching of HV synchronization signals.

The SDA 5231-5 can also be used to process the data line 16 (VPS).

## a) Signal Processing

The analog signal is processed at the amplitude filter (clamping of the video input signal and separation of the sync. impulse) and by means of the data slicing level. The data slicer compensates the attenuation of the data signal due to mistuning and a non linear frequency response the IF-amplifier.

As in case of sync. impulse separation, an adaptive circuit is used for separating the data, i.e. the clipping level is always in the middle of the sync. impulse and/or the data signal, independent of the signal amplitude.

Both the clipping level and the control voltage for the AGC (Automatic Gain Control) are generated while bit synchronization takes place at the beginning of the teletext line and are stored until the teletext line has been fully scanned.

## b) Synchronization of Data Clock

Clock synchronization is obtained by means of a phase detector + a phaseshifter.

A control voltage proportional to the phase difference between the free running oscillator and the incoming data bits is generated by the phase detector. A small time constant is used during bit synchronization, for the rest of the time a 10 times larger constant is used.

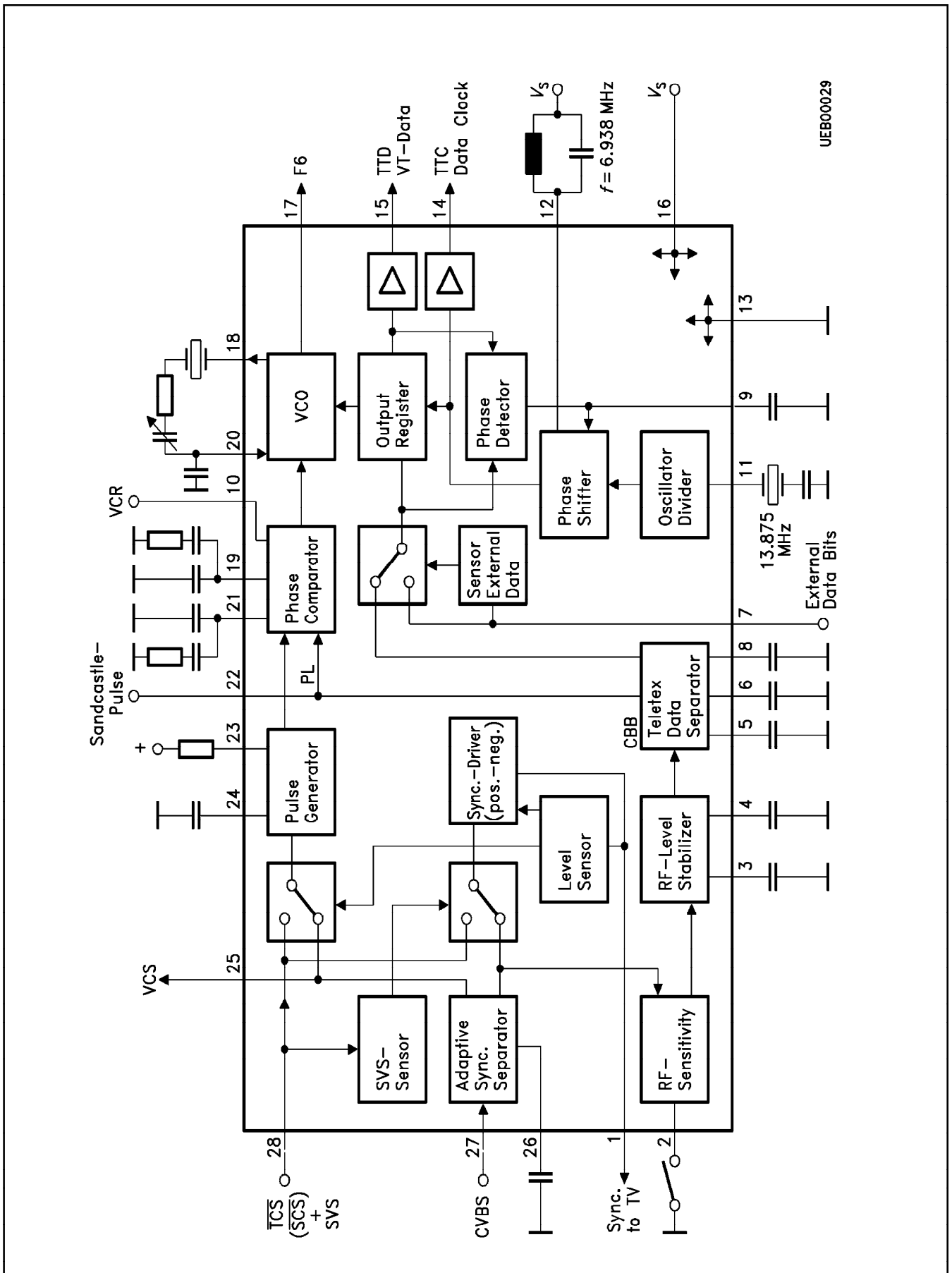
## c) Generation of 6-MHz System Clock

The teletext processor generates a picture pixel raster from the 6-MHz system clock. Thus, synchronization of the 6-MHz clock with the CVBS line frequency is necessary for any mixed-mode with teletext.

By shortening all sync. impulses to approximately  $2\ \mu\text{s}$ , interference from synchronization frame pulses can be avoided by means of a mono flop. The SANDCASTLE derived from the 6-MHz clock signal is synchronized in a phase-locked loop to the shortened sync. impulse. A shorter time constant is used during synchronization: If the CVBS signal is noisy or during after-hours operation, 2 points are important: Data acquisition has to be stopped, and the 6-MHz VCO must oscillate with its nominal frequency. For this purpose the teletext processor controls the VCS signal and switches off the signal component PL of the SANDCASTLE signal, if the CVBS signal is noisy or does not exist.

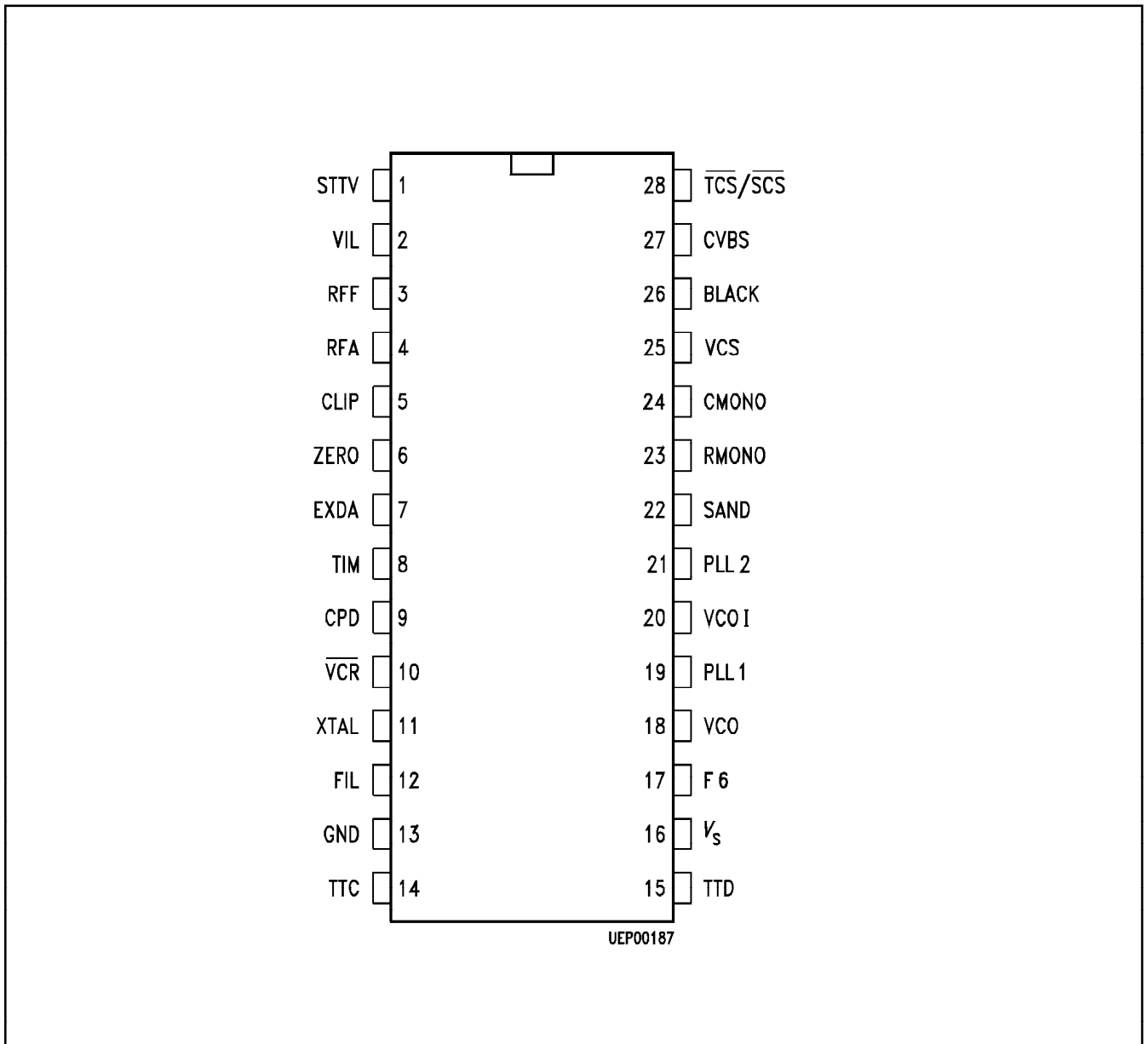
## d) Operating-Mode Switch

Operation Mode	Switch by	System Clock Sync. to	Usage
CVBS	Pin 28 = NC	CVBS	i.e. sub-titles
TCS	$V_{28} < 6.1\ \text{V}$	CVBS	interlace/non-interlace mode
SCS	Pin 1 = NC	SCS	Slave-Mode i.e. external synchronization



Block Diagram

**Pin Configuration**  
(top view)



## Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	STTV	Sync.-output	<b>Sync.-Output:</b> positive or negative synchronous signal to synchronize the TV set. Connection of load resistor to pin 1 (1.2 k $\Omega$ ) against $V_s$ = negative synchronous signal. Connection of load resistor to pin 1 against ground = positive synchronous signal.
2	VIL	Level selection	<b>CVBS Input Level Selection:</b> with LOW the gain is adjusted to a 1 V level and with an open input to 2.5 V level.
3	RFF	RF-filter	<b>RF-Level Stabilizer:</b> capacitor for filter time constant
4	RFA	RF-amplitude	<b>RF-Level Stabilizer:</b> capacitor for internal amplitude-dependent control voltage
5	CLIP	Clipping level	Input capacitor for <b>Clipping Level</b> of adapted <b>Data Separation</b>
6	ZERO	Zero level	Input capacitor for <b>Zero Level</b> of adapted <b>Data Separation</b>
7	EXDA	External teletext data	Data input for <b>External Teletext Data</b> (already separated)
8	TIM	Time characteristics	Capacitor for <b>Time Characteristics</b> of adapted <b>Data Separation</b>
9	CPD	Clock phase detector	<b>Clock Phase Detector:</b> connection for input capacitor
10	VCR	Video tape recorder mode	<b>Video Tape Recorder Mode:</b> switch-over to short horizontal hold-time constant
11	XTAL	Crystal	<b>13.875-MHz Crystal Connection:</b> frequency for double teletext data rate
12	FIL	Filter connection	<b>Filter Connection</b> for 6.9375-MHz data clock
13	GND	Ground	<b>Ground</b> (0 V)
14	TTC	TTC-output	<b>TTC Output</b>
15	TTD	TTD-output	<b>TTD Output</b>
16	$V_s$	$V_s$	<b>Supply Voltage +</b>
17	F6	F6-output	<b>F6 Output:</b> 6-MHz clock (signal with negligible harmonic wave)
18	VCO	VCO-output	<b>6-MHz VCO Output</b> for frequency-determining resonant circuit
19	PLL1	PLL-low-pass-filter	<b>PLL-Low-Pass-Filter</b> with small time-constant by async. operation (filter 2)

## Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function	Description
20	VCOI	VCO-input	<b>6-MHz VCO input</b> for frequency-determining resonant circuit
21	PLL2	PLL-low-pass-filter	<b>PLL-Low-Pass-Filter</b> with bigger time-constant for standard operation
22	SAND	Sandcastle pulse	<b>Sandcastle Pulse</b>
23	RMONO	R-Monoflop	<b>Chronology Resistor</b> of the monoflops
24	CMONO	C-Monoflop	<b>Chronology Capacitor</b> of the monoflops
25	VCS	VCS-output	<b>VCS-Output:</b> synchronous signal separated from comp. video
26	BLACK	Black level input capacitor	<b>Black Level Input Capacitor</b> for the adapted synchronous pulse separator
27	CVBS	CVBS-input	<b>CVBS Input Signal</b> via coupling capacitor with 1 V signal level when pin 2 is connected to ground
28	$\overline{TCS}/\overline{SCS}$	$\overline{TCS}$ -, ( $\overline{SCS}$ )-input	<b>Synchronous Signal-Input</b> $\overline{TCS}$ during text playback (or $\overline{SCS}$ , when pin 1 is open)

## Absolute Maximum Ratings

$T_A = 25\text{ °C}$  (all voltages are referred to  $V_{SS}$ )

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_{16/13}$		13.2	V
Storage temperature range	$T_{stg}$	- 40	125	°C
Output current VCS	$- I_{25H}$		5	mA
Output current TTD	$- I_{15H}$		10	mA
Output current TTC	$- I_{14H}$		10	mA
Output current F6	$- I_{17H}$		10	mA
Output current sync.	$I_1$		5	mA
Thermal resistance system-air	$R_{thSA}$		50	K/W

## Operating Range

Supply voltage	$V_{16/13}$	10.8	13.2	V
Ambient temperature in operation	$T_A$	0	70	°C

**Characteristics**

$T_A = 25^\circ\text{C}; V_S = 12\text{ V} \pm 10\%$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply current	$I_S$	53	70	100	mA

**CVBS Input, pin 27**

Input signal level					
Pin 2 to ground	$V_{27}$	0.7	1	1.4	V
Pin 2 open	$V_{27}$	1.75	2.5	3.5	V
Synchronous signal amplitude	$V_{27\text{ Sync}}$	0.1		1	V
Teletext data level					
Pin 2 to ground	$V_{27\text{ VTD}}$	0.3	0.46	0.7	V
Pin 2 open	$V_{27\text{ VTD}}$	0.75	1.15	1.75	V
Generator resistor	$R_{G27}$			250	$\Omega$

**Adaptation to CVBS Level**

Input voltage					
$V_{27} = 1\text{ V}$ when	$V_{2/13\text{ L}}$	0		0.8	V
$V_{27} = 2.5\text{ V}$ when	$V_{2/13\text{ H}}$	2.0		5.5	V
Input current					
	$-I_{2\text{L}}$	0		150	$\mu\text{A}$
	$I_{2\text{H}}$	0		1.3	mA

**Teletext Data**

Output signal TTD	$v_{15}$	2.5	3.5	4.5	V
Transition times	$t_r, t_f$	20	30	45	ns
Max. permissible capacitive load	$C_{15/13}$			40	pF
Data clock signal TTC	$v_{14}$	2.5	3.5	4.5	V
Transition times	$t_r, t_f$	20	30	45	ns
Max. permissible capacitive load	$C_{14/13}$			40	pF
Time deviation with respect to TTD	$t_d$	- 20	0	20	ns
DC voltage at outputs	$V_{14, 15/13}$		4		V



**Characteristics (cont'd)**

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	

**Synchronous Pulse Separation VCS**

(Signal at teletext decoder)

Output voltage	$V_{25L}$ $V_{25H}$	0 2.4		0.4 5.5	V V
Output current	$I_{25L}$ $-I_{25H}$			0.5 1.5	mA mA
Delay with respect to CVBS sync.	$t_d$		0.5		$\mu$ S

**Sync Output Driver**

(Signal at TV set)

Output voltage TCS operation	$V_1$		0.45		V
Comp. video operation	$V_1$			1	V
Positive synchronous signal DC voltage load resistor to ground	$V_{1/13}$	1.4			V
Output current	$-I_1$			3	mA
Negative synchronous signal DC voltage load resistor to $V_s$	$V_{1/13}$		10.1		V
Output current	$I_1$			3	mA

**6-MHz Clock F6**

F6-output signal (negligible harmonic content)	$V_{17}$	1	2	3	V
Transition times	$t_r, t_f$	20		40	ns
Max. permissible capacitive load	$C_{17/13}$			40	pF
DC voltage at output	$V_{17/13}$	4		8.5	V

**Synchronisation Selection SVS**

Input current during TCS operation $V_{28} = 0 \dots 6.1$ V CVBS <sup>1)</sup>	$-I_{28}$ $-I_{28}$	40	70	100	$\mu$ A $\mu$ A
CVBS $V_{28} = 10 \dots V_s$	$I_{28}$	-5		5	$\mu$ A

**TCS Operation**

Input voltage Load resistor at pin 1	$V_{28L}$	0		0.8	V
Load resistor at pin 1	$V_{28H}$	2		6.1	V

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	

SCS Operation

Input voltage Pin 1 open	$V_{28L}$	0		1.5	V
Pin 1 open	$V_{28H}$	3.5		6.1	V
Line synchronous pulse width TCS operation	$t_p$		2		$\mu\text{s}$
SCS operation	$t_p$		3		$\mu\text{s}$

VCR Operation

Input voltage during VCR operation	$V_{10/13L}$	0		0.8	V
Standard operation	$V_{10/13H}$	2		$V_s$	V
Input current	$I_{10}$	- 10	0	10	$\mu\text{A}$

Sandcastle Pulse Input

Phase locked mode Input voltage PL	$V_{22/13L}$	0		3	V
Input voltage PL	$V_{22/13H}$	3.9		5.5	V
PL-low-time for free-wheeling oscillator	$t_{PL}$	100			ms
Reset pulse for data separation Input voltage CBB	$V_{22/13L}$	0		0.5	V
Input voltage CBB	$V_{22/13H}$	1		5.5	V
Input current	$I_{22}$	- 10		10	$\mu\text{A}$

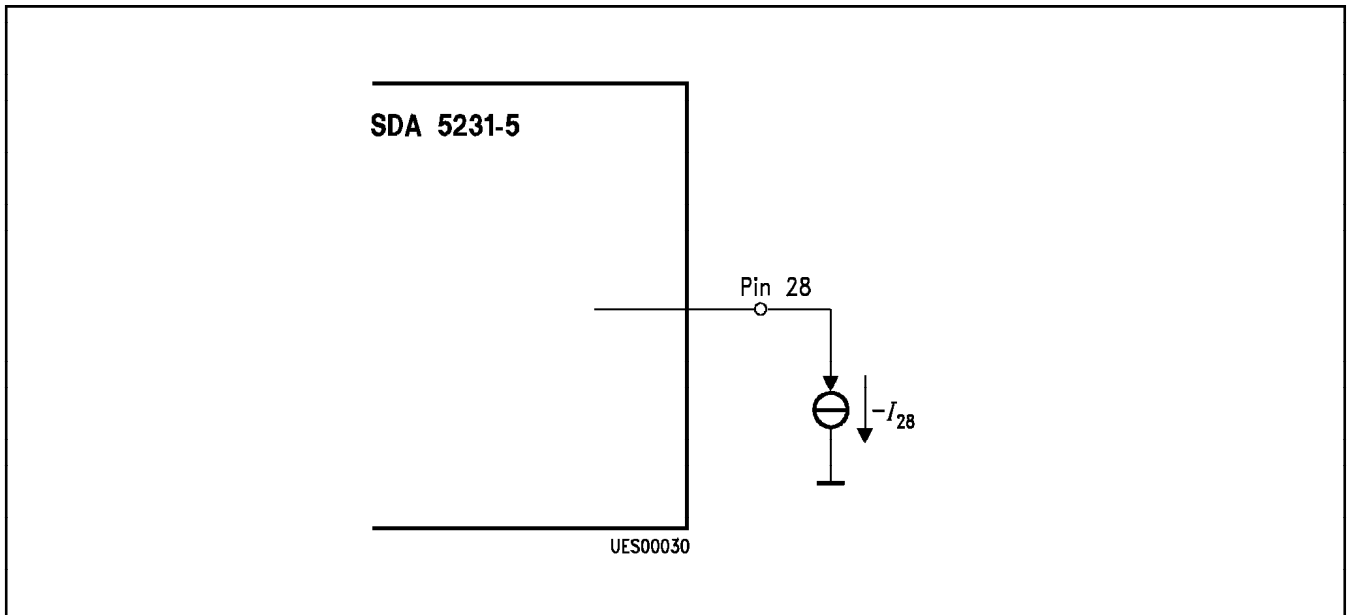
Input for External Data (current source driving)

Internal data processing Input current <sup>2)</sup> Voltage $I_7 = - 10$ to $+ 100 \mu\text{A}$	$I_7$ $V_7$	- 10	0	100	$\mu\text{A}$
External data processing Input current for low <sup>2)</sup> for high <sup>2)</sup> Voltage $I_7 = - 25$ to $- 1000 \mu\text{A}$	$I_{7L}$ $I_{7H}$ $V_7$	- 175 - 1000 7	- 40 - 500 8	- 25 - 325	$\mu\text{A}$ $\mu\text{A}$ V

1) **Remarks:** Test circuit 1

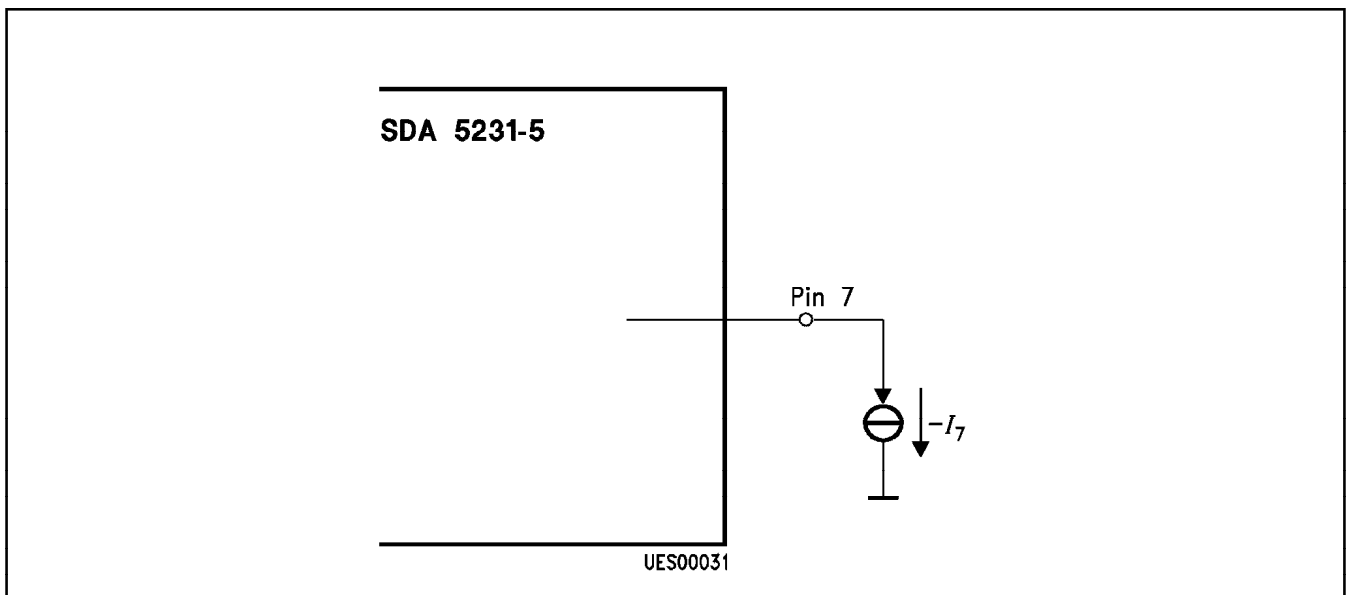
2) Test circuit 2

Test Circuits



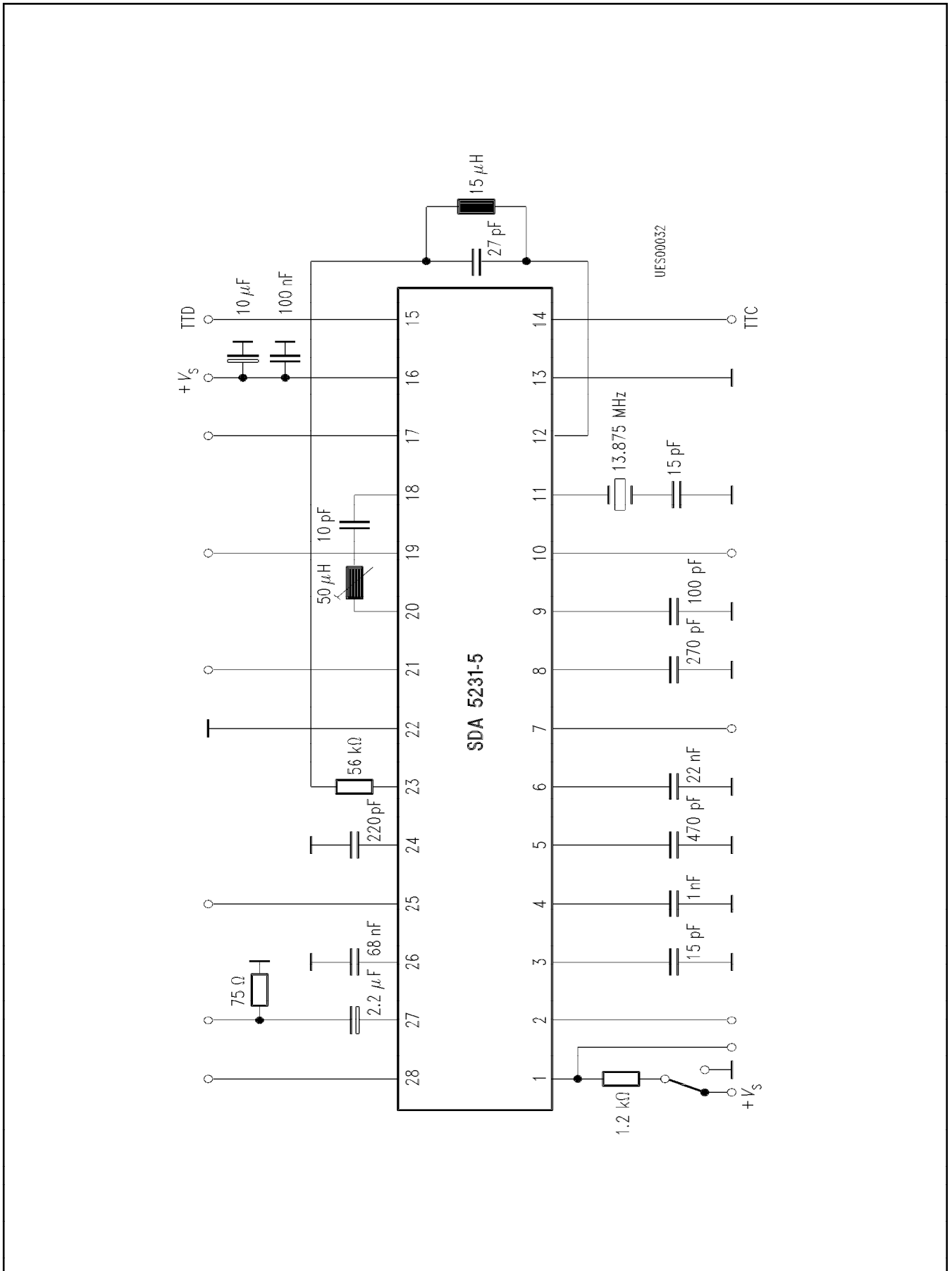
Test Circuit 1

During CVBS operation the output current of pin 28 shall not exceed  $15 \mu\text{A}$  (the pin 12 of the decoder SDA 5242-3 is high-impedance connected)

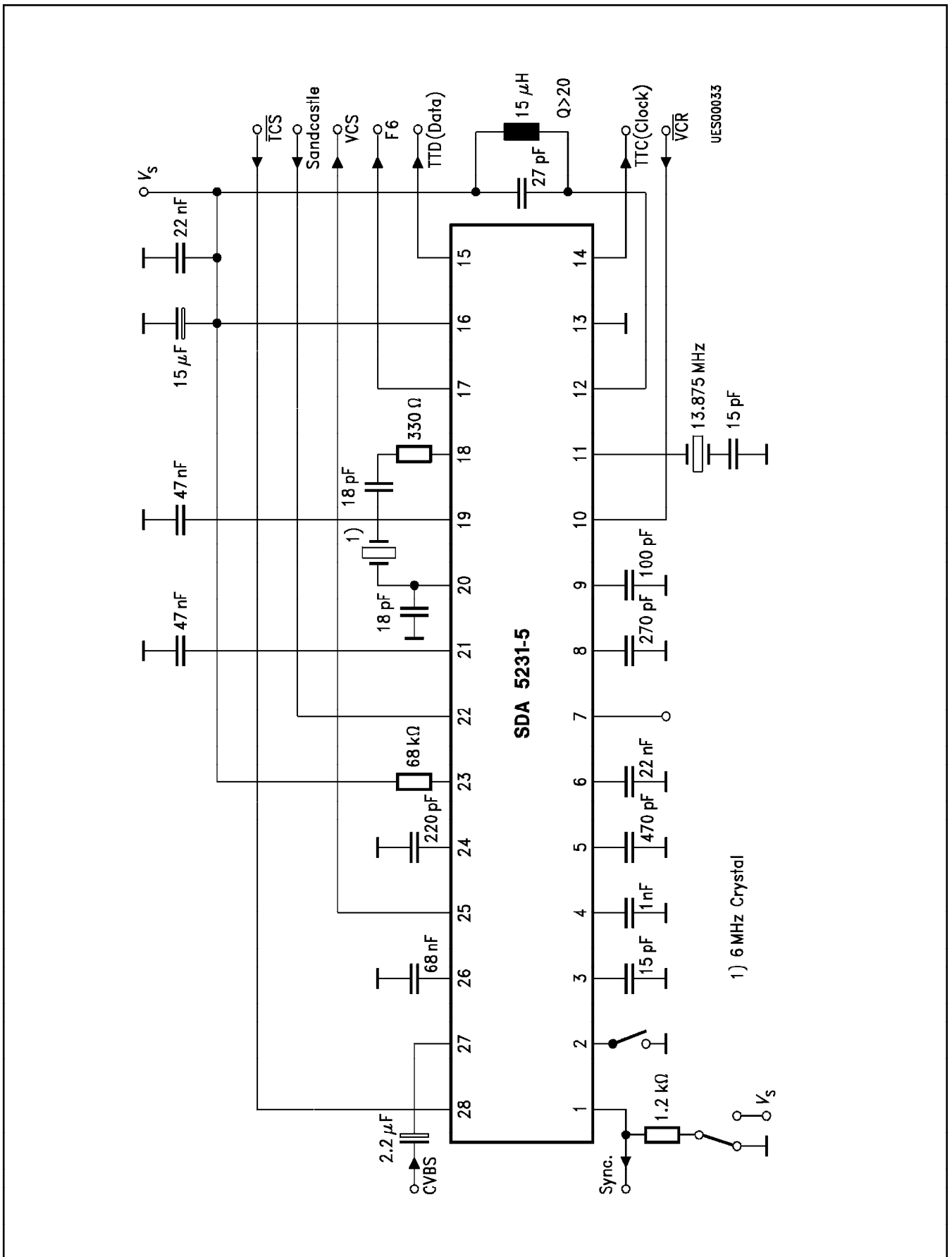


Test Circuit 2

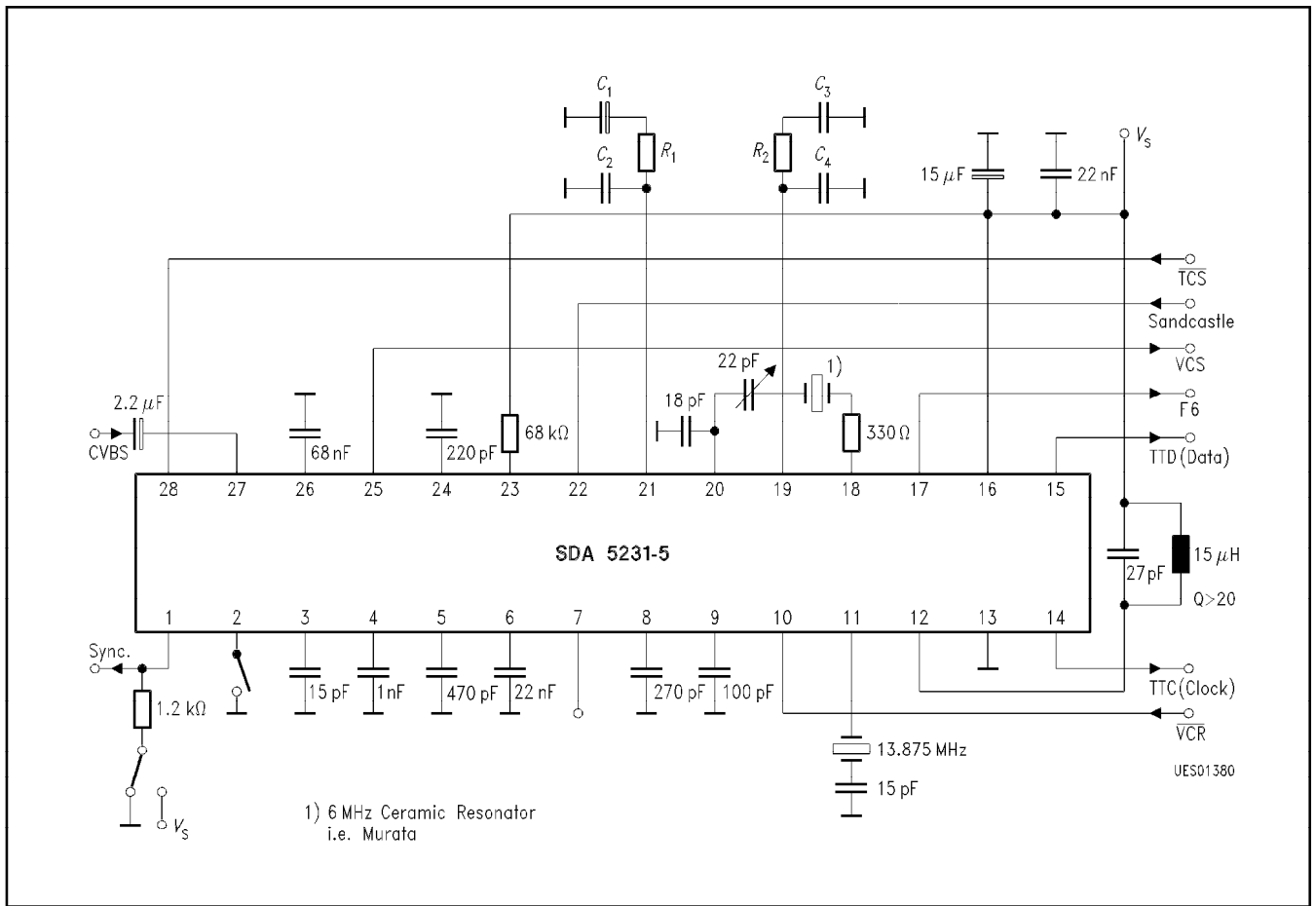
The output current of pin 7 cannot be higher than  $10 \mu\text{A}$  if the processing of the teletext data (which is in CVBS) must occur.



Test Circuit 3

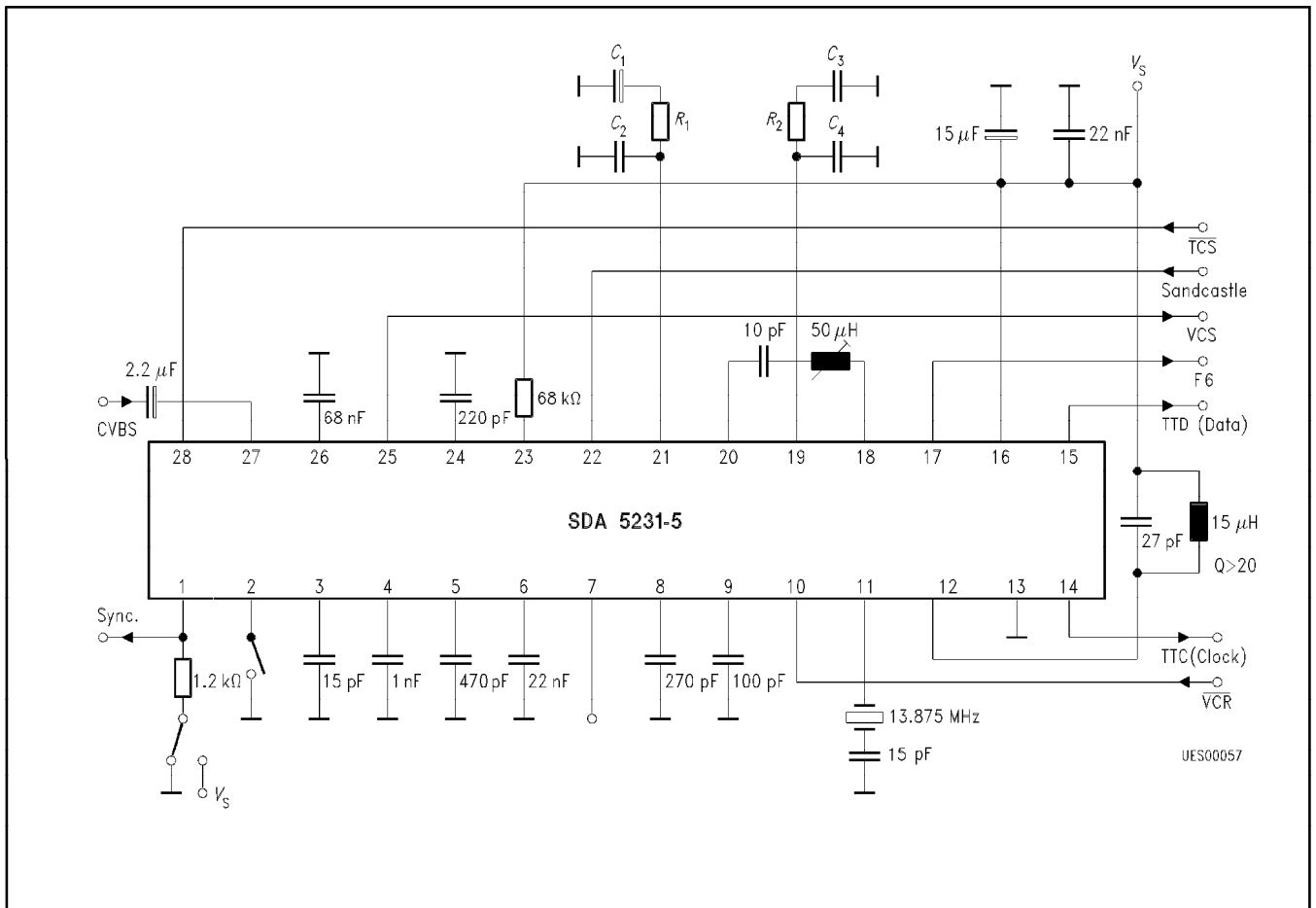


Application Circuit Crystal



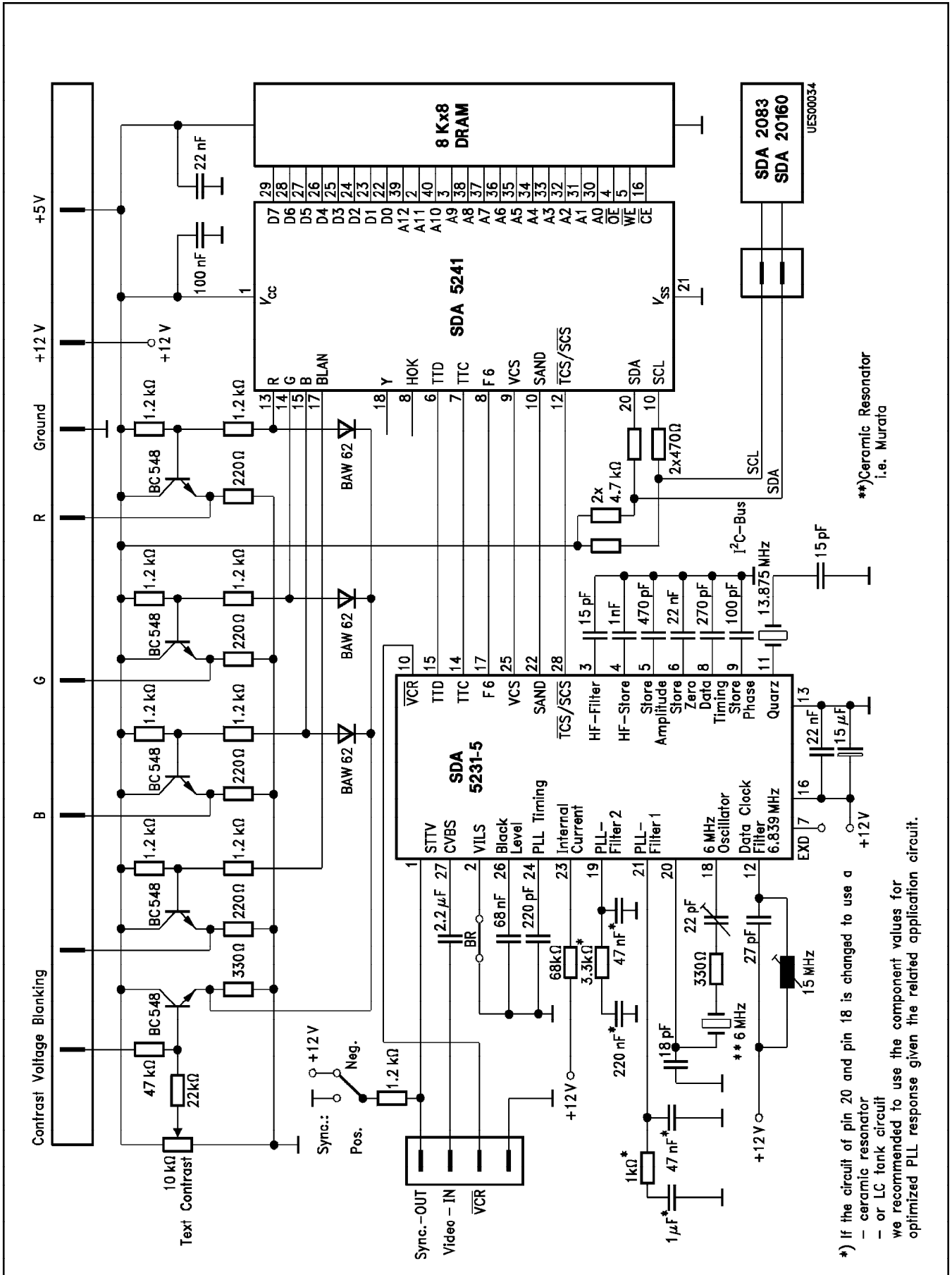
**Application Circuit Ceramic Resonator**

Loop Filter Components	Standard Application	Optimized PLL Behaviour
C <sub>1</sub>	1 μF	10 μF
C <sub>2</sub>	47 nF	1 μF
C <sub>3</sub>	220 nF	330 nF
C <sub>4</sub>	47 nF	33 nF
R <sub>1</sub>	1 kΩ	500 Ω
R <sub>2</sub>	3.3 kΩ	3.3 kΩ



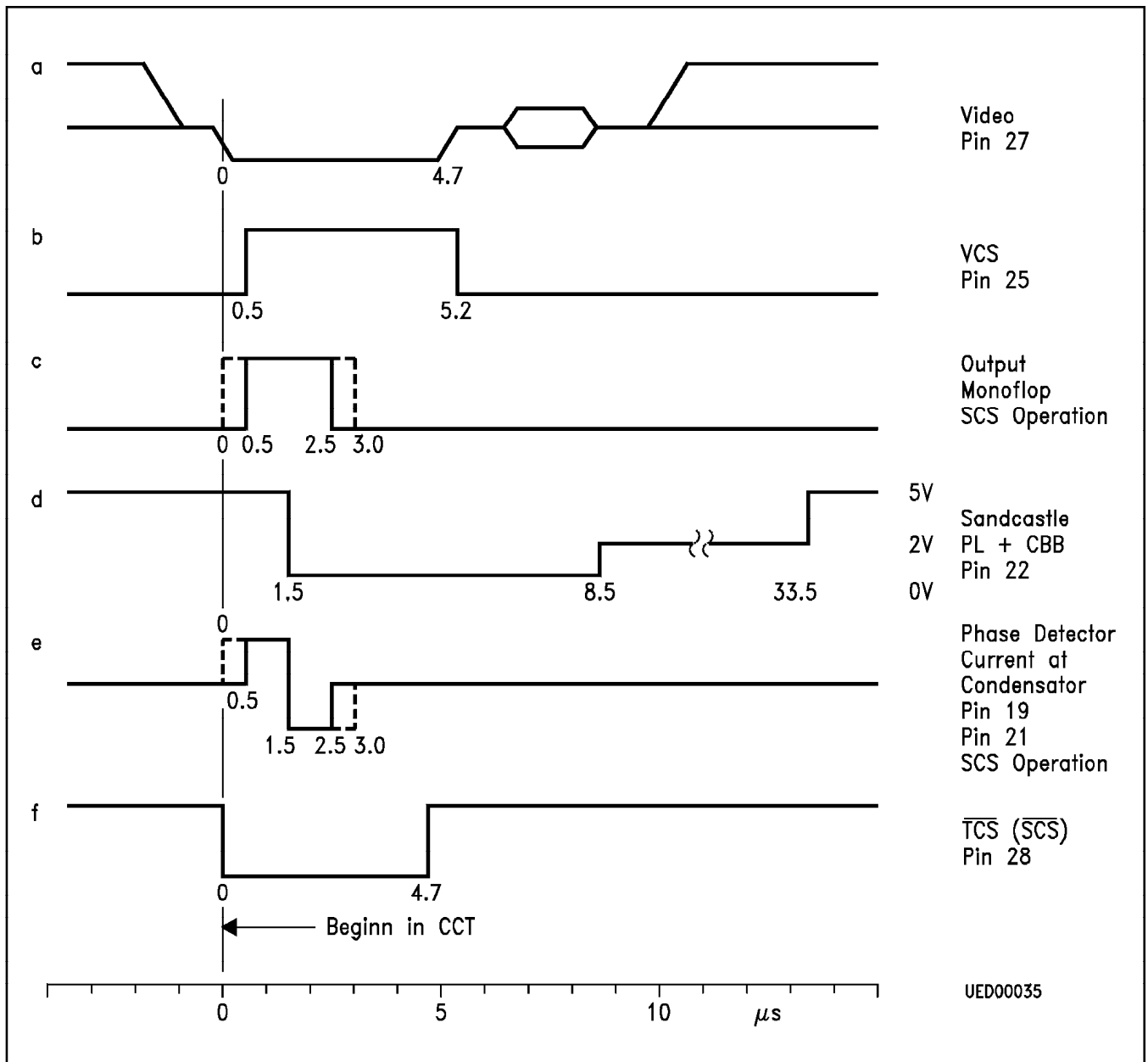
Application Circuit LC-Tank-Circuit

Loop Filter Components	Standard Application	Optimized PLL Behaviour
C <sub>1</sub>	47 μF	47 μF
C <sub>2</sub>	47 nF	4.7 μF
C <sub>3</sub>	47 nF	2.2 μF
C <sub>4</sub>	47 nF	220 nF
R <sub>1</sub>	82 Ω	82 Ω
R <sub>2</sub>	3,3 kΩ	390 Ω

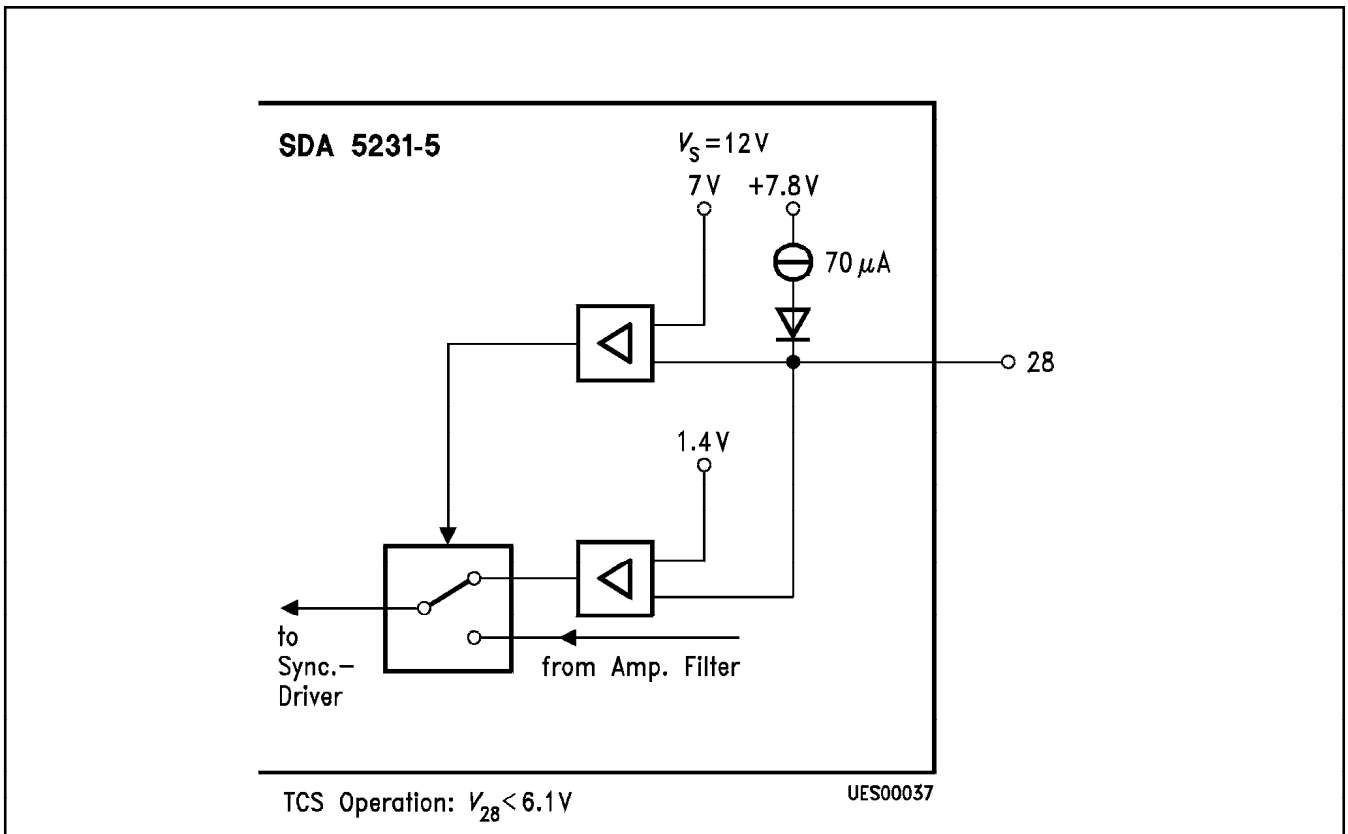


Application Circuit with SDA 5241

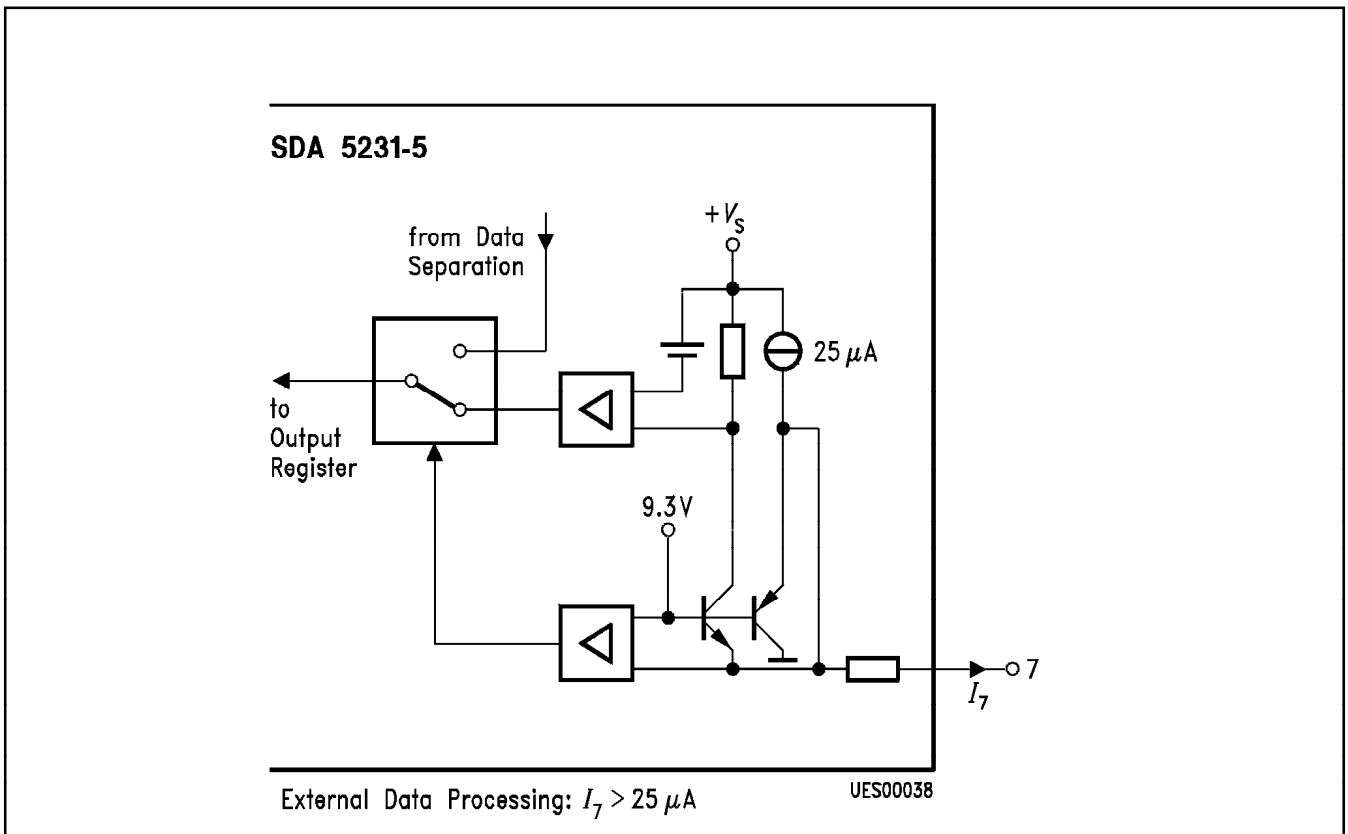




Pulse Diagrams



Pin 28



Pin 7