NEC

MOS FIELD EFFECT TRANSISTOR
μPA2707GR

SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The μPA2707GR is N-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of notebook computer.

FEATURES

- Low on-state resistance
  $R_{DS(on)1}$ = 4.3 mΩ MAX. (V_{GS} = 10 V, I_D = 9.0 A)
  $R_{DS(on)2}$ = 5.6 mΩ MAX. (V_{GS} = 4.5 V, I_D = 9.0 A)
- Low C_{iss}: C_{iss} = 6600 pF TYP. (V_{DS} = 10 V, V_{GS} = 0 V)
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2707GR-E1	Power SOP8
μPA2707GR-E1-A Note	Power SOP8
μPA2707GR-E2	Power SOP8
μPA2707GR-E2-A Note	Power SOP8

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±19	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	±76	A
Total Power Dissipation Note2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) Note2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current Note3	I_{AS}	19	A
Single Avalanche Energy Note3	E_{AS}	36	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω, L = 100 μH, V_{GS} = 20 → 0 V

THERMAL RESISTANCE

Channel to Ambient Note	$R_{th(ch-A)}$	114	°C/W
Channel to Drain Lead Note	$R_{th(ch-L)}$	22	°C/W

Note Mounted on glass epoxy board of 1 inch x 1 inch x 0.8 mm

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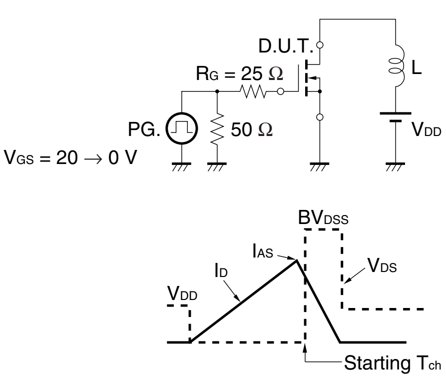
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

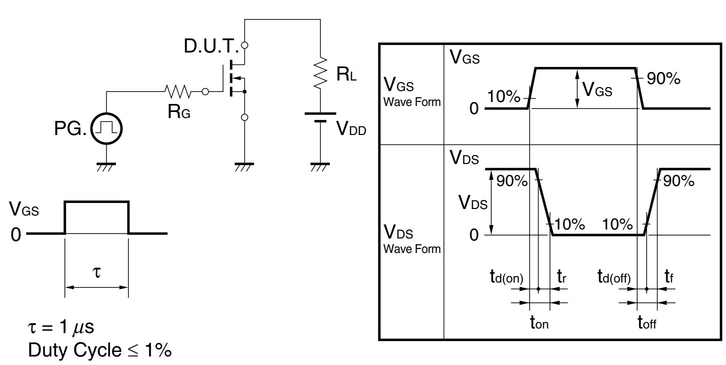
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0		2.5	V
Forward Transfer Admittance **Note**	$\| y_{fs} \|$	V_{DS} = 10 V, I_D = 10 A	12			S
Drain to Source On-state Resistance **Note**	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 10 A		3.3	4.3	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 10 A		4.1	5.6	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V		6600		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		970		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		530		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15 V, I_D = 10 A		24		ns
Rise Time	t_r	V_{GS} = 10 V		29		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		130		ns
Fall Time	t_f			39		ns
Total Gate Charge	Q_G	V_{DD} = 15 V		52		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 5 V		16		nC
Gate to Drain Charge	Q_{GD}	I_D = 19 A		18		nC
Body Diode Forward Voltage **Note**	$V_{F(S-D)}$	I_F = 19 A, V_{GS} = 0 V		0.8		V
Reverse Recovery Time	t_{rr}	I_F = 19 A, V_{GS} = 0 V		42		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		41		nC
Gate Resistance	R_G	f = 1 MHz		1.2		Ω

Note Pulsed

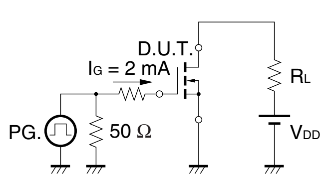
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

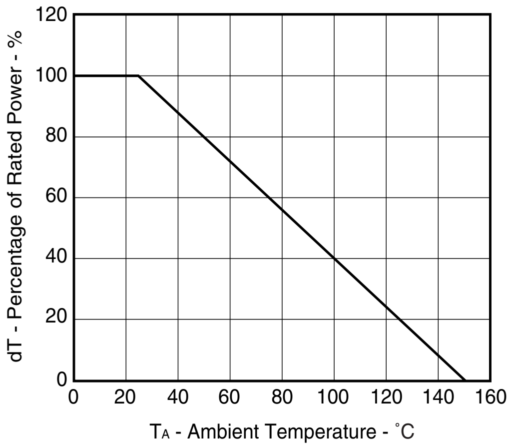


TEST CIRCUIT 3 GATE CHARGE

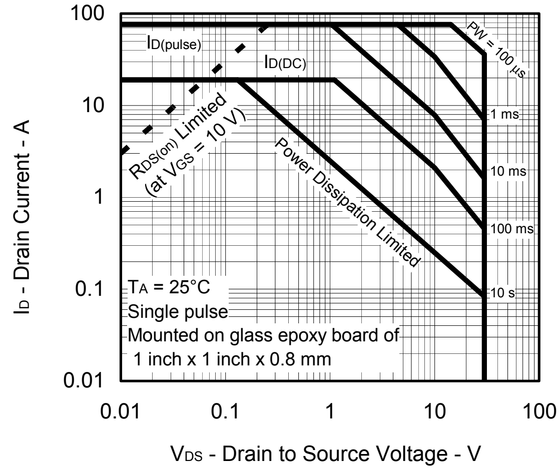


TYPICAL CHARACTERISTICS (T_A = 25°C)

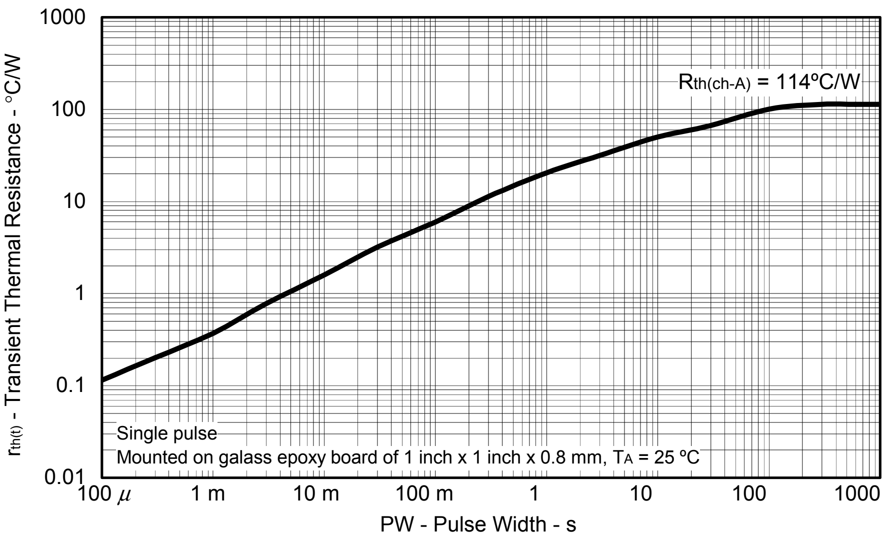
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



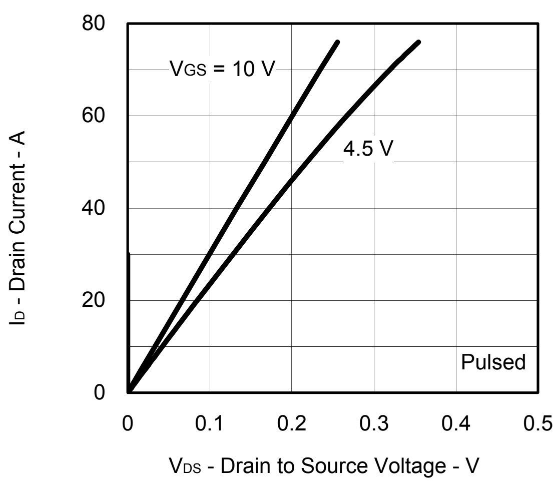
FORWARD BIAS SAFE OPERATING AREA



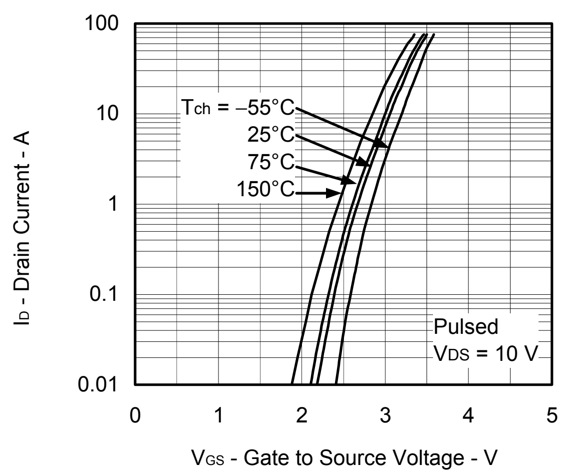
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



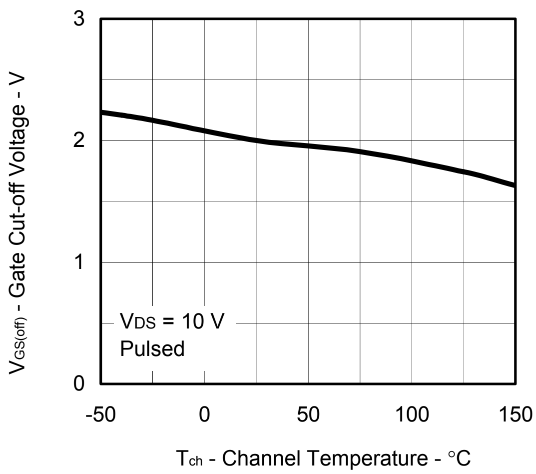
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



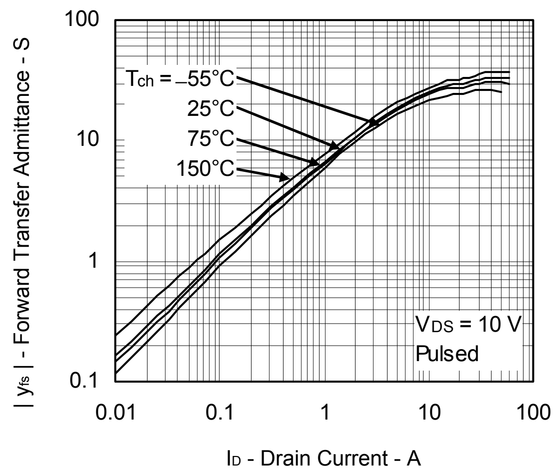
FORWARD TRANSFER CHARACTERISTICS



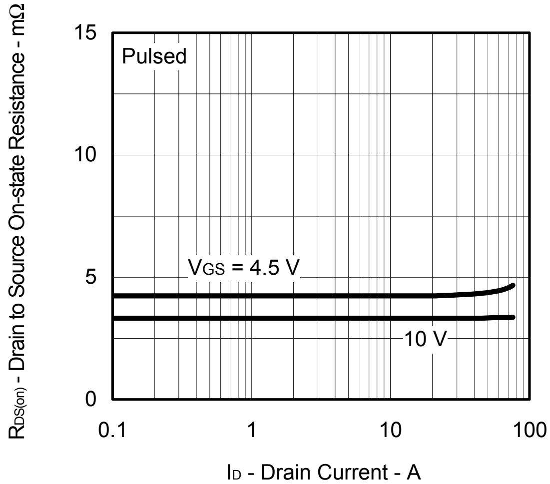
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



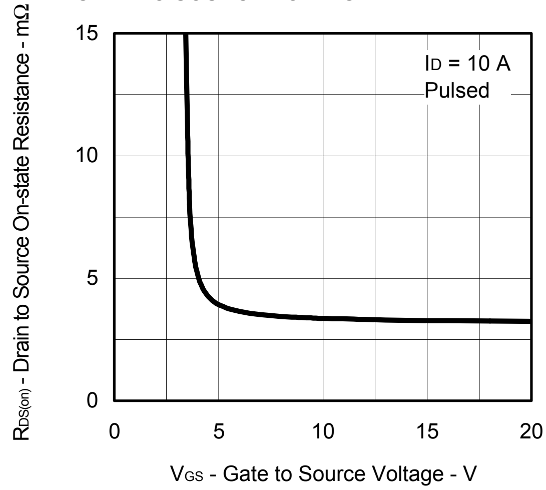
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



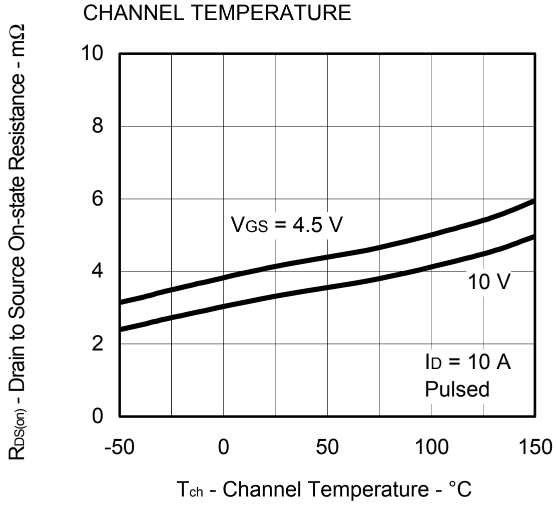
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



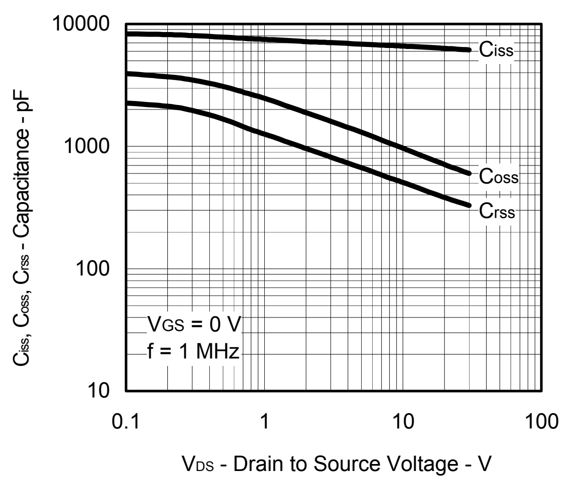
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



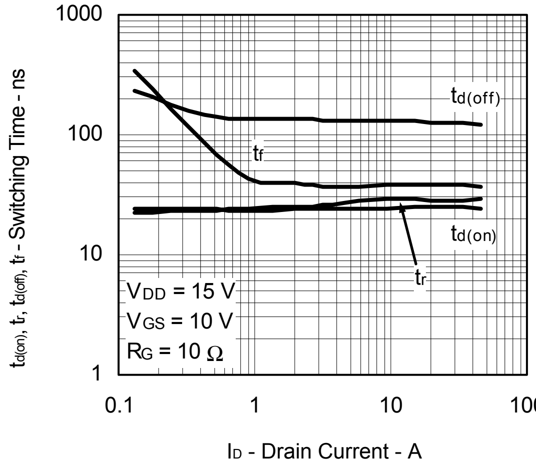
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



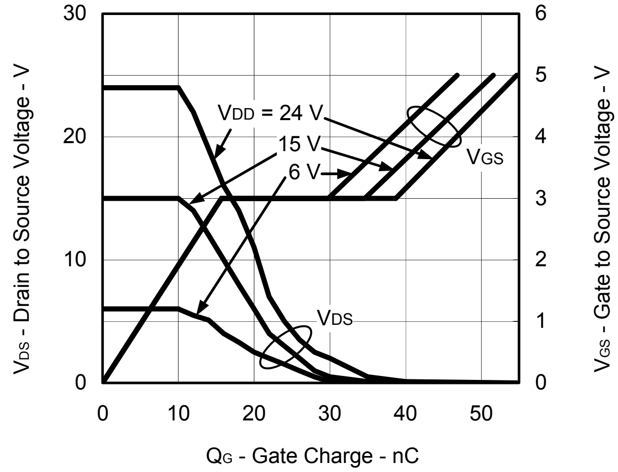
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



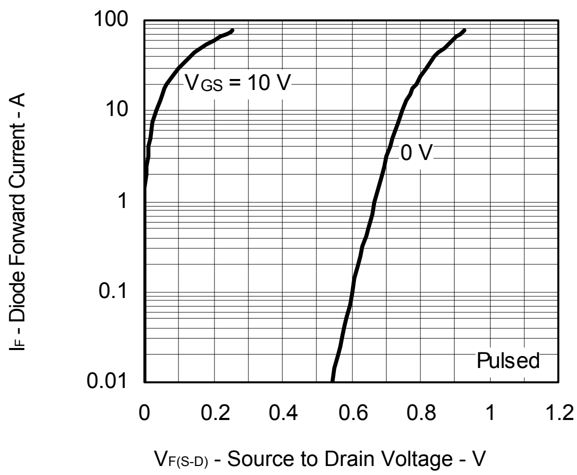
SWITCHING CHARACTERISTICS



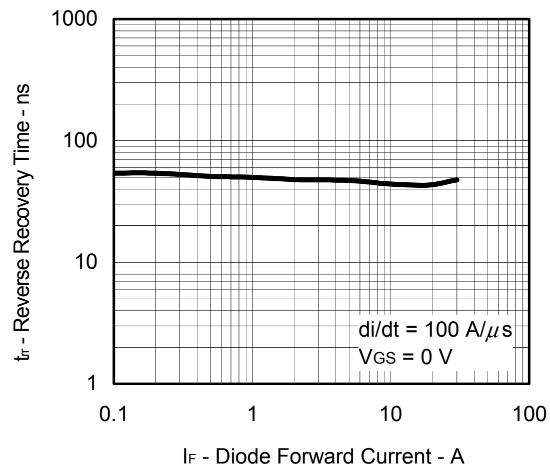
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



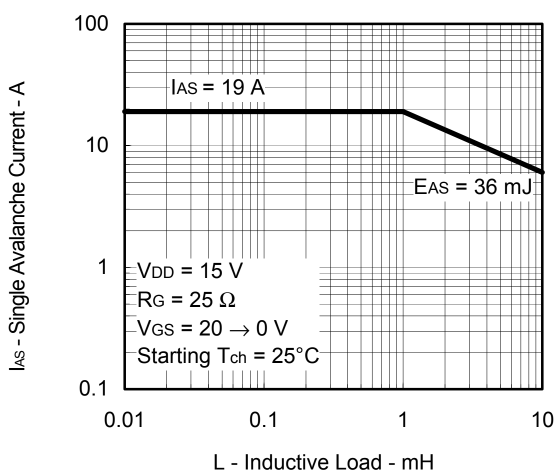
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



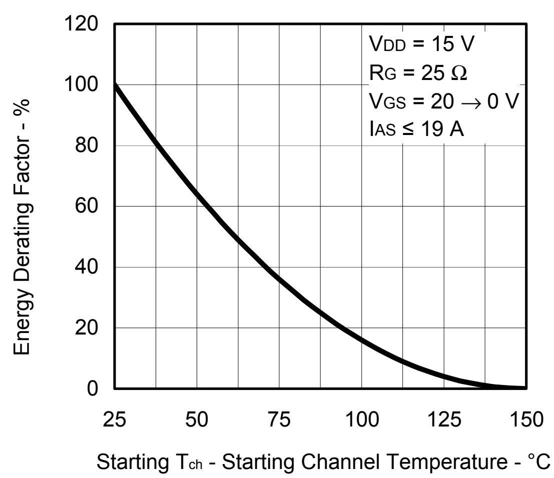
REVERSE RECOVERY TIME vs.
DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD

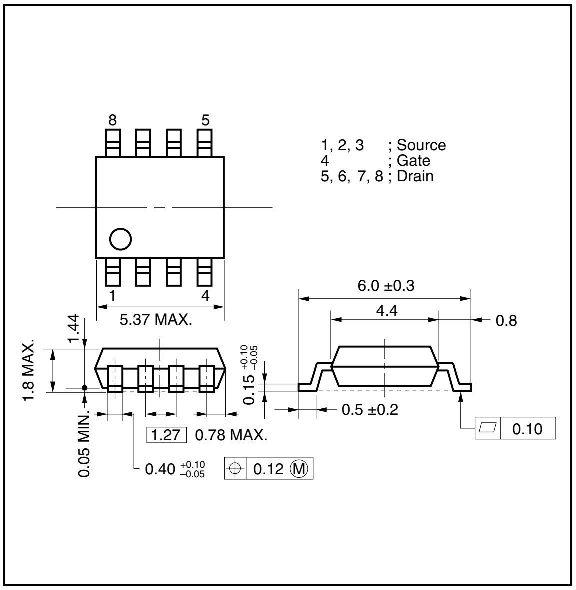


SINGLE AVALANCHE ENERGY
DERATING FACTOR

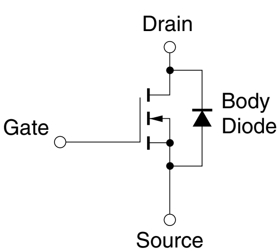


PACKAGE DRAWING (Unit: mm)

Power SOP8



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.