

MOS FIELD EFFECT TRANSISTOR μ PA2503

N-CHANNEL MOS FIELD EFFECT TRANSISTOR FOR SWITCHING

DESCRIPTION

The μ PA2503, which has a heat spreader, is N-channel MOS Field Effect Transistor designed for power management applications of notebook computers.

FEATURES

- μ PA2503 has a thin surface mount package with a heat spreader. The land size is same as 8-pin TSSOP.
- Low on-state resistance

 $R_{DS(on)1}$ = 9.5 m Ω MAX. (VGS = 10.0 V, ID = 8.0 A)

 $R_{DS(on)2} = 15.1 \text{ m}\Omega \text{ MAX.} \text{ (V}_{GS} = 4.5 \text{ V}, I_D = 8.0 \text{ A)}$

• Low Ciss: 1200 pF TYP. (VDS = 10.0 V, VGS = 0 V)

ORDERING INFORMATION

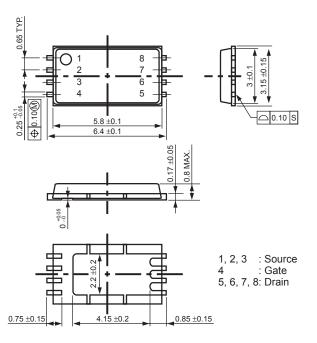
PART NUMBER	PACKAGE
μ PA2503TM	8PIN HWSON

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

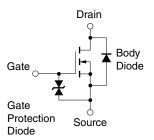
Drain to Source Voltage (Vgs = 0 V)	VDSS	30.0	V
Gate to Source Voltage (VDS = 0 V)	Vgss	±20.0	V
Drain Current (DC) Note1	ID(DC)	±16.0	Α
Drain Current (pulse) Note2	ID(pulse)	±64.0	Α
Total Power Dissipation Note1	PT	2.7	W
Channel Temperature	Tch	150	°C
Storage Temperature	Tstg	-55 to +150	°C
Single Avalanche Current Note3	las	16.0	Α
Single Avalanche Energy Note3	Eas	25.6	mJ

- **Notes 1.** Mounted on FR-4 board of 25 cm² x 1.6 mm, PW \leq 10 sec
 - **2.** PW \leq 10 μ s, Duty Cycle \leq 1%
 - 3. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20.0 \rightarrow 0 V

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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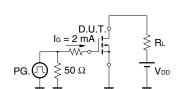
ELECTRICAL CHARACTERISTICS (TA = 25°C)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 30.0 V, V _{GS} = 0 V			1.0	μΑ
Gate Leakage Current	Igss	V _{GS} = ±18.0 V, V _{DS} = 0 V			±10.0	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10.0 V, I _D = 1.0 mA	1.5		2.5	V
Forward Transfer Admittance Note	y fs	V _{DS} = 10.0 V, I _D = 8.0 A	5			S
Drain to Source On-state Resistance Note	RDS(on)1	V _{GS} = 10.0 V, I _D = 8.0 A		7.5	9.5	mΩ
	RDS(on)2	V _{GS} = 4.5 V, I _D = 8.0 A		11.0	15.1	mΩ
Input Capacitance	Ciss	V _{DS} = 10.0 V		1200		pF
Output Capacitance	Coss	V _{GS} = 0 V		320		pF
Reverse Transfer Capacitance	Crss	f = 1.0 MHz		190		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15.0 V, I _D = 8.0 A		12		ns
Rise Time	t r	V _{GS} = 10.0 V		17		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		52		ns
Fall Time	t _f			15		ns
Total Gate Charge	Q _G	V _{DD} = 15.0 V		15		nC
Gate to Source Charge	Qgs	V _{GS} = 5.0 V		4		nC
Gate to Drain Charge	Q _{GD}	I _D = 16.0 A		7		nC
Body Diode Forward Voltage Note	V _F (S-D)	I _F = 16.0 A, V _{GS} = 0 V		0.84		٧
Reverse Recovery Time	trr	I _F = 16.0 A, V _{GS} = 0 V		28		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		18		nC

Note Pulsed: PW \leq 350 μ s, Duty Cycle \leq 2%

TEST CIRCUIT 1 AVALANCHE CAPABILITY

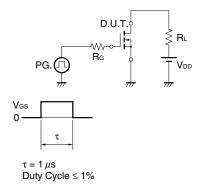
$V_{GS} = 20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD} V_{DD}

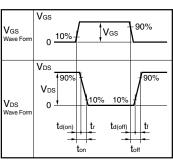


TEST CIRCUIT 3 GATE CHARGE

Starting Tch

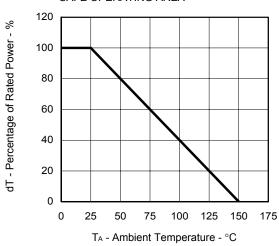
TEST CIRCUIT 2 SWITCHING TIME



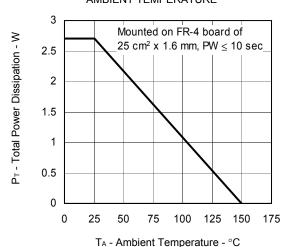


TYPICAL CHARACTERISTICS (TA = 25°C)

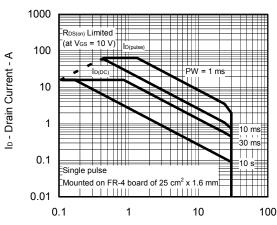
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

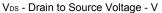


TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

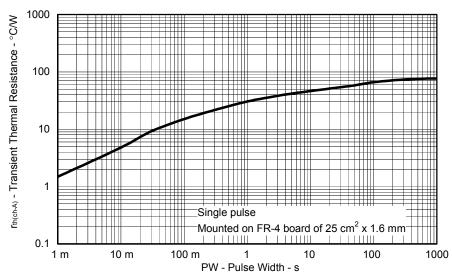


FORWARD BIAS SAFE OPERATING AREA





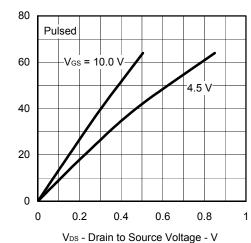
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



Ip - Drain Current - A

VGS(off) - Gate Cut-off Voltage - V

DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



1 0.01 Table 10 0.01 0.01

V_{DS} = 10.0 V Pulsed

100

10

0.001

1

1.5

2

V_{GS} - Gate to Source Voltage - V

3

3.5

4

4.5

2.5

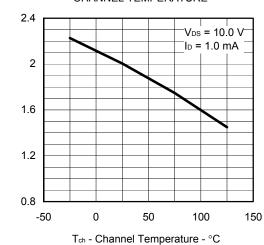
FORWARD TRANSFER CHARACTERISTICS

= 125°C

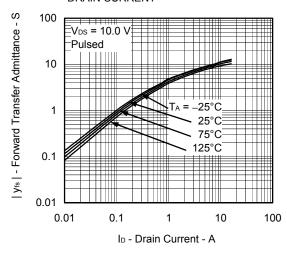
75°C

25°C -25°C

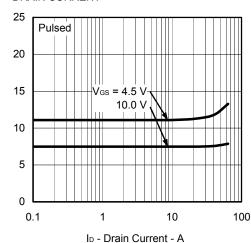
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



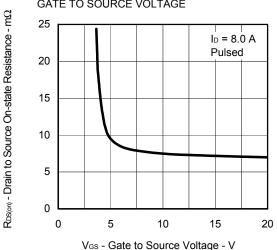
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

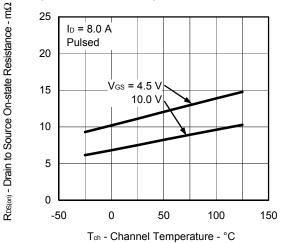


DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

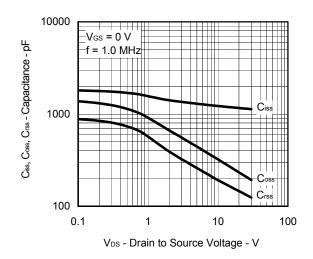


R_{DS(on)} - Drain to Source On-state Resistance - mΩ

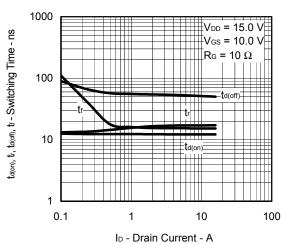
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



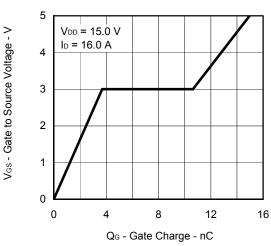
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



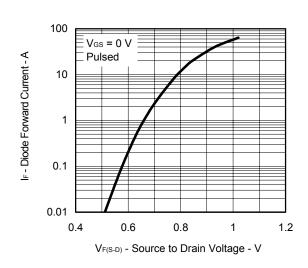
SWITCHING CHARACTERISTICS



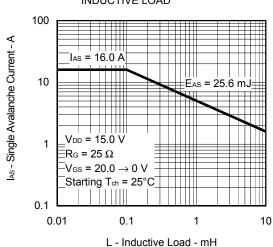
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



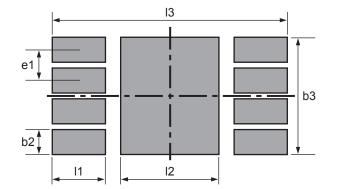
e1: 0.65 b2: 0.35 b3: 2.7 l1: 1.3

I2: 3.7 I3: 7.1

(Unit: mm)

EXAMPLE OF THE LAND PATTERN

Please optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.



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