Features

- **ARM7TDMI® ARM® Thumb® Processor Core**
- **Two 16-bit Fixed-point OakDSPCore® Cores**
- **256 x 32-bit Boot ROM**
- **88K Bytes of Integrated Fast RAM for Each DSP**
- **Flexible External Bus Interface with Programmable Chip Selects**
- **Dual Codec Interface**
- **Multi-level Priority, Individually Maskable, Vectored Interrupt Controller**
- **Three 16-bit Timers/Counters**
- **Additional Watchdog Timer**
- **Two USARTs with FIFO and Modem Control Lines**
- **Industry -standard Serial Peripheral Interface (SPI)**
- **Up to 24 General-purpose I/O Pins**
- **On-chip SDRAM Controller for Embedded ARM7TDMI and OakDSPCore**
- **JTAG Debug Interface**
- **Software Development Tools Available for ARM7TDMI and OakDSPCore**
- **Supported by a Wide Range of Ready-to-use Application Software, including Multitasking Operating System, Networking, Modems and Voice Processing Functions**
- **Available in 160-lead PQFP Package**
- **2.5V Power Supply for the core and the PLL Pins, 3.3V Power Supply for Other I/O Pins**

Description

The Atmel AT75C320 Smart Internet Appliance Processor (SIAP™) is a high-performance processor specially designed for Internet appliance applications, such as Internet telephony (Voice-over-Internet Protocol – VoIP). The AT75C320 is a derivative version of the AT75C310. The device is built around an ARM7TDMI microcontroller core running at 40 MIPS with two DSP co-processors running at 60 MIPS each – all three processors delivering unmatched performance for low power consumption.

In a typical standalone VoIP phone, one DSP handles the voice processing functions (voice compression, acoustic echo cancellation, etc.), while the other one deals with the telephony functions (dialing, line echo cancellation, callerID detection, high-speed modem, etc.). In such an application, the power of the ARM7TDMI allows it to run the VoIP protocol stack as well as all the system control tasks.

Atmel provides the AT75C320 with three levels of software modules:

- a special port of the Linux® kernel as the proposed operating system;
- a comprehensive set of tunable DSP algorithms for modems and voice processing, specially tailored to be run by the DSP subsystems;
- a broad range of application level software modules such as H.323 telephony or POP-3/SMTP e-mail services.

Smart Internet Appliance Processor (SIAP™)

AT75C320

Preliminary

Rev. 1769A–07/01

AT75C320 Pin Configuration

Table 1. AT75C320 Pinout in PQFP160 Package

Pin	PQFP160
1	NC
2	NC
3	D10
4	D11
5	NCE3
6	D12
7	D13
8	SRXB
9	NWE0
10	GND
11	VDD3V3
12	D14
13	D15
14	NC
15	NWE1
16	NC
17	VDD2V5
18	GND
19	VDD2V5
20	XTALIN
21	XTALOUT
22	GND
23	PLL_GND
24	XREF240
25	PLL_VDD2V5
26	GND
27	VDD2V5
28	RXDA
29	TXDA
30	NRTSA
31	NCTSA
32	NDCDB
33	NDTRA
34	NDSRA
35	GND
36	VDD3V3
37	NDCDA
38	TXDB
39	RXDB
40	PB7

Pin	PQFP160
41	NC
42	PB6/NWDOVF
43	PB5/NRIA
44	PB4
45	PB3/NCTSA
46	DBW32
47	GND
48	VDD3V3
49	RESET
50	IRQ0
51	PB2/TIOB1
52	PB9
53	PB1/TIOA1
54	PB8
55	PB0/TCLK1
56	VDD2V5
57	GND
58	TST
59	NTRST
60	TCK
61	TMS
62	TDI
63	TDO
64	PA0/OakAIN0
65	PA1/OakAIN1
66	PA2/OakAOUT0
67	PA3/OakAOUT1
68	PA19/ACLK
69	PA4/OakBIN0
70	GND
71	VDD3V3
72	PA5/OakBIN1
73	PA6/OakBOUT0
74	PA7/OakBOUT1
75	PA8/TCLK0
76	PA9/TIOA0
77	PA10/TIOB0
78	PA11/SCKA
79	NC
80	NC

Pin	PQFP160
81	PA12/NPCS1
82	VDD2V5
83	GND
84	A0
85	A1
86	A2
87	A3
88	VDD3V3
89	BO208
90	NWR
91	NWAIT
92	NREQ
93	FIQ
94	NGNT
95	SCLKA
96	FSA
97	STXA
98	SRXA
99	A4
100	A5
101	A6
102	A7
103	NPCSS
104	SPCK
105	MISO
106	MOSI
107	VDD3V3
108	GND
109	VDD2V5
110	GND
111	A8
112	A9
113	A10
114	A11
115	A12
116	VDD3V3
117	GND
118	A13
119	A14
120	A15

Pin	PQFP160
121	NC
122	NC
123	A16
124	A17
125	A18
126	A19
127	A20
128	A21
129	VDD2V5
130	GND
131	VDD3V3
132	D0
133	DQM0
134	D1
135	DQM1
136	D2
137	D3
138	D4
139	RAS
140	CAS
141	CS0
142	CS1
143	DCK
144	WE
145	D5
146	STXB
147	FSB
148	SCLKB
149	D6
150	D7
151	GND
152	VDD3V3
153	NCE0
154	D8
155	D9
156	NSOE
157	GND
158	GND
159	NC
160	NC

AT75C320 Pin Description

Table 2. AT75C320 Pin Description

Block	PQFP Pin Name	Type	Function
Common Bus	A[21:0]	O	Address Bus
	D[15:0]	I/O	Data Bus
	NREQ	I	Bus Request
	NGNT	O	Bus Grant
Synchronous Dynamic Memory Controller	DCK	O	SDRAM Clock
	DQM[1:0]	O	Memory Data Byte Masks
	CS0	O	SDRAM Chip Select
	CS1	O	SDRAM Chip Select
	WE	O	SDRAM Write Enable
	RAS	O	Row Address Select
	CAS	O	Column Address Select
Static Memory Controller	NCE0, NCE3	O	Chip Selects
	NWE[1:0]	O	Byte Select/Write
	NSOE	O	Enable Output
	NWR	O	Enable Memory Block Write
	NWAIT	I	Enable Enable Wait States
I/O Port A	PA[12:0], PA19	I/O	General Purpose I/O Lines. Multiplexed with Peripheral I/Os
I/O Port B	PB[9:0]	I/O	General Purpose I/O Lines. Multiplexed with Peripheral I/Os
DSP Subsystem A	OakAIN[1:0]	I	OakDSPCore A User Inputs
	OakAOUT[1:0]	O	OakDSPCore A User Outputs
DSP Subsystem B	OakBIN[1:0]	I	OakDSPCore B User Inputs
	OakBOUT[1:0]	O	OakDSPCore B User Outputs
Timer/Counter 0	TCLK0	I	Timer 0 External Clock
	TIOA0	I/O	Timer 0 Signal A
	TIOB0	I/O	Timer 0 Signal B
Timer/Counter 1	TCLK1	I	Timer 1 External Clock
	TIOA1	I/O	Timer 1 Signal A
	TIOB1	I/O	Timer 1 Signal B
Watchdog	NWDOVF	O	Watchdog Overflow
Serial Peripheral Interface	MISO	I/O	Master In/Slave Out
	MOSI	I/O	Master Out/Slave In
	SPCK	I/O	Serial Clock
	NPCSS	I/O	Chip Select/Slave Select

Table 2. AT75C320 Pin Description (Continued)

Block	PQFP Pin Name	Type	Function
USART A	RXDA	I	Receive Serial Data
	TXDA	O	Transmit Serial Data
	NRTSA	O	Request to Send
	NCTSA	I	Clear To Send
	NDTRA	O	Data Terminal Ready
	NDSRA	I	Data Set Ready
	NDCDA	I	Data Carrier Detect
	NRIA	I	Ring Indicator
	SCKA	I/O	Serial Clock
USART B	RXDB	I	Receive Serial Data
	TXDB	O	Transmit Serial Data
JTAG Interface	NTRST	I	TAP Reset
	TCK	I	TAP Clock
	TMS	I	JTAG Test Mode Select
	TDI	I	JTAG Test Data Input
	TDO	O	JTAG Test Data Output
Codec Interface A	SCLKA	I/O	Codec Serial Clock
	FAS	I/O	Frame Pulse
	STXA	O	Transmit Data to Codec
	SRXA	I	Receive Data from Codec
Codec Interface B	SCLKB	I/O	Codec Serial Clock
	FSB	I/O	Frame Pulse
	STXB	O	Transmit Data to Codec
	SRXB	I	Receive Data from Codec
Miscellaneous	RESET	I	Master Reset
	FIQ/LOWP	I	Fast Interrupt/Low Power
	IRQ0	I	External Interrupt request
	XREF	I	External 96 MHz PLL Reference
	XTALIN	I	External Crystal Input
	XTALOUT	O	External Crystal Output
	TST	I	Test Mode
	DBW32	I	External Data Width for CS0
	BO206	I	Package Size Option

Block Diagram

Figure 1. AT75C320 Block Diagram

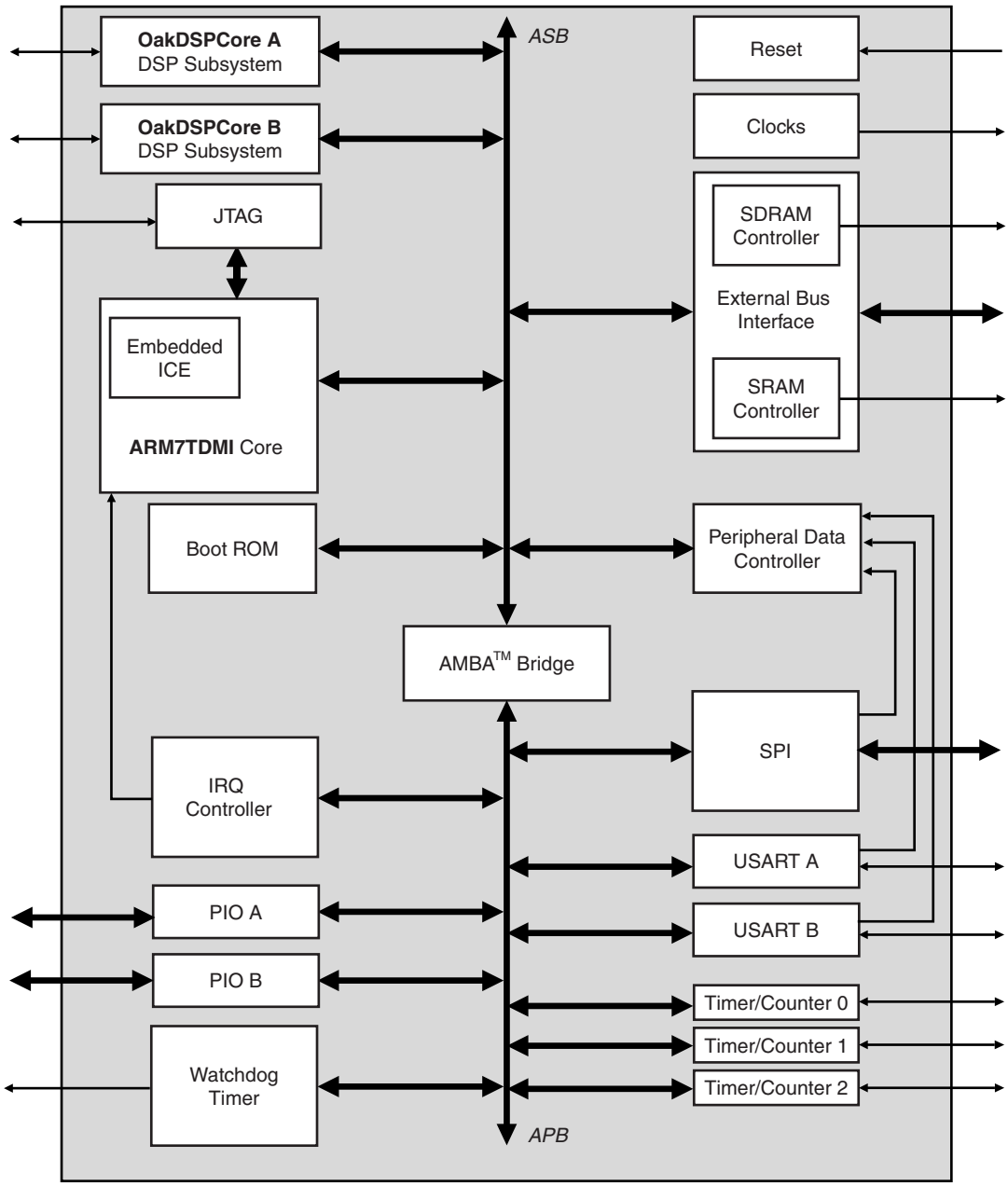
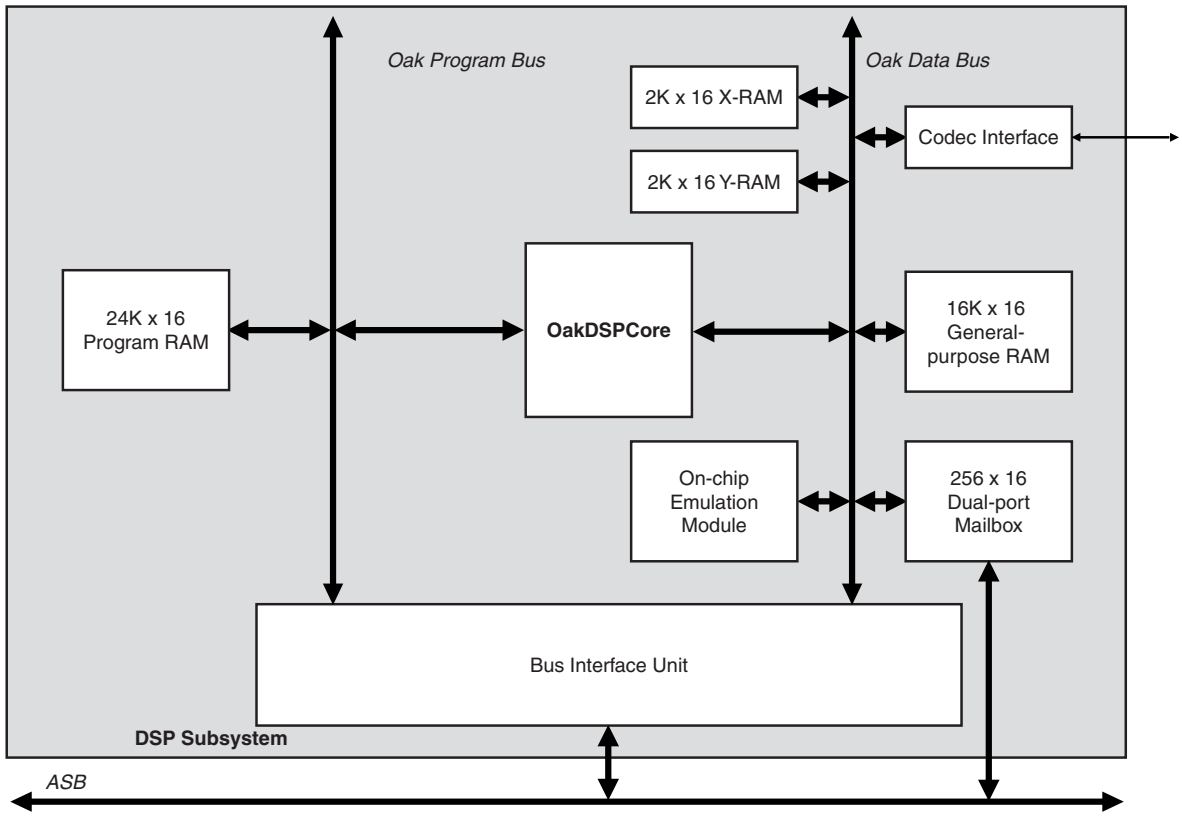
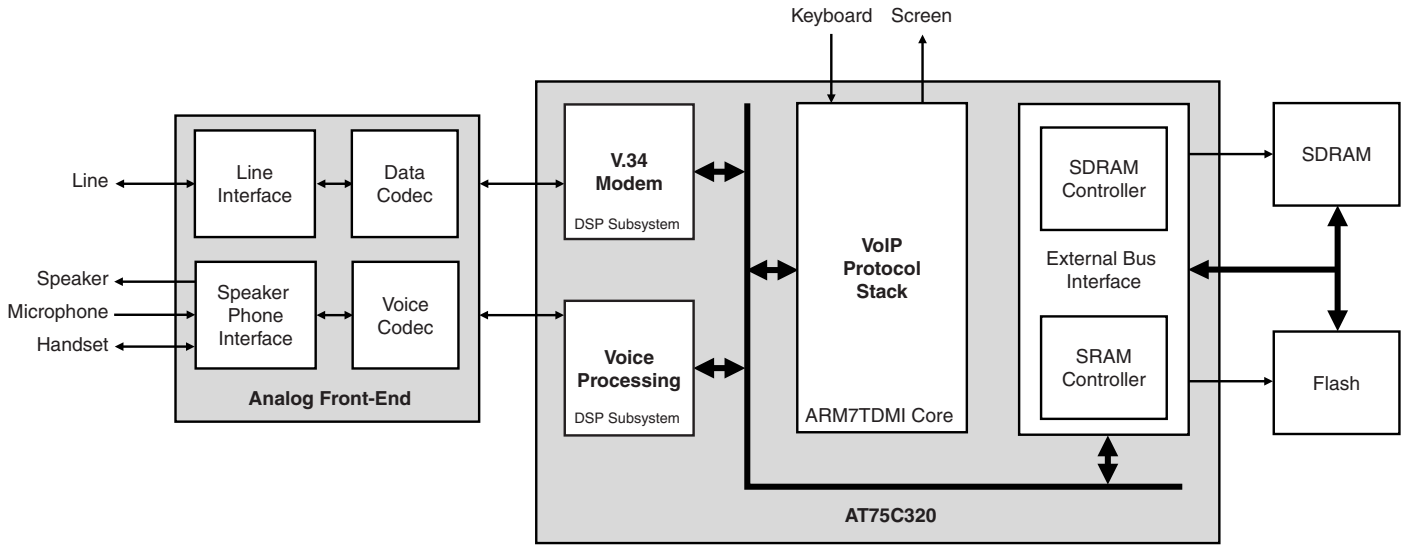


Figure 2. DSP Subsystem Block Diagram



Application Example

Figure 3. Standalone Internet Telephone



Functional Description

ARM7TDMI Core

The ARM7TDMI is a three-stage pipeline, 32-bit RISC processor. The processor architecture is Von Neumann load/store architecture which is characterized by a single data and address bus for instructions and data. The CPU has two instruction sets: the ARM and the Thumb instruction set. The ARM instruction set has 32-bit wide instructions and provides maximum performance. Thumb instructions are 16 bits wide and give maximum code density. Instructions operate on 8-, 16- and 32-bit data types.

The CPU has seven operating modes. Each operating mode has dedicated banked registers for fast exception handling. The processor has a total of 37 32-bit registers, including six status registers.

DSP Subsystem

The AT75C320 has two identical DSP subsystems.

Each DSP subsystem is composed of:

- An OakDSPCore running at 60 MIPS
- 2K x 16 of X-RAM
- 2K x 16 of Y-RAM
- 16K x 16 of general purpose data RAM
- 24K x 16 of loadable program RAM
- One 256 x 16 dual-port mailbox
- One codec interface

The DSP subsystem is fully autonomous. The local X- and Y-RAM allow it to reach its maximum processing rate, and a local large data RAM enables complex DSP algorithms to be implemented. The large size of the loadable program RAM permits the use of functions as complex as a V.34 modem or a low bit-rate vocoder.

During boot time, the ARM7TDMI core has the ability to maintain the OakDSPCore in reset state and to upload DSP boot code. When the OakDSPCore reverts to an active state, this boot code can be used to get the complete DSP application code from the ARM7TDMI through the mailbox.

When the OakDSPCore is running, the dual-port mailbox is used as the communication channel between the ARM7TDMI and the OakDSPCore.

One programmable codec interface is directly connected to each OakDSPCore. It allows the connection of most industrial voice, multimedia or data codecs.

Boot ROM

The ARM7TDMI has the ability to boot either from an external memory or from the on-chip 256 x 32-bit boot ROM.

Boot Code Operation

The internal boot sequence allows programming of the ARM7TDMI program RAM through a serial port. When the download is complete, a branch is executed to the downloaded code.

EBI: External Bus Interface

The EBI generates the signals that control access to external memory or memory-mapped peripherals. The EBI is fully programmable and can address up to 64M bytes. The interface to external devices is composed of common address and data buses and separate control lines to allow the connection of static or dynamic devices.

The main features are:

- External memory mapping
- Up to four chip select lines
- 32- or 16-bit data bus
- Byte write or byte select lines
- Remap of boot memory
- Support for both static and dynamic memories
- Two different read protocols for static memories
- Support for early read/early write for dynamic memories
- Programmable wait state generation
- Programmable data float time

AIC: Advanced Interrupt Controller

The AT75C320 has an 8-level priority interrupt controller. The interrupt controller outputs are connected to the NFIQ (fast interrupt request) and the NIRQ (normal interrupt request) of the ARM7TDMI core. The processor's NFIQ can only be asserted by the external fast interrupt request input (FIQ). The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals or by the external interrupt request line IRQ0.

An 8-level priority encoder allows the application to define the priority between the different interrupt sources. Interrupt sources are programmed to be level sensitive or edge sensitive. External sources can be programmed to be positive- or negative-edge triggered, or low- or high-level sensitive.

PIO: Parallel I/O Controller

The AT75C320 has 24 programmable I/O lines. They can all be programmed as inputs or outputs. To optimize the use of available package pins, most of them are multiplexed with external signals of on-chip peripherals.

The PIO lines are controlled by two separate and identical PIO controllers called PIOA and PIOB.

The PIO controllers enable the generation of an interrupt on input change and insertion of a simple glitch filter on each PIO line.

Some I/O lines have enough drive capability to power a LED.

USART: Universal Synchronous/ Asynchronous Receiver/ Transmitter

The AT75C320 provides two identical full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the peripheral data controller.

The main features are:

- Programmable baud rate generator
- Parity, framing and overrun error detection
- Line break generation and detection
- Automatic echo, local loopback and remote loopback
- Multi-drop mode: address detection and generation
- Interrupt generation
- Dedicated peripheral data controller channels
- 6-, 7-, 8- and 9-bit character length
- In addition to the Tx and Rx signals, the USART A provides several modem control lines.

SPI: Serial Peripheral Interface

The AT75C320 includes an SPI that provides communication with external devices in master or slave mode.

The SPI has one external chip select that can be connected to two devices. The data length is programmable from 8- to 16-bit.

Timer/Counter

The AT75C320 features three identical 16-bit timer/counters. They can be independently programmed to perform a wide range of functions, including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse width modulation.

The triple timer/counter block has three external clock inputs, five internal clock inputs and two multi-purpose signals that can be configured by the user. Each timer drives an internal interrupt signal that can be programmed to generate processor interrupts via the advanced interrupt controller.

Watchdog Timer

The AT75C320 has an internal watchdog timer that can be used to prevent system lock-up if the software becomes trapped in a deadlock.

Special Functions

The AT75C320 provides registers that implement the following special functions:

- Chip identification
- Reset status

Application Software

The AT75C320 is supported by a comprehensive range of software modules. As a result of the widespread use of the ARM7TDMI and the OakDSPCore, a wide range is available, either directly from Atmel or from third parties.

The application software modules are in three categories: OS level, DSP level and application level.

OS Level

The AT75C320 is supplied with a customized port of the Linux kernel. It features device drivers for all the on-chip peripherals, including the DSP subsystems, and supports virtual file system usage. It also supports the native TCP/IP facilities that have made Linux a success in Internet applications. This kernel is available in source code under the terms of the Gnu Public License.

Many other operating systems exist for the ARM7TDMI core.

DSP Level

A wide range of DSP functions are available for the OakDSPCore. Among others, Atmel supplies modules for a V.34 modem, G723.1 and G729A voice codecs, silence compression and echo cancellation.

Application Level

A rich software toolkit is available with support for popular communication protocols (H.323, POP-3/SMTP, etc.), connection processes, multimedia applications, full-feature telephony and audio software suites.

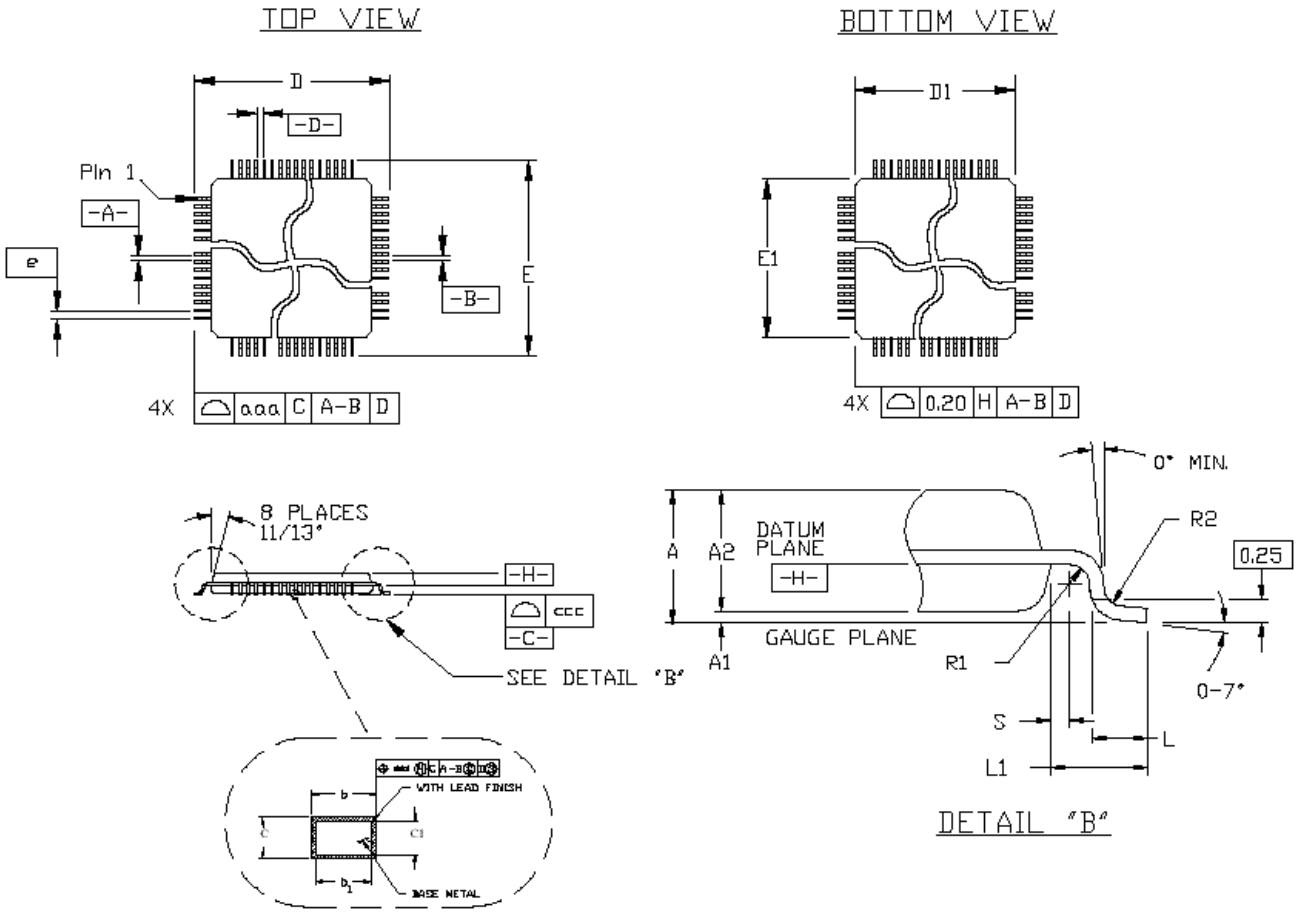
Development Tools

Both the ARM7TDMI and the OakDSPCore are industry-standard cores. They are supported by a comprehensive range of state-of-the-art development tools, including assemblers, C-compilers, source level debuggers and hardware emulators.

Packaging

The AT75C320 is supplied in a 160-lead PQFP package. This provides the best compromise between external connectivity and cost.

Figure 4. PQFP Package Drawing



For package data, see Table 3, Table 4 and Table 5 below.

Package Data

Table 3. Common Dimensions (mm)

Symbol	Min	Nom	Max
c	0.11		0.23
c1	0.11		0.17
L	0.65	0.88	1.03
L1		1.95 REF	
R2	0.13		0.3
R1	0.13		
S	0.4		
Tolerances of Form and Position			
aaa		0.25	
bbb		0.20	
ccc			0.10

Table 4. Dimensions Specific to 160-lead Package (mm)

A	A1	A2			b		b1			D	D1	E	E1	E	ddd
Max	Min	Min	Nom	Max	Min	Max	Min	Nom	Max	BSC	BSC	BSC	BSC	BSC	BSC
4.07	0.25	3.17	3.42	3.67	0.22	0.38	0.22	0.3	0.33	31.90	28.00	31.90	28.00	0.65	0.12

Table 5. 160-lead PQFP Package Electrical Characteristics

Body Size	R (mΩ)		C_s (pF)		C_m (pF)		L_s (nH)		L_m (nH)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
28 x 28	42	64	1.2	1.6	0.5	0.7	5.6	8.6	3.5	5.7

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