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PowerPC™

Advance Information

EC603e™ Embedded RISC Microprocessor (PID6) Hardware Specifications

The EC603e microprocessor from Motorola is an implementation of the PowerPC™ family of reduced instruction set computing (RISC) microprocessors. The EC603e microprocessor for embedded systems is functionally equivalent to the MPC603e with the exception of the floating-point unit which is not supported on the EC603e microprocessor.

The EC603e microprocessor is implemented in both a 2.5-volt version (PID 0007t EC603e microprocessor, abbreviated as PID7t) and a 3.3-volt version (PID 0006 EC603e microprocessor, abbreviated as PID6). This document describes the pertinent physical characteristics of the PID6. For functional characteristics of the processor, refer to the *MPC603e & EC603e RISC Microprocessors User's Manual*.

This document contains the following topics:

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1.1 Overview

The PID6 implementation of the EC603e microprocessor is a low-power implementation of the PowerPC microprocessor family of reduced instruction set computer (RISC) microprocessors. The PID6 implements the 32-bit portion of the PowerPC architecture specification, which provides 32-bit effective addresses, and integer data types of 8, 16, and 32 bits. For 64-bit PowerPC microprocessors, the PowerPC architecture provides 64-bit integer data types, 64-bit addressing, and other features required to complete the 64-bit architecture.

The PID6 provides four software controllable power-saving modes. Three of the modes (the nap, doze, and sleep modes) are static in nature, and progressively reduce the amount of power consumed by the processor. The fourth is a dynamic power management mode that causes the functional units in the PID6 to automatically enter a low-power mode when the functional units are idle without affecting operational performance, software execution, or any external hardware.

The PID6 is a superscalar processor capable of issuing and retiring as many as three instructions per clock. Instructions can execute out of order for increased performance; however, the PID6 makes completion appear sequential.

The PID6 integrates four execution units—an integer unit (IU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput for PID6–based systems. Most integer instructions execute in one clock cycle.

The PID6 provides independent on-chip, 16-Kbyte, four-way set-associative, physically addressed caches for instructions and data, as well as on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least-recently used (LRU) replacement algorithm. The PID6 also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of four entries each. Effective addresses are compared simultaneously with all four entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

The PID6 has a selectable 32- or 64-bit data bus and a 32-bit address bus. The PID6 interface protocol allows multiple masters to compete for system resources through a central external arbiter. The PID6 provides a three-state coherency protocol that supports the exclusive, modified, and invalid cache states. This protocol is a compatible subset of the MESI (modified/exclusive/shared/invalid) four-state protocol and operates coherently in systems that contain four-state caches. The PID6 supports single-beat and burst data transfers for memory accesses, and supports memory-mapped I/O.

The PID6 uses an advanced, 3.3-V CMOS process technology and maintains full interface compatibility with TTL devices.

1.2 Features

This section summarizes features of the PID6's implementation of the PowerPC architecture. Major features of the PID6 are as follows:

- High-performance, superscalar microprocessor
  - — As many as three instructions issued and retired per clock
  - — As many as five instructions in execution per clock
  - — Single-cycle execution for most instructions
- Four independent execution units and one register file
  - — BPU featuring static branch prediction
  - — A 32-bit IU
  - — LSU for data transfer between data cache and GPRs
  - — SRU that executes condition register (CR), special-purpose register (SPR) instructions, and integer add/compare instructions
  - — Thirty-two GPRs for integer operands
- High instruction and data throughput
  - — Zero-cycle branch capability (branch folding)
  - — Programmable static branch prediction on unresolved conditional branches
  - — Instruction fetch unit capable of fetching two instructions per clock from the instruction cache
  - — A six-entry instruction queue that provides lookahead capability
  - — Independent pipelines with feed-forwarding that reduces data dependencies in hardware
  - — 16-Kbyte data cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - — 16-Kbyte instruction cache—four-way set-associative, physically addressed; LRU replacement algorithm
  - — Cache write-back or write-through operation programmable on a per page or per block basis
  - — BPU that performs CR lookahead operations
  - — Address translation facilities for 4-Kbyte page size, variable block size, and 256-Mbyte segment size
  - — A 64-entry, two-way set-associative ITLB
  - — A 64-entry, two-way set-associative DTLB
  - — Four-entry data and instruction BAT arrays providing 128-Kbyte to 256-Mbyte blocks
  - — Software table search operations and updates supported through fast-trap mechanism
  - — 52-bit virtual address; 32-bit physical address
- Facilities for enhanced system performance
  - — A 32- or 64-bit split-transaction external data bus with burst transfers
  - — Support for one-level address pipelining and out-of-order bus transactions
- Integrated power management
  - — Low-power 3.3-volt design
  - — Internal processor/bus clock multiplier that provides 1/1, 1.5/1, 2/1, 2.5/1, 3/1, 3.5/1, and 4/1 ratios
  - — Three power saving modes: doze, nap, and sleep
  - — Automatic dynamic power reduction when internal functional units are idle
- In-system testability and debugging features through JTAG boundary-scan capability

1.3 General Parameters

The following list provides a summary of the general parameters of the PID6.

Technology	0.5 µ CMOS, four-layer metal
Die size	11.67 mm x 8.4 mm (98 mm^2)
Transistor count	2.6 million
Logic design	Fully-static
Package	Surface mount 240-pin ceramic quad flat pack (CQFP) or 255-pin ceramic ball grid array (CBGA)
Power supply	3.3 ± 5% V dc

1.4 Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the PID6.

1.4.1 DC Electrical Characteristics

The tables in this section describe the PID6 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	–0.3 to 4.0	V
PLL supply voltage	AVdd	–0.3 to 4.0	V
I/O supply voltage	OVdd	–0.3 to 4.0	V
Input voltage	V_{in}	–0.3 to 5.5	V
Storage temperature range	T_{stg}	–55 to 150	°C

Notes:

1. Functional operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution**: V_{in} must not exceed OVdd by more than 2.5 V at any time including during power-on reset.
3. **Caution**: OVdd must not exceed Vdd/AVdd by more than 2.5 V at any time including during power-on reset.
4. **Caution**: Vdd/AVdd must not exceed OVdd by more than 0.4 V at any time including during power-on reset.

Table 2 provides the recommended operating conditions for the PID6.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Value	Unit
Core supply voltage	Vdd	3.3 ± 165mv	V
PLL supply voltage	AVdd	3.3 ± 165mv	V
I/O supply voltage	OVdd	3.3 ± 165mv	V
Input voltage	V_{in}	–0.3 to 5.5	V
Die-junction temperature	T_j	0 to 105	°C

Note:

1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3 provides the packages thermal characteristics for the PID6.

Table 3. Package Thermal Characteristics

Characteristic	Symbol	Value	Rating
Wire-bond CQFP package die junction-to-case thermal resistance (typical)	θ_{JC}	2.2	°C/W
Wire-bond CQFP package die junction-to-lead thermal resistance (typical)	θ_{JB}	18.0	°C/W
CBGA package die junction-to-case thermal resistance (typical)	θ_{JC}	0.08	°C/W
CBGA package die junction-to-ball thermal resistance (typical)	θ_{JB}	2.8	°C/W

Note: Refer to Section 1.8, “System Design Information,” for more details about thermal management.

Table 4 provides the DC electrical characteristics for the PID6.

Table 4. DC Electrical Specifications

At recommended operating conditions. See Table 2

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage (all inputs except SYSCLK)	V_{IH}	2.0	5.5	V	
Input low voltage (all inputs except SYSCLK)	V_{IL}	-0.3	0.8	V	
SYSCLK input high voltage	CV_{IH}	2.4	5.5	V	
SYSCLK input low voltage	CV_{IL}	-0.3	0.4	V	
Input leakage current, V_{in} = 3.465 V	I_{in}	—	10	µA	1
V_{in} = 5.5 V	I_{in}	—	245	µA	1
Hi-Z (off-state) leakage current, V_{in} = 3.465 V	I_{TSI}	—	10	µA	1
V_{in} = 5.5 V	I_{TSI}	—	245	µA	1
Output high voltage, I_{OH} = –9 mA	V_{OH}	2.4	—	V	1

Table 4. DC Electrical Specifications (Continued)

At recommended operating conditions. See Table 2

Characteristic	Symbol	Min	Max	Unit	Notes
Output low voltage, I_{OL} = 14 mA	V_{OL}	—	0.4	V	
Capacitance, V_{in} = 0 V, f = 1 MHz (excludes $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	10.0	pF	2
Capacitance, V_{in} = 0 V, f = 1 MHz (for $\overline{TS}$, $\overline{ABB}$, $\overline{DBB}$, and $\overline{ARTRY}$)	C_{in}	—	15.0	pF	2

Notes:

1. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and JTAG signals.
2. Capacitance is periodically sampled rather than 100% tested.

Table 5 provides the power consumption for the PID6.

Table 5. Power Consumption

At recommended operating conditions. See Table 2

CPU Clock: SYSCLK	Processor (CPU) Frequency		Unit	Notes
	100 MHz	133.33 MHz		
Full-On Mode (DPM Enabled)				
Typical	3.2	4.2	W	1, 3
Max.	4.0	5.3	W	1, 2
Doze Mode				
Typical	1.0	1.3	W	1, 2
Nap Mode				
Typical	70	85	mW	1, 2
Sleep Mode				
Typical	40	50	mW	1, 2
Sleep Mode—PLL Disabled				
Typical	5	6	mW	1, 2
Sleep Mode—PLL and SYSCLK Disabled				
Typical	3	3	mW	1, 2

Notes:

1. These values apply for all valid bus ratios (PLL_CFG[0–3] settings). The values do not include I/O supply power (OVdd) or PLL supply power (AVdd). OVdd power is system dependent, but is typically <10% of Vdd power. Worst-case power consumption for AVdd = 15 mw.
2. Maximum power is measured at Vdd = 3.465 V using a worst-case instruction mix.
3. Typical power is an average value measured at Vdd = AVdd = OVdd = 3.3 V in a system executing typical applications and benchmark sequences.

1.4.2 AC Electrical Characteristics

This section provides the AC electrical characteristics for the PID6. After fabrication, parts are sorted by maximum processor core frequency as shown in Section 1.4.2.1, “Clock AC Specifications,” and tested for conformance to the AC specifications for that frequency. These specifications are for 100 and 133.33 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0–3] signals. Parts are sold by maximum processor core frequency; see Section 1.10, “Ordering Information.”

1.4.2.1 Clock AC Specifications

Table 6 provides the clock AC timing specifications as defined in Figure 1.

Table 6. Clock AC Timing Specifications

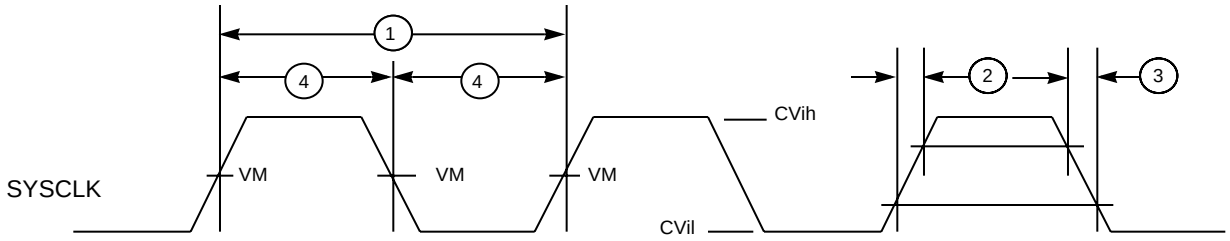
At recommended operating conditions. See Table 2

Num	Characteristic	100 MHz		133.33 MHz		Unit	Notes
		Min	Max	Min	Max		
	Processor frequency	50	100	50	133.33	MHz	1
	VCO frequency	100	266.66	100	266.66	MHz	1
	SYSCLK (bus) frequency	16.67	66.67	16.67	66.67	MHz	
1	SYSCLK cycle time	15.0	60.0	15.0	60.0	ns	
2,3	SYSCLK rise and fall time	—	2.0	—	2.0	ns	2
4	SYSCLK duty cycle measured at 1.4 V	40.0	60.0	40.0	60.0	%	3
	SYSCLK jitter	—	±150	—	±150	ps	4
	Internal PLL relock time	—	100	—	100	µs	3, 5

Notes:

1. **Caution**: The SYSCLK frequency and PLL_CFG[0–3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0–3] signal description in Section 1.8, “System Design Information,” for valid PLL_CFG[0–3] settings.
2. Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.
3. Timing is guaranteed by design and characterization, and is not tested.
4. Cycle-to-cycle jitter, and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 1 provides the SYSCLK input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 1. SYSCLK Input Timing Diagram

1.4.2.2 Input AC Specifications

Table 7 provides the input AC timing specifications for the PID6 as defined in Figure 2 and Figure 3.

Table 7. Input AC Timing Specifications

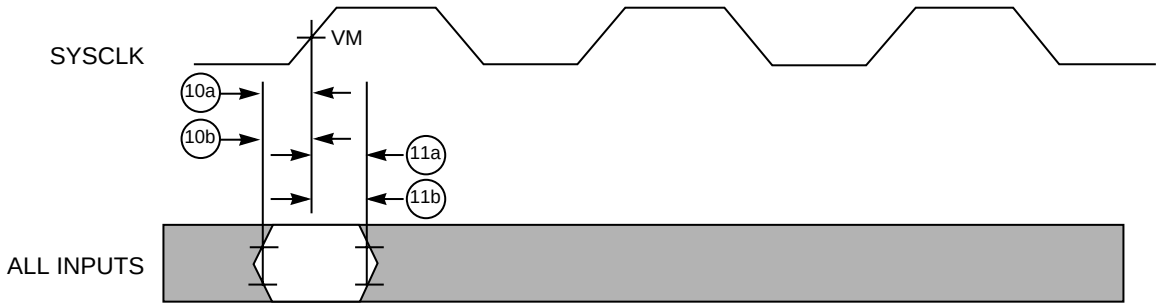
At recommended operating conditions. See Table 2

Num	Characteristic	100 MHz		133.33 MHz		Unit	Notes
		Min	Max	Min	Max		
10a	Address/data/transfer attribute inputs valid to SYSCLK (input setup)	3.0	—	3.0	—	ns	2
10b	All other inputs valid to SYSCLK (input setup)	5.0	—	5.0	—	ns	3
10c	Mode select inputs valid to $\overline{\text{HRESET}}$ (input setup) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$ and $\overline{\text{TLBISYNC}}$)	$8*t_{sysclk}$	—	$8*t_{sysclk}$	—	ns	4,5, 6,7
11a	SYSCLK to address/data/transfer attribute inputs invalid (input hold)	1.0	—	1.0	—	ns	2
11b	SYSCLK to all other inputs invalid (input hold)	1.0	—	1.0	—	ns	3
11c	$\overline{\text{HRESET}}$ to mode select inputs invalid (input hold) (for $\overline{\text{DRTRY}}$, $\overline{\text{QACK}}$, and $\overline{\text{TLBISYNC}}$)	0	—	0	—	ns	4,6,7

Notes:

1. All input specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the 1.4 V of the rising edge of the input SYSCLK (see Figure 2). Both input and output timings are measured at the pin.
2. Address/data/transfer attribute input signals are composed of the following—A[0–31], AP[0–3], TT[0–4], TC[0–1], $\overline{\text{TBST}}$, TSIZ[0–2], $\overline{\text{GBL}}$, DH[0–31], DL[0–31], DP[0–7].
3. All other input signals are composed of the following—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{BG}}$, $\overline{\text{AACK}}$, $\overline{\text{DBG}}$, $\overline{\text{DBWO}}$, $\overline{\text{TA}}$, $\overline{\text{DRTRY}}$, $\overline{\text{TEA}}$, $\overline{\text{DBDIS}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$, $\overline{\text{INT}}$, $\overline{\text{SMI}}$, $\overline{\text{MCP}}$, TBEN, $\overline{\text{QACK}}$, $\overline{\text{TLBISYNC}}$.
4. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 3).
5. t_{sysclk} is the period of the external clock (SYSCLK) in nanoseconds.
6. These values are guaranteed by design, and are not tested.
7. This specification is for configuration mode select only. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

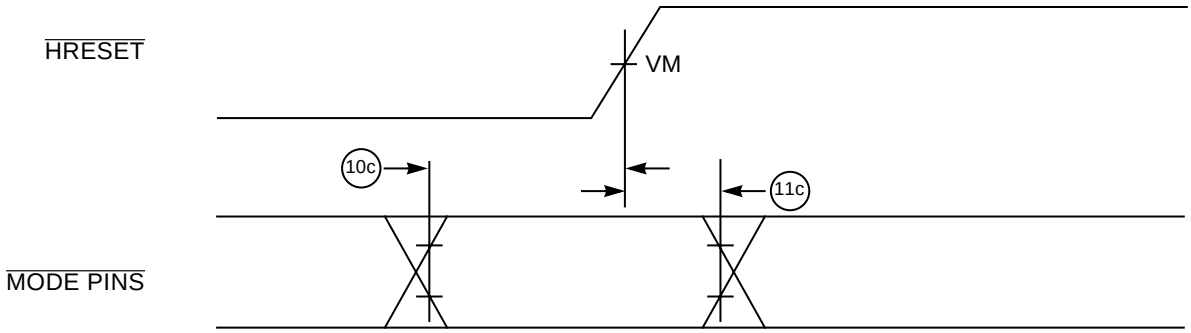
Figure 2 provides the input timing diagram for the PID6.



VM = Midpoint Voltage (1.4 V)

Figure 2. Input Timing Diagram

Figure 3 provides the mode select input timing diagram for the PID6.



VM = Midpoint Voltage (1.4 V)

Figure 3. Mode Select Input Timing Diagram

1.4.2.3 Output AC Specifications

Table 8 provides the output AC timing specifications for the PID6 as defined in Figure 4.

Table 8. Output AC Timing Specifications[1]

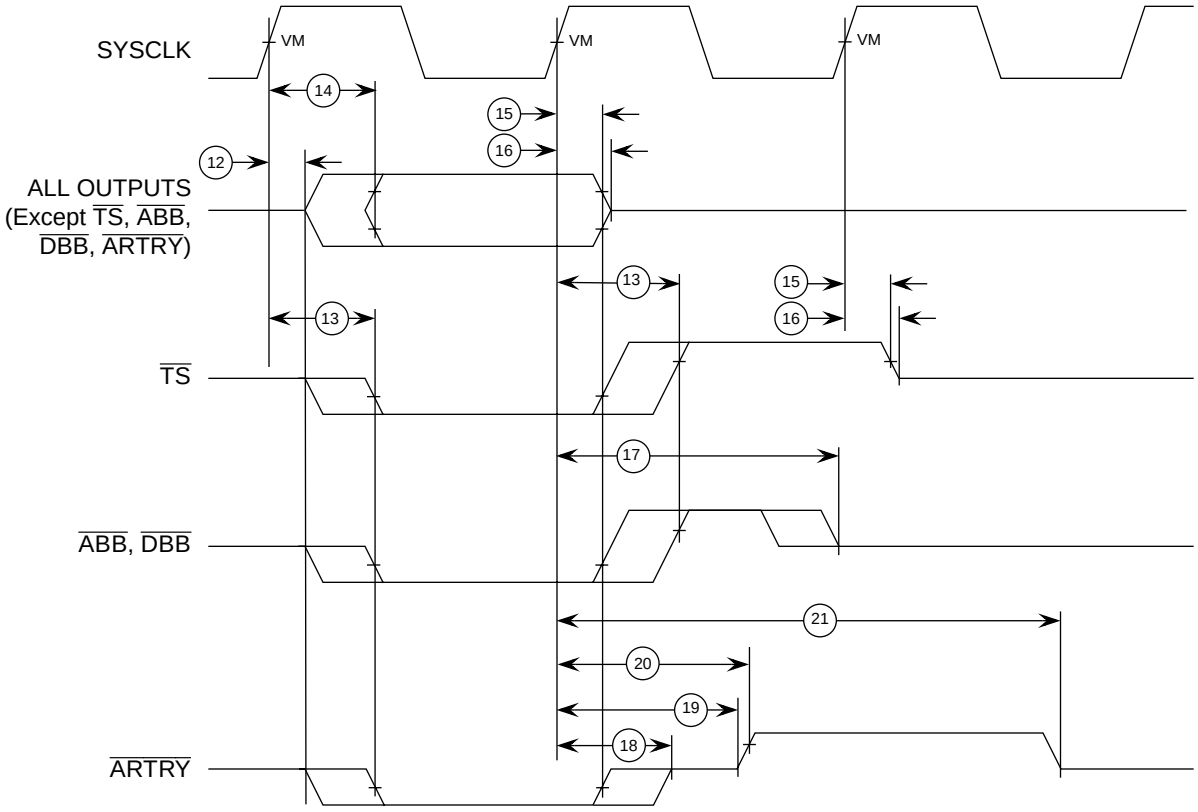
At recommended operating conditions. See Table 2. C_L = 50 pF[2]

Num	Characteristic	100 MHz		133.33 MHz		Unit	Notes
		Min	Max	Min	Max		
12	SYSCLK to output driven (output enable time)	1.0	—	1.0	—	ns	
13a	SYSCLK to output valid (5.5 V to 0.8 V—$\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	11.0	—	11.0	ns	4
13b	SYSCLK to output valid ($\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	10.0	—	10.0	ns	6
14a	SYSCLK to output valid (5.5 V to 0.8 V—all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	13.0	—	13.0	ns	4
14b	SYSCLK to output valid (all except $\overline{TS}$, $\overline{ABB}$, $\overline{ARTRY}$, $\overline{DBB}$)	—	11.0	—	11.0	ns	6
15	SYSCLK to output invalid (output hold)	1.5	—	1.5	—	ns	3
16	SYSCLK to output high impedance (all except $\overline{ARTRY}$, $\overline{ABB}$, $\overline{DBB}$)	—	9.5	—	9.5	ns	
17	SYSCLK to $\overline{ABB}$, $\overline{DBB}$, high impedance after precharge	—	1.2	—	1.2	t_{sysclk}	5,7
18	SYSCLK to $\overline{ARTRY}$ high impedance before precharge	—	9.0	—	9.0	ns	
19	SYSCLK to $\overline{ARTRY}$ precharge enable	0.2 * t_{sysclk}+1.0	—	0.2 * t_{sysclk}+1.0	—	ns	3,5,8
20	Maximum delay to $\overline{ARTRY}$ precharge	—	1.2	—	1.2	t_{sysclk}	5,8
21	SYSCLK to $\overline{ARTRY}$ high impedance after precharge	—	2.25	—	2.25	t_{sysclk}	5,8

Notes:

1. All output specifications are measured from the 1.4 V of the rising edge of SYSCLK to the TTL level (0.8 V or 2.0 V) of the signal in question. Both input and output timings are measured at the pin (see Figure 4).
2. All maximum timing specifications assume C_L = 50 pF.
3. This minimum parameter assumes C_L = 0 pF.
4. SYSCLK to output valid (5.5 V to 0.8 V) includes the extra delay associated with discharging the external voltage from 5.5 V to 0.8 V instead of from Vdd to 0.8 V (5 V CMOS levels instead of 3.3 V CMOS levels).
5. t_{sysclk} is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Output signal transitions from GND to 2.0 V or Vdd to 0.8 V.
7. Nominal precharge width for $\overline{ABB}$ and $\overline{DBB}$ is 0.5 t_{sysclk}.
8. Nominal precharge width for $\overline{ARTRY}$ is 1.0 t_{sysclk}.

Figure 4 provides the output timing diagram for the PID6.



VM = Midpoint Voltage (1.4 V)

Figure 4. Output Timing Diagram

1.4.3 JTAG AC Timing Specifications

Table 9 provides the JTAG AC timing specifications as defined in Figure 5 through Figure 8.

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK)

At recommended operating conditions. See Table 2., C_L = 50 pF

Num	Characteristic	Min	Max	Unit	Notes
	TCK frequency of operation	0	16	MHz	
1	TCK cycle time	62.5	—	ns	
2	TCK clock pulse width measured at 1.4 V	25	—	ns	
3	TCK rise and fall times	0	3	ns	
4	$\overline{\text{TRST}}$ setup time to TCK rising edge	13	—	ns	1
5	$\overline{\text{TRST}}$ assert time	40	—	ns	
6	Boundary-scan input data setup time	6	—	ns	2
7	Boundary-scan input data hold time	27	—	ns	2
8	TCK to output data valid	4	25	ns	3
9	TCK to output high impedance	3	24	ns	3

Table 9. JTAG AC Timing Specifications (Independent of SYSCLK) (Continued)

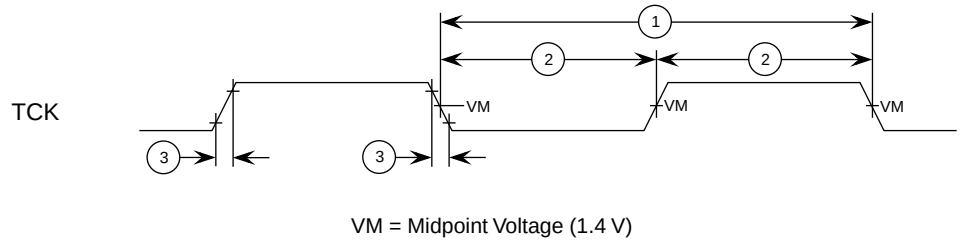
At recommended operating conditions. See Table 2., C_L = 50 pF

Num	Characteristic	Min	Max	Unit	Notes
10	TMS, TDI data setup time	0	—	ns	
11	TMS, TDI data hold time	25	—	ns	
12	TCK to TDO data valid	4	24	ns	
13	TCK to TDO high impedance	3	15	ns	

Notes:

1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Non-test signal input timing with respect to TCK.
3. Non-test signal output timing with respect to TCK.

Figure 5 provides the JTAG clock input timing diagram.



VM = Midpoint Voltage (1.4 V)

Figure 5. JTAG Clock Input Timing Diagram

Figure 6 provides the $\overline{\text{TRST}}$ timing diagram.

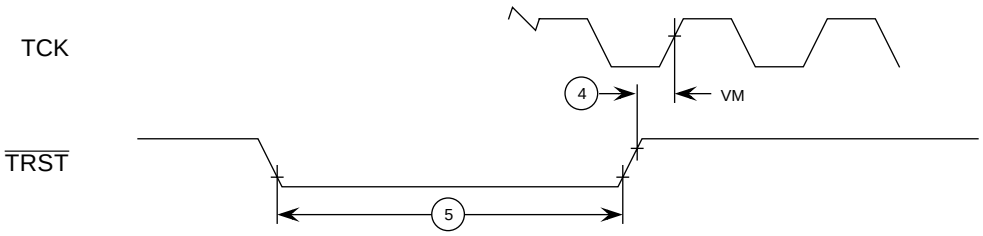


Figure 6. $\overline{\text{TRST}}$ Timing Diagram

Figure 7 provides the boundary-scan timing diagram.

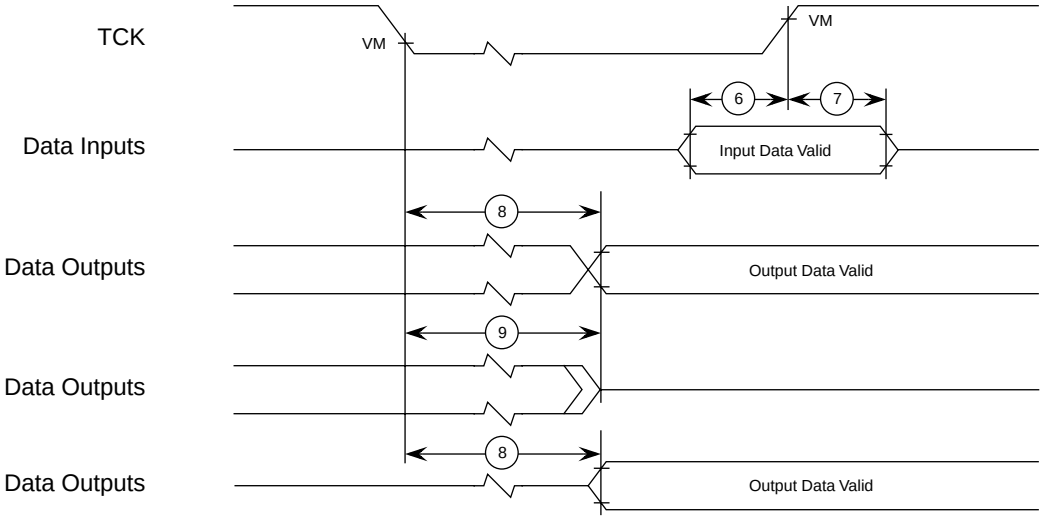


Figure 7. Boundary-Scan Timing Diagram

Figure 8 provides the test access port timing diagram.

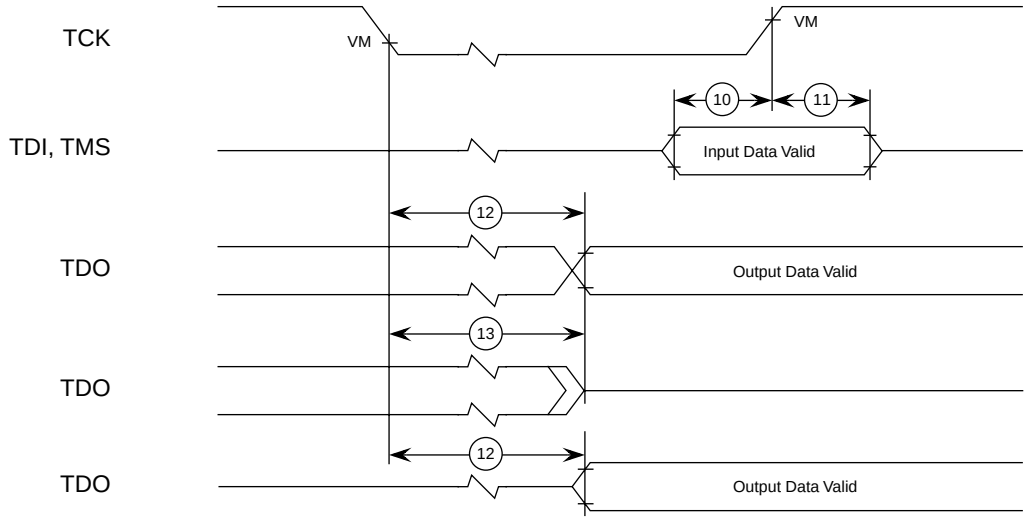


Figure 8. Test Access Port Timing Diagram

1.5 Pin Assignments

The following sections contain the pinout diagrams for the PID6. Note that the PID6 is offered in both ceramic quad flat pack (CQFP) and ceramic ball grid array (CBGA) packages.

1.5.1 Pinout Diagram for the CQFP Package

Figure 9 contains the pinout diagram of the CQFP package for the PID6.

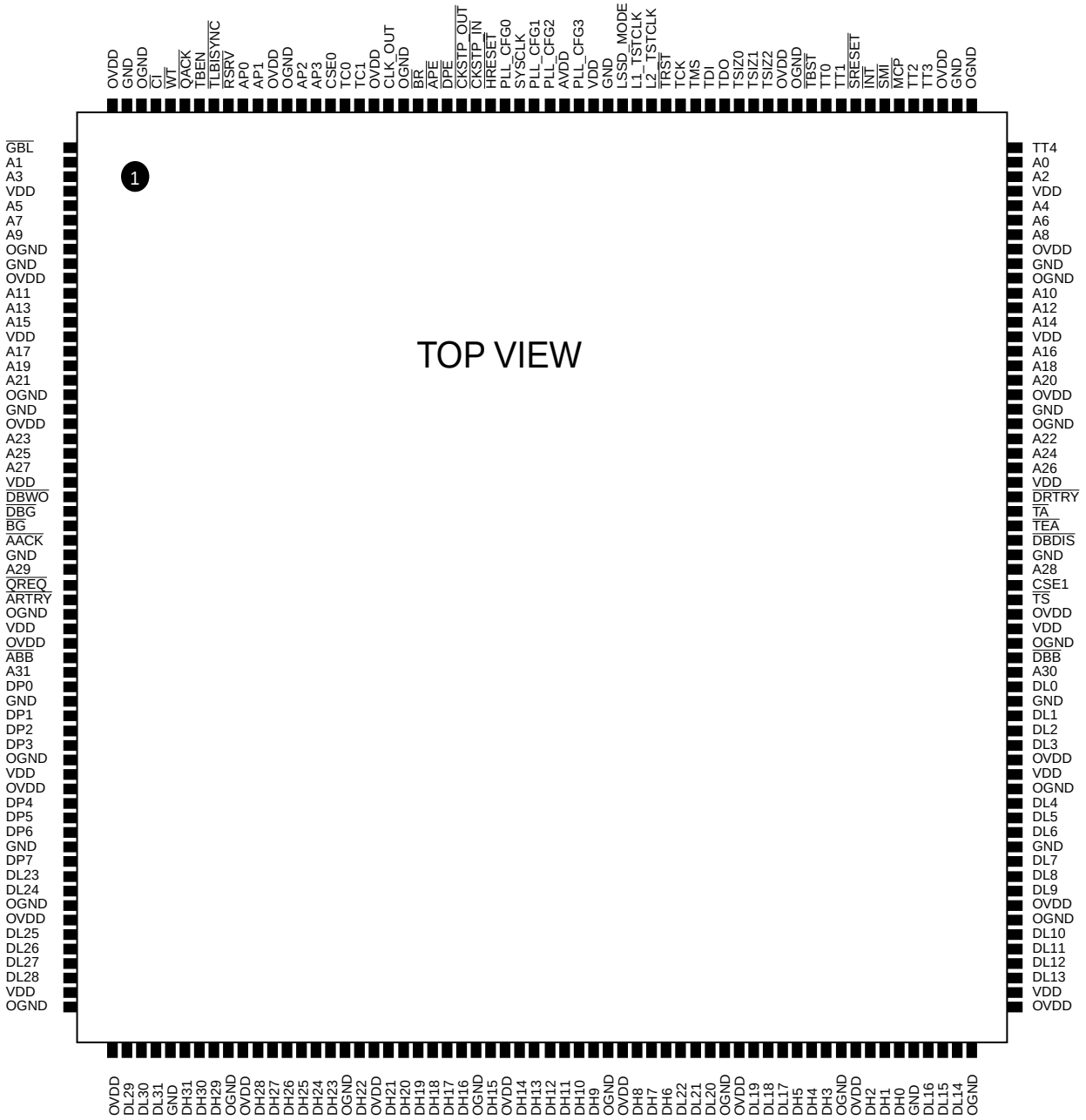
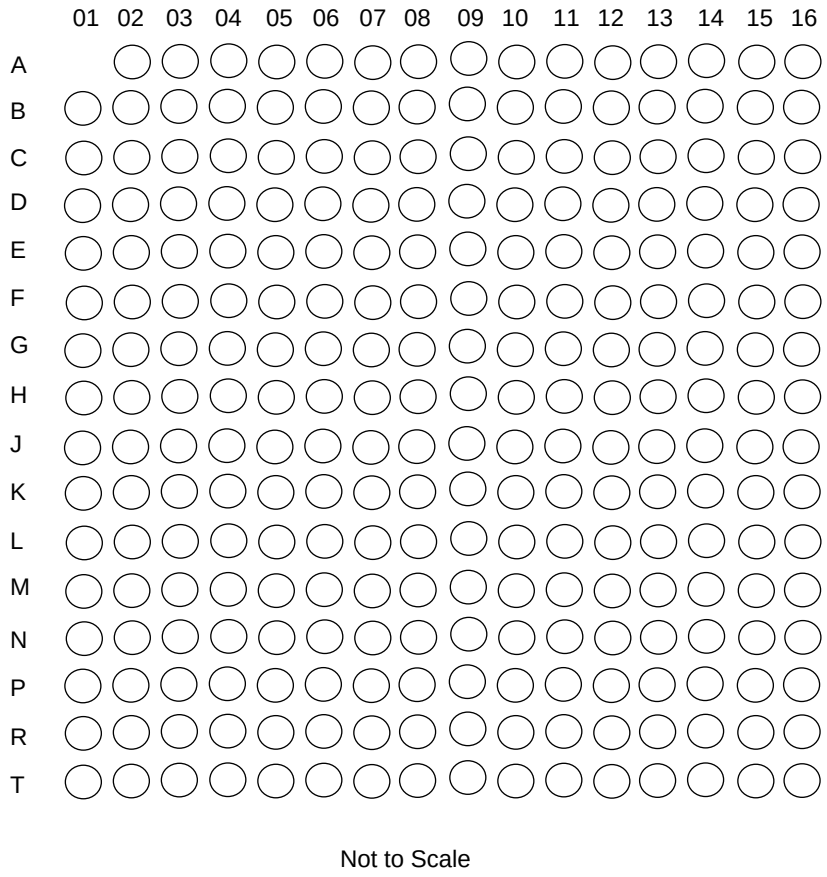


Figure 9. Pinout Diagram for the CQFP Package

1.5.2 Pinout Diagram for the CBGA Package

Figure 10 (in part A) shows the pinout of the CBGA package as viewed from the top surface. Part B shows the side profile of the CBGA package to indicate the direction of the top surface view.

Part A



Part B

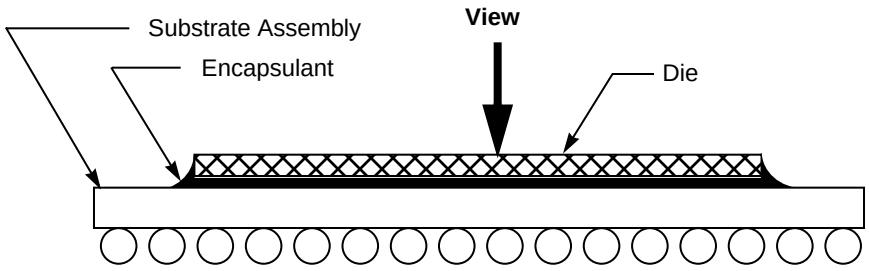


Figure 10. Pinout of the CBGA Package as Viewed from the Top Surface

1.6 Pinout Listings

The following sections contain the pinout listings for the PID6 CQFP and CBGA packages.

1.6.1 Pinout Listing for the CQFP Package

Table 10 provides the pinout listing for the PID6 CQFP package.

Table 10. Pinout Listing for the 240-pin CQFP Package

Signal Name	Pin Number	Active	I/O
A[0–31]	179, 2, 178, 3, 176, 5, 175, 6, 174, 7, 170, 11, 169, 12, 168, 13, 166, 15, 165, 16, 164, 17, 160, 21, 159, 22, 158, 23, 151, 30, 144, 37	High	I/O
$\overline{\text{AACK}}$	28	Low	Input
$\overline{\text{ABB}}$	36	Low	I/O
AP[0–3]	231, 230, 227, 226	High	I/O
$\overline{\text{APE}}$	218	Low	Output
$\overline{\text{ARTRY}}$	32	Low	I/O
AVDD	209	High	Input
$\overline{\text{BG}}$	27	Low	Input
$\overline{\text{BR}}$	219	Low	Output
$\overline{\text{CI}}$	237	Low	Output
CLK_OUT	221	—	Output
$\overline{\text{CKSTP\_IN}}$	215	Low	Input
$\overline{\text{CKSTP\_OUT}}$	216	Low	Output
CSE[0–1][1]	225, 150	High	Output
$\overline{\text{DBB}}$	145	Low	I/O
$\overline{\text{DBDIS}}$	153	Low	Input
$\overline{\text{DBG}}$	26	Low	Input
$\overline{\text{DBWO}}$	25	Low	Input
DH[0–31]	115, 114, 113, 110, 109, 108, 99, 98, 97, 94, 93, 92, 91, 90, 89, 87, 85, 84, 83, 82, 81, 80, 78, 76, 75, 74, 73, 72, 71, 68, 67, 66	High	I/O
DL[0–31]	143, 141, 140, 139, 135, 134, 133, 131, 130, 129, 126, 125, 124, 123, 119, 118, 117, 107, 106, 105, 102, 101, 100, 51, 52, 55, 56, 57, 58, 62, 63, 64	High	I/O
DP[0–7]	38, 40, 41, 42, 46, 47, 48, 50	High	I/O
$\overline{\text{DPE}}$	217	Low	Output
$\overline{\text{DRTRY}}$	156	Low	Input
$\overline{\text{GBL}}$	1	Low	I/O
GND	9, 19, 29, 39, 49, 65, 116, 132, 142, 152, 162, 172, 182, 206, 239	Low	Input
$\overline{\text{HRESET}}$	214	Low	Input
$\overline{\text{INT}}$	188	Low	Input

Table 10. Pinout Listing for the 240-pin CQFP Package (Continued)

Signal Name	Pin Number	Active	I/O
$\overline{\text{LSSD\_MODE}}$[2]	205	Low	Input
L1_TSTCLK[2]	204	—	Input
L2_TSTCLK[2]	203	—	Input
$\overline{\text{MCP}}$	186	Low	Input
OGND	8, 18, 33, 43, 53, 60, 69, 77, 86, 95, 103, 111, 120, 127, 136, 146, 161, 171, 181, 193, 220, 228, 238	Low	Input
OVDD[3]	10, 20, 35, 45, 54, 61, 70, 79, 88, 96, 104, 112, 121, 128, 138, 148, 163, 173, 183, 194, 222, 229, 240	High	Input
PLL_CFG[0–3]	213, 211, 210, 208	High	Input
$\overline{\text{QACK}}$	235	Low	Input
$\overline{\text{QREQ}}$	31	Low	Output
$\overline{\text{RSRV}}$	232	Low	Output
$\overline{\text{SMI}}$	187	Low	Input
$\overline{\text{SRESET}}$	189	Low	Input
SYSCLK	212	—	Input
$\overline{\text{TA}}$	155	Low	Input
TBEN	234	High	Input
$\overline{\text{TBST}}$	192	Low	I/O
TC[0–1]	224, 223	High	Output
TCK	201	—	Input
TDI	199	High	Input
TDO	198	High	Output
$\overline{\text{TEA}}$	154	Low	Input
$\overline{\text{TLBISYNC}}$	233	Low	Input
TMS	200	High	Input
$\overline{\text{TRST}}$	202	Low	Input
TSIZ[0–2]	197, 196, 195	High	I/O
$\overline{\text{TS}}$	149	Low	I/O
TT[0–4]	191, 190, 185, 184, 180	High	I/O
VDD[3]	4, 14, 24, 34, 44, 59, 122, 137, 147, 157, 167, 177, 207	High	Input
$\overline{\text{WT}}$	236	Low	Output

Notes:

1. There are two CSE signals in the EC603e microprocessor—CSE0 and CSE1. The $\overline{\text{XATS}}$ signal in the PowerPC 603™ microprocessor is replaced by the CSE1 signal in the PID6.
2. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
3. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core.

1.6.2 Pinout Listing for the CBGA Package

Table 11 provides the pinout listing for the PID6 CBGA package.

Table 11. Pinout Listing for the 255-pin CBGA Package

Signal Name	Pin Number	Active	I/O
A[0–31]	C16, E04, D13, F02, D14, G01, D15, E02, D16, D04, E13, GO2, E15, H01, E16, H02, F13, J01, F14, J02, F15, H03, F16, F04, G13, K01, G15, K02, H16, M01, J15, P01	High	I/O
$\overline{\text{AACK}}$	L02	Low	Input
$\overline{\text{ABB}}$	K04	Low	I/O
AP[0–3]	C01, B04, B03, B02	High	I/O
$\overline{\text{APE}}$	A04	Low	Output
$\overline{\text{ARTRY}}$	J04	Low	I/O
AVDD	A10	—	—
$\overline{\text{BG}}$	L01	Low	Input
$\overline{\text{BR}}$	B06	Low	Output
$\overline{\text{CI}}$	E01	Low	Output
$\overline{\text{CKSTP\_IN}}$	D08	Low	Input
$\overline{\text{CKSTP\_OUT}}$	A06	Low	Output
CLK_OUT	D07	—	Output
CSE[0–1]	B01, B05	High	Output
$\overline{\text{DBB}}$	J14	Low	I/O
$\overline{\text{DBG}}$	N01	Low	Input
$\overline{\text{DBDIS}}$	H15	Low	Input
$\overline{\text{DBWO}}$	G04	Low	Input
DH[0–31]	P14, T16, R15, T15, R13, R12, P11, N11, R11,T12, T11, R10, P09, N09, T10, R09, T09, P08, N08, R08, T08, N07, R07, T07, P06, N06, R06, T06, R05, N05, T05, T04	High	I/O
DL[0–31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P03, N03, N04, R03, T01, T02, P04, T03, R04	High	I/O
DP[0–7]	M02, L03, N02, L04, R01, P02, M04, R02	High	I/O
$\overline{\text{DPE}}$	A05	Low	Output
$\overline{\text{DRTRY}}$	G16	Low	Input
$\overline{\text{GBL}}$	F01	Low	I/O
GND	C05, C12, E03, E06, E08, E09, E11, E14, F05, F07, F10, F12, G06, G08, G09, G11, H05, H07, H10, H12, J05, J07, J10, J12, K06, K08, K09, K11, L05, L07, L10, L12, M03, M06, M08, M09, M11, M14, P05, P12	—	—
$\overline{\text{HRESET}}$	A07	Low	Input
$\overline{\text{INT}}$	B15	Low	Input
L1_TSTCLK [1]	D11	—	Input

Table 11. Pinout Listing for the 255-pin CBGA Package (Continued)

Signal Name	Pin Number	Active	I/O
L2_TSTCLK [1]	D12	—	Input
$\overline{\text{LSSD\_MODE}}$ [1]	B10	Low	Input
$\overline{\text{MCP}}$	C13	Low	Input
NC	B07, B08, C03, C06, C08, D05, D06, F03, H04, J16	Low	Input
OVDD	C07, E05, E07, E10, E12, G03, G05, G12, G14, K03, K05, K12, K14, M05, M07, M10, M12, P07, P10	—	—
PLL_CFG[0–3]	A08, B09, A09, D09	High	Input
$\overline{\text{QACK}}$	D03	Low	Input
$\overline{\text{QREQ}}$	J03	Low	Output
$\overline{\text{RSRV}}$	D01	Low	Output
$\overline{\text{SMI}}$	A16	Low	Input
$\overline{\text{SRESET}}$	B14	Low	Input
SYSCLK	C09	—	Input
$\overline{\text{TA}}$	H14	Low	Input
TBEN	C02	High	Input
$\overline{\text{TBST}}$	A14	Low	I/O
TC[0–1]	A02, A03	High	Output
TCK	C11	—	Input
TDI	A11	High	Input
TDO	A12	High	Output
$\overline{\text{TEA}}$	H13	Low	Input
$\overline{\text{TLBISYNC}}$	C04	Low	Input
TMS	B11	High	Input
$\overline{\text{TRST}}$	C10	Low	Input
$\overline{\text{TS}}$	J13	Low	I/O
TSIZ[0–2]	A13, D10, B12	High	I/O
TT[0–4]	B13, A15, B16, C14, C15	High	I/O
$\overline{\text{WT}}$	D02	Low	Output
VDD[2]	F06, F08, F09, F11, G07, G10, H06, H08, H09, H11, J06, J08, J09, J11, K07, K10, L06, L08, L09, L11	—	—

Notes:

1. These are test signals for factory use only and must be pulled up to OVdd for normal machine operation.
2. OVdd inputs supply power to the I/O drivers and Vdd inputs supply power to the processor core. Future members of the 603 family may use different OVdd and Vdd input levels.

1.7 Package Description

The following sections provide the package parameters and the mechanical dimensions for the PID6.

1.7.1 CQFP Package Description

The following sections provide the package parameters and mechanical dimensions for the Motorola CQFP package.

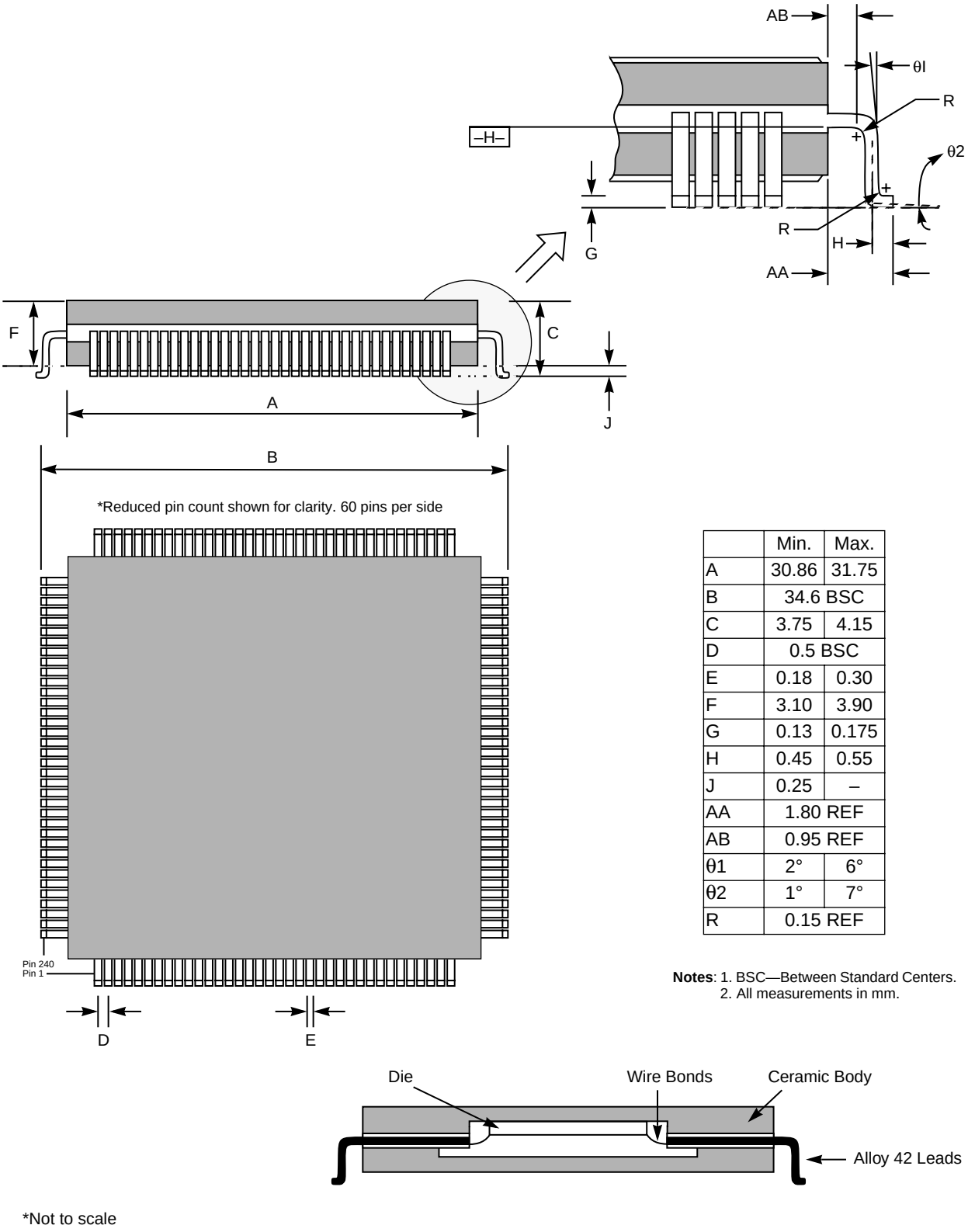
1.7.1.1 Package Parameters

The package parameters are as provided in the following list. The package type is 32 mm x 32 mm, 240-pin ceramic quad flat pack.

Package outline	32 mm x 32 mm
Interconnects	240
Pitch	0.5 mm

1.7.1.2 Mechanical Dimensions of the CQFP Package

Figure 11 shows the mechanical dimensions of the Motorola CQFP package.



	Min.	Max.
A	30.86	31.75
B	34.6 BSC	
C	3.75	4.15
D	0.5 BSC	
E	0.18	0.30
F	3.10	3.90
G	0.13	0.175
H	0.45	0.55
J	0.25	–
AA	1.80 REF	
AB	0.95 REF	
θ1	2°	6°
θ2	1°	7°
R	0.15 REF	

Notes: 1. BSC—Between Standard Centers.
2. All measurements in mm.

Figure 11. Mechanical Dimensions of the Wire-Bond CQFP Package

1.7.2 CBGA Package Description

The following sections provide the package parameters and mechanical dimensions for the CBGA package.

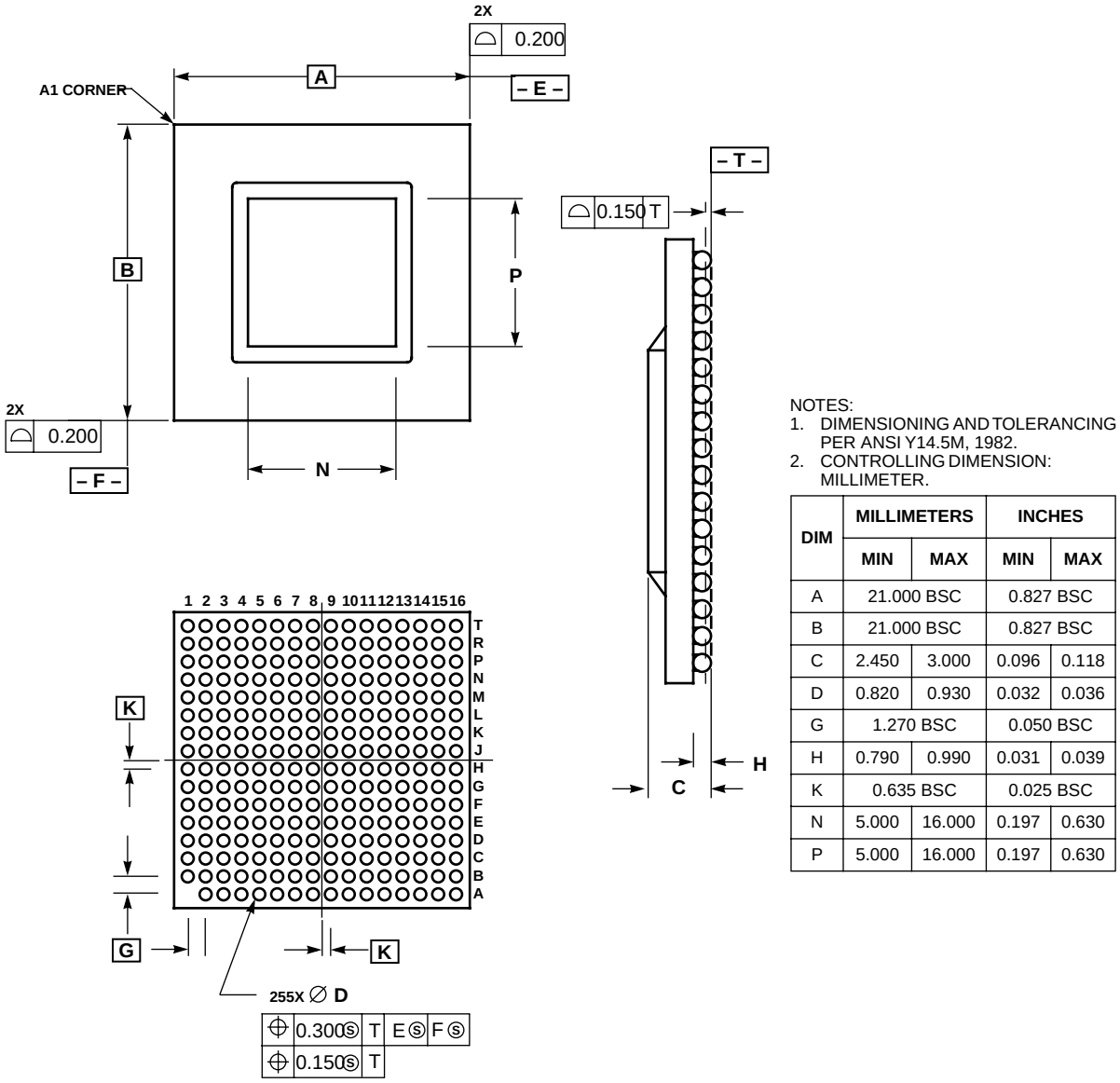
1.7.2.1 Package Parameters

The package parameters are as provided in the following list. The package type is 21 x 21 mm, 255-pin ceramic ball grid array (CBGA).

Package outline	21 mm
Interconnects	255
Pitch	1.27 mm
Minimum module height	2.45 mm
Maximum module height	3.00 mm
Ball diameter	0.89 mm (35 mil)

1.7.2.2 Mechanical Dimensions of the CBGA Package

Figure 12 provides the mechanical dimensions and bottom surface nomenclature of the CBGA package.



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.000 BSC		0.827 BSC	
B	21.000 BSC		0.827 BSC	
C	2.450	3.000	0.096	0.118
D	0.820	0.930	0.032	0.036
G	1.270 BSC		0.050 BSC	
H	0.790	0.990	0.031	0.039
K	0.635 BSC		0.025 BSC	
N	5.000	16.000	0.197	0.630
P	5.000	16.000	0.197	0.630

Figure 12. Mechanical Dimensions and Bottom Surface Nomenclature of the CBGA Package

1.8 System Design Information

This section provides electrical and thermal design recommendations for successful application of the PID6.

1.8.1 PLL Configuration

The PID6 PLL, shown in Table 12 for nominal frequencies, is configured by the PLL_CFG[0–3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation.

Table 12. PLL Configuration

PLL_CFG [0–3]	CPU Frequency in MHz (VCO Frequency in MHz)									
	Bus-to-Core Multiplier	**Core-to-VCO Multiplier**	**Bus 16.67 MHz**	**Bus 20 MHz**	**Bus 25 MHz**	**Bus 33.33 MHz**	**Bus 40 MHz**	**Bus 50 MHz**	**Bus 60 MHz**	**Bus 66.67 MHz**
0000	1x	2x	—	—	—	—	—	50 (100)	60 (120)	66.67 (133)
0001	1x	4x	—	—	—	—	—	50 (200)	60 (240)	66.67 (266)
1100	1.5x	2x	—	—	—	50 (100)	60 (120)	75 (150)	90 (180)	100 (200)
0100	2x	2x	—	—	—	66.67 (133)	80 (160)	100 (200)	120 (240)	133.33 (266)
0101	2x	4x	—	—	50 (200)	66.67 (266)	—	—	—	—
0110	2.5x	2x	—	50 (100)	62.5 (125)	83.33 (166)	100 (200)	125 (250)	—	—
1000	3x	2x	50 (100)	60 (120)	75 (150)	100 (200)	120 (240)	—	—	—
1110	3.5x	2x	58.4 (117)	70 (140)	87.5 (175)	116.67 (233)	—	—	—	—
1010	4x	2x	66.67 (133)	80 (160)	100 (200)	133.33 (266)	—	—	—	—
0011	PLL bypass									
1111	Clock off									

Notes:

1. PLL_CFG[0–3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PID6; see Section 1.4.2.1, “Clock AC Specifications,” for valid SYSCLK and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In clock-off mode, no clocking occurs inside the PID6 regardless of the SYSCLK input.

1.8.2 PLL Power Supply Filtering

The AVdd power signal is provided on the PID6 to provide power to the clock generation phase-locked loop. To ensure stability of the internal clock, the power supplied to the AVdd input signal should be filtered using a circuit similar to the one shown in Figure 13. The circuit should be placed as close as possible to the AVdd pin to ensure it filters out as much noise as possible.

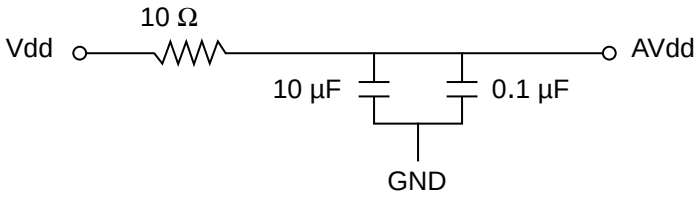


Figure 13. PLL Power Supply Filter Circuit

1.8.3 Decoupling Recommendations

Due to the PID6's dynamic power management feature, large address and data buses, and high operating frequencies, the PID6 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PID6 system, and the PID6 itself requires a clean, tightly regulated source of power. Therefore, it is strongly recommended that the system designer place at least one decoupling capacitor at each Vdd and OVdd pin of the PID6. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should vary in value from 220 pF to 10 µF to provide both high- and low-frequency filtering, and should be placed as close as possible to their associated Vdd or OVdd pin. Suggested values for the Vdd pins—220 pF (ceramic), 0.01 µF (ceramic), and 0.1 µF (ceramic). Suggested values for the OVdd pins—0.01 µF (ceramic), 0.1 µF (ceramic), and 10 µF (tantalum). Only SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd and OVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should also have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100 µF (AVX TPS tantalum) or 330 µF (AVX TPS tantalum).

1.8.4 Connection Recommendations

To ensure reliable operation, it is recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to Vdd. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

1.8.5 Pull-up Resistor Requirements

The PID6 requires high-resistive (weak: 10 KΩ) pull-up resistors on several control signals of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the PID6 or other bus master. These signals are—$\overline{\text{TS}}$, $\overline{\text{ABB}}$, $\overline{\text{DBB}}$, $\overline{\text{ARTRY}}$.

In addition, the PID6 has three open-drain style outputs that require pull-up resistors (weak or stronger: 4.7 KΩ–10 KΩ) if they are used by the system. These signals are—$\overline{\text{APE}}$, $\overline{\text{DPE}}$, and $\overline{\text{CKSTP\_OUT}}$.

During inactive periods on the bus, the address and transfer attributes on the bus are not driven by any master and may float in the high-impedance state for relatively long periods of time. Since the PID6 must continually monitor these signals for snooping, this float condition may cause excessive power draw by the input receivers on the PID6. It is recommended that these signals be pulled up through weak (10 KΩ) pull-up resistors or restored in some manner by the system. The snooped address and transfer attribute inputs are—A[0–31], AP[0–3], TT[0–4], $\overline{\text{TBST}}$, TSIZ[0–2], and $\overline{\text{GBL}}$.

The data bus input receivers are normally turned off when no read operation is in progress and do not require pull-up resistors on the data bus.

1.8.6 Thermal Management Information

This section provides thermal management information for the ceramic quad-flat package (CQFP) and the ceramic ball grid array (CBGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design—the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods—adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly (CBGA package); see Figure 14. This spring force should not exceed 5.5 pounds of force.

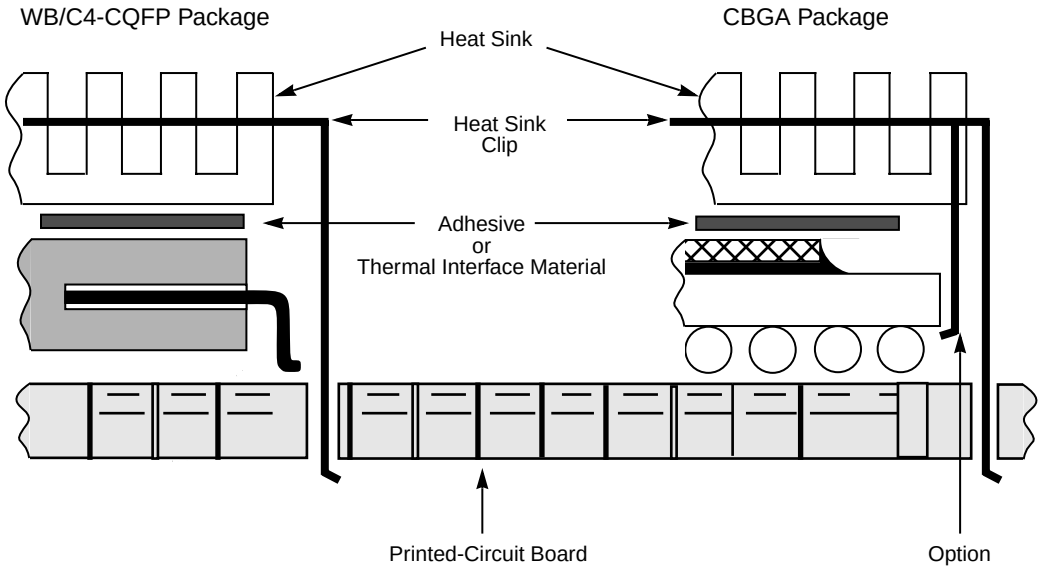


Figure 14. Package Exploded Cross-Sectional View with Several Heat Sink Options

The board designer can choose between several types of heat sinks to place on the PID6. There are several commercially-available heat sinks for the PID6 provided by the following vendors:

Chip Coolers Inc. 333 Strawberry Field Rd. Warwick, RI 02887-6979	800-227-0254 (USA/Canada) 401-739-7600
International Electronic Research Corporation (IERC) 135 W. Magnolia Blvd. Burbank, CA 91502	818-842-7277
Thermalloy 2021 W. Valley View Lane P.O. Box 810839	214-243-4321

Dallas, TX 75731

Wakefield Engineering 617-245-5900
60 Audubon Rd.
Wakefield, MA 01880

Aavid Engineering 603-528-3400
One Kool Path
Laconia, NH 03247-0440

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

1.8.6.1 Internal Package Conduction Resistance

For this packaging technology the intrinsic thermal conduction resistance (shown in Table 3) versus the external thermal resistance paths are shown in Figure 15 for a package with an attached heat sink mounted to a printed-circuit board.

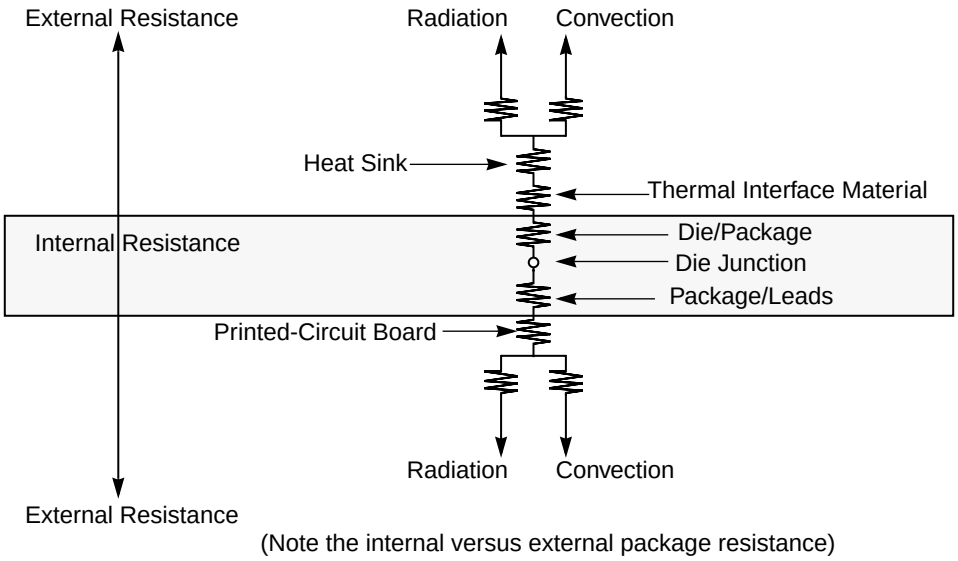


Figure 15. Package with Heat Sink Mounted to a Printed-Circuit Board

1.8.6.2 Adhesives and Thermal Interface Materials

A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 16 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 14). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors—thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.

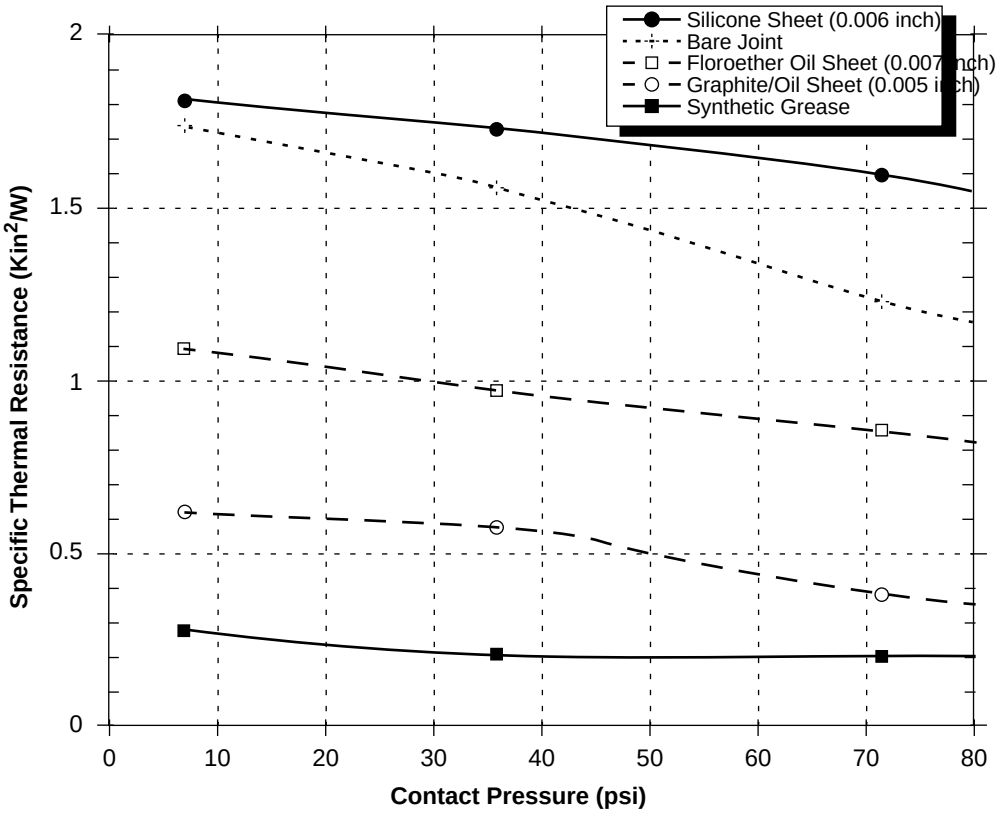


Figure 16. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Dow-Corning Corporation 517-496-4000
Dow-Corning Electronic Materials
PO Box 0997
Midland, MI 48686-0997

Chomerics, Inc. 617-935-4850
77 Dragon Court
Woburn, MA 01888-4850

Thermagon Inc. 216-741-7659
3256 West 25th Street
Cleveland, OH 44109-1668

Loctite Corporation 860-571-5100
1001 Trout Brook Crossing
Rocky Hill, CT 06067

AI Technology (e.g. EG7655) 609-882-2332
1425 Lower Ferry Rd
Trent, NJ 08618

1.8.6.3 Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

Where:

T_j is the die-junction temperature
T_a is the inlet cabinet ambient temperature
T_r is the air temperature rise within the computer cabinet
θ_{jc} is the junction-to-case thermal resistance
θ_{int} is the adhesive or interface material thermal resistance
θ_{sa} is the heat sink base-to-ambient thermal resistance
P_d is the power consumed by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 2. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30 to 40 °C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10 °C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1 °C/W. Assuming a T_a of 30 °C, a T_r of 5 °C, a CQFP package θ_{jc} = 2.2, and a power consumption (P_d) of 4.5 watts, the following expression for T_j is obtained:

Die-junction temperature: T_j = 30 °C + 5 °C + (2.2 °C/W + 1.0 °C/W + R_{sa}) * 4.5 W

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (R_{sa}) versus airflow velocity is shown in Figure 17.

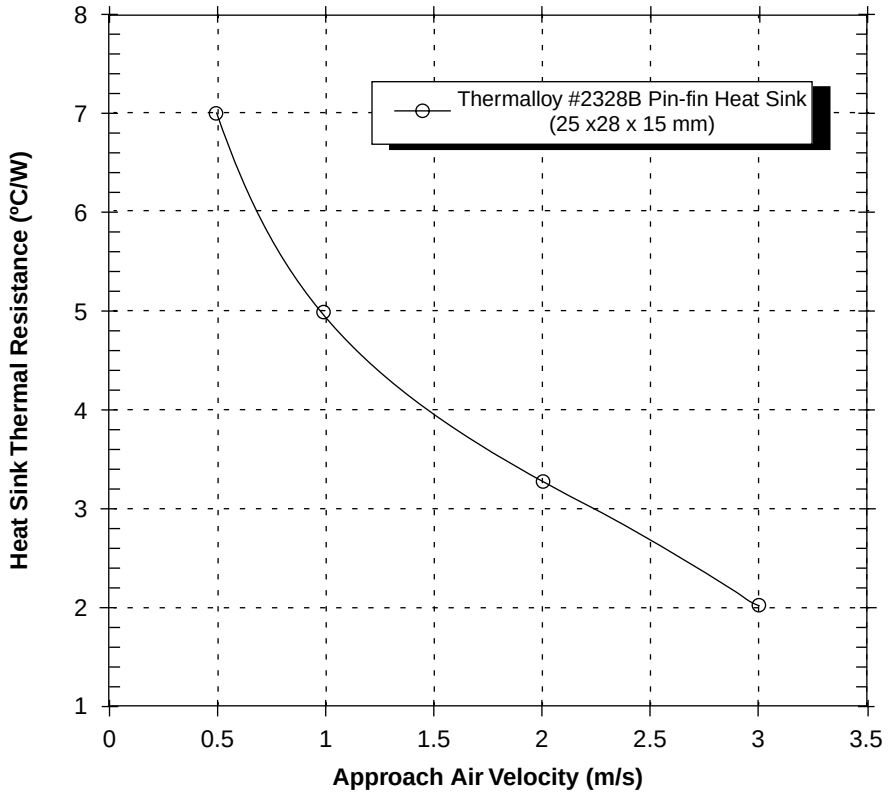


Figure 17. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity

Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7 °C/W, thus

$$T_j = 30°C + 5°C + (2.2\ °C/W + 1.0\ °C/W + 7\ °C/W) * 4.5\ W,$$

resulting in a die-junction temperature of approximately 81 °C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature—airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several “compact” thermal-package models are available within FLOTHERM®. These are available upon request.

1.9 Document Revision History

Table 13. Document Revision History

Document Revision	Substantive Change(s)
Rev 1	In Table 6, the minimun processor frequency for the 100 mhz and the 133 mhz parts was changed to 50 mhz. The maximum VCO frequency was changed to 266.66 mhz on and the minimum VCO frequency on the 133 mhz part was changed to 100 mhz.
	In Table 12 the CPU and VCO frequencies were changed to correspond to the the valid clock specifications as shown in Table 6.

1.10 Ordering Information

This section provides the part numbering nomenclature for the PID6. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office.

Figure 18 provides the Motorola part numbering nomenclature for the PID6. In addition to the processor frequency, the part numbering scheme also consists of a part modifier and application modifier. The part modifier indicates any enhancement(s) in the part from the original production design. The bus divider may specify special bus frequencies or application conditions. Each part number also contains a revision code. This refers to the die mask revision number and is specified in the part numbering scheme for identification purposes only.

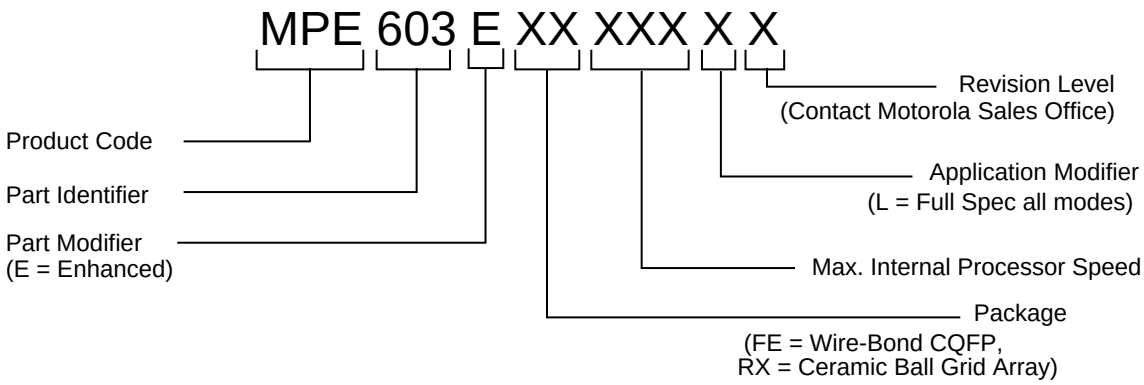


Figure 18. Motorola Part Number Key

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