

# System Reset (with built-in watchdog timer) Monolithic IC MM1145

## Outline

This IC has a built-in watchdog timer, with 2 channels for a clock monitoring function that monitors the microcomputer and outputs an intermittent reset signal if the microcomputer runs wild. Also, it has a power supply voltage monitoring function (system reset function) which generates a reset signal if power supply voltage is momentarily interrupted or drops, and performs power ON reset during normal power supply recovery and when power is turned on.

## Features

1. Built-in edge trigger input watchdog timer
2. 2 clock pulse monitoring
3. Power ON reset time ( $T_{PR}$ ) and watchdog timer monitoring time ( $T_{WD}$ ) can be set individually with external elements (R, C)
4. Excellent watchdog timer monitoring time ( $T_{WD}$ ) precision  
 A type :  $\pm 20\%$   
 B type :  $\pm 30\%$
5. Watchdog function stop pin allows use as system reset IC
6. Accurate power supply voltage drop detection  
 4.2V $\pm 3.5\%$
7. Detection voltage has hysteresis  
 100mV typ.  $\pm 0.14\%/^{\circ}\text{C}$
8. Low reset minimum voltage
9. Low current consumption  
 150 $\mu\text{A}$  typ.

## Package

SOP-8C (MM1145AF, MM1145BF)

## Applications

Voltage detection for CPUs, microcomputers, etc. and clock pulse monitoring

## Series Table

Model	$V_{SL}$	$T_{PR}$	$T_{WD}$	$T_{WR}$
MM1145A	4.2	100ms	50ms	10ms
MM1145B		40ms	110ms	10ms

\* $C_T=0.02\mu\text{F}$ ,  $R_C=1\text{M}\Omega$

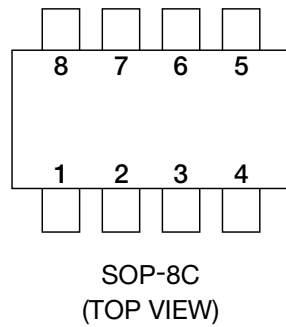
$V_{SL}$  : Reset detection voltage

$T_{PR}$  : Reset hold time during  $V_{CC}$  rise

$T_{WD}$  : Watchdog timer monitoring time

$T_{WR}$  : Reset time

## Pin Assignment

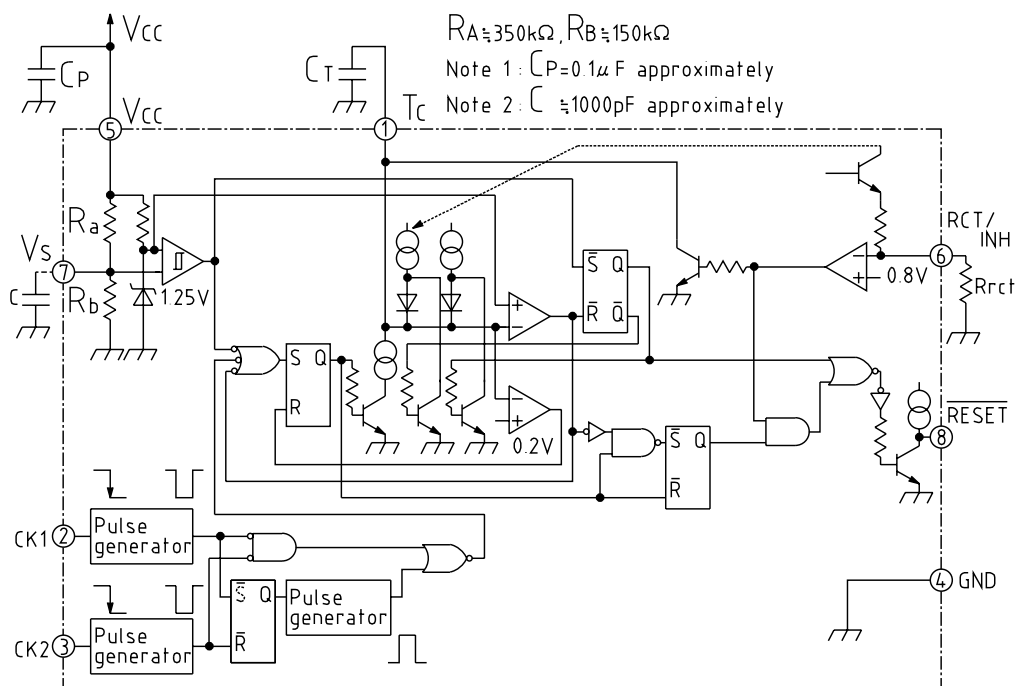


1	TC
2	CK1
3	CK2
4	GND
5	V <sub>CC</sub>
6	RCT
7	V <sub>S</sub>
8	$\overline{\text{RESET}}$

## Pin Description

Pin No.	Pin name	Function
1	TC	T <sub>WD</sub> , T <sub>WR</sub> , T <sub>PR</sub> time setting pins. Time determined by external capacitor.
2	CK1	Clock input pin 1 Clock input from logic system
3	CK2	Clock input pin 2 Clock input from logic system
4	GND	GND pin
5	V <sub>CC</sub>	Power supply pin Detection voltage 4.2V
6	RCT	Watchdog timer stop pin and T <sub>WD</sub> adjustment pin Operation modes : Operation → V <sub>CC</sub> , Stop → GND T <sub>WD</sub> time determined by external resistor R <sub>RCT</sub> and C <sub>T</sub>
7	V <sub>S</sub>	Detection voltage adjustment pin
8	$\overline{\text{RESET}}$	Reset output pin (low output)

## Block Diagram





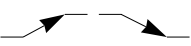
## Absolute Maximum Ratings

Item	Symbol	Rating	Units
Power supply voltage	$V_{CC \text{ max.}}$	-0.3~+7.5	V
CK pin input voltage	$V_{CK}$	-0.3~ $V_{CC}+0.3$ ( $\leq +7.5$ )	V
VS pin input voltage	$V_{VS}$	-0.3~ $V_{CC}+0.3$ ( $\leq +7.5$ )	V
Voltage applied to RCT pin	$V_{RCT}$	-0.3~ $V_{CC}+0.3$ ( $\leq +7.5$ )	V
Voltage applied to RESET pin	$V_{OH}$	-0.3~ $V_{CC}+0.3$ ( $\leq +7.5$ )	V
Allowable loss	$P_d$	300	mW
Storage temperature	$T_{STG}$	-40~+125	°C

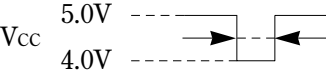
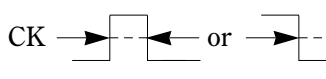
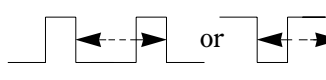
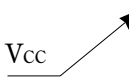
## Recommended Operating Conditions

Item	Symbol	Rating	Units
Power supply voltage	$V_{CC}$	+2.2~+7.0	V
RESET sync current	$I_{OL}$	0~4.0	mA
Clock monitoring time setting	$T_{WD}$	1.95~10000	ms
Power supply voltage rise and fall times	$t_{rV}, t_{rV}$	<300	µs
Clock rise and fall times	$t_{rC}, t_{rC}$	<100	µs
$C_T$ pin capacitance	$C_T$	0.002~2	µF
RCT pin resistance	$R_{RCT}$	0.39~2	MΩ
Operating temperature	$T_{OP}$	-25~+75	°C

## Electrical Characteristics (DC) (Except where noted otherwise, $T_a=25^\circ\text{C}$ , $V_{CC}=5.0\text{V}$ )

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units		
Consumption current	$I_{CC}$	During watchdog timer operation		150	180	µA		
Detection voltage	$V_{SL}$	$V_S=OPEN, V_{CC}$ 	4.05	4.20	4.35	V		
	$V_{SH}$	$V_S=OPEN, V_{CC}$ 	4.15	4.30	4.45			
Detection voltage temperature coefficient	$\frac{V_S}{\Delta T}$	$V_{SH}-V_{SL}, V_{CC}$ 		±0.01		%/°C		
Hysteresis voltage	$V_{HYS}$		50	100	150	mV		
CK input threshold	$V_{TH}$		0.8	1.2	2	V		
CK input current	$I_{IH}$	$V_{CK}=5.0\text{V}$		0	1	µA		
	$I_{IL}$	$V_{CK}=0\text{V}$	-14.5	-8.5	-4.5			
Output voltage (High)	$V_{OH}$	$I_{\overline{RESET}} = -1\mu\text{A}, V_S=OPEN$	4.0	4.5		V		
Output voltage (Low)	$V_{OL1}$	$I_{\overline{RESET}} = 0.5\text{mA}, V_S=0\text{V}$		0.10	0.20	V		
	$V_{OL2}$	$I_{\overline{RESET}} = 2.0\text{mA}, V_S=0\text{V}$		0.15	0.35 0.30			
Output sync current	$I_{OL}$	$V_{\overline{RESET}} = 1.0\text{V}, V_S=0\text{V}$	2	4		mA		
$C_T$ charge current	MM1145A	$I_{CT1}$	During watchdog timer operation		-0.40	-0.48	-0.60	µA
					-0.17	-0.22	-0.30	
	MM1145B	$I_{CT2}$	During power ON reset operation		-0.21	-0.31	-0.62	µA
					-0.62	-0.93	-2.33	
Minimum operating power supply voltage to ensure RESET	$V_{CCL}$	$V_{\overline{RESET}} = 0.4\text{V}$ $I_{\overline{RESET}} = 0.1\text{mA}$		0.8	1.0	V		

**Electrical Characteristics (DC)** (Except where noted otherwise, Ta=25°C, Vcc=5.0V)  
(Except where noted otherwise, resistance unit is Ω)

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units
V <sub>CC</sub> input pulse width	T <sub>PI</sub>	V <sub>CC</sub> 	8			μs
CK input pulse width	T <sub>CKW1</sub> T <sub>CKW2</sub>	CK 	3			μs
CK input cycle *7	T <sub>CK1</sub> T <sub>CK2</sub>		200			μs
Watchdog timer monitoring time *1	MM1145A	T <sub>WD</sub> C <sub>T</sub> =0.02μF, R <sub>RCT</sub> =1M	40	50	60	ms
	MM1145B		80	110	140	
Watchdog timer reset time *2	MM1145A	T <sub>WR</sub> C <sub>T</sub> =0.02μF, R <sub>RCT</sub> =1M	5	10	15	ms
	MM1145B		5	10	15	
Reset hold time for power supply rise *3	MM1145A	T <sub>PR</sub> C <sub>T</sub> =0.02μF R <sub>RCT</sub> =1M 	50	100	150	ms
	MM1145B		20	40	60	
Output delay time from V <sub>CC</sub> *4	T <sub>PD</sub>	RESET pin, R <sub>L</sub> =10k, C <sub>L</sub> =20pF		2	10	μs
Output rise time *5	t <sub>R</sub>	RESET pin, R <sub>L</sub> =10k, C <sub>L</sub> =20pF		2.0	4.0	μs
Output fall time *5	t <sub>F</sub>	RESET pin, R <sub>L</sub> =10k, C <sub>L</sub> =20pF		0.2	1.0	μs

Notes:

\*1 Monitoring time is the time from the last pulse (negative edge) of the timer clear clock pulse until reset pulse output.

In other words, reset output is output if a clock pulse is not input during this time.

\*2 Reset time means reset pulse width. However, this does not apply to power ON reset.

\*3 Reset hold time is the time from when V<sub>CC</sub> exceeds detection voltage (V<sub>SHR</sub>) during power ON reset until reset release (RESET output high).

\*4 Output delay time is the time from when power supply voltage drops below detection voltage (V<sub>SL</sub>) until reset state occurs (RESET output low).

\*5 The voltage range when measuring output rise and fall time is 10~90%.

\*7 1 Set CK1 and CK2 input cycles within the following range.

$$T_{CK1} \leq nT_{CK2} < T_{WD} \text{ (ms) (n} \leq 1)$$

RESET output may go low even if CK1 and CK2 are input without these conditions being met.

(Recommended use is for T<sub>CK1</sub> ≤ nT<sub>CK2</sub>)

2 T<sub>CK1</sub>, T<sub>CK2</sub> ≤ 200 μs results in the following operation.

Discharge switches to charging with the CK2 pulse (negative edge) that inputs 200μs after C<sub>T</sub> switches from charging to discharge by the CK2 pulse (negative edge). RESET output stays high while this operation is being repeated. (However, T<sub>CK1</sub>, T<sub>CK2</sub> ≥ 20μs.)

### Formula for C<sub>T</sub> Pin External Constant

Watchdog timer monitoring time (T<sub>WD</sub>), watchdog timer reset time (T<sub>WR</sub>) and reset hold time (T<sub>PR</sub>) during power supply rise can be changed by varying C<sub>T</sub> capacitance. T<sub>WD</sub> also can be changed with R<sub>RCT</sub>.

The variable times are expressed by the following.

1. MM1145A

$$T_{PR} (ms) \approx 5000 \times C_T (\mu F)$$

$$T_{WD} (ms) \approx 2500 \times C_T (\mu F) \times R_{RCT} (M\Omega)$$

$$T_{WR} (ms) \approx 500 \times C_T (\mu F)$$

Example : when C<sub>T</sub>=0.02μF, R<sub>RCT</sub>=1MΩ

$$T_{PR} \approx 100ms$$

$$T_{WD} \approx 50ms$$

$$T_{WR} \approx 10ms$$

2. MM1145B

$$T_{PR} (ms) \approx 2000 \times C_T (\mu F)$$

$$T_{WD} (ms) \approx 5500 \times C_T (\mu F) \times R_{RCT} (M\Omega)$$

$$T_{WR} (ms) \approx 500 \times C_T (\mu F)$$

Example : when C<sub>T</sub>=0.02μF, R<sub>RCT</sub>=1MΩ

$$T_{PR} \approx 40ms$$

$$T_{WD} \approx 110ms$$

$$T_{WR} \approx 10ms$$

### Formula for Watchdog Timer Monitoring Time (T<sub>WD</sub>) Adjustment

The ratio between T<sub>PR</sub> and T<sub>WD</sub> can be changed within the range below by adjusting T<sub>WD</sub> with R<sub>RCT</sub>.

1. MM1145A

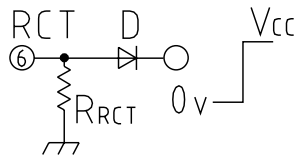
$$T_{WD}/T_{PR} \approx 2.0 \times R_{RCT} (0.39 (M\Omega) \leq R_{RCT} \leq 2 (M\Omega))$$

2. MM1145B

$$T_{WD}/T_{PR} \approx 2.75 \times R_{RCT} (0.39 (M\Omega) \leq R_{RCT} \leq 2 (M\Omega))$$

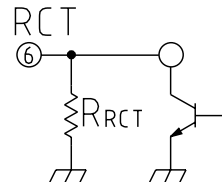
### How to Use RCT Pin

Example 1



1. Watchdog timer operates when RCT pin is open.
2. Watchdog timer stops operating when RCT pin is connected to ground.

Example 2



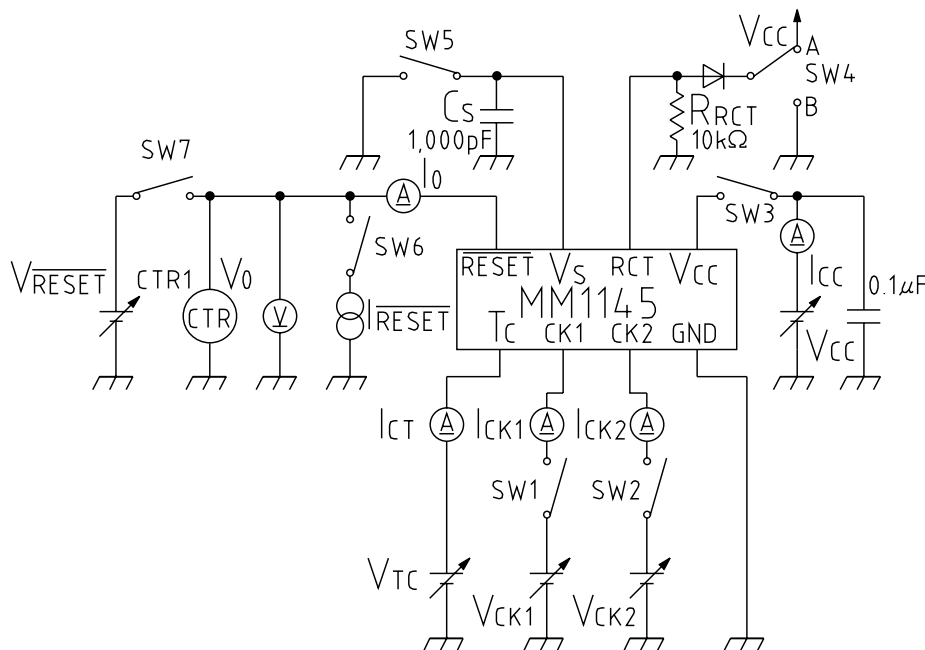
### Description of Operation

1.  $\overline{RESET}$  goes low when V<sub>CC</sub> rises to approximately 0.8V.  
Approximately 1μA (V<sub>CC</sub>=0.8V) of pull up current is output from RESET.
2. Capacitor C<sub>T</sub> charging starts when V<sub>CC</sub> rises to V<sub>SH</sub> (≈ 4.3V). Output is in reset state at this time.
3. Output reset is released ( $\overline{RESET}$  goes high) after a certain time (T<sub>PR</sub>), from when C<sub>T</sub> starts charging until discharge (the time from when C<sub>T</sub> voltage reaches a certain threshold value VT1 (≈ 1.4V) until C<sub>T</sub> voltage drops to a certain threshold value VT2 (≈ 0.2V).  
Reset hold time : T<sub>PR</sub> is as follows.  
T<sub>PR</sub> (ms) ≈ 5000 × C<sub>T</sub> (μF)  
C<sub>T</sub> charging starts again after reset release, and watchdog timer operation begins.  
Clock input during power ON reset time (T<sub>PR</sub>) will cause mis-operation.
4. If CK1 and CK2 are input in that order (or simultaneously) during C<sub>T</sub> charging, CK2 negative edge trigger causes the TC pin to switch from charging to discharge.
5. Discharge switches to charging when C<sub>T</sub> voltage drops to threshold value VT2 (≈ 0.2V). Steps 4 and 5 are repeated while a normal clock is input from the logic system.

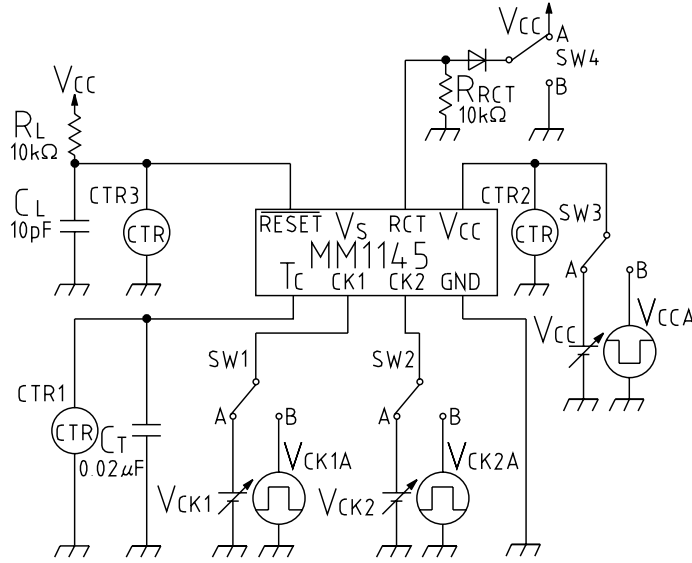
6. Operation is as follows if either clock CK1 or CK2 ceases (the figure shows CK1).  
 Output goes to reset state ( $\overline{\text{RESET}}$  goes low) when  $C_T$  voltage reaches reset ON threshold value  $V_{T1}$  ( $\approx 1.4V$ ).  
 The formula for  $C_T$  charging time ( $T_{WD}$ : watchdog timer monitoring time) until reset is output is as follows.  
 $T_{WD} \text{ (ms)} \approx 2500 \times C_T \text{ (}\mu\text{F)}$
7. Watchdog timer reset time  $T_{WR}$  is the discharge time until  $C_T$  voltage drops to reset OFF threshold value  $V_{T2}$  from reset ON threshold value  $V_{T1}$ . The formula is as follows.  
 $T_{WR} \text{ (ms)} \approx 500 \times C_T \text{ (}\mu\text{F)}$   
 After reset OFF threshold value is reached, output reset is released and  $C_T$  starts charging. Thereafter, steps 4 and 5 are repeated if a normal clock is input, and when one of the clocks ceases, 6 and 7 are repeated.  
 In the same way, 6 and 7 are repeated if both clocks CK1 and CK2 cease.
8. Reset is output when  $V_{CC}$  drops to  $V_{SL}$  ( $\approx 4.2V$ ).  $C_T$  is charged simultaneously.
9.  $C_T$  charging starts when  $V_{CC}$  rises to  $V_{SH}$ .  
 When  $V_{CC}$  drops momentarily,  $C_T$  charging begins after the charge is first discharged, if the time from  $V_{CC}$  dropping below  $V_{SL}$  until it rises to  $V_{SH}$  is longer than the  $V_{CC}$  input pulse width standard value  $T_{PI}$ .
10. Output reset is released after  $V_{CC}$  goes above  $V_{SH}$  and after  $T_{PR}$ , and the watchdog timer starts.
11. Watchdog timer operation can be stopped by switching  $R_{CT}$  voltage from high to low. (Clocks CK1 and CK2 are invalid. Regardless of status, TC pin voltage discharges quickly and goes to 0V.) This operation can be applied from any timing. In this state the IC functions as a reset IC with power ON reset.
12. Watchdog timer operation re-starts when  $R_{CT}$  voltage switches to high.
13. When power is OFF, reset is output if  $V_{CC}$  goes below  $V_{SL}$ .
14. When  $V_{CC}$  drops to 0V, reset output is held until  $V_{CC}$  reaches 0.8V.

## Measuring Circuit

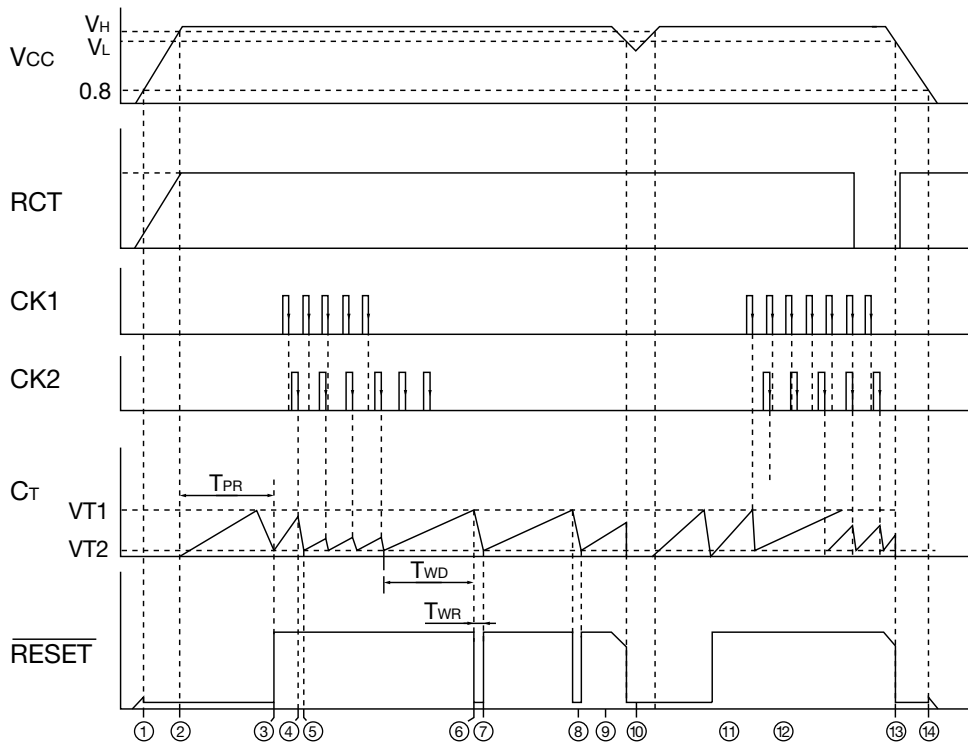
### Measuring Circuit 1



Measuring Circuit 2



Timing Chart



Basic Circuit Diagram

