OKI Semiconductor

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MSM7728

Single Rail Linear CODEC

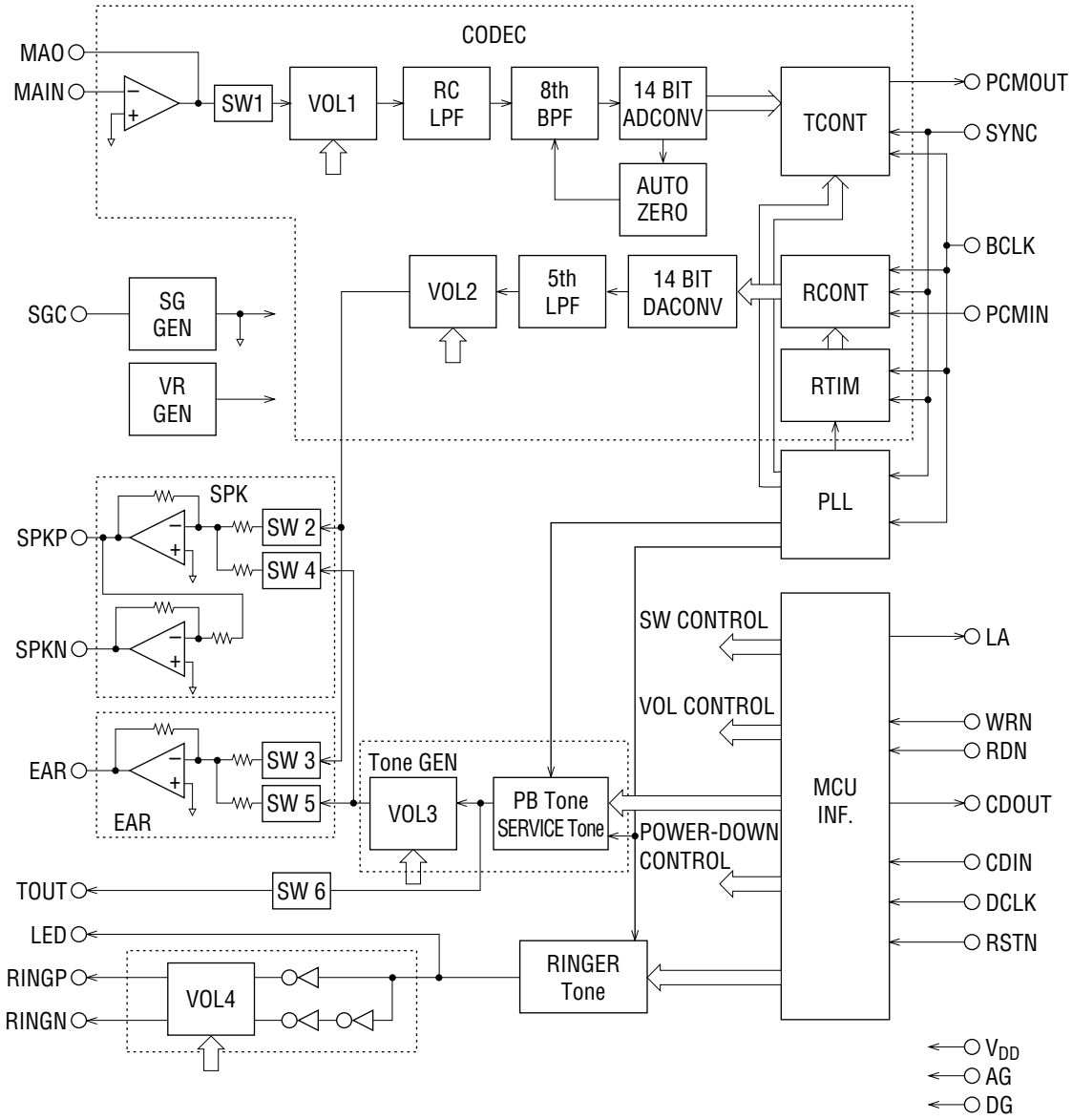
GENERAL DESCRIPTION

The MSM7728 is a single-channel linear CODEC CMOS IC for voice signals that contains filters for A/D and D/A conversions.
Designed especially for a single-power supply and low-power applications, the device is optimized for applications for the analog interfaces of audio signal processing DSPs and digital wireless systems.
The analog outputs include the speaker drive output, earphone drive output and ringer output. Therefore, the sound interface can be configured with a few external circuits.

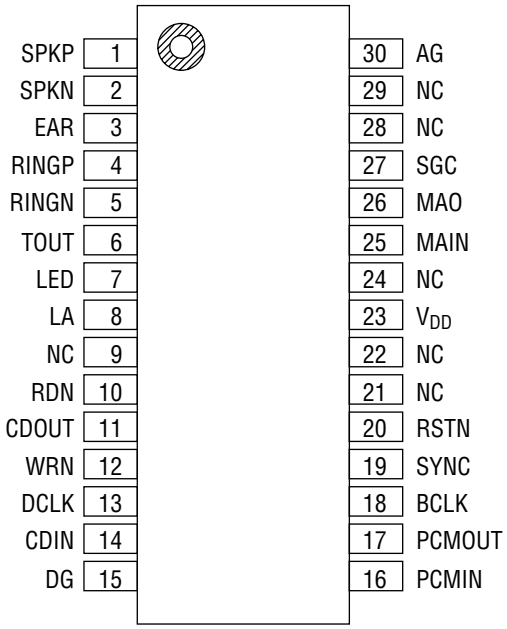
FEATURES

- Single power supply : 2.5 V to 3.6 V
- Low power consumption
  Operating mode : 36 mW Typ.
  Power down mode : 0.003 mW Typ.
- Digital signal input/output interface : 14-bit serial code in 2's complement format
- Transmission clock frequency : 112 kHz min., 2048 kHz max.
- Filter characteristics : Complies with ITU-T Recommendation G.714
- Built-in PLL eliminates a master clock
- Built-in PB tone signal generator
- Built-in service tone generator
- Built-in ringer tone generator
- General latch output: 1 bit
- Both transmit and receive gain adjustable by external control
- Receive interface: Speaker direct drive output
  Earphone interface output : 600 Ω, 1 mW max.
  Ringer output : 70 nF, 4 V_{PP}
- Transmit gain adjustable using an external resistor
- Transmit microphone amplifier is eliminated by the gain setting of a maximum of 36 dB.
- Built-in reference voltage supply
- Serial 8-bit processor interface
- Package:
  30-pin plastic SSOP (SSOP30-P-56-0.65-K) (Product name: MSM7728GS-K)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



NC: No connection

30-Pin Plastic SSOP

PIN AND FUNCTIONAL DESCRIPTIONS

V_{DD}

Power supply pin for 2.5 to 3.6 V (Typically 3.0 V).

AG

Analog signal ground.

DG

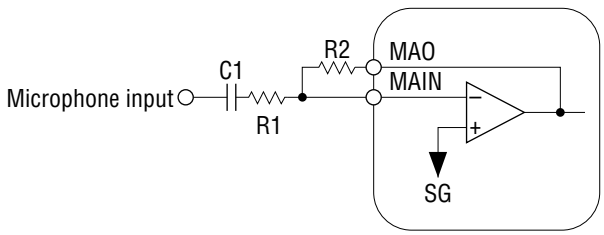
Ground pin for the digital signal circuits.
This ground is separated from the analog signal ground in this device. The DG pin must be connected to the AG pin on the printed circuit board.

SGC

Bypass capacitor pin for generating the signal ground voltage level.
Insert a 0.1 µF capacitor with excellent high frequency characteristics between the AG pin and the SGC pin.

MAIN, MAO

Transmit microphone input and level adjustment.
MAIN is connected to the inverting input of the op-amp, and MAO is connected to the output of the op-amp. This amplifier can set up a gain to a maximum of 36dB by using an external resistor.
Level adjustment should be performed in a way below.
A transmit level of +6, 0, –6, or –12dB can be selected using control data from the processor interface.
When CODEC is turned off, the MAO output goes high impedance.



R1 : variable
R2 > 20 kΩ
C1 > 1/(2 × 3.14 × 30 × R1) (F)

Gain = R2/R1 < 63

SPKP, SPKN

These pins are used for speaker driving.
The SPKN output is reversed in phase against the SPKP output when the gain is 1.
The receive output signal amplitude is $2.2V_{PP}$ at maximum.
These outputs swing around the SG potential (signal ground potential, $V_{DD}/2$) and can drive the minimum 0.6kΩ load in pushpull driving mode.
The maximum output amplitude is $4.4V_{PP}$ in pushpull driving mode (a load is inserted between SPKN and SPKP).
Control data from the processor interface allows selecting the D/A conversion output, PB tone output, or service tone output and also can provide a level control and mute control. When SPK is turned off, the SG potential is output with high resistance.

EAR

Analog output for external accessary circuit.
This output swings around the SG potential and can drive the minimum 0.6kΩ against the SG potential.
Control data from the processor interface allows selecting the D/A conversion output, PB tone output, or service tone output and also can provide a level control and mute control. When EAR is turned off, the SG potential is output with high resistance.

BCLK

Shift clock signal input for PCMIN and PCMOUT.
The frequency is equal to the data signaling rate.

SYNC

Synchronizing signal input.
In the transmit section, the PCM output signal from the PCMOUT pin is output synchronously with this synchronizing signal. This synchronizing signal triggers the PLL and synchronizes all timing signals of the transmit section.
In the receive section, 14 bits required are selected from serial input of PCM signals on the PCMIN pin by the synchronizing signal.
Signals in the receive section are synchronized by this synchronizing signal. This signal must be synchronized in phase with the BCLK.
When this signal frequency is 8 kHz, the transmit and receive paths have the frequency characteristics specified by ITU-T G. 714. The frequency characteristics for 8 kHz are specified in this data sheet.
For different frequencies of the SYNC signal, the frequency values in this data sheet should be translated according to the following equation:

$$\frac{\text{Frequency values described in the data sheet}}{8\ \text{kHz}} \times \text{the SYNC frequency values to be actually used}$$

PCMIN

PCM signal input.
A serial PCM signal input to this pin is converted to an analog signal synchronously with the SYNC signal and BCLK signal.
The data signaling rate of the PCM signal is equal to the frequency of the BCLK signal.
The PCM signal is shifted at the falling edge of the BCLK signal. The PCM signal is latched into an internal register when shifted by 14 bits.
The top of the data (MSD) is identified at the rising edge of SYNC.
The input signal should be input in the 14-bit 2's complement format.
The MSD bit represents the polarity of the signal with respect to the signal ground.

PCMOUT

PCM signal output.
The PCM output signal is output starting with MSD in sequential order, synchronously with the rising edge of the BCLK signal.
MSD may be output at the rising edge of the SYNC signal, depending on the timing between BCLK and SYNC.
This pin is in a high impedance state except during 14-bit PCM output. It is also high impedance when the CODEC is turned off.
A pull-up resistor must be connected to this pin, because its output is configured as an open drain.
The output coding format is in 14-bit 2's complement.
The MSD represents a polarity of the signal with respect to the signal ground.

Table 1

Input/Output Level	PCMIN/PCMOUT
	MSD
+Full scale	0 1 1 1 1 1 1 1 1 1 1 1 1 1
+1	0 0 0 0 0 0 0 0 0 0 0 0 0 1
0	0 0 0 0 0 0 0 0 0 0 0 0 0 0
–1	1 1 1 1 1 1 1 1 1 1 1 1 1 1
–Full scale	1 0 0 0 0 0 0 0 0 0 0 0 0 0

WRN, RDN, DCLK, CDIN, CDOUT

Serial control ports for microcontroller interface.
Writing data to 8-bit control registers allows controling the transmit speech path/receive speech path mute, transmit speech path/receive speech path level, PB tone, service tone, and ringer.
WRN is the write control signal input, RDN is the read control signal input, DCLK is the clock signal input for data shift, CDIN is the control data input, CDOUT is the control data output.
When reset (RSTN=0), the control registers are reset to the initial values as described in "Control Data Description".
The initial values remains unchanged until control data is written after reset.
Writing of control data: When WRN is at digital "0", data that is entered in CDIN is shifted at the rising edge of the DCLK signal pulse and is latched in an internal control register.
Reading of control data: When RDN is at digital "0", control data is output from CDOUT at the rising edge of a DCLK signal pulse.
See Figure 2 for write and read timings.

RINGP, RINGN

Ringer (sounder) drive outputs.
The sounder can be structured by putting a piezo-electric type sounding body (equivalent capacitance: less than 70nF) between RINGP and RINGN.

LED

Ringer digital level output. This pin is used for LED blinking synchronous with the ringer.

LA

General latch output. This output is used as a control signal for a peripheral circuit because this output can be set to digital "0" or "1" by writing data from a microcontroller interface.

TOUT

PB tone/service tone output. When SW6 is in the ON state, tone is output.
The output resistance of this pin is approximately 10kΩ, which should be taken into account when using it externally.

RSTN

Control register reset signal input. When this pin is set to digital "0" level.
All control registers are reset to the initial values.
Be sure to reset the control registers after turning on the power.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	V_{DD}	AG = DG = 0 V	–0.3 to +7.0	V
Analog Input Voltage	V_{AIN}	AG = DG = 0 V	–0.3 to V_{DD} + 0.3	V
Digital Input Voltage	V_{DIN}	AG = DG = 0 V	–0.3 to V_{DD} + 0.3	V
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage	V_{DD}	—	2.5	3.0	3.6	V
Operating Temperature	Ta	—	–30	+25	+85	°C
Analog Input Voltage	V_{AIN}	Gain = 1	—	—	1.4	V_{PP}
High Level Input Voltage	V_{IH}	SYNC, BCLK, PCMIN, WRN, RDN, DCLK, CDIN, RSTN	0.45 × V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}		0	—	0.16 × V_{DD}	V
Clock Frequency	F_C	BCLK	14 × Fs	—	128 × Fs	kHz
Sync Pulse Frequency	F_S	SYNC	4.0	8.0	12	kHz
Clock Duty Ratio	D_C	BCLK	40	50	60	%
Digital Input Rise Time	t_{Ir}	SYNC, BCLK, PCMIN, WRN, RDN, DCLK, CDIN, RSTN	—	—	50	ns
Digital Input Fall Time	t_{If}		—	—	50	ns
Sync Signal Timing	t_{XS}	BCLK→SYNC, See Fig.1	100	—	—	ns
	t_{SX}	SYNC→BCLK, See Fig.1	100	—	—	ns
High Level Sync Pulse Width *1	t_{WSH}	SYNC, See Fig.1	1 BCLK	—	—	—
Low Level Sync Pulse Width *1	t_{WSL}	SYNC, See Fig.1	1 BCLK	—	—	—
PCMIN Setup Time	t_{DS}	Refer to Fig.1	100	—	—	ns
PCMIN Hold Time	t_{DH}	Refer to Fig.1	100	—	—	ns
Digital Output Load	R_{DL}	Pull-up resistor	0.5	—	—	kΩ
	C_{DL}	—	—	—	100	pF
DCLK Pulse Width	t_{WCL}	DCLK Low width, See Fig.2	50	—	—	ns
	t_{WCH}	DCLK High width, See Fig.2	50	—	—	
WRN Timing	t_{WR1}	DCLK→WRNL, See Fig.2	50	—	—	ns
	t_{WR2}	WRNL→DCLK, See Fig.2	50	—	—	
	t_{WR3}	DCLK→WRNH, See Fig.2	50	—	—	ns
	t_{WR4}	WRNH→DCLK, See Fig.2	50	—	—	
WRN Period	P_{WRN}	—	9DCLK	—	—	—

*1 For example, the minimum pulse width of SYNC is 488 ns when the frequency of BCLK is 2048 kHz.

RECOMMENDED OPERATING CONDITIONS (Continued)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
RDN Timing	t_{RD1}	DCLK→RDNL, See Fig.2	50	—	—	ns
	t_{RD2}	RDNL→DCLK, See Fig.2	50	—	—	
	t_{RD3}	DCLK→RDNH, See Fig.2	50	—	—	ns
	t_{RD4}	RDNH→DCLK, See Fig.2	50	—	—	
RDN Period	P_{RDN}	—	9DCLK	—	—	—
CDIN Setup Time	t_{CDS}	See Fig.2	50	—	—	ns
CDIN Hold Time	t_{CDH}	See Fig.2	50	—	—	
Analog Input Allowable DC Offset	V_{off}	Transmit gain stage, Gain = 0 dB	–100	—	+100	mV
		Transmit gain stage, Gain = 20 dB	–10	—	+10	mV
Allowable Jitter Width	—	SYNC, BCLK	—	—	1000	ns
PCM Data Output Delay Time	t_{SD}	C_L = 50 pF + 1 LSTTL Pull-up resistor = 500 Ω	20	—	100	ns
	t_{XD1}		20	—	100	
	t_{XD2}		20	—	100	
	t_{XD3}		20	—	100	
Control Data Output Delay Time	t_{CD1}	—	50	—	—	ns
	t_{CD2}		50	—	—	

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(Fs = 8 kHz, V_{DD} = 2.5 V to 3.6 V, Ta = –30°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current	I_{DD1}	Operating mode, No signal	V_{DD} = 3.6 V	—	20	—	mA
			V_{DD} = 3.0 V	—	12	—	mA
	I_{DD2}	Power-off mode		—	70	200	µA
High Level Input Voltage	V_{IH}	SYNC, BCLK, PCMIN, WRN, RDN, CDIN, DCLK, RSTN		0.45 × V_{DD}	—	V_{DD}	V
Low Level Input Voltage	V_{IL}			0.0	—	0.16 × V_{DD}	V
High Level Input Leakage Current	I_{IH}	—		—	—	2.0	µA
Low Level Input Leakage Current	I_{IL}	—		—	—	0.5	µA
Digital Output Low Voltage	V_{OL}	PCMOUT pull-up resistor = 500 Ω		0.0	0.2	0.4	V
		LA, LED, CDOUT I_{OL} = 0.4mA					
Digital Output High Voltage	V_{OH}	LA, LED, CDOUT I_{OH} = 1µA		V_{DD} – 0.2			V
Digital Output Leakage Current	I_O	—		—	—	10	µA
Input Capacitance	C_{IN}	—		—	5	—	pF

Transmit Analog Interface Characteristics

(Fs = 8 kHz, V_{DD} = 2.5 V to 3.6 V, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Resistance	R_{INX}	MAIN	10	—	—	MΩ
Output Load Resistance	R_{LGX}	MAO with respect to SG potential	30	—	—	kΩ
Output Load Capacitance	C_{LGX}		—	—	30	pF
Output Amplitude	V_{OGX}		–0.7	—	+0.7	V
Offset Voltage	V_{OSGX}	MAO with respect to SG potential (DC Gain = 1)	–20	—	+20	mV

Receive Analog Interface Characteristics

(Fs = 8 kHz, V_{DD} = 2.5 V to 3.6 V, Ta = –30°C to +85°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output Resistance	R_OSP	SPKP, SPKN	—	—	10	Ω
	R_OER	EAR	—	—	100	Ω
	R_OTO	TOUT	—	10	—	kΩ
Output Load Resistance	R_{LSP}	SPKP-SPKN	600	—	—	Ω
	R_{LER}	EAR with respect to SG potential	600	—	—	Ω
Output Load Capacitance	C_{LAO}	Output open	—	—	50	pF
Output Amplitude	V_{OAO}	SPKP, SPKN, EAR	–1.1	—	+1.1	V
Offset Voltage	V_{OSA}	SPKP, SPKN, EAR, TOUT with respect to SG potential	–100	—	+100	mV

AC Characteristics

(Fs = 8 kHz, V_{DD} = 2.5 V to 3.6 V, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Overall Frequency Response	Loss 1	60	0	Analog to Analog	20	—	—	dB
	Loss 2	300			–0.2	—	+0.4	
	Loss 3	1020			Reference value			
	Loss 4	2020			–0.2	—	+0.4	
	Loss 5	3000			–0.2	—	+0.4	
	Loss 6	3400			0	—	1.6	
Transmit Frequency Response (Expected Value)	Loss T1	60	0		20	—	—	dB
	Loss T2	300			–0.15	—	+0.2	
	Loss T3	1020			Reference value			
	Loss T4	2020			–0.15	—	+0.2	
	Loss T5	3000			–0.15	—	+0.2	
	Loss T6	3400			0	—	0.8	
Receive Frequency Response (Expected Value)	Loss R1	300	0		–0.15	—	+0.2	dB
	Loss R2	1020			Reference value			
	Loss R3	2020			–0.15	—	+0.2	
	Loss R4	3000			–0.15	—	+0.2	
	Loss R5	3400			0.0	—	0.8	
Overall Signal to Distortion Ratio	SD 1	1020	3	Analog to Analog *1 V_{DD} = 2.7 to 3.3 V	57.0	—	—	dB
	SD 2		0		57.0	—	—	
	SD 3		–10		50.0	—	—	
	SD 4		–30		32.0	—	—	
	SD 5		–40		23.0	—	—	
	SD 6		–45		20.0	—	—	
Transmit Signal to Distortion Ratio (Expected Value)	SD T1	1020	3	*1	58	—	—	dB
	SD T2		0		58	—	—	
	SD T3		–10		58	—	—	
	SD T4		–30		38	—	—	
	SD T5		–40		28	—	—	
	SD T6		–45		23	—	—	
Receive Signal to Distortion Ratio (Expected Value)	SD R1	1020	3	*1	60	—	—	dB
	SD R2		0		60	—	—	
	SD R3		–10		60	—	—	
	SD R4		–30		40	—	—	
	SD R5		–40		30	—	—	
	SD R6		–45		25	—	—	

*1 Psophometric filter is used.

AC Characteristics (Continued)

(Fs = 8 kHz, V_{DD} = 2.5 V to 3.6 V, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition	Min.	Typ.	Max.	Unit
Overall Gain Tracking	GT 1	1020	3	Analog to Analog	–0.4	+0.01	+0.4	dB
	GT 2		–10		Reference value			
	GT 3		–40		–0.4	0.0	+0.4	
	GT 4		–50		–1.0	–0.03	+1.0	
	GT 5		–55		–1.5	+0.15	+1.5	
Transmit Gain Tracking (Expected Value)	GT T1	1020	3		–0.3	+0.01	+0.3	dB
	GT T2		–10		Reference value			
	GT T3		–40		–0.3	0.0	+0.3	
	GT T4		–50		–0.6	–0.03	+0.6	
	GT T5		–55		–1.2	+0.15	+1.2	
Receive Gain Tracking (Expected Value)	GT R1	1020	3		–0.3	–0.06	+0.3	dB
	GT R2		–10		Reference value			
	GT R3		–40		–0.3	–0.02	+0.3	
	GT R4		–50		–0.6	–0.02	+0.6	
	GT R5		–55		–1.2	–0.27	+1.2	
Transmit Idle Channel Noise (Expected Value)	Nidle T	—	—	AIN: no signal	—	–72	–68	dBmOp
Receive Idle Channel Noise (Expected Value)	Nidle R	—	—	*1	—	–76	–74	
Output Level (Initial value) *2	AV T	1020	0	MAO-PCMOUT	0.312	0.350	0.393	Vrms
	AV_{SPK}			PCMIN-SPKP*3	0.245	0.275	0.309	
	AV_{EAR}			PCMIN-EAR *3				
Output Level (Deviation of Temperature and Power)	AV Tt			V_{DD} = 2.5 to 3.6 V Ta = –30 to +85°C	–0.2	—	+0.2	dB
	AV Rt				–0.2	—	+0.2	dB
Absolute Delay	T_d	1020	0	A to A BCLK = 128 kHz	—	—	0.6	ms
Transmit Group Delay	t_{GD} T1	500	0	*4	—	—	0.325	ms
	t_{GD} T2	600 to 2600			—	—	0.175	
	t_{GD} T3	2800			—	—	0.325	
Receive Group Delay	t_{GD} R1	500 to 2600	0	*4	—	0.00	0.125	ms
	t_{GD} R2	2800			—	0.12	0.325	
Crosstalk Attenuation	CR T	1020	0	TRANS → RECV	75	85	—	dB
	CR R			RECV → TRANS	70	80	—	

*1 Psophometric filter is used.

*2 AVT is the input level to output 0dBm0 pattern. VOL1 0dB setting.
AV_{SPK} is the level to be output from SPKP pin when 0dBm0 pattern is input.
AV_{EAR} is the level to be output from EAR pin when 0dBm0 pattern is input.

*3 VOL2 0dB setting

*4 The minimum value of group delay distortion is referenced.

AC Characteristics (Continued)

(Fs = 8 kHz, V_{DD} = 2.5 V to 3.6 V, Ta = –30°C to +85°C)

Parameter	Symbol	Freq. (Hz)	Level (dBm0)	Condition		Min.	Typ.	Max.	Unit
Discrimination	DIS	4.6 kHz to 72 kHz	0	0 to 4000 Hz		30	32	—	dB
Out-of-band Spurious	S	300 to 3400	0	4.6 kHz to 100 kHz		—	–37.5	–35	dBm0
Intermodulation Distortion	IMD	fa = 470 fb = 320	–4	2fa – fb		—	–52	–40	dBm0
Power Supply Noise Rejection Ratio	PSR T	0 to 50 kHz	50 mV_{PP}	Measured inband		—	30	—	dB
	PSR R								
PB Acknowledge Tone Output Level	V PB	SPKP, EAR VOL3 standard		High group		–27	–22	–19	dBV
				Low group		–28	–23	–20	
		TOUT		High group		–16	–11	–8	
				Low group		–17	–12	–9	
Service Tone Output Level	V RT	SPKP, EAR		VOL3 standard		–18	–15	–13	dBV
		TOUT				–8	–3	–1	
PB Acknowledge Tone Frequency Distortion	Df_{PB}	—				–1.5	—	+1.5	%
Service Tone Frequency Distortion	Df_{RT}					–1.5	—	+1.5	
VOL1 Gain Setting Value	Gv_{11}	1020	0	Referenced to 0dB setting	6dBsetting	5	6	7	dB
	Gv_{12}				–6dBsetting	–7	–6	–5	
	Gv_{13}				–12dBsetting	–13	–12	–11	
VOL2 Gain Setting Value	Gv_{21}	1020	0	Referenced to 0dB setting	6dBsetting	5	6	7	dB
	Gv_{22}				3dBsetting	2	3	4	
	Gv_{23}				–3dBsetting	–4	–3	–2	
	Gv_{24}				–6dBsetting	–7	–6	–5	
	Gv_{25}				–9dBsetting	–10	–9	–8	
	Gv_{26}				–12dBsetting	–13	–12	–11	
	Gv_{27}				–15dBsetting	–16	–15	–14	
VOL3 Gain Setting Value	Gv_{31}	1020	0	Referenced to 0dB setting	12dBsetting	10.5	12	13.5	dB
	Gv_{32}				8dBsetting	6.5	8	9.5	
	Gv_{33}				4dBsetting	2.5	4	5.5	
	Gv_{34}				–4dBsetting	–5.5	–4	–2.5	
	Gv_{35}				–8dBsetting	–9.5	–8	–6.5	
	Gv_{36}				–12dBsetting	–13.5	–12	–10.5	
	Gv_{37}				–16dBsetting	–17.5	–16	–14.5	

Ringing Tone

(Fs = 8 kHz, V_{DD} = 2.5 V to 3.6 V, Ta = –30°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Ringing Tone Output Amplitude	Sound volume1	730Ω between RINGP and RINGN	Sound volume max.	3.5	—	—	V_{PP}
	Sound volume2		Sound volume mid.	1.5	—	—	
	Sound volume3		Sound volume sma.1	0.5	—	—	
	Sound volume4		Sound volume sma.2	0.25	—	—	

TIMING DIAGRAMS

CODEC Interface Timing

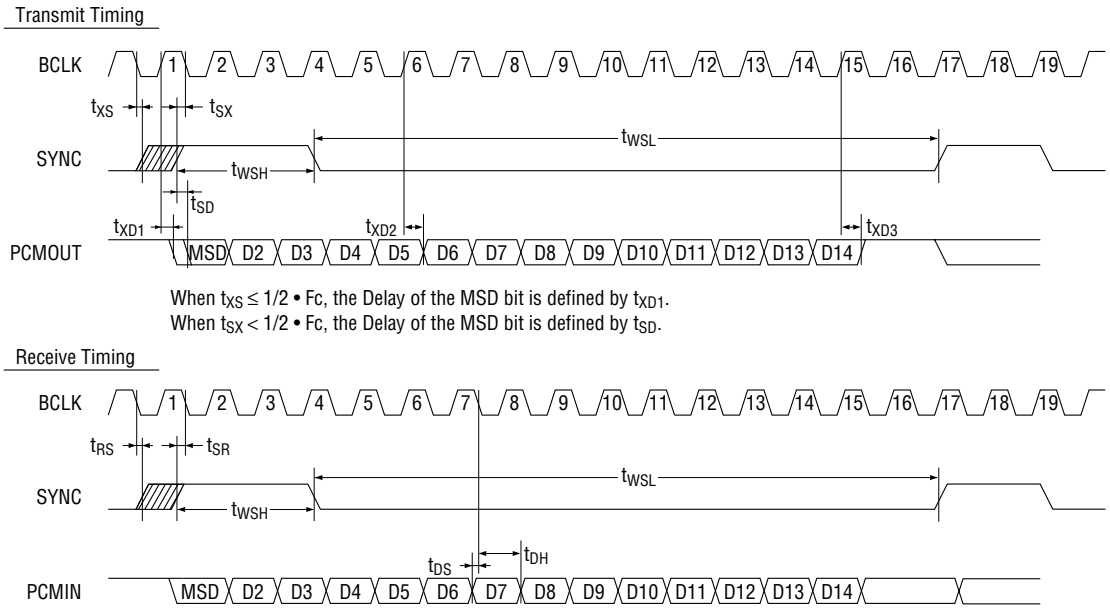


Figure 1 Basic Timing Diagram

Processor Interface Timing

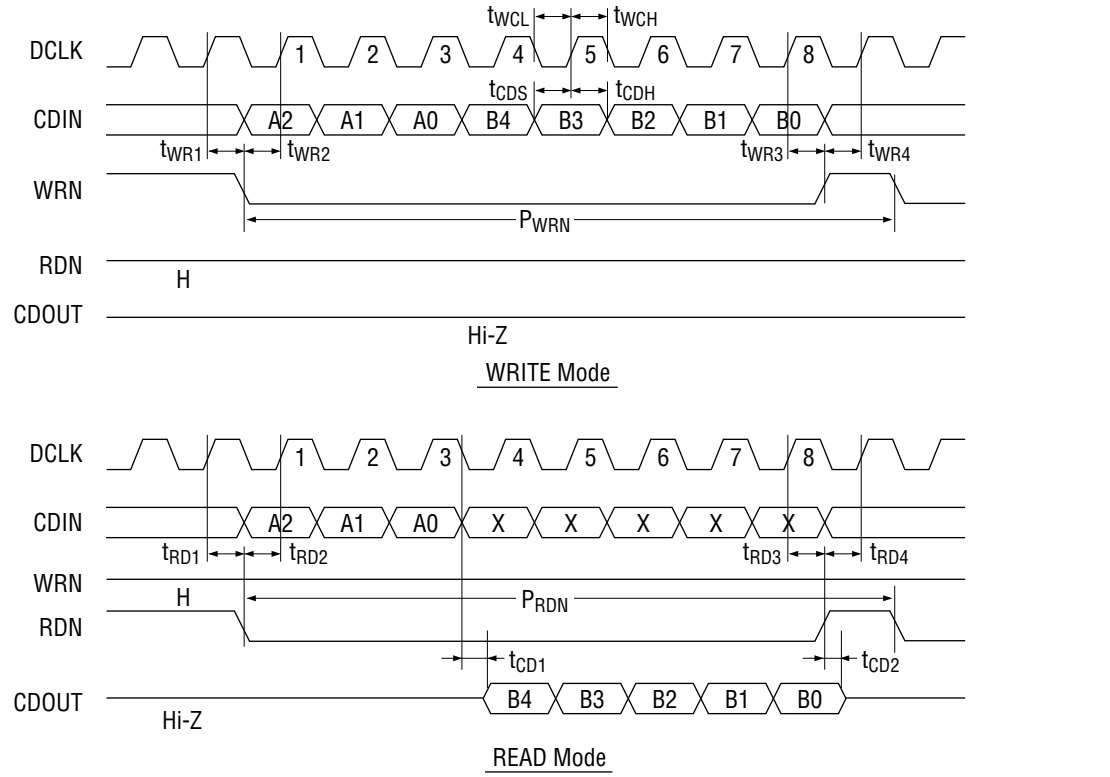


Figure 2 Processor Timing Diagram

FUNCTIONAL DESCRIPTION

Control Data Description

The MSM7728 has eight registers to control the analog pass switch, volume, and tone via an external CPU.
The data interface consists of 3-bit address data and 5-bit control data in the serial 8-bit format. The register map is as shown below.

	AD2	AD1	AD0	B4	B3	B2	B1	B0	Function	Read
CR0	0	0	0	VOL1			VOL2		VOL1, VOL2 gain setting	Enable
CR1	0	0	1	VOL3			VOL4		VOL3, VOL4 gain setting	Enable
CR2	0	1	0	SW5	SW4	SW3	SW2	SW1	SW ON/OFF control	Enable
CR3	0	1	1	—	—	—	LA	SW6	Latch output/SW ON/OFF control	Enable
CR4	1	0	0	PB tone					PB tone setting ON/OFF control	Disable
CR5	1	0	1	Service tone					Service tone setting ON/OFF control	Disable
CR6	1	1	0	Ringer tone					Ringer tone setting ON/OFF control	Disable
CR7	1	1	1	Power ON/OFF					Power ON/OFF control	Enable

Description of Each Register

CR0 - - - VOL1, VOL2 control

A2	A1	A0	B4	B3	B2	B1	B0		Function		Remarks
0	0	0	0	0					VOL1 gain setting	0dB (standard)	VOL1 and VOL2: Simultaneous setting Standard after reset is released
			0	1						6dB	
			1	0						–6dB	
			1	1						–12dB	
					0	0	0		VOL2 gain setting	0dB (standard)	
					0	0	1			6dB	
					0	1	0			3dB	
					0	1	1			–3dB	
					1	0	0			–6dB	
					1	0	1			–9dB	
					1	1	0			–12dB	
					1	1	1			–15dB	

CR1 - - - VOL3, VOL4 control

A2	A1	A0	B4	B3	B2	B1	B0		Function		Remarks
0	0	1	0	0	0				VOL3 gain setting	0dB (standard)	VOL3 and VOL4: Simultaneous setting Standard after reset is released
			0	0	1					12dB	
			0	1	0					8dB	
			0	1	1					4dB	
			1	0	0					–4dB	
			1	0	1					–8dB	
			1	1	0					–12dB	
			1	1	1					–16dB	
						0	0		Ringer sound volume	Middle (standard)	
						0	1			Maximum	
						1	0			Small 1	
						1	1			Small 2	

CR2 - - - SWcontrol

A2	A1	A0	B4	B3	B2	B1	B0		Function	Remarks
0	1	0							1: SW1 ON, 0: SW1 OFF	SW1 to SW5: Simultaneous setting Standard after reset is released
									1: SW2 ON, 0: SW2 OFF	
									1: SW3 ON, 0: SW3 OFF	
									1: SW4 ON, 0: SW4 OFF	
									1: SW5 ON, 0: SW5 OFF	

CR3 - - - SW & latch control

A2	A1	A0	B4	B3	B2	B1	B0		Function	Remarks
0	1	1	0	0	0				0: SW6 OFF, 1: SW6 ON	SW6 and LA: Simultaneous setting SW6: OFF, LA=0 after reset is released
									0: LA=0, 1: LA=1	

CR4 - - - PB tone control

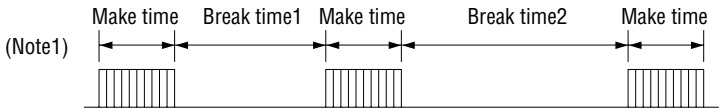
A2	A1	A0	B4	B3	B2	B1	B0	HEX Code	Function	Remarks
1	0	0	1	0	0	0	0	9 0h	PBtone 697Hz, 1209Hz	Output destination of PB tone: EAR SPKP SPKN PB OFF after reset is released
			1	0	0	0	1	9 1h	PBtone 697Hz, 1336Hz	
			1	0	0	1	0	9 2h	PBtone 697Hz, 1477Hz	
			1	0	0	1	1	9 3h	PBtone 697Hz, 1633Hz	
			1	0	1	0	0	9 4h	PBtone 770Hz, 1209Hz	
			1	0	1	0	1	9 5h	PBtone 770Hz, 1336Hz	
			1	0	1	1	0	9 6h	PBtone 770Hz, 1477Hz	
			1	0	1	1	1	9 7h	PBtone 770Hz, 1633Hz	
			1	1	0	0	0	9 8h	PBtone 852Hz, 1209Hz	
			1	1	0	0	1	9 9h	PBtone 852Hz, 1336Hz	
			1	1	0	1	0	9 Ah	PBtone 852Hz, 1477Hz	
			1	1	0	1	1	9 Bh	PBtone 852Hz, 1633Hz	
			1	1	1	0	0	9 Ch	PBtone 941Hz, 1209Hz	
			1	1	1	0	1	9 Dh	PBtone 941Hz, 1336Hz	
			1	1	1	1	0	9 Eh	PBtone 941Hz, 1477Hz	
			1	1	1	1	1	9 Fh	PBtone 941Hz, 1633Hz	
			0	0	0	0	0	8 0h	PBtone OFF	

CR5 - - - Service tone control

A2	A1	A0	B4	B3	B2	B1	B0	HEX Code	Frequency	Intermittent Time (Note1)			Remarks
										Make Time	Break Time1	Break Time2	
1	0	1	1	0	0	0	0	B 0h	400Hz	0.125sec	0.125sec	—	Output destination of PB tone: EAR SPKP SPKN
			1	0	0	0	1	B 1h	400Hz	0.5sec	0.5sec	—	
			1	0	0	1	0	B 2h	400Hz	0.25sec	0.25sec	—	
			1	0	1	0	0	B 4h	400Hz	Continuous	—	—	
			1	0	1	0	1	B 5h	1000Hz	Continuous	—	—	
			1	0	1	1	0	B 6h	2000Hz	Continuous	—	—	
			1	1	0	0	1	B 9h	400Hz/16Hz	1sec	2sec	—	
			1	1	0	1	0	B Ah	400Hz/16Hz	0.5sec	∞	—	
			1	1	0	1	1	B Bh	400Hz/16Hz	0.032sec	0.032sec	—	
			0	0	0	0	0	A 0h	Above tones stop				

CR6 - - - Ringer tone control

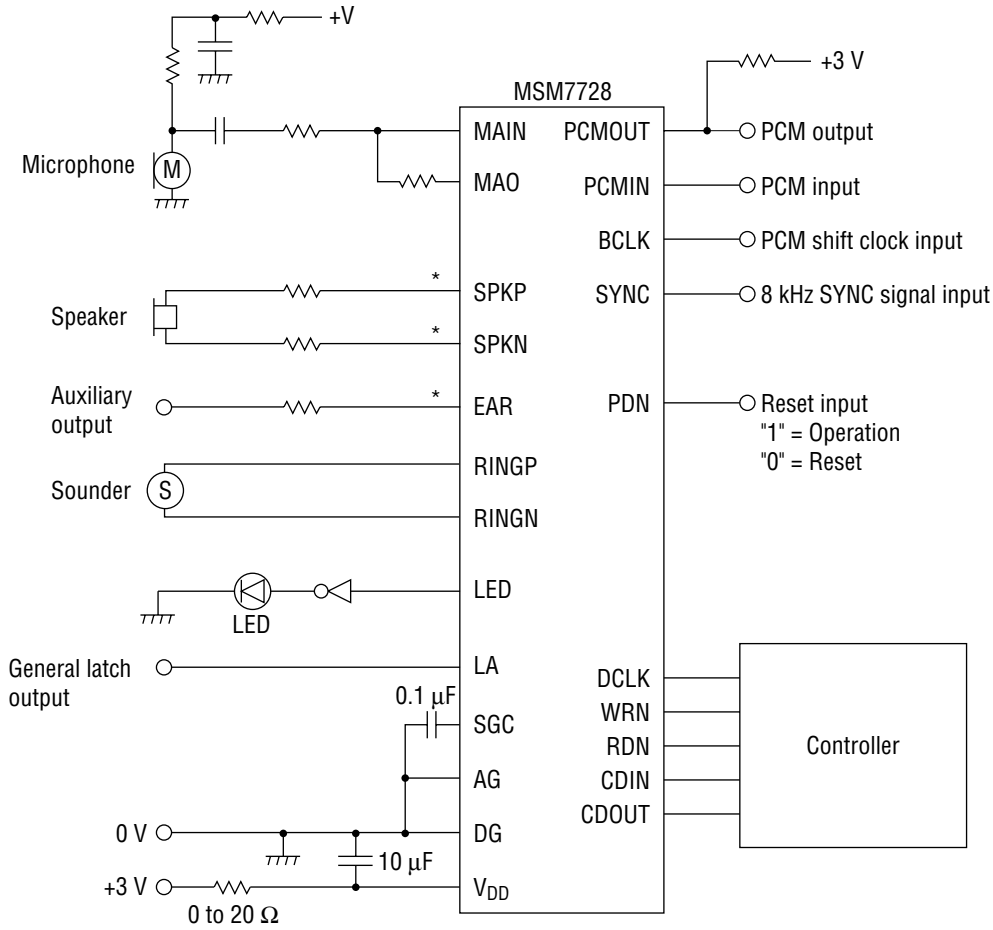
A2	A1	A0	B4	B3	B2	B1	B0	HEX Code	Frequency	Intermittent Time (Note1)			Remarks
										Make Time	Break Time1	Break Time2	
1	1	0	1	0	0	0	0	D 0h	16Hz alternation of 1kHz/1.3kHz	1sec	2sec	—	Output destination of PB tone: RINGP RINGN
			1	0	0	0	1	D 1h		0.5sec	0.5sec	—	
			1	0	0	1	0	D 2h		0.25sec	0.25sec	2.25sec	
			1	0	0	1	1	D 3h		Continuous	—	—	
			1	0	1	0	0	D 4h	16Hz alternation of 2kHz/2.6kHz	1sec	2sec	—	
			1	0	1	0	1	D 5h		0.5sec	0.5sec	—	
			1	0	1	1	0	D 6h		0.25sec	0.25sec	2.25sec	
			1	0	1	1	1	D 7h		Continuous	—	—	
			1	1	0	0	1	D 9h	400Hz	Continuous	—	—	
			1	1	0	1	0	D Ah	1kHz	Continuous	—	—	
			1	1	0	1	1	D Bh	2kHz	Continuous	—	—	
			0	0	0	0	0	C 0h	Above tones stop				



CR7 - - - Power-on/off control

A2	A1	A0	B4	B3	B2	B1	B0	Function	Remarks
1	1	1						0: CODEC power-off , 1: CODEC power-on	All paths enter a power-down state after reset is released
								0: SPK power-off , 1: SPK power-on	
								0: EAR power-off , 1: EAR power-on	
								0: toneGEN power-off , 1: toneGEN power-on	
								0: SG/VR/PLL power-off , 1: SG/VR/PLL power-on	

APPLICATION CIRCUIT

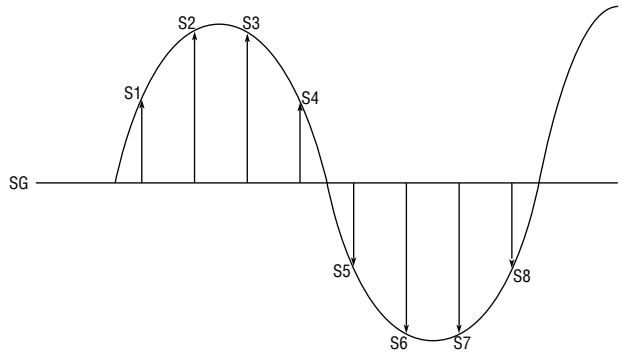


* The analog output swings at a maximum of ±1.0 V above and below the $V_{DD}/2$ offset level.

APPLICATION INFORMATION

Digital pattern for 0 dBm0

The digital pattern for 0 dBm0 is shown below.
(SYNC frequency = 8 kHz, signal frequency = 1 kHz)



Sample No.	MSD	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14
S1	0	0	1	0	0	0	1	0	1	0	1	0	1	1
S2	0	1	0	1	0	0	1	1	1	0	1	1	1	0
S3	0	1	0	1	0	0	1	1	1	0	1	1	1	0
S4	0	0	1	0	0	0	1	0	1	0	1	0	1	1
S5	1	1	0	1	1	1	0	1	0	1	0	1	0	0
S6	1	0	1	0	1	1	0	0	0	1	0	0	0	1
S7	1	0	1	0	1	1	0	0	0	1	0	0	0	1
S8	1	1	0	1	1	1	0	1	0	1	0	1	0	0

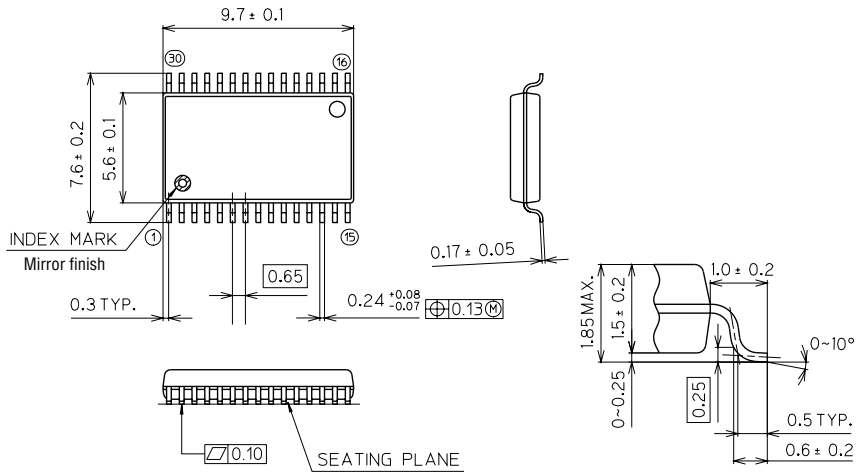
NOTES ON USE

- To ensure proper electrical characteristics, use bypass capacitors with excellent high frequency characteristics for the power supply and keep them as close as possible to the device pins.
- Connect the AG pin and the DG pin as close as possible. Connect them to the system ground with low impedance.
- Mount the device directly on the PC board. Do not use an IC socket. If use of an IC socket is unavoidable, use a short lead type socket.
- When mounting the device on a frame, use electro-magnetic shielding, if any electro-magnetic wave source such as power supply transformers is surrounding the device.
- Keep the voltage on the V_{DD} pin not lower than –0.3 V to avoid latch-up that may otherwise occur when power is turned on.
- Use a low noise (particularly, low level type of high frequency spike noise or pulse noise) power supply to avoid erroneous operation and the degradation of the characteristics of the device.

PACKAGE DIMENSIONS

(Unit : mm)

SSOP30-P-56-0.65-K



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	0.19 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).