

# MN39571PT

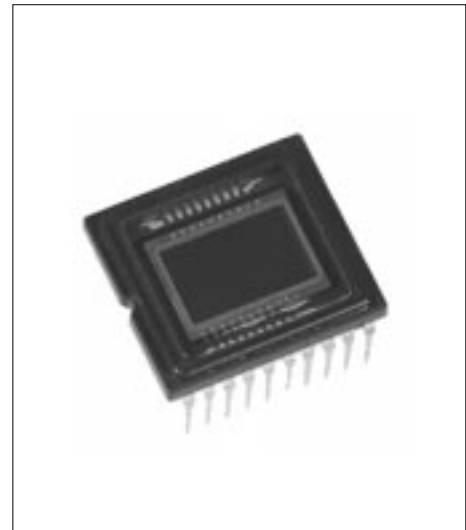
## 9.2mm (type-1/2) 2,310k pixel CCD Area Image Sensor

### ■ Overview

The MN39571PT is a super high resolution CCD area image sensor which includes 2,310k pixels in type-1/2 image format size.

Adopting RGB Bayer arrangement in primary color filter array on chip provides excellent color reproduction. As the aspect ratio of image area is 3:2 which is the same as that of 35mm film, pictures can be taken in similar framing manner to use of a usual film camera.

As The MN39571PT has also a skipping readout mode for image monitoring by LCD panel, you can fix the composition in real time.



Part Number	Size	System	Color or B/W
MN39571PT	9.2mm(type-1/2)	IS	Color

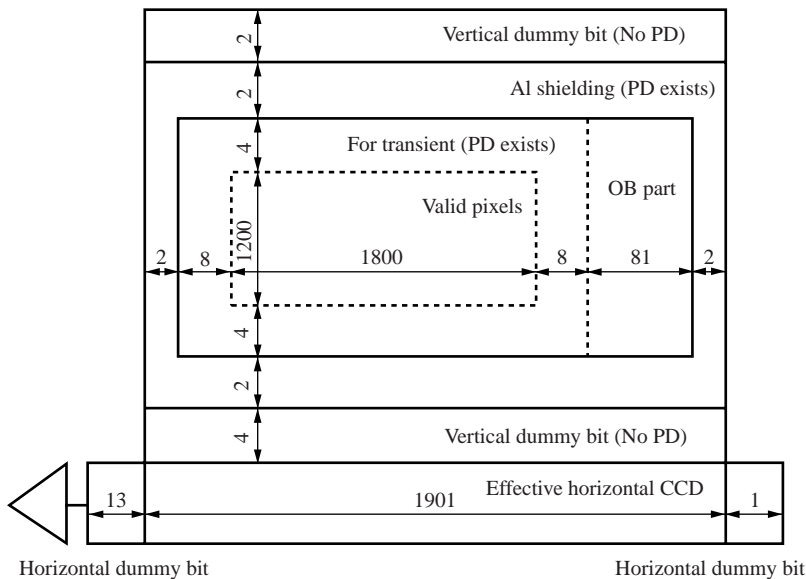
### ■ Features

- Photographic grade super high resolution by 2,310k pixels in type-1/2 format
- Responds to 5:1 skipping readout mode for LCD monitoring
- The same aspect ratio of 3:2 as a 35mm film
- Newly developed small plastic package  
Outline dimensions : 14.0mm(W) × 12.4mm(D) × 3.4mm(t)(Without lead pins)

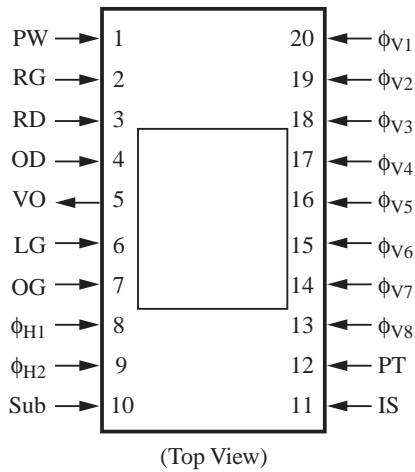
### ■ Applications

- Digital still camera
- FA, OA cameras

### ■ Device Configuration Diagram



■ Pin Assignments



■ Pin Descriptions

Pin No.	Symbol	Descriptions	Pin No.	Symbol	Descriptions
1	PW	P-well	14	$\phi_{V7}$	Vertical shift register clock pulse 7
2	RG	Reset gate			
3	RD	Reset drain	15	$\phi_{V6}$	Vertical shift register clock pulse 6
4	OD	Output drain			
5	VO	Video output	16	$\phi_{V5}$	Vertical shift register clock pulse 5
6	LG	Output load transistor gate			
7	OG	Output gate	17	$\phi_{V4}$	Vertical shift register clock pulse 4
8	$\phi_{H1}$	Horizontal register clock pulse (1)			
9	$\phi_{H2}$	Horizontal register clock pulse (2)	18	$\phi_{V3}$	Vertical shift register clock pulse 3
10	Sub	Substrate			
11	IS	Horizontal CCD input source	19	$\phi_{V2}$	Vertical shift register clock pulse 2
12	PT	P-well for protection circuit			
13	$\phi_{V8}$	Vertical shift register clock pulse 8	20	$\phi_{V1}$	Vertical shift register clock pulse 1

■ Absolute Maximum Ratings and Operating Conditions

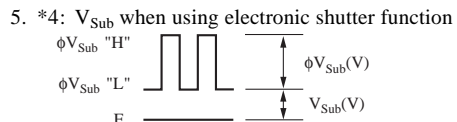
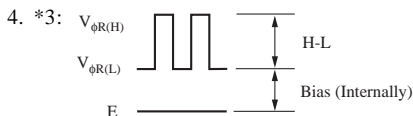
Parameter	Symbol	Rating		Operating condition			Unit	
		min	max	min	typ	max		
Output drain voltage	$V_{OD}$	-0.2	18.0	15.2	15.5	15.8	V	
Reset drain voltage	$V_{RD}$	-0.2	18.0	15.2	15.5	15.8	V	
Input source voltage	$V_{IS}$	-0.2	18.0	15.2	15.5	15.8	V	
Protection P-well voltage	$V_{PT}^{*2}$	-10.0	0.2	-9.3	-9.0	-8.7	V	
P-well voltage	$V_{PW}$	Reference voltage		—	0	—	V	
Output load transistor gate voltage	$V_{LG}$	—	—	Supplied internally			V	
Output gate voltage	$V_{OG}$	—	—	Supplied internally			V	
Reset pulse voltage	H-L	$V_{\phi RG(H-L)}^{*3}$	—	8.0	3.0	3.3	3.6	V
	Bias	$V_{\phi RG(Bias)}^{*3}$	-0.5	—	Supplied internally			V
Horizontal register clock pulse voltage 1	$V_{\phi H1(H)}$	—	8.0	3.0	3.3	3.6	V	
	$V_{\phi H1(L)}$	-0.2	—	-0.2	0	0.2		
Horizontal register clock pulse voltage 2	$V_{\phi H2(H)}$	—	8.0	3.0	3.3	3.6	V	
	$V_{\phi H2(L)}$	-0.2	—	-0.2	0	0.2		
Vertical shift register clock pulse voltage 1,5	$V_{\phi V1,5(H)}^{*2}$	—	18.0	15.2	15.5	15.8	V	
	$V_{\phi V1,5(M)}^{*2}$	—	—	-0.2	0	0.2		
	$V_{\phi V1,5(L)}^{*2}$	-10.0	—	-9.3	-9.0	-8.7		
Vertical shift register clock pulse voltage 3,7	$V_{\phi V3,7(H)}^{*2}$	—	18.0	15.2	15.5	15.8	V	
	$V_{\phi V3,7(M)}^{*2}$	—	—	-0.2	0	0.2		
	$V_{\phi V3,7(L)}^{*2}$	-10.0	—	-9.3	-9.0	-8.7		
Vertical shift register clock pulse voltage 2,6	$V_{\phi V2,6(M)}^{*2}$	—	15.0	-0.2	0	0.2	V	
	$V_{\phi V2,6(L)}^{*2}$	-10.0	—	-9.3	-9.0	-8.7		
Vertical shift register clock pulse voltage 4,8	$V_{\phi V4,8(M)}^{*2}$	—	15.0	-0.2	0	0.2	V	
	$V_{\phi V4,8(L)}^{*2}$	-10.0	—	-9.3	-9.0	-8.7		
Substrate voltage	$V_{Sub}^{*2}$	Supplied internally					V	
	$\phi V_{Sub}^{*4,*5}$	-0.2	45.0	26.5	27.0	27.5		
Operating temperature	$T_{opr}$	-10	60	—	25	—	°C	
Storage temperature	$T_{stg}$	-30	70	—	—	—	°C	

Note)1. Standard light input defines

Standard light input is the one when the exposure is done at a lens aperture of F8, using a light source of 2856 K and 1050 nt, and placing a color temperature conversion filter LB-40 (HOYA) and an IR cutting filter CAW-500 (t = 2.5 mm) in the light path.

- 2. \*1:  $V_{Sub}$  internal settings guarantee blooming at 400 times light input of the standard light input.
- 3. \*2:  $V_{PT}$  is set so that the following conditions are set for VL of the vertical shift clock.

$$V_{PT} \leq VL$$



- 6. \*5: Separate power supply is recommended for  $\phi V_{Sub}$

■ Optical Characteristics

Part Number	Color or B/W	Effective pixels		S/N typ (dB)	Saturation output typ (mV)	Sensitivity F8 typ (mV)	Vertical smear Sm typ(%)	Image lag typ (%)	Horizontal resolution typ (TV-lines)	Vertical resolution typ (TV-lines)
		H	V							
MN39571PT	Color	1816	1208	—	500	340	0.01	—	—	—

Note)1. 1/7.5 sec frame storage. Horizontal register clock frequency 24 MHz

2. \*1: Mechanical shutter saturation output

■ Package Dimensions (Unit : mm)

- WDIP020-P-0500A

