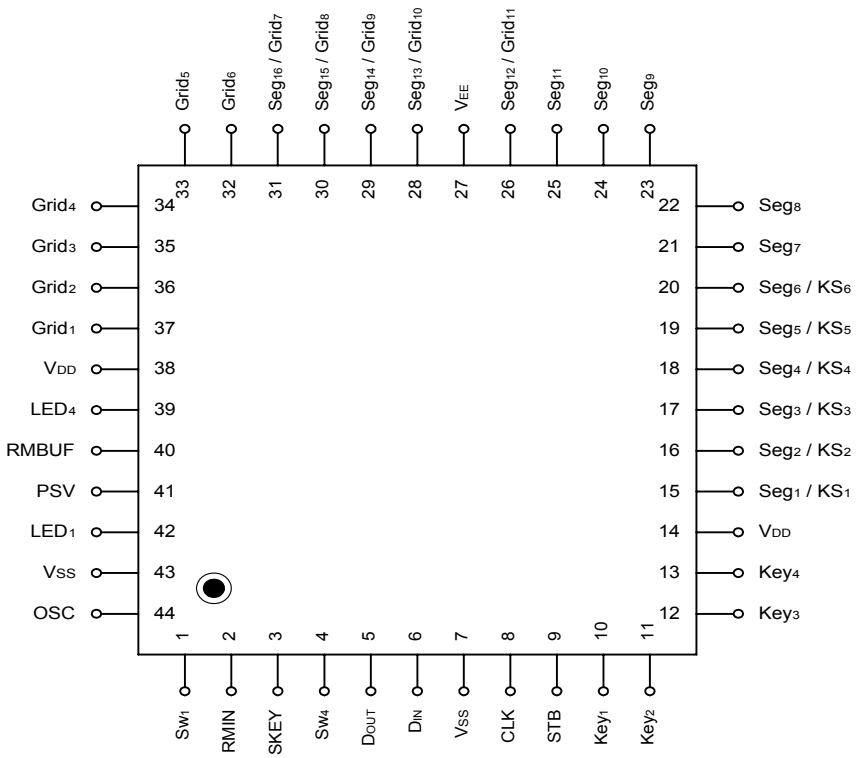
■ Features

- Serial interface (CLK, STB, D_{IN}, D_{OUT})
- Key scanning (6× 4 matrices)
- Programming display modes (11-digit & 11-segment to 6-digit & 16-segment)
- Programming dimming step
- High-voltage output (V_{DD}-35V max).
- 2 channels LED ports.
- 2-pin General-purpose input port
- Built-in oscillator
- No external resistor necessary for driver outputs (provides PMOS open-drain and pull-low resistor output)
- Remote signal input port
- Remote signal output port
- 3 STANDBY master output ports (controlled by remote STANDBY-KEY, STANDBY-KEY and STANDBY SCAN-KEY)
- 8 WAKE UP master output ports (controlled by 2 remote WAKE_UP-KEY, 3 WAKE_UP SCAN-KEY, remote STANDBY-KEY, STANDBY-KEY and STANDBY SCAN-KEY)
- NEC 6121/6122 infrared protocol support

■ General Description

The AD7312 is a VFD (Vacuum Fluorescent Display) controller/driver with STANDBY controller. It is driven on a 1/4 to 1/11 duty factor (include key scan). It consists of 5 segment output lines, 6 segment/key scan output lines, 6 grid output lines, 5 segment/grid output drive lines, 2 LED output ports, a display memory, a control circuit, and a key scan circuit. In addition, it includes 2 input ports, RMIN and SKEY, RMIN receives the signal form the STANDBY-KEY of remote sensor, SKEY can be controlled by an external switch. Both of them and STANBY SCAN-KEY can control the output level (High) of PSV port to realize the STANDBY function. To leave the standby mode, we can use the 2 remote WAKE_UP-KEY, 3 WAKE_UP SCAN-KEY, remote STANDBY-KEY, STANDBY-KEY and STANDBY SCAN-KEY to control the output level (Low) of PSV port to realize the Wake Up function. Serial data is input to the AD7312 through a four-line serial interface.

■ Pin Assignments

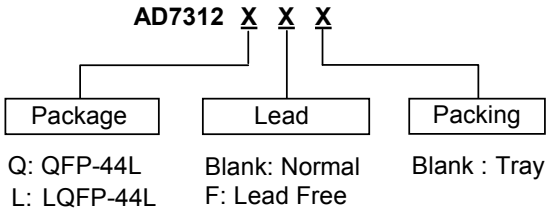


Use all power pins.

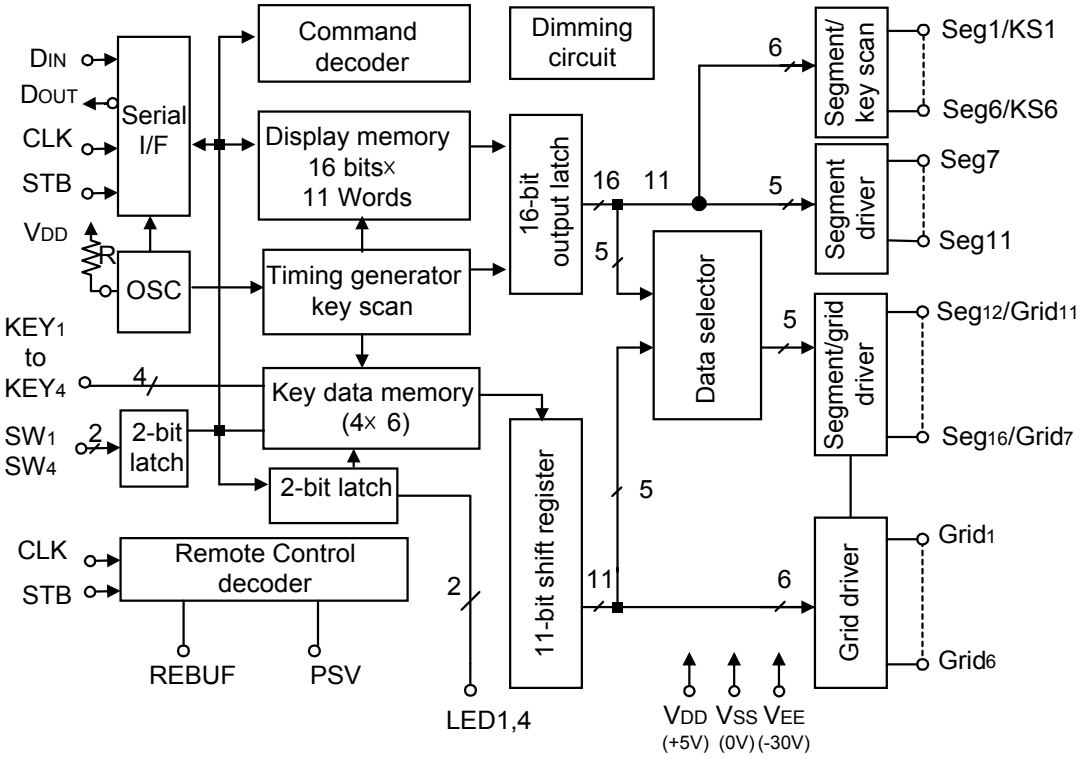
■ Pin Descriptions

Symbol	Name	No.	Description
D_{IN}	Data input	6	Input serial data at rising edge of shift clock, starting from the low order bit.
D_{OUT}	Data output	5	Output serial data at the falling edge of the shift clock, starting from low order bit. This is N-ch open-drain output pin.
STB	Strobe	9	Initializes serial interface at the rising or falling edge of the AD7312. It then waits for reception of a command. Data input after STB falling is processed as a command. While command data is processed, current processing is stopped, and the serial interface is initialized. While STB is high, CLK is ignored.
CLK	Clock input	8	Reads serial data at the rising edge, and outputs data at the falling edge.
OSC	Oscillator pin	44	Connect resistor in between this pin and Vdd to set up the oscillation frequency.
Seg_7 to Seg_{11}	High-voltage output (Segment)	21 to 25	Segment output pins
Seg_1/KS_1 to Seg_6/KS_6	High-voltage output	15 to 20	Multi-function pins, Segment output pins (Dual function as key scan source)
$Grid_1$ to $Grid_6$	High-voltage output (Grid)	32 to 37	Grid output pins
$Seg_{12}/Grid_{11}$ to $Seg_{16}/Grid_7$	High-voltage output (Segment/grid)	26, 28 to 31	These pins are selectable for segment or grid driving.
LED_1 and LED_4	LED output	39 and 42	CMOS output
RMBUF	Remote Control Buffer	40	CMOS output
PSV	Power Saving Output	41	CMOS output
KEY_1 to KEY_4	Key data input	10 to 13	Data input to these pins is latched at the end of the display cycle.
V_{DD}	Logic power	14, 38	Logic power supply
V_{SS}	Logic ground	7, 43	Connect this pin to system GND.
V_{EE}	Pull-down level	27	Driver power supply
SW_1 and SW_4	Switch input	1 and 4	These pins constitute a 2-bit general-purpose input port.
RMIN	Remote Control Input	2	Input pin
SKEY	Standby Key Input	3	Input pin

■ Ordering Information



■ Block Diagram



■ Absolute Maximum Ratings (T_A=25°C,V_{SS}=0V)

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{DD}	-0.5 to +7.0	V
Driver Supply Voltage	V_{EE}	V_{DD} +0.5 to V_{DD} -40	V
Logic Input Voltage	V_{I1}	-0.5 to V_{DD} +0.5	V
VFD Driver Output Voltage	V_{O2}	V_{EE}-0.5 to V_{DD} +0.5	V
LED Driver Output Current	I_{O1}	+15	mA
VFD Driver Output Current	I_{O2}	-40 (grid) -15 (segment)	mA
Operating Ambient Temperature	T_{OPT}	-25 to +85	°C
Storage Temperature	T_{STG}	-50 to +125	°C

■ Operating Conditions (T_A=0 to +70 °C,V_{SS}=0V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}		4.5	5	5.5	V
High-Level Input Voltage	V_{IH}		0.7·V_{DD}		V_{DD}	V
Low-Level Input Voltage	V_{IL}		0		0.3·V_{DD}	V
Driver Supply Voltage	V_{EE}		0		V_{DD}-35	V

■ DC Characteristics (T_A=0 to 70 °C, V_{DD}=4.5 to 5.5V, V_{SS}=0V, V_{EE}=V_{DD}-35V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
High-Level Output Voltage	V_{OH1}	LED_1/LED_4, I_{OH1}=-1mA	0.9V_{DD}			V
Low-Level Output Voltage	V_{OL1}	LED_1/LED_4, I_{OL1}=12mA			1	V
Low-Level Output Voltage	V_{OL2}	D_{OUT}, I_{OL2}=2mA			0.4	V
High-Level Output Current	I_{OH21}	V_O=V_{DD}-2V, Seg_1 to Seg_{11}	-3			mA
High-Level Output Current	I_{OH22}	V_O=V_{DD}-2V, $Grid_1$ to $Grid_6$ Seg_{12}/$Grid_{11}$ to Seg_{16}/$Grid_7$	-15			mA
Driver Leakage Current	I_{OLEAK}	V_O=V_{DD}-35V, driver off			-10	μA
Output Pull-Down Resistor	R_L	Driver output	50	100	150	kΩ
High-Level Input Voltage	V_{IH}		0.7V_{DD}			V
Low-Level Input Voltage	V_{IL}				0.3V_{DD}	V

■ AC Characteristics (T_a=0 to +70 °C,V_{DD}=4.5 to 5.5 V, V_{EE}=-30V)

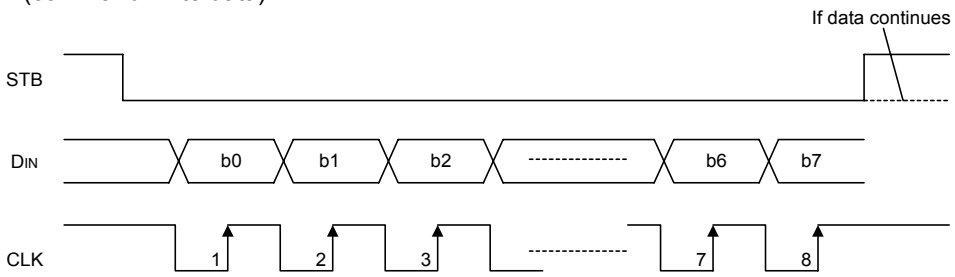
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Oscillation Frequency	f_{OSC}	R=51 kΩ		350	500	650	KH_Z
Maximum Clock Frequency	$f_{max.}$	Duty=50%				1	MH_Z
Clock Pulse Width	PW_{CLK}			500			ns
Strobe Pulse Width	PW_{STB}			1			μs
Data Setup Time	t_{SETUP}			100			ns
Data Hold Time	t_{HOLD}			100			ns
Clock-Strobe Time	$t_{CLK-STB}$	CLK ↑ →STB ↑		1			μs
Wait Time	t_{WAIT}	CLK ↑ →CLK ↓ (Note)		1			μs
Propagation delay time	t_{PHZ}	CLK→D_{OUT}				300	ns
	t_{PZL}	C_L=15pF,R_L=10 kΩ				100	ns
Rise time	t_{TZH}	C_L=300pF	Seg_n,$Grid_n$			2	μs
Fall time	t_{THZ}					160	μs

Note : Refer to page 8.

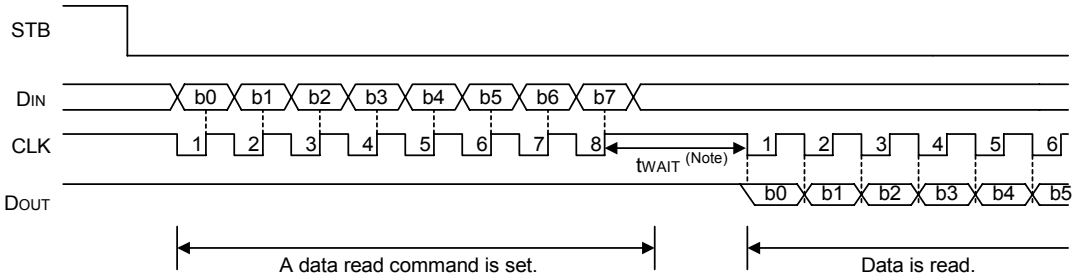
■ Timing Diagram

(1)Serial Communication Format

Reception (command/write data)



Transmission (read data)

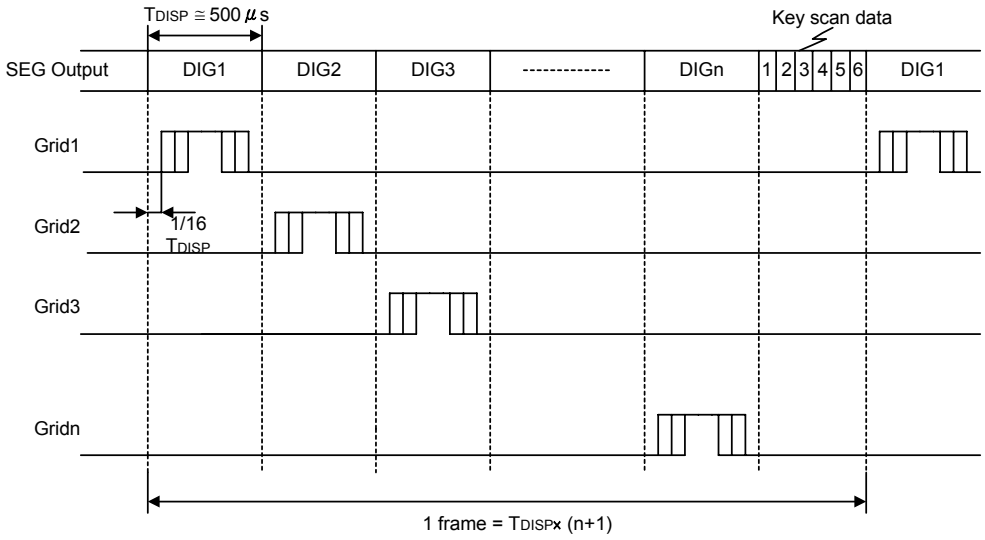


Because the D_{OUT} pin is an N-ch, open-drain output pin, be sure to connect an external pull-up resistor to this pin (1kΩ to 10 kΩ).

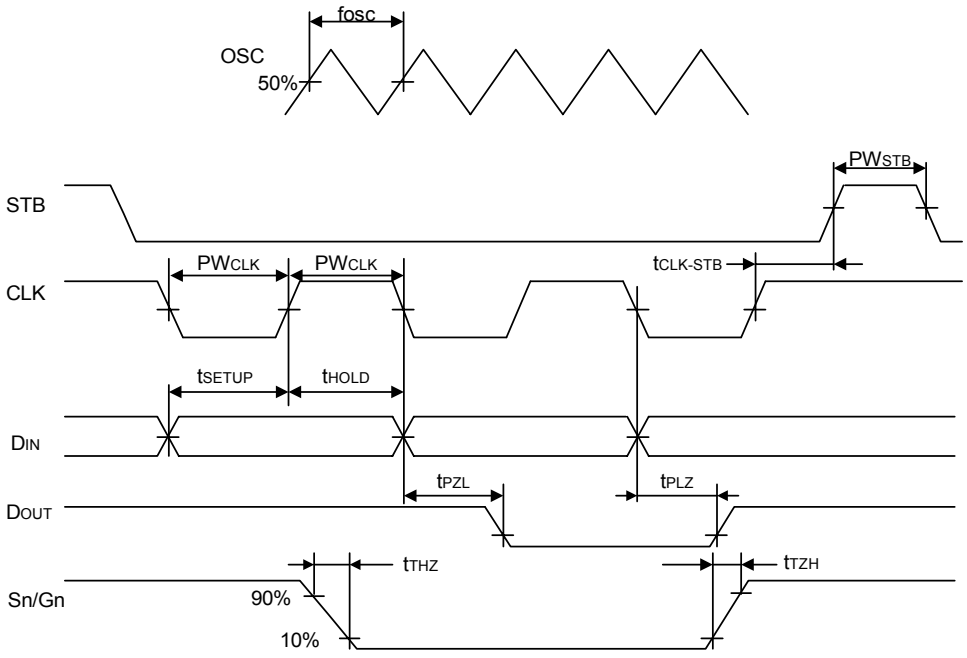
Note : When data is read, a wait time t_{WAIT} of 1 μs is necessary since the rising of the eighth clock that has set the command, until the falling of the first clock that has read the data.

(2) Key Scanning and Display Timing

On cycle of key scanning consists of one frame, and data in a 6× 4 matrix is stored in RAM.

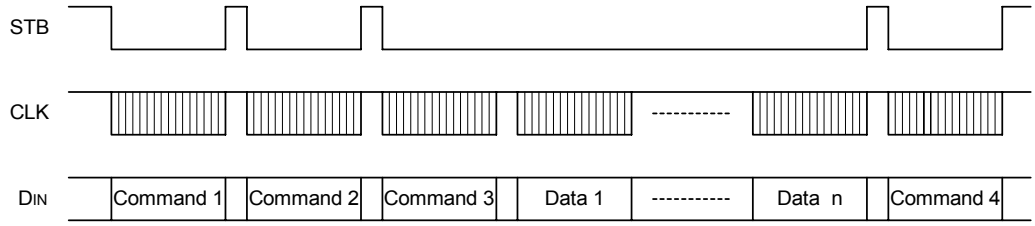


Switching characteristic waveforms



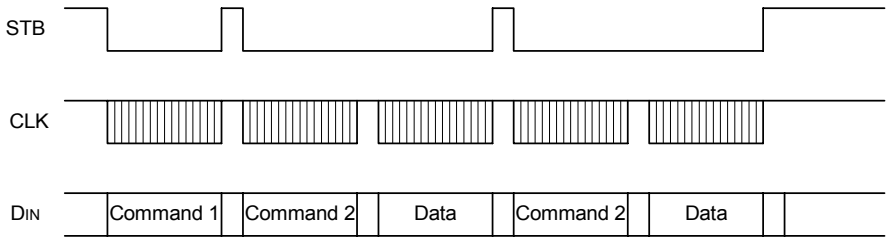
Applications

Updating display memory by incrementing address



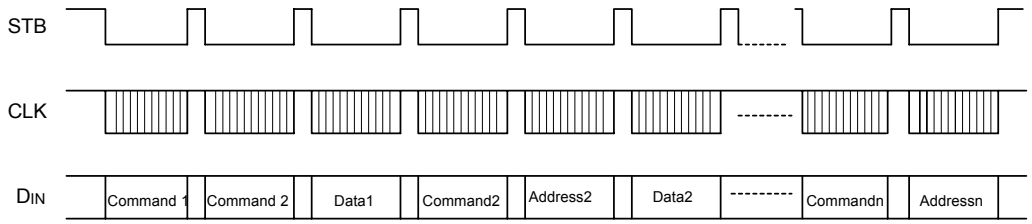
Command 1: sets display mode
Command 2: sets data(write data to display memory)
Command 3: sets address
Data 1 to n: transfers display data (22bytes max.)
Command 4: controls display

Updating specific display memory and write registers



Command 1: sets data
Command 2: sets address
Data: display data

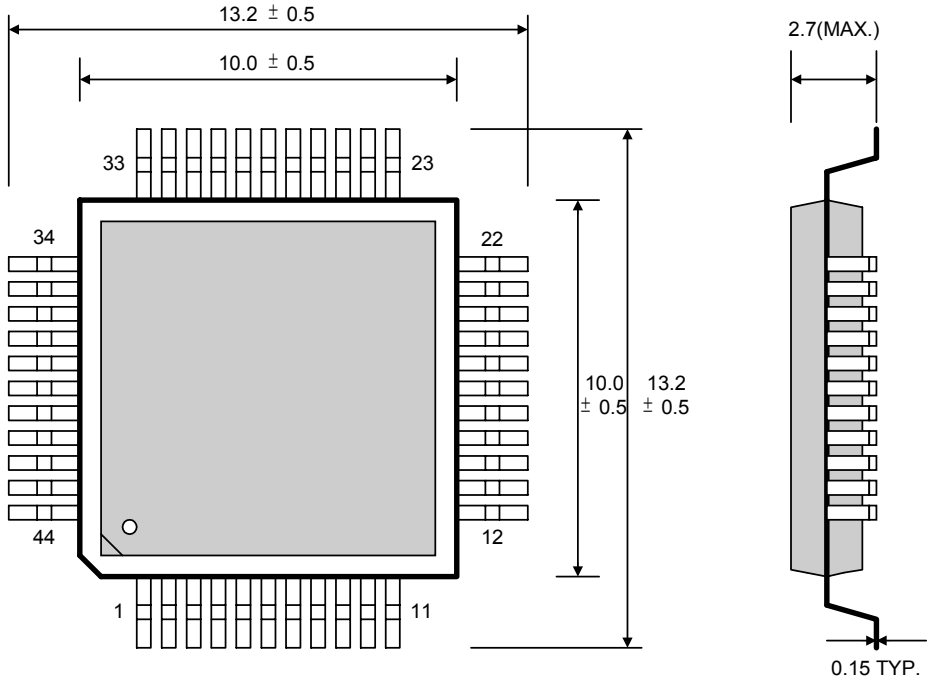
Reading specific registers

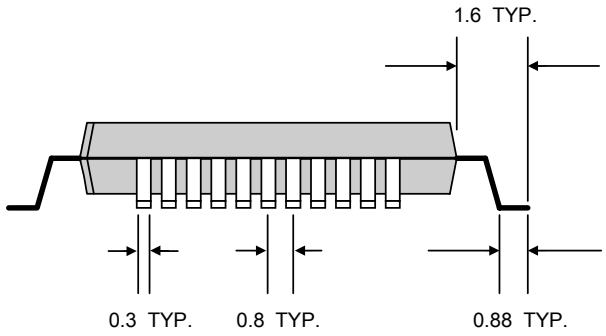


■ Package Information

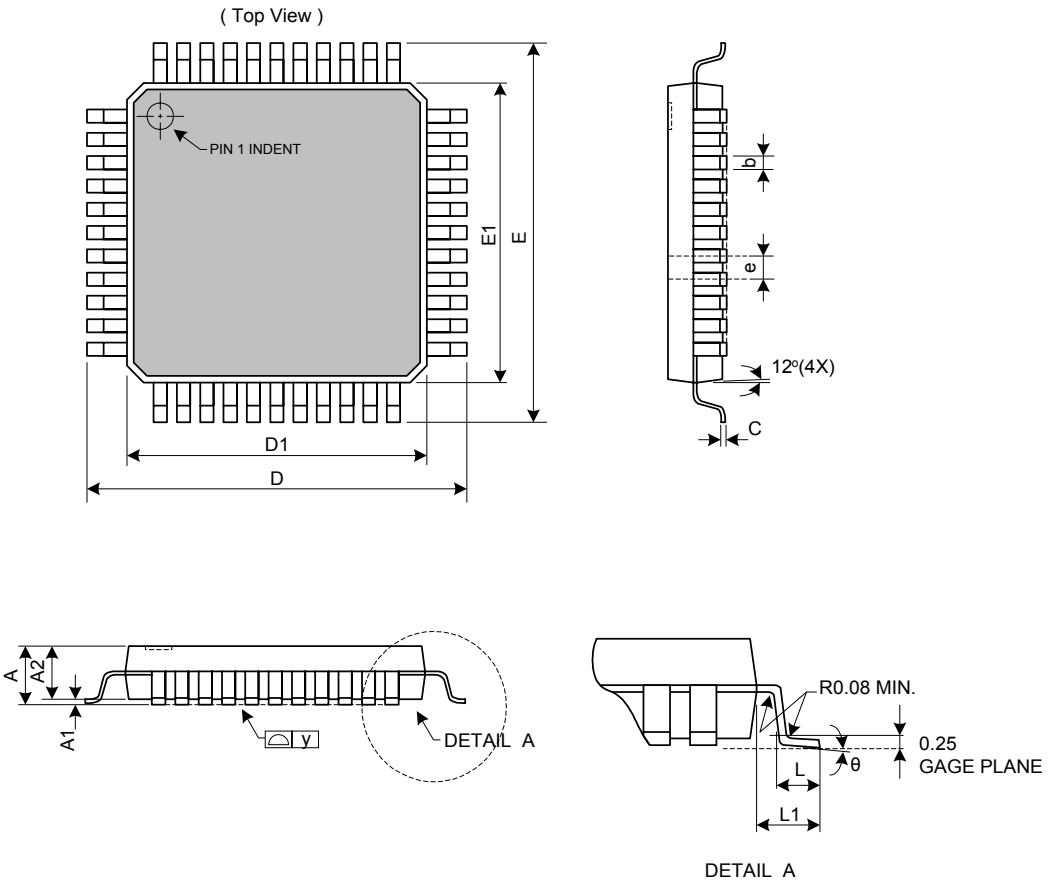
(1) Package Type: QFP-44L

Dimension in millimeter (mm.)



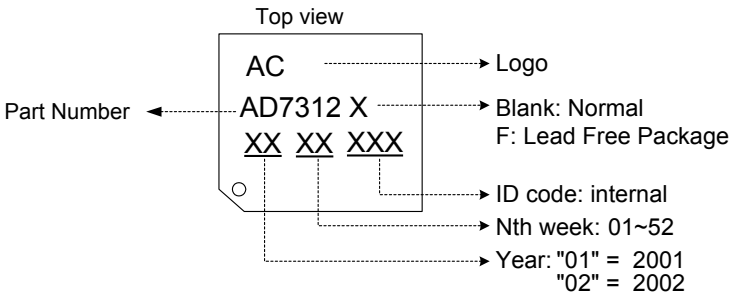


(2) Package Type: LQFP-44L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	1.60	-	-	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09	-	0.20	0.004	-	0.008
E	11.50	12.00	12.50	0.453	0.472	0.492
E1	9.50	10.00	10.50	0.374	0.394	0.413
D	11.80	12.00	12.20	0.465	0.472	0.480
D1	9.90	10.00	10.10	0.390	0.394	0.398
e	-	0.80	-	-	0.031	-
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	-	1.00	-	-	0.039	-
θ	0˚	3.5˚	7˚	0˚	3.5˚	7˚
y	0.00	-	0.08	0.000	-	0.003

■ Marking Information



QFP44/LQFP44