TCD6000

6 CHANNEL CLASS-T DIGITAL AUDIO PROCESSOR USING DIGITAL POWER PROCESSING™ TECHNOLOGY

Technical Information – Preliminary **Revision 1.0 – September 2004**

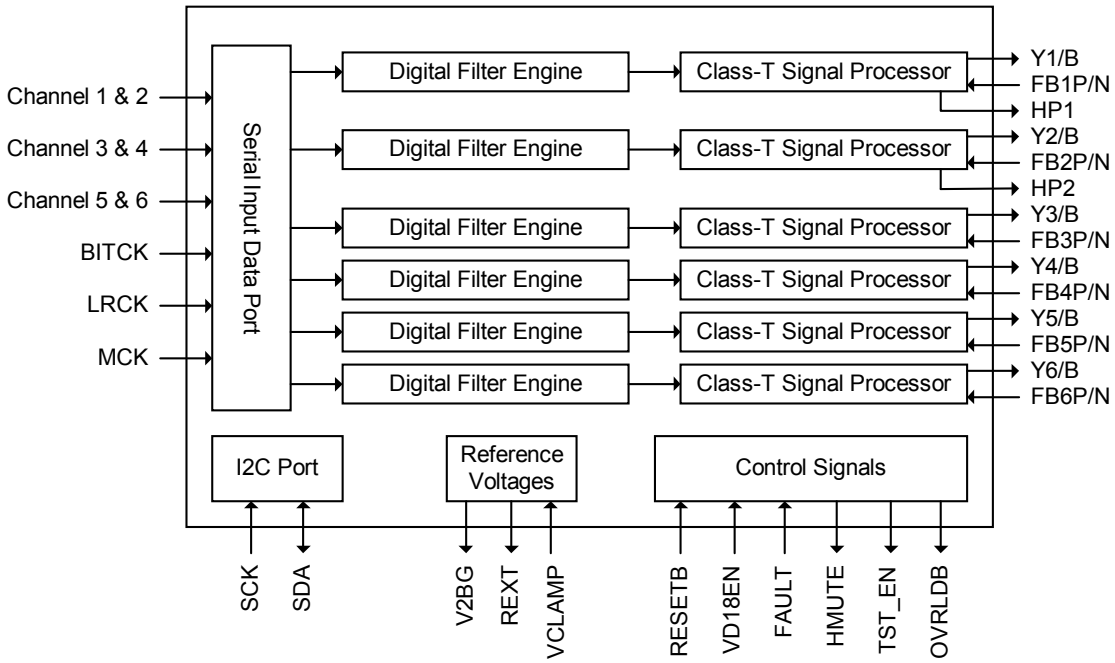
General Description

The TCD6000 is a high-performance 6-channel digital audio amplifier processor. It receives 6 digital audio channels (3 pairs) and outputs 6 complementary single-bit digital data streams suitable for driving Tripath or other switching output stages.

The TCD6000 accepts data at audio sample rates ranging from 32kHz to 192kHz and incorporates digital interpolation and sigma-delta conversion to produce streamed digital output signals. When combined with switching output stages, the TCD6000 allows the implementation of a complete digital audio system incorporating Class-T Digital Audio Amplification.

Features

- Class-T architecture combining ultra-low distortion with high efficiency
- Inputs support I^2S and other PCM audio formats
- Up to 24-bit resolution (16, 18, 20, and 24 bit)
- 104dB dynamic range
- THD+N less than 0.03%
- Input sampling rates up to 192kHz
- I^2C compatible interface
- Stereo headphone amplifier
- Predictive Gain Control
- Digital volume control
  - 128dB range
  - 1/2 dB step size in 1/8 dB increments
  - Zero crossing detection for click free transitions
  - Optional mute mode leaves headphone amplifiers operating
- Automatic DC offset cancellation
- 130uV noise floor (PGC = 1/8, low post gain)
- Digital de-emphasis filtering for 32, 44.1 and 48kHz sampling rates



Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	Max	UNITS
VD33	3.3V Digital Power Supply	-0.3	4.0	V
VA33	3.3V Analog Power Supply	-0.3	4.0	V
VA50	5V Analog Power Supply	-0.3	6.0	V
Vlogic3	Input Logic Level (DATAx, MCK, BITCLK, LRCLK, SCK, SDA, RESET, ADDRx)	-0.3	VD33+0.3	V
Vin5	Input Level (VCLAMP, FBxx, FAULT)	-0.3	VD50+0.3	
TA	Operating Free-air Temperature Range	-40	85	°C
T_{STORE}	Storage Temperature Range	-55	150	°C
T_{JMAX}	Maximum Junction Temperature		150	°C
ESD_{HB}	ESD Susceptibility – Human Body Model (Note 2) All pins		2000	V
ESD_{MM}	ESD Susceptibility – Machine Model (Note 3) All pins		200	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. See the table below for Operating Conditions.
Note 2: Human body model, 100pF discharged through a 1.5KΩ resistor.
Note 3: Machine model, 220pF – 240pF discharged through all pins.

Recommended Operating Conditions (Note 4)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VA50	5V Analog Power Supply	4.5	5	5.5	V
VA33	3.3V Analog Power Supply	3.0	3.3	3.6	V
VD33	3.3V Digital Power Supply	3.0	3.3	3.6	V
V_{HI-3}	Vlogic3 Input High	2.1		VD33	V
V_{LO-3}	Vlogic3 Input Low	0		0.8	V
T_A	Operating Temperature Range	-40	25	85	C

Note 4: Recommended Operating Conditions indicate conditions for which the device is functional. See Digital, Analog, and Switching Characteristics for guaranteed specific performance limits.

Power and Thermal Characteristics

T_A = 25 °C. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PTOTAL	Total Power Dissipation	VA50 = 5.0V VA33 = 3.3V VD33 = 3.3V		880		mW
IA50	VA50 Power Supply Current	VA50 = 5.0V		65	90	mA
IA33	VA33 Power Supply Current	VA33 = 3.3V		50		mA
ID33	VD33 Power Supply Current	VD33 = 3.3V		20		mA
I33	Combined VD33+VA33 Power Supply Current (Note 5)	VD33 = 3.3V VA33 = 3.3V			100	mA
θ_{JA}	Junction-to-ambient Thermal Resistance (still air)			35°		C/W

Note 5: Separate IA33 and ID33 maximums are not tested.

Digital Characteristics

T_A = 25 °C. Unless otherwise noted, the MCK frequency is 12.288. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH33}	High-Level Input Voltage	VD33 = 3.3V	2.1			V
V_{IL33}	Low-Level Input Voltage	VD33 = 3.3V			0.8	V
$FAULT_{IH5}$	FAULT High-Level Input Voltage	VA50 = 5.0V	3.5			V
$FAULT_{IL5}$	FAULT Low-Level Input Voltage	VA50 = 5.0V			0.8	V
$FAULT_{OFF}$	FAULT Off Input Voltage	VA50 = 5.0V	2		3	V
V_{OH33}	High-Level Output Voltage	VD33 = 3.0V, I_{OL} = -50uA	2.9			V
		VD33 = 3.0V, I_{OL} = -4mA	2.48			V
V_{OH5}	High-Level Output Voltage	VA50 = 4.5V, I_{OL} = -50uA	4.4			V
		VA50 = 4.5V, I_{OL} = -8mA	3.8			V
V_{OL33}	Low-Level Output Voltage	VD33 = 3.0V, I_{OL} = 50uA			0.1	V
		VD33 = 3.0V, I_{OL} = 4mA			0.44	V
V_{OL5}	Low-Level Output Voltage	VA50 = 4.5V, I_{OL} = 50uA			0.1	V
		VA50 = 4.5V, I_{OL} = 8mA			0.44	V

Performance Characteristics

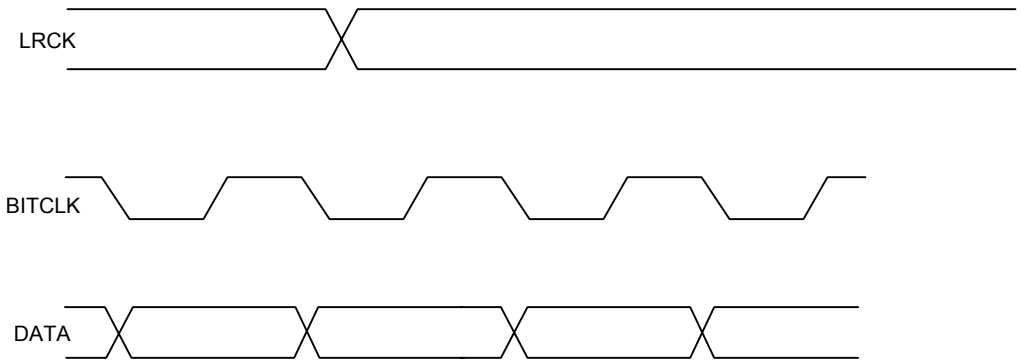
T_A = 25 °C. Unless otherwise noted, the power stage used for testing is the TP2150B, the supply voltage is VPP=|VNN|=28V, R_L = 4Ω, PGC = 1, post-gain = high, the MCK frequency is 12.288 MHz, fs = 48kHz, the input frequency is 1kHz, and the measurement bandwidth is 20kHz. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
P_{OUT}	Output Power (continuous RMS/Channel)	THD+N = 0.1% THD+N = 1.0% THD+N = 10%		60 75 105		W W W
THD + N	Total Harmonic Distortion Plus Noise	P_{OUT} = 20W/Channel		0.03		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), P_{OUT} = 10W/Channel		-80		dB
SNR	Signal-to-Noise Ratio	PGC = 1, post-gain = high, A Weighted, P_{OUT} = 100W/Channel		98		dB
CS	Channel Separation	0dBr = 10W		84		dB
η	Power Efficiency	Pout = 100W/Channel		87		%
A_{VERROR}	Channel to Channel Gain Error	P_{OUT} = 10W/Channel			0.2	dB
e_{NOUT}	Output Noise Voltage (A-Weighted)	PGC = 1, post-gain = high PGC = 1/8, post-gain = high PGC = 1/8, post-gain = low		260 150 130		μV μV μV
V_{OFFSET}	Output Offset Voltage	After automatic DC calibration	-95	±40	+95	mV

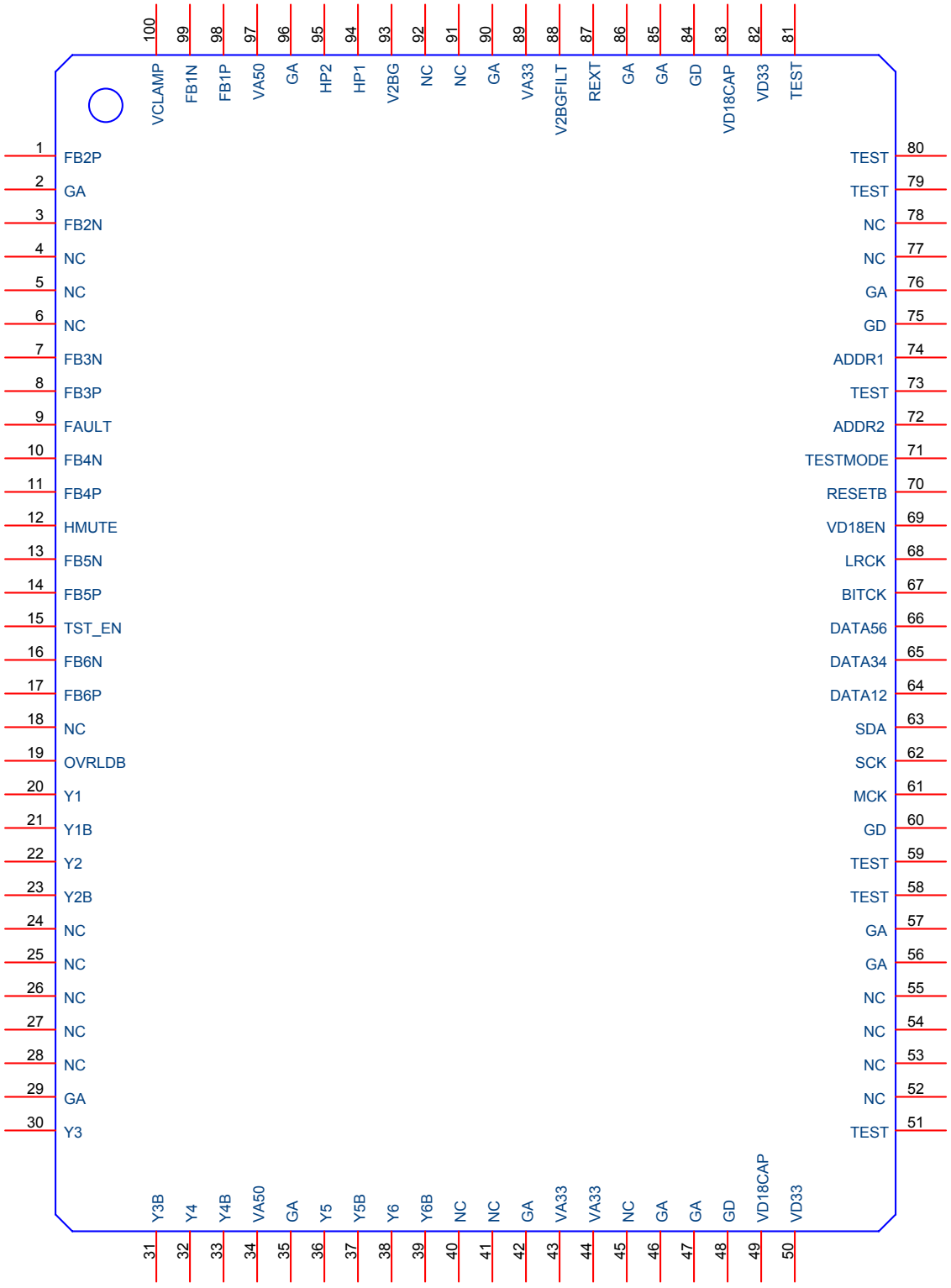
Switching Characteristics

T_A = 25 °C. Unless otherwise noted, the MCK frequency is 12.288 MHz and the measurement bandwidth is 20kHz. See Application/Test Circuit on page 8.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Master Clock Timing					
fMCK	Frequency		8.192		24.56	MHz
	Duty Cycle		40		60	%
	Left-Right Clock Timing					
fLRCK	1X Mode		32	44.1	48	KHz
	2X Mode			96		KHz
	4X Mode			192		kHz
	Serial Interface Timing					
tBITCK	BITCK period					
	1X Mode		488.2	354.3	325.5	ns
	2X Mode			177.1		ns
	4X Mode			88.6		ns
	Control Interface Timing					
tSCK	SCK Period		200			ns
tSCKL	SCK Pulse Width Low		80			ns
tSCKH	SCK Pulse Width High		80			ns
tSDAset	SDA Setup Time		40			ns
tSDAhold	SDA Hold Time		40			ns
tSDA rise	SDA Rise Time				20	ns
tSDAfall	SDA Fall Time				20	ns



TCD6000 Pin Layout

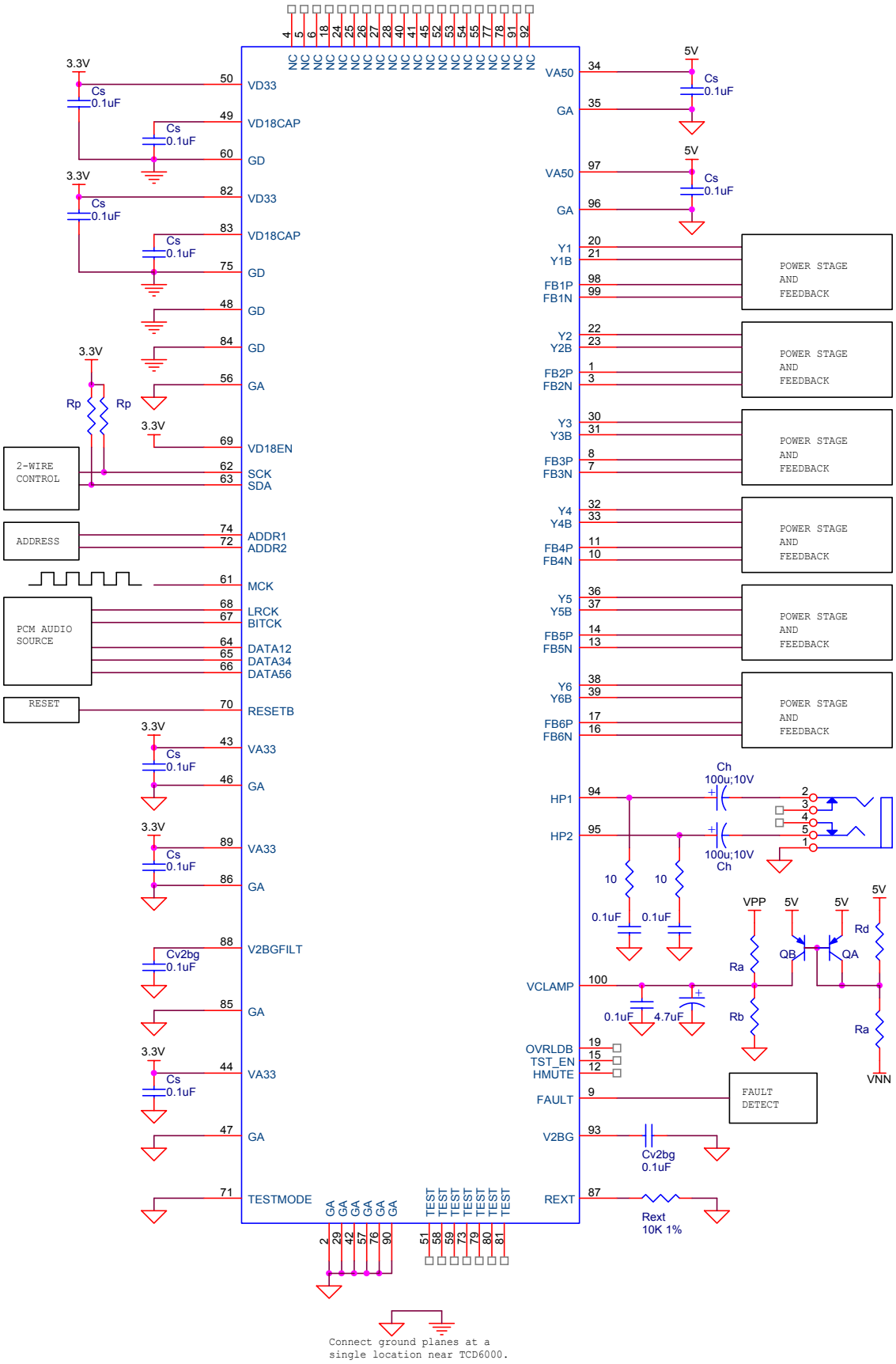


TCD6000 Pin Description

Pin	Function	Type	Description
1	FB2P	Input	Switching feedback
2	GA	Ground	Analog Ground
3	FB2N	Input	Switching feedback
4	NC	Not connected internally	must be kept floating
5	NC	Not connected internally	must be kept floating
6	NC	Not connected internally	must be kept floating
7	FB3N	Input	Switching feedback
8	FB3P	Input	Switching feedback
9	FAULT	Input	3-level digital input to detect power stage fault condition
10	FB4N	Input	Switching feedback
11	FB4P	Input	Switching feedback
12	HMUTE	5V Logic Output	Digital output – indicates processor channels are muted
13	FB5N	Input	Switching feedback
14	FB5P	Input	Switching feedback
15	TST_EN	5V Logic Output	Digital output to put power stage in to test mode
16	FB6N	Input	Switching feedback
17	FB6P	Input	Switching feedback
18	NC	Not connected internally	must be kept floating
19	OVRLDB	5V Logic Output	Digital output – indicates that one or more channels are near saturation
20	Y1	5V Logic Output	Switching modulator output
21	Y1B	5V Logic Output	Switching modulator output
22	Y2	5V Logic Output	Switching modulator output
23	Y2B	5V Logic Output	Switching modulator output
24	NC	Not connected internally	must be kept floating
25	NC	Not connected internally	must be kept floating
26	NC	Not connected internally	must be kept floating
27	NC	Not connected internally	must be kept floating
28	NC	Not connected internally	must be kept floating
29	GA	Ground	Analog Ground
30	Y3	5V Logic Output	Switching modulator output
31	Y3B	5V Logic Output	Switching modulator output
32	Y4	5V Logic Output	Switching modulator output
33	Y4B	5V Logic Output	Switching modulator output
34	VA50	Power	5V analog power supply
35	GA	Ground	Analog ground
36	Y5	5V Logic Output	Switching modulator output
37	Y5B	5V Logic Output	Switching modulator output
38	Y6	5V Logic Output	Switching modulator output
39	Y6B	5V Logic Output	Switching modulator output
40	NC	Not connected internally	must be kept floating
41	NC	Not connected internally	must be kept floating
42	GA	Ground	Analog ground
43	VA33	Power	3.3V analog power supply
44	VA33	Power	3.3V analog power supply
45	NC	Not connected internally	must be kept floating
46	GA	Ground	Analog ground
47	GA	Ground	Analog ground
48	GD	Ground	Digital Ground
49	VD18CAP	Output	Decoupling point for internal 1.8V regulator
50	VD33	Power	3.3V digital power supply
51	TEST	Float	Test pin – must be kept floating
52	NC	Not connected internally	must be kept floating
53	NC	Not connected internally	must be kept floating
54	NC	Not connected internally	must be kept floating
55	NC	Not connected internally	must be kept floating
56	GA	Power	Analog ground
57	GA	Power	Analog ground
58	TEST	Float	Test pin – must be kept floating
59	TEST	Float	Test pin – must be kept floating
60	GD	Ground	Digital ground
61	MCK	3.3V Logic Input	Master clock digital input
62	SCK	3.3V Logic Input	I^2C clock input
63	SDA	3.3V Logic Input	I^2C serial data input

64	DATA12	3.3V Logic Input	PCM audio input for channels 1 and 2
65	DATA34	3.3V Logic Input	PCM audio input for channels 3 and 4
66	DATA56	3.3V Logic Input	PCM audio input for channels 5 and 6
67	BITCK	3.3V Logic Input	PCM audio bit clock input
68	LRCK	3.3V Logic Input	PCM audio left/right clock input
69	VD18EN	3.3V Logic Input	1.8V internal regulator enable
70	RESETB	3.3V Logic Input	Reset input – resets internal registers
71	TESTMODE	3.3V Logic Input	Test mode enable – must be kept grounded
72	ADDR2	3.3V Logic Input	Chip address select 2
73	TEST	Float	Test pin – must be kept floating
74	ADDR1	3.3V Logic Input	Chip address select 1
75	GD	Ground	Digital ground
76	GA	Ground	Analog ground
77	NC	Not connected internally	must be kept floating
78	NC	Not connected internally	must be kept floating
79	TEST	Float	Test pin – must be kept floating
80	TEST	Float	Test pin – must be kept floating
81	TEST	Float	Test pin – must be kept floating
82	VD33	Power	3.3V digital power supply
83	VD18CAP	Output	Decoupling point for internal 1.8V regulator
84	GD	Ground	Digital ground
85	GA	Ground	Analog ground
86	GA	Ground	Analog ground
87	REXT	Output	Analog current reference input – requires 10K ohms +/- 1% to GA
88	V2BGFILT	Output	Reference Voltage
89	VA33	Power	3.3V analog power supply
90	GA	Ground	Analog ground
91	NC	Not connected internally	must be kept floating
92	NC	Not connected internally	must be kept floating
93	V2BG	Output	Reference Voltage
94	HP1	Output	Headphone amplifier output channel 1
95	HP2	Output	Headphone amplifier output channel 2
96	GA	Ground	Analog ground
97	VA50	Power	5V analog power supply
98	FB1P	5V Logic Output	Switching feedback
99	FB1N	5V Logic Output	Switching feedback
100	VCLAMP	Input	Soft clamp threshold voltage input to control audio signal clipping

TCD6000 Connection Diagram



TCD6000 Operation Overview

POWER SUPPLY

The TCD6000 requires both 3.3V and 5V supplies. Pins labeled VD33 correspond to the digital power networks, and pins labeled VA33 and VA50 correspond to the analog power networks. All should be separately decoupled to their respective grounds.

All TCD6000 logic inputs are 3.3V unless otherwise specified.

VD18EN

VD18EN is a logic input that enables the internal 1.8V regulator. It should be tied to VD33.

REXT

The REXT pin should be connected to ground through an external 10KΩ. This connection is used by the TCD6000 as a current reference. The 10KΩ resistor must have an accuracy of +/- 1%.

V2BG and V2BGFILT

The V2BG and V2BGFILT pin should each be AC coupled to GA with a 0.1uF capacitor.

RESETB

When pulled low, the RESETB pin will force all control registers from sub-address 00h to 6Fh and 80h to EFh to their default state. Registers from sub-address 70h to 7Fh and F0h to FFh remain unchanged.

FAULT

The TCD6000 has no fault detection circuitry of its own. Over/under voltage, over current, and over temperature fault detection are expected to be done externally. However, a FAULT input has been provided as an alternate "mute" input. The default (non-muted) state for FAULT is “floating”. The pin will self-bias to approximately 2.5V. If FAULT is taken to either 5V or 0V the TCD6000 will go in to hard mute. If FLD (register 3Ah bit D2) is set to ‘1’, the TCD6000 will automatically un-mute after FAULT is released (forced or floated back to 2.5V). If FLD is cleared to ‘0’, the TCD6000 will remain latched in this FAULT-based muted condition until the FAULT pin is released and FLC (register 3Ah bit D1) undergoes a ‘0’ to ‘1’ transition.

AUTOMATIC DC OFFSET CALIBRATION

When the TCD6000 comes out of hard mute (register 2Ch bit D1 transitions from ‘1’ to ‘0’) an automatic DC offset calibration sequence is started. During this sequence, the TCD6000 calibrates itself and its external components to minimize DC offset at the speaker outputs that can be caused by process variations and component tolerance.

The automatic DC offset calibration sequence takes a maximum of 1 second if the PGC is disabled and 4 seconds if the PGC is enabled. The additional time is required because each different amplifier gain level may require a different calibration level. Therefore, each of the four PGC levels will require calibration upon un-muting.

Automatic DC offset calibration produces 10 bit offset values for each channel that are stored in internal registers. When Automatic DC offset calibration is enabled, the 10 bit values that are in use can be read in the Calibration Readback registers (registers 02h – 09h). When the PGC is enabled, four different values are stored for each channel. The values that are seen in the Calibration Readback registers will change as the PGC Setting changes.

PREDICTIVE GAIN CONTROL

The Predictive Gain Control (PGC) automatically sets one of four different pre-gain levels depending on the Channel Volume level (registers 25h – 2Ah). The PGC allows less gain to be used for lower volume levels. This results in greater digital resolution and lower noise floor. When PGC is enabled (register 3Dh bit D7 is set to '1'), PGC settings are changed automatically by the Channel Volume. When PGC is disabled, the system's pre-gain level is always set to full gain.

Channel Volume Range	PGC Setting
FFh – F4h	Full Gain
F3h – E8h	1/2 Gain
E7h – DCh	1/4 Gain
DBh – 00h	1/8 Gain

POST-GAIN

When the GNn control bits are cleared to '0', the TCD6000 operates in low post-gain mode. In this mode, the noise floor is lowered but the system may not be able to obtain the maximum power output from the power stage. When the GNn control bits are set to '1', the TCD6000 operates in high post-gain mode. In this mode, gain is increased by 25% (about 2dB). The system will now be able to obtain the maximum power output from the power stage but the noise floor will have increased accordingly.

The user may use low post-gain at low volume levels to take advantage of the lower noise floor and use high post-gain at higher volume levels to take advantage of the full range of the power stage. Precautions must be taken while changing post-gain to prevent DC offset. The automatic DC offset cancellation settings will have been affected by changes in post-gain. To avoid this problem, the software that is controlling the TCD6000 through the I^2C port should store DC calibration values for each post-gain setting and swap between them as in the following procedure:

1. Set post-gain to low and channel volumes to 00h.
2. Un-mute.
3. Wait for calibration to complete.
4. Read values in the "Calibration Readback" registers and write them to the "Calibration Bank" registers.
5. Mute.
6. Set post-gain to high and channel volumes to 00h.
7. Un-mute.

Now the calibration bank contains the DC calibration values for low post-gain and the TCD6000 has stored the DC calibration values for high post-gain in its internal registers. When the CFn bits (register 2Fh bits D5..D0) are set to '1', the values stored in the Calibration Bank are used. When the CFn bits are cleared to '0', the internal registers that hold the automatic DC calibration values for high post-gain are used. If the PGC is enabled, the software should only switch between low and high post-gain modes when the PGC is in 1/8 Gain mode. This is because the values stored in the Calibration Bank will only be valid for the PGC mode that was in effect when the channel volumes were set to 00h and automatic DC calibration took place.

Special care should be taken when using this scheme to prevent events from interfering with DC calibration. FAULT should be latched so that a proper calibration can take place during un-mute. Clocks should be kept synchronized to prevent Sync Reset.

I^2C INTERFACE

The I^2C interface is a simple bi-directional bus interface for allowing a microcontroller to read and write control registers in the TCD6000. Every component hooked up to the I^2C bus has its own unique address whether it is a CPU, memory or some other complex function chip. Each of these chips can act as a receiver and/or transmitter depending on its functionality. The TCD6000 acts as a slave while a microcontroller would act as a master.

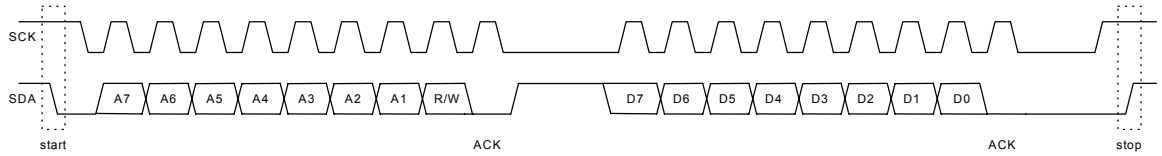
The TCD6000 device address is 80h, 82h, 84h, or 86h depending on the state of the ADDRn pins. The TCD6000 constantly monitors the I^2C data input and waits until its device address appears before writing into or reading from its control registers. The 8^{th} bit of the address determines whether the master is reading

or writing. When the last bit is HIGH, the master is reading from a register on the slave. When the last bit is LOW, the master is writing to a register on the slave.

ADDR2	ADDR1	TCD6000 write address	TCD6000 read address
0	0	80h	81h
0	1	82h	83h
1	0	84h	85h
1	1	86h	87h

The I^2C interface consists of a serial data input (SDA) and a clock input (SCK) and is capable of both reading and writing. Both SCK and SDA are bidirectional lines connected to VD33 via a pull-up resistor. When the bus is free both lines are HIGH.

The SCK clock frequency is typically less than 400 kHz. Data is transmitted serially in groups of 8 bits, followed by an acknowledge bit. The data on the SDA line is expected to be stable while SCK is HIGH.



A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master. Data transfer with acknowledge is obligatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data has been received. The receiver can hold the SCK line LOW after an acknowledge to force the transmitter to wait until the receiver is ready to accept another byte.

When addressed as a slave, the following protocol must be adhered to, once a slave acknowledge has been returned, an 8-bit sub-address will be transmitted. If the LSB of the slave address was ‘1’, a repeated START condition will have to be issued after the address byte; if the LSB is ‘0’ the master will transmit to the slave with direction unchanged.

When the master writes data to the slave, the following events occur:

0. SDA and SCK are both HIGH.
1. A start condition is generated when the master pulls SDA LOW.
2. The master begins toggling SCK and transmits the slave’s device address on SDA with a 0 in the LSB (ex. 80h).
3. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
4. The slave holds SCK low until it is ready to receive the next byte.
5. The slave releases SCK and the master begins toggling SCK and transmits the control register address on SDA.
6. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
7. The slave holds SCK low until it is ready to receive the next byte.
8. The slave releases SCK and the master begins toggling SCK and transmits the data byte on SDA.
9. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
10. The slave holds SCK low until it is ready to receive the next byte.
11. To transmit additional data bytes, repeat steps 8 through 10.
12. A stop condition is generated when SCK is released and SDA goes HIGH while SCK is still high.

When the master reads data from the slave, the following events occur:

0. SDA and SCK are both HIGH.
1. A start condition is generated when the master pulls SDA LOW.
2. The master begins toggling SCK and transmits the slave's device address on SDA with a 1 in the LSB (ex. 81h).
3. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
4. The slave holds SCK low until it is ready to receive the next byte.
5. The slave releases SCK and the master begins toggling SCK and transmits the control register address on SDA.
6. On the ninth SCK pulse, the master releases SDA and the slave acknowledges by pulling SDA LOW.
7. The slave holds SCK low until it is ready to transmit data.
8. The slave releases SCK and the master begins toggling SCK and the slave transmits the data byte on SDA.
9. On the ninth SCK pulse, the slave releases SDA and the master acknowledges by pulling SDA LOW.
10. The slave holds SCK low until it is ready to transmit the next byte.
11. To read additional data bytes, repeat steps 8 through 10.
12. A stop condition is generated when SCK is released and SDA goes HIGH while SCK is still high.

When writing to the TCD6000, the first data byte after the device address is a sub-address. Subsequent data will be written to TCD6000 control registers referred to by the sub-address. When reading from the TCD6000, data will be read starting from the most recently written sub-address.

Control registers from sub-addresses 00h through 7Fh can also be accessed at sub-addresses 80h through FFh. The difference is that sub-addresses 80h through FFh are auto-increment registers. Repeated reads and writes to these registers will automatically increment the sub-address.

For example, if a microcontroller wanted to write a value of E6h to all of the volume registers, it would write the following bytes through its I^2C port: <start> 80h A5h E6h E6h E6h E6h E6h E6h <stop>. If it wanted to read those values back it would send: <start> 80h A5h <stop> <start> 81h <read> <read> <read> <read> <read> <read> <stop>.

Control Registers

This section describes the user-programmable registers controlling many features of the TCD6000. They are programmed using the I^2C interface.

Control bits shown in gray are for Tripath use only and should be set to the values shown. All registers not shown are reserved and should not be changed.

Control Register Mapping

Sub-Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	Mute Status	0	0	0	MUS	SMU	FMU	HMU	AMU
01h	Volume Status	0	0	VZ6	VZ5	VZ4	VZ3	VZ2	VZ1
02h	Calibration Readback	CR19	CR18	CR17	CR16	CR15	CR14	CR13	CR12
03h	Calibration Readback	CR29	CR28	CR27	CR26	CR25	CR24	CR23	CR22
04h	Calibration Readback	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
05h	Calibration Readback	0	0	CR31	CR30	CR21	CR20	CR11	CR10
06h	Calibration Readback	CR49	CR48	CR47	CR46	CR45	CR44	CR43	CR42
07h	Calibration Readback	CR59	CR58	CR57	CR56	CR55	CR54	CR53	CR52
08h	Calibration Readback	CR69	CR68	CR67	CR66	CR65	CR64	CR63	CR62
09h	Calibration Readback	0	0	CR61	CR60	CR51	CR50	CR41	CR40
20h	Freeze Control	0	0	0	0	0	0	0	CHG
21h	Filter Bypass Control	DCB	DEB	DRB	0	0	0	0	0
22h	Sampling Rate Control	0	0	0	1Xf	1Xs	0	S4X	S2X
23h	Operation Control	0	1	0	0	HFR	0	R1	R0
24h	Digital Input Format	0	DP	BCK	CCK	I2S	DA	DW1	DW0
25h	Channel 1 Volume	V17	V16	V15	V14	V13	V12	V11	V10
26h	Channel 2 Volume	V27	V26	V25	V24	V23	V22	V21	V20
27h	Channel 3 Volume	V37	V36	V35	V34	V33	V32	V31	V30
28h	Channel 4 Volume	V47	V46	V45	V44	V43	V42	V41	V40
29h	Channel 5 Volume	V57	V56	V55	V54	V53	V52	V51	V50
2Ah	Channel 6 Volume	V67	V66	V65	V64	V63	V62	V61	V60
2Bh	Volume Ramp Rate	RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0
2Ch	Channel Mute Control	M6	M5	M4	M3	M2	M1	HM	AM
2Dh	Auto-Mute Timing	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
2Eh	Volume Change Control	0	0	0	0	VR1	VR0	VRE	ZCE
2Fh	DC Calibration Control	0	CAB	CF6	CF5	CF4	CF3	CF2	CF1
30h	Calibration Bank	CB19	CB18	CB17	CB16	CB15	CB14	CB13	CB12
31h	Calibration Bank	CB29	CB28	CB27	CB26	CB25	CB24	CB23	CB22
32h	Calibration Bank	CB39	CB38	CB37	CB36	CB35	CB34	CB33	CB32
33h	Calibration Bank	0	0	CB31	CB30	CB21	CB20	CB11	CB10
34h	Calibration Bank	CB49	CB48	CB47	CB46	CB45	CB44	CB43	CB42
35h	Calibration Bank	CB59	CB58	CB57	CB56	CB55	CB54	CB53	CB52
36h	Calibration Bank	CB69	CB68	CB67	CB66	CB65	CB64	CB63	CB62
37h	Calibration Bank	0	0	CB61	CB60	CB51	CB50	CB41	CB40
38h	Force DC	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
39h	Dither Control	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0

3Ah	Fault Latch Control	0	0	0	0	0	FLD	FLC	0
3Bh	Saturation Clamp LSB	1	1	1	1	1	1	1	1
3Ch	Saturation Clamp MSB	1	1	1	0	0	1	1	1
3Dh	Predictive Gain Control	PGC	0	0	0	0	0	0	0
73h	Output Delay Control	0	0	YSGL	0	YD3	YD2	YD1	YD0
74h	Headphone and Logic	0	HMP	HPO	TO	0	0	0	0
75h	Test	0	0	0	0	0	0	0	0
76h	Output Timing Control	DEL	DCB	0	0	STB	BB2	BB1	BB0
77h	Individual Hard Mute	0	HM6	HM5	HM4	HM3	HM2	HM1	0
78h	Gain Control	GN1	0	0	0	0	0	0	0
7Ah	Gain Control	GN2	0	0	0	0	0	0	0
7Bh	Gain Control	GN6	GN5	GN4	GN3	0	0	0	0
7Dh	B Cal Control	0	BC6	BC5	BC4	BC3	BC2	BC1	0

Mute Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00h	Mute Status	0	0	0	MUS	SMU	FMU	HMU	AMU
Default		0	0	0	0	0	0	0	0

This is a read only register that indicates the status of various mute conditions. A '1' indicates that that particular mute is active.

AMU = Auto Mute
HMU = Hard Mute
FMU = Fault Mute
SMU = Sync Mute

MUS is the logical OR of D3..D1. If any of the above mute states are active, MUS will be set to '1'.

Volume Status

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01h	Volume Status	0	0	VZ6	VZ5	VZ4	VZ3	VZ2	VZ1
Default		0	0	0	0	0	0	0	0

These are read only bits that are set to '1' when their respective volume registers are cleared to 0. For example, when register 27h has a value of 8Ch, VZ3 is cleared to '0'. When register 27h has a value of 00h, VZ3 is set to '1'.

Calibration Readback

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02h	Calibration Readback	CR19	CR18	CR17	CR16	CR15	CR14	CR13	CR12
03h	Calibration Readback	CR29	CR28	CR27	CR26	CR25	CR24	CR23	CR22
04h	Calibration Readback	CR39	CR38	CR37	CR36	CR35	CR34	CR33	CR32
05h	Calibration Readback	0	0	CR31	CR30	CR21	CR20	CR11	CR10
06h	Calibration Readback	CR49	CR48	CR47	CR46	CR45	CR44	CR43	CR42
07h	Calibration Readback	CR59	CR58	CR57	CR56	CR55	CR54	CR53	CR52
08h	Calibration Readback	CR69	CR68	CR67	CR66	CR65	CR64	CR63	CR62
09h	Calibration Readback	0	0	CR61	CR60	CR51	CR50	CR41	CR40
Default		0	0	0	0	0	0	0	0

These read only registers show the current automatic DC calibration values. The DC calibration values are 10 bit words so they are stored in separate bytes. For example, for channel 1, the 8 most significant bits are stored in register 02h, while the 2 least significant bits are stored in register 05h – bits D1 and D0.

When PGC is enabled, four different automatic DC calibration values are stored internally – one for each PGC setting. As the channel volume is changed across PGC boundaries, the Calibration Readback value will change to reflect the new PGC setting.

For example, if the user changes channel 1 volume from FFh down to F0h, the PGC level has changed from "full" down to "1/2". Internally, the TCD6000 switches from the DC calibration value that it calculated for full PGC to the DC calibration value that it calculated for 1/2 PGC. The value present in the channel 1 Calibration Readback register also changes to indicate the 1/2 PGC DC calibration value.

Freeze Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
20h	Freeze Control	0	0	0	0	0	0	0	CHG
Default		0	0	0	0	0	0	0	0

While CHG is set to '1', any value that is written to a register takes effect immediately. However, while CHG is cleared to '0', any changes that are made to registers 00h through 6Fh and 80h through EFh will not take effect until CHG is set to '1'. For example, if the user wanted to set all channels to a volume of F6h at the same time, the user could clear CHG, set registers 25h through 2Ah to F6h one at a time, then set CHG to '1'.

Registers 70h through 7Fh and F0h through FFh are not affected by CHG.

Filter Bypass Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
21h	Filter Bypass Control	DCB	DEB	DRB	0	0	0	0	0
Default		0	0	0	0	0	0	0	0

This register allows users to bypass any of the 3 digital filters incorporated in the TCD6000:

DCB = DC blocking filter
DEB = De-Emphasis filter
DRB = Droop correction filter

Setting these bits to '1' bypasses the corresponding filter.

The DC blocking filter eliminates the DC component in an incoming signal. The frequency response of the DC blocking filter is shown in Figure 1 for the 1X, 2X, and 4X modes.

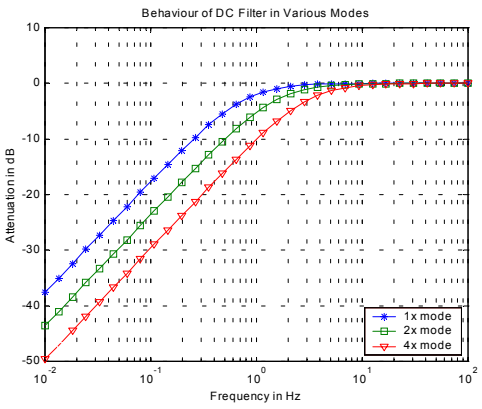


Figure 1. DC Blocking Filter Characteristics

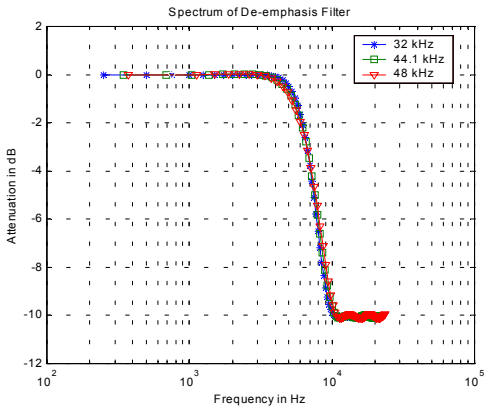


Figure 2. De-Emphasis Filter Characteristics

The De-Emphasis filter is used to re-shape the frequency response and reduce gain for frequencies above 3.183 kHz. It is only available in the 1X mode. If enabled, it needs to be selected for 1 of 4 possible input data rates (32 kHz, 44.1kHz, or 48 kHz), as specified by bits D4 and D3 in the Sampling Rate and De-Emphasis Control Register (address 22h).

The frequency response of the De-emphasis filter is shown in Figure 2 for all 3 input data rates.
The De-Emphasis Filter Selection bit is ignored for the 2X and 4X input data-sampling modes.

A Droop correction filter is included in the TCD6000 to correct for droop and ripple in the frequency response of the entire signal processing chain. The frequency response of the droop filter for the 1X, 2X, and 4X sampling modes is shown below.

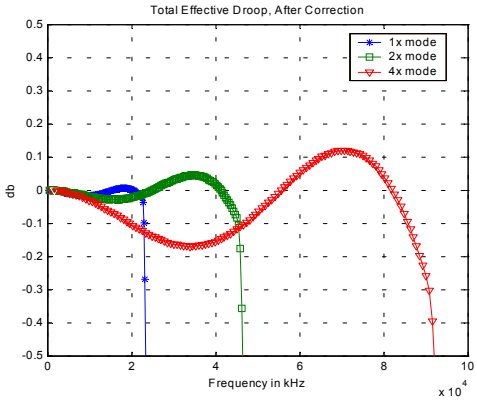


Figure 3. Frequency response of the Droop Correction Filter

Sampling Rate Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
22h	Sampling Rate Control	0	0	0	1Xf	1Xs	0	S4X	S2X
Default		0	0	0	0	0	0	0	0

This register allows the user to specify the data-sampling rate (1X, 2X or 4X). When the 1X mode is selected and the de-emphasis filter is enabled, 1Xf and 1Xs select between 32 kHz, 44.1kHz, and 48 kHz de-emphasis filters.

Bits S4X	S2X	
0	0	1X mode (32 kHz, 44.1 kHz, or 48 kHz)
0	1	2X mode (96 kHz)
1	0 or 1	4X mode (192 kHz)

Bits 1Xf	1Xs	
0	0	data-sampling rate is 44.1 kHz
0	1	data-sampling rate is 32 kHz
1	0	data-sampling rate is 48 kHz
1	1	not used

If the 2X or the 4X modes are selected, the de-emphasis filter is automatically disabled, and the setting of bit D6 in the Filter Bypass Control register (address 21h) will be ignored.

Operation Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
23h	Operation Control	0	1	0	0	HFR	0	R1	R0
Default		0	1	0	0	0	0	1	1

This register allows the user to specify 2 operational characteristics of the TCD6000:

- The Sync Reset mode (control bits R0 and R1)
- The High Frequency Master Clock option (control bit HFR)

If the Left/Right channel clock (LRCK) and Bit clock (BITCK) are not properly synchronized with the Master clock (MCK) and R0 is set to ‘1’, a “Sync Reset” is generated. If R1 is also set to ‘1’ a hard mute is issued during the Sync Reset and released after the Sync Reset is released.

During a Sync Reset the DATAnn inputs are ignored and digital silence is substituted. The TCD6000 waits for the clocks to be synchronized before coming out of reset. During Sync Reset, the internal automatic DC offset calibration values are cleared. When the clocks are restored, the system will need to be re-calibrated by hard muting and un-muting or by forcing a DC calibration value in the Calibration Bank.

The Sync Reset is different from an external reset, which is created by pulling the RESETB pin low. A Sync Reset will not change the values of I2C addressable read/write registers.

R1 enables a "Hard-mute" upon Sync Reset. When the Sync Reset condition is removed, an auto-calibration will take place before the outputs are restored. R0 must be set to '1' for R1 to have any effect.

The Master Clock (MCK) input frequency is determined by a combination of the S4X, S2X, and HFR bits and the sampling frequency. The phase of MCK is not critical, as long as the frequency is correctly set. When the HFR bit (register 23h, bit D3) is set to '1', the TCD6000 divides MCK by 2 so that higher frequency system clocks may be used. The duty cycle of MCK should be between 48% and 52% unless HFR is set to '1'. In this case, the division automatically creates a 50% duty cycle internal clock.

HFR	S4X	S2X	MCK pulses per sample
0	0	0	256
0	0	1	128
0	1	0	64
0	1	1	64
1	0	0	512
1	0	1	256
1	1	0	128
1	1	1	128

The following table shows some examples of the MCK clock frequency based on sampling rate and HFR:

Data sampling rate	32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz
MCK frequency (HFR = '0')	8.192 MHz	11.289 MHz	12.288 MHz	12.288 MHz	12.288 MHz
MCK frequency (HFR = '1')	16.384 MHz	22.578 MHz	24.576 MHz	24.576 MHz	24.576 MHz

Digital Input Format

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
24h	Digital Input Format	0	DP	BCK	CCK	I2S	LRA	DW1	DW0
Default		0	0	1	0	0	0	1	1

This register allows the user to specify the following digital interface characteristics:

- Input data width (DW0 and DW1)
- Input data alignment with respect to LRCK clock edges (LRA)
- Polarity of the LRCK clock (CCK)
- Polarity of the BITCK clock (BCK)
- Polarity of the input data (DP)

The TCD6000 receives PCM digital audio data in I2S format or variations thereof. The format consists of an audio data input (DATAnn), a bit clock (BITCK) that runs at 64x the sampling frequency, and a 1x sampling frequency clock (LRCK). In addition, a master clock (MCK) synchronizes all digital operations inside the device. Each DATAnn input carries serial data for 2 channels. The LRCK clock differentiates between odd

and even channel data. BITCK is synchronized with the serial data input, and latches data on either rising edges or falling edges of BITCK (programmable option).

The TCD6000 has 3 serial data inputs (DATA12, DATA34, and DATA56) and therefore can receive 6 channels of audio data. The group of bits received on a DATAnn input during a half period of LRCK clock is called a PCM data sample. It is a 2's complement representation of the amplitude of sound on that channel at that time.

There are 32 pulses of BITCK for every half period of LRCK. So, in theory, it is possible to read up to 32 bits of data per sample. However, only a maximum of 24 bits are read. The device will also accept 16, 18, and 20 bit formats depending on what has been specified in the control registers.

The most significant bit of data always arrives first and the least significant bit last. Data can be left aligned or right aligned to the LRCK clock. If data is left aligned, the most significant bit of data arrives at the beginning of the LRCK half-period. If data is right aligned, the least significant bit of data arrives just before the end of the LRCK half-period.

DW1 and DW0 define the input data width. Any data outside of the selected data width will be ignored.

DW1	DW0	Input Data Width
0	0	16 bit
0	1	18 bit
1	0	20 bit
1	1	24 bit

LRA specifies the left/right data alignment scheme. When LRA is '0', data is left aligned to LRCK transitions. When LRA is '1', data is right aligned to LRCK transitions.

If data is left aligned, the most significant bit of data can arrive on the first or the second BITCK pulse. The I2S format specifies that it arrive on the second BITCK pulse. When the I2S control bit is '1', the data conforms to the I2S standard - the most significant data bit is read during the second BITCK pulse. When the I2S control bit is '0', the most significant data bit is read during the first BITCK pulse. If data is right aligned, the I2S control bit has no effect.

When CCK is '0', even channel data (channels 2, 4, and 6) is read while LRCK is high and odd channel data (channels 1, 3, and 5) is read while LRCK is low. When CCK is '1', odd channel data is read while LRCK is high and even channel data is read while LRCK is low.

When BCK is '1', data is latched on the falling edge of BITCK. When BCK is '0', data is latched on the rising edge of BITCK.

DP is used to specify the polarity of the 2's complement audio data. If DP is '0', the data is non-inverted. If DP is '1', the data is inverted.

Figure 1 shows several examples of digital input format. Notice that for a given stereo audio sample, the TCD6000 reads even channels first and then the odd channels. I2S and most of its variations first send left channel data and then right channel data within stereo audio sample frames. Therefore, the TCD6000 sends left channel input data to output channels 2, 4 and 6 and right channel input data to output channels 1, 3, and 5.

Inverting CCK to send left channel data to odd channels can potentially cause phase shift problems. For example, if standard I2S data is received with register 24h = 0Bh instead of 1Bh, stereo data frames are read beginning with the rising edge of LRCK instead of the falling edge. This means that left and right channel data will be out of phase by ½ of a LRCK cycle.

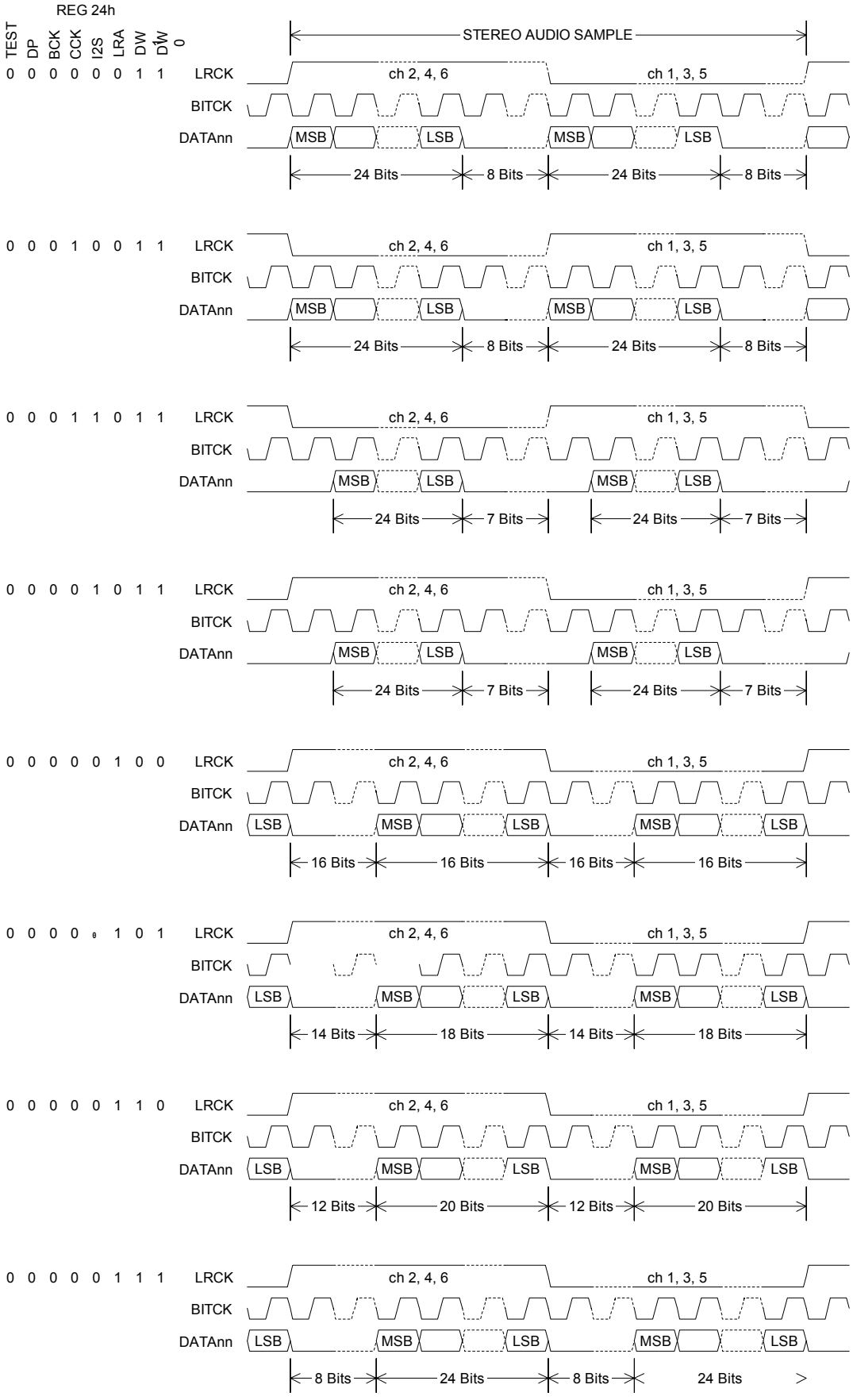


Figure 1 Digital Audio Input Formats

Channel Volume

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
25h	Channel 1 Volume	V17	V16	V15	V14	V13	V12	V11	V10
26h	Channel 2 Volume	V27	V26	V25	V24	V23	V22	V21	V20
27h	Channel 3 Volume	V37	V36	V35	V34	V33	V32	V31	V30
28h	Channel 4 Volume	V47	V46	V45	V44	V43	V42	V41	V40
29h	Channel 5 Volume	V57	V56	V55	V54	V53	V52	V51	V50
2Ah	Channel 6 Volume	V67	V66	V65	V64	V63	V62	V61	V60
Default		0	0	0	0	0	0	0	0

The TCD6000 has 6 channel volume registers, one for each channel. The 8-bit value in each register represents the volume loudness for the corresponding channel. The least significant bit, D0, represents a volume increment of 0.5dB. Therefore the total range available is 128dB. Maximum volume is achieved when the volume register contains a value of FFh, and no sound is heard if its value is 00h.

In addition, a “coarse gain” adjustment (1X, 2X, 4X, and 8X) is made possible by programming the Volume Change Control Register.

Volume Ramp Rate

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Bh	Volume Ramp Rate	RR7	RR6	RR5	RR4	RR3	RR2	RR1	RR0
Default		1	0	0	0	0	0	0	0

The TCD6000 can be programmed to have volume changes take effect immediately or be ramped at a predefined rate for all channels. If the Volume Ramp Enable bit is set, the Volume Ramp Rate Register defines the ramp rate.

Although the Volume Control Registers define the channel volume within an accuracy of ½ dB, volume will be ramped internally in 1/8 dB steps when ramping is enabled.

The number entered into the Volume Ramp Rate Register can be from 0 (00h) to 255 (FFh). If the number entered is N, the time delay between two consecutive 1/8 dB volume increments is equal to:

N x (4 periods of LRCK)

As an example, if N = 100 and data samples are coming in at a 44.1kHz rate, the period of LRCK is 22.67usec. The delay between two consecutive 1/8 dB volume increments is:

100 x 4 x 22.67usec = 9068usec

Therefore if the volume change is 60 dB (480 increments of 1/8 dB), the total ramp time will be:

480 x 9068usec = 4.32 second

Channel Mute Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Ch	Channel Mute Control	M6	M5	M4	M3	M2	M1	HM	AM
Default		0	0	0	0	0	0	1	0

The TCD6000 has 3 different Mute functions: Soft-Mute, Hard-Mute, and Auto-Mute.

The **Soft-Mute** function will turn off volume selectively on any of the 6 channels. Setting control bits M1 through M6 to '1' will issue a Soft-Mute on the corresponding channels. If the VRE bit in the Volume Change Control Register is set, the volume will first ramp down at a rate defined by the Volume Ramp Rate Register. Soft-Mute has no affect on whether the differential outputs (Y1 and Y1B through Y6 and Y6B) continue to switch or not. Clearing bits M1 through M6 to '0' will re-establish volume on all channels at a rate defined by the Volume Ramp Enable settings.

The **Hard-Mute** function is enabled by setting control bit HM high. This function starts with a Soft-Mute on all channels simultaneously. If the VRE bit in the Volume Change Control Register is set, the volume will first ramp down at a rate defined by the Volume Ramp Rate Register. Once volume is turned off on all channels, all differential outputs (Y1 and Y1B through Y6 and Y6B) stop switching. This will reduce power consumption in the power stages driven by the TCD6000.

When control bit HM is cleared to '0', the Hard-Mute condition is removed, and the TCD6000 goes through an automatic DC calibration cycle. Once the calibration cycle is complete, volume is re-established on all channels at a rate defined by the Volume Ramp Enable settings.

The **Auto-Mute** function is enabled by setting the AM bit to '1'. This function detects digital silence (all data input bits at 0) on all 6 channels lasting more than a pre-defined delay. It then issues a Hard-Mute. The delay is determined by the contents of the Auto-Mute Timing Register (described below). Upon arrival of non-zero data on any channel, the Hard-Mute condition is automatically removed. The volume on all 6 channels is re-established at a rate defined by the Volume Ramp Enable settings. The Auto-Mute function reduces power consumption in the power stages during periods of silence.

Auto-Mute Timing

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Dh	Auto-Mute Timing	AM7	AM6	AM5	AM4	AM3	AM2	AM1	AM0
Default		0	0	0	0	0	0	0	0

This register is only used if the Auto-Mute function is enabled. Its contents specify the duration of silence on all 6 channels before a Hard-Mute condition is issued. If the number entered is "N", the duration of silence is equal to:

$$(2N + 1) \times (1{,}048{,}576 \text{ periods of LRCK})$$

As an example, if N = 1 and the period of LRCK is 22.67usec, the period of silence required before a Hard-Mute condition is issued is:

$$3 \times 1{,}048{,}576 \times 22.67\text{usec} = 71.3 \text{ seconds}$$

Volume Change Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Eh	Volume Change Control	0	0	0	0	VR1	VR0	VRE	ZCE
Default		0	0	0	0	0	1	0	0

This register is used to specify 3 characteristics of volume change for all channels:

- Coarse Gain (control bits VR0 and VR1)
- Volume Ramp Enable (control bit VRE)
- Zero-Crossing Enable (control bit ZCE)

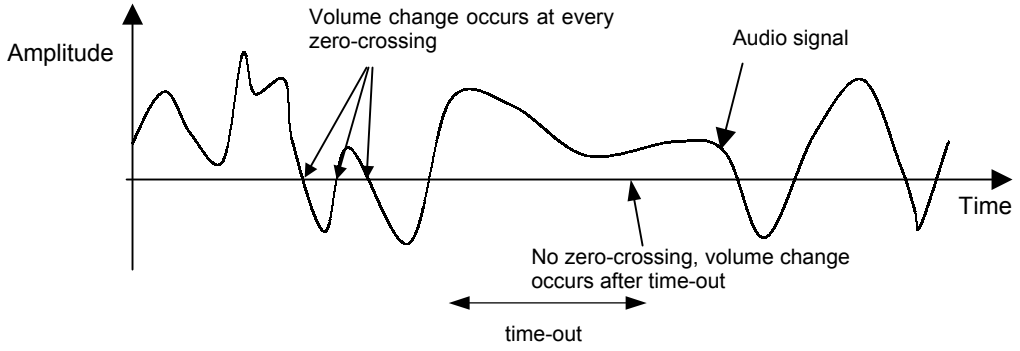
Coarse Gain is a simple volume adjustment made by shifting bits to the left. Coarse Gain is set by selecting one of four combinations for bits VR0 and VR1. Coarse Gain affects all 6 channels globally.

Coarse Gain can cause premature digital clipping when used with PGC because internal digital gain approaches maximum at each PGC boundary. Therefore when using PGC, Coarse Gain should not be enabled until maximum volume has been reached on all channels.

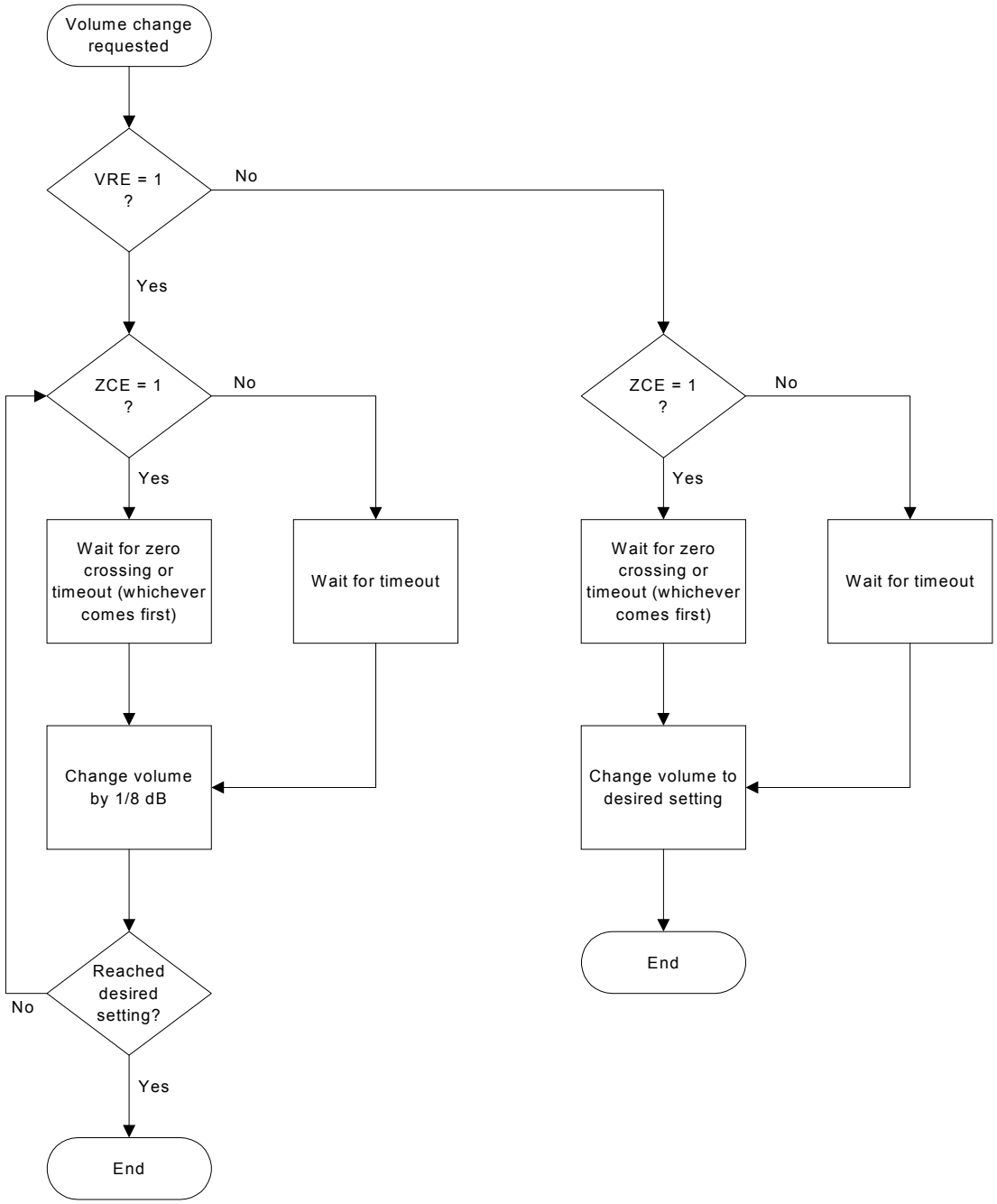
Bits	VR1	VR0	
	0	0	1X volume
	0	1	2X volume
	1	0	4X volume
	1	1	8X volume

The VRE control bit is the Volume Ramp Enable bit. If VRE = '1', the contents of the Volume Ramp Rate Register will be read and determine how fast the volume can ramp up or down on all 6 channels. Refer to the Volume Ramp Rate Register section for a more detailed explanation of how the ramp rate is calculated.

The ZCE control bit is the Zero-Crossing Enable bit. A polarity inversion on the audio input signal is called a "Zero-Crossing". Changing volume only at Zero-Crossings helps to avoid popping sounds. If ZCE is set to '1', volume will only be allowed to change at Zero-Crossings. However, if a Zero-Crossing does not occur within a time defined by the Volume Ramp Rate Register (called "time-out" in the graph below), volume will change anyway. If the Zero-Crossing feature is enabled, the VRE control bit will still control whether the volume change occurs in one large step or in 1/8 dB steps at Zero-Crossings.



Volume Change Flowchart



Automatic DC Offset Calibration Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	Automatic DC Calibration Control	0	CAB	CF6	CF5	CF4	CF3	CF2	CF1
Default		0	0	0	0	0	0	0	0

The CFn bits control which DC offset calibration values will be used. If a particular channel's CFn bit is set to '1', the value stored in the Calibration Bank registers will be used. If CFn is cleared to '0', the Automatic DC Offset Calibration values that were calculated after coming out of hard mute will be used.

Setting the CAB bit to '1' will bypass Automatic DC Offset Calibration.

Calibration Bank

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
30h	Calibration Bank	CB19	CB18	CB17	CB16	CB15	CB14	CB13	CR12
31h	Calibration Bank	CB29	CB28	CB27	CB26	CB25	CB24	CB23	CR22
32h	Calibration Bank	CB39	CB38	CB37	CB36	CB35	CB34	CB33	CR32
33h	Calibration Bank	0	0	CB31	CB30	CB21	CB20	CB11	CR10
34h	Calibration Bank	CB49	CB48	CB47	CB46	CB45	CB44	CB43	CR42
35h	Calibration Bank	CB59	CB58	CB57	CB56	CB55	CB54	CB53	CR52
36h	Calibration Bank	CB69	CB68	CB67	CB66	CB65	CB64	CB63	CR62
37h	Calibration Bank	0	0	CB61	CB60	CB51	CB50	CB41	CR40
Default		0	0	0	0	0	0	0	0

These registers store calibration values that can be forced instead of the automatic DC calibration values. Register 2Fh controls whether the automatic values will be used or the Calibration Bank values. The DC calibration values are 10 bit words so they are stored in separate bytes. For example, for channel 1, the 8 most significant bits are stored in register 30h, while the 2 least significant bits are stored in register 05h – bits D1 and D0.

Force DC

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
38h	Force DC	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Default		0	0	0	1	1	1	0	0

This register is used to force a DC offset in the system. It is used for testing purposes. It should be changed from its default setting to 00h for normal operation.

Dither Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
39h	Dither Control	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0
Default		0	0	0	0	0	0	0	0

This register is used to set the amount of dither in the system. It should be set to 3Ch for normal operation.

Fault Latch Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
3Ah	Fault Latch Control	0	0	0	0	0	FLD	FLC	0
Default		0	0	0	0	0	1	0	0

FLD and FLC control the TCD6000 behavior after FAULT has been asserted.

If FLD is set to '1', the TCD6000 will automatically un-mute after FAULT is released (floated).

If FLD is cleared to '0', the TCD6000 will remain latched in this FAULT-based muted condition until the FAULT pin is released and FLC undergoes a '0' to '1' transition.

Saturation Clamp

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
3Bh	Saturation Clamp LSB	1	1	1	1	1	1	1	1
3Ch	Saturation Clamp MSB	1	1	1	0	0	1	1	1

The Saturation Clamp is a 16 bit word that determines the internal digital saturation point. It should be set to E7FFh for the maximum range of operation.

Predictive Gain Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
3Dh	Predictive Gain Control	PGC	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0

Predictive Gain Control is enabled when PGC is set to '1'. It is disabled when PGC is cleared to '0'. PGC should not be turned on or off while not in hard-mute. Doing so will have unpredictable results.

Output Delay Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
73h	Output Delay Control	0	0	YSGL	0	YD3	YD2	YD1	YD0
Default		0	0	0	0	0	0	0	0

During automatic DC calibration the TCD6000 expects to be able to turn off both the high and low side FETs by pulling Y and Yb low. However, some power stages like the Tripath TPD2075 and TPD2125 only have a single Y input instead of complimentary Y and Yb inputs. When using this type of power stage, YSGL should be cleared to '1'. Then, during automatic DC calibration, HPO should be set to '1'. This keeps the HMUTE output high during automatic DC calibration. After waiting for automatic DC calibration to complete, HPO can be set to '0' to resume normal switching. When using other power stages, YSGL can be kept at '0'.

The YDn bits control the loop delay of the Class-T amplification channels. This can be used to control the maximum output switching frequency. Each channel receives the same amount of additional delay which defaults to 15nS but can be increased from 15nS to 240nS in 15nS steps.

YD<3:0>	Actual count	Processor Y-output delay
0000 (POR default)	1	15 nS
0001	2	30 nS
0010	3	45 nS
0011	4	60 nS
0100	5	75 nS
0101	6	90 nS
0110	7	105 nS
0111	8	120 nS
1000	9	135 nS
1001	10	150 nS
1010	11	165 nS
1011	12	180 nS
1100	13	195 nS
1101	14	210 nS
1110	15	225 nS
1111	16	240 nS

Truth table for Y-output delay control.

Headphone and Logic Output Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
74h	Headphone and Logic Output	0	HMP	HPO	TO	0	0	0	0
Default		0	0	0	0	0	0	0	0

Setting the TO control bit to '1' forces the TST_EN output pin to go high. This pin can be used to put the power stage IC into test mode. If the power stage does not have a TST_EN input, the TST_EN output can be used as a general purpose logic output.

The HPO control bit immediately stops all switching without muting the headphone amplifier outputs.

The HMP bit controls whether the HMUTE output is active high or active low. Setting HMP to '1' causes the HMUTE output to be active low.

Output Timing Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
76h	Output Timing Control	DEL	DCB	0	0	STB	BB2	BB1	BB0
Default		0	0	0	0	0	0	0	0

Control bits BB0 through BB2 are used to program a “break before make” delay in the Y outputs.

Break before make is a dead time at the Y-outputs where both Y and YB of each channel are low together for a period of time in order to prevent shoot-through current in the output power MOSFET devices.

BB<2:0>	BBM Delay
000	0 nS
001	15 nS
010	30 nS
011	45 nS
100	60 nS
101	75 nS
110	90 nS
111	105 nS

Break before make (BBM) delay table

The STB control bit enables a 16-bit Startup Burst for driving bootstrapped output stages.

The DCB control bit controls the method of automatic DC calibration that will be used. DCB should be set to ‘1’ if a bridged output stage is being used. DCB should be cleared to ‘0’ if a single ended output stage is being used. The BCn bits work in conjunction with the DCB bit. When DCB is set to '1', the BCn bits should be set to '1'. When DCB is cleared to '0', the BCn bits should be cleared to '0'.

The DEL control bit enables the on-chip delay compensation. Delay compensation corrects for loop instability that can be caused by propagation delay through power stages. It should always be set to ‘1’.

Individual Hard Mute Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
77h	Individual Hard Mute Control	0	HM6	HM5	HM4	HM3	HM2	HM1	0
Default		0	0	0	0	0	0	0	0

Setting an HMn bit to ‘1’ stops switching on an individual output channel. Clearing the bit to ‘0’ resumes normal operation.

Post-Gain Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
78h	Post Gain Control	GN1	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0
7Ah	Post Gain Control	GN2	0	0	0	0	0	0	0
Default		0	0	0	0	0	0	0	0
7Bh	Post Gain Control	GN6	GN5	GN4	GN3	0	0	0	0
Default		0	0	0	0	0	0	0	0

When the GNn control bits are cleared to ‘0’, the TCD6000 operates in low post-gain mode. In this mode, the noise floor is lowered but the system may not be able to obtain the maximum power output from the power stage. When the GNn control bits are set to ‘1’, the TCD6000 operates in high post-gain mode. In this mode, gain is increased by 25%. The system will now be able to obtain the maximum power output from the power stage but the noise floor will have increased accordingly.

B Cal Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
7Dh	Force Offset and B Cal Control	0	BC6	BC5	BC4	BC3	BC2	BC1	0
Default		0	0	0	0	0	0	0	0

The BCn control bits control the method of automatic DC calibration that will be used. The BCn bits should be set to ‘1’ if a bridged output stage is being used. The BCn bits should be cleared to ‘0’ if a single ended output stage is being used. The BCn bits work in conjunction with the DCB bit. When DCB is set to '1', the BCn bits should be set to '1'. When DCB is cleared to '0', the BCn bits should be cleared to '0'.

I2C Programming Examples

Initialization string for a Tripath TP2150B with PGC off:

sub-address	value	
20h	00000000b	Un-freeze registers. System starts in mute so the instruction sequence is not important.
21h	11000000b	Turn off de-emphasis and DC blocking filters. Turn on droop correction filter.
22h	00010000b	48kHz sampling rate.
23h	01000011b	MCK will be 48kHz * 256 = 12.288MHz. Sync Reset is on and it will trigger a hard-mute.
24h	00011011b	Standard I2S format.
25h	00h	Channel 1 Volume
26h	00h	Channel 2 Volume
27h	00h	Channel 3 Volume
28h	00h	Channel 4 Volume
29h	00h	Channel HP1 Volume
2Ah	00h	Channel HP2 Volume
2Bh	00h	Leave Volume Ramp Rate at 00h while not changing volume.
2Ch	00000010b	Start out in hard-mute. Turn off Auto-Mute.
2Dh	00h	Auto-Mute Timing
2Eh	00000011b	Coarse Gain = 1x. Volume Ramp Enable and Zero Crossing Enable
2Fh	01100000b	Bypass DC calibration for headphone outputs.
30h	00h	CalibBank0Ex
31h	00h	CalibBank1Ex
32h	00h	CalibBank2Ex
33h	00h	CalibBank012Ex
34h	00h	CalibBank3Ex
35h	00h	CalibBank4Ex
36h	00h	CalibBank5Ex
37h	00h	CalibBank345Ex
38h	00h	Clear Force DC register.
39h	3Ch	Set Dither Control to 3Ch.
3Ah	00000100b	Enable Fault Latch.
3Bh	FFh	Always set Saturation Clamp to these values.
3Ch	E7h	Always set Saturation Clamp to these values.
3Dh	00000000b	Turn on PGC.
73h	00001011b	Use 195nS delay to slow down switching (adjust as needed for each design).
74h	00000000b	HMUTE is active high, HPO = 0, TST_EN output is low.
75h	00h	Test.
76h	10001011b	Enable Delay compensation. Use A-cal for single ended output. Enable startup burst for bootstrap. BBM = 45nS (adjust as needed for each design).
77h	00000000b	Individual channel hard mutes are inactive.
78h	10000000b	Channel 1 high post-gain.
79h	00h	Test.
7Ah	10000000b	Channel 2 high post-gain.
7Bh	11110000b	Channel 3, 4, 5, and 6 high post-gain.
7Ch	00h	Test.
7Dh	00000000b	All channels use A-cal for single ended output.

To Un-mute a TP2150B:

sub-address	value	
2Ch	00000000b	Remove Hard-Mute to begin automatic DC calibration.

<If PGC is on, wait 4 seconds for automatic DC calibration. If PGC is off, wait 1 second for calibration.>

OUTPUT CHARACTERISTICS

The TCD6000 outputs consist of six pairs of complementary 1-bit digital data streams, one pair per audio channel. They switch from 0V to 5V (+/- 10%) and constitute a pulse-density-modulated (PDM) form of the audio signal. They are used to drive Tripath power stages in a switching amplifier configuration.

The output power of a power stage can be expressed as V^2/R, V being the voltage amplitude of the power stage output and R the speaker input impedance, typically 4 to 8 ohms.

The audio signal is recovered by filtering the PDM signal through an LC filter located at the inputs of the speaker. The following figure shows the power stage output waveform and the filtered signal at the speaker inputs:

Typical waveform at power stage output

Typical waveform at speaker inputs after LC filtering

TCD6000 outputs are pulse density modulated outputs. Their frequency varies constantly over time and can typically reach a maximum value of 800 kHz.

A Mute output (HMUTE) can be connected to all 6 power stages to force them into a tri-state mode when a hard mute condition is encountered. The HMUTE output can be programmed to be either active-high or active-low (bit D6 in control register 74h).

An overload is detected whenever the combination of input signal amplitude and volume programmed in the TCD6000 results in output signal saturation and distortion. The OVRLDB pin goes active low when this condition occurs.

A test output pin is also provided (TST_EN) for external testing purposes. Setting bit D4 in control register 74h will force this output to an active high state.

The HMUTE, OVRLDB and TST_EN outputs are 5V digital outputs.

The TCD6000 also includes a pair of stereo headphone outputs (HP1 and HP2), which are connected to channels 1 and 2. These outputs are analog with maximum 3V peak-to-peak amplitude. They have a common mode voltage of 2V and should therefore be AC coupled to the headphone jack. If the headphone outputs are not being used, these pins may be left unconnected.

FEEDBACK CONNECTIONS

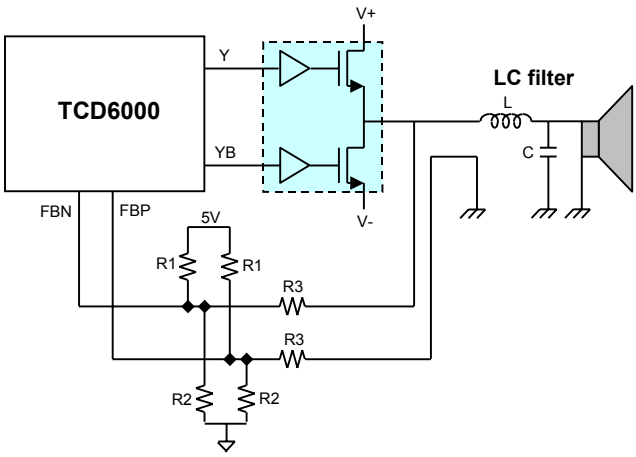


Figure 2 - Feedback network for single ended configurations (1 channel shown)

Differential feedback from the power stage outputs to the TCD6000 FB inputs is required. This feedback is taken directly from the outputs of the power stage, before the LC filter stage. It allows the TCD6000 to compensate for power stage distortion (non-linearity, power supply noise, etc.) and to deliver an ultra-low THD that is unique to class-T technology. Total harmonic distortion is typically less than 0.03% with most power stages.

Resistors R1, R2, and R3 create a voltage divider structure to reduce the unfiltered output of the power stage for the feedback pins. In single ended output configurations like the one shown in Figure 2, the feedback voltage should be approximately 4Vpp. R1 and R2 bias the feedback signal to approximately 2.5V and R3 scales the large output voltages down to 4Vpp. The input impedance of the TCD6000 feedback pins is approximately 25K.

To solve for the values of the feedback resistors in a single ended configuration:

$$R1 = \text{User specified, typically } 1K\Omega$$

$$R2 = \frac{R1 * VPP}{(VPP - 4 - \frac{VPP * R1}{25K})}$$

$$R3 = \frac{R1 * VPP}{4}$$

The above equations assume that VPP = |VNN|.

For example, in a system with VPP_{MAX} = +28V and VNN_{MAX} = -28V,

R1 = 1kΩ, 1%
R2 = 1.224kΩ, use 1.21kΩ, 1%
R3 = 7.00kΩ, use 6.98kΩ, 1%

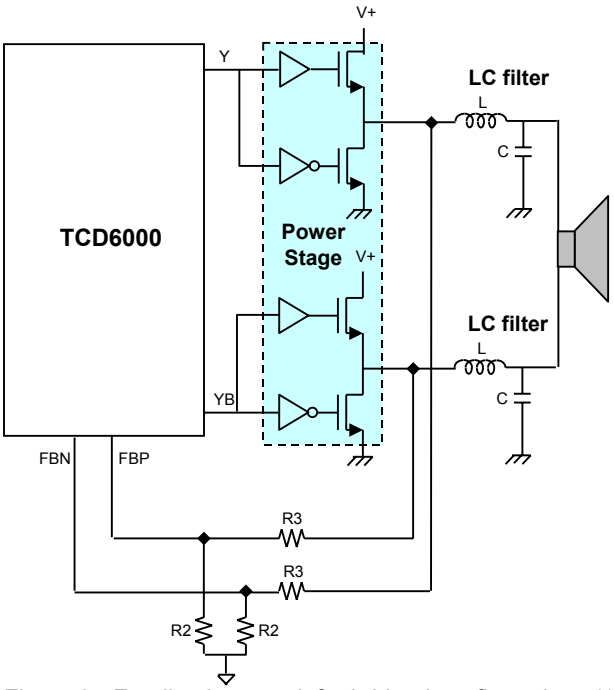


Figure 3 - Feedback network for bridged configurations (1 channel shown)

In bridged configurations like the one shown in Figure 3, R1 is absent (infinity). Since the feedback is now bridged, the feedback voltage should be cut in half to 2Vpp.

To solve for the values of the feedback resistors in a bridged configuration:

$$R2 = \text{User specified, typically } 1K\Omega$$

$$R3 = \frac{25K * R2}{25K + R2} * \frac{VPP - 2}{2}$$

For example, in a system with VPP_{MAX}=30V,

R2 = 1kΩ, 1%
R3 = 13.462kΩ, use 13.3kΩ, 1%

VCLAMP PIN BIASING

The VCLAMP pin must have a DC voltage applied which is proportional to the peak to peak voltage swing of the power output switching stage in the amplifier system. More explicitly, the potential at VCLAMP should be 0.525 times the peak to peak differential voltage seen at each channel's *feedback* pins (i.e., the full final value voltage swing neglecting any RC settling time effects). This means that the component values used in the circuitry biasing the VCLAMP pin are a direct function of the chosen feedback network components. In a full bridged system, proper VCLAMP biasing is achieved via a simple two resistor divider between V+ (the output stage power supply) and ground, shown in the right-hand portion of the circuit below (excluding the portion in the dotted line box). In a single ended (half bridge) system, VCLAMP biasing is achieved by the entire six element circuit below.

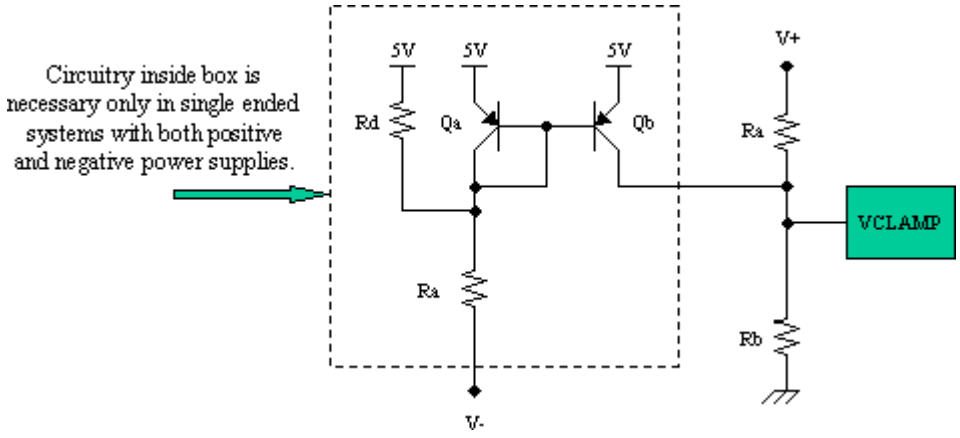


Figure 4 - VCLAMP biasing

In a bridged system, stated in terms of the components described in the feedback section, the values for Ra and Rb are determined as follows (Rd = 0.176 x Ra):

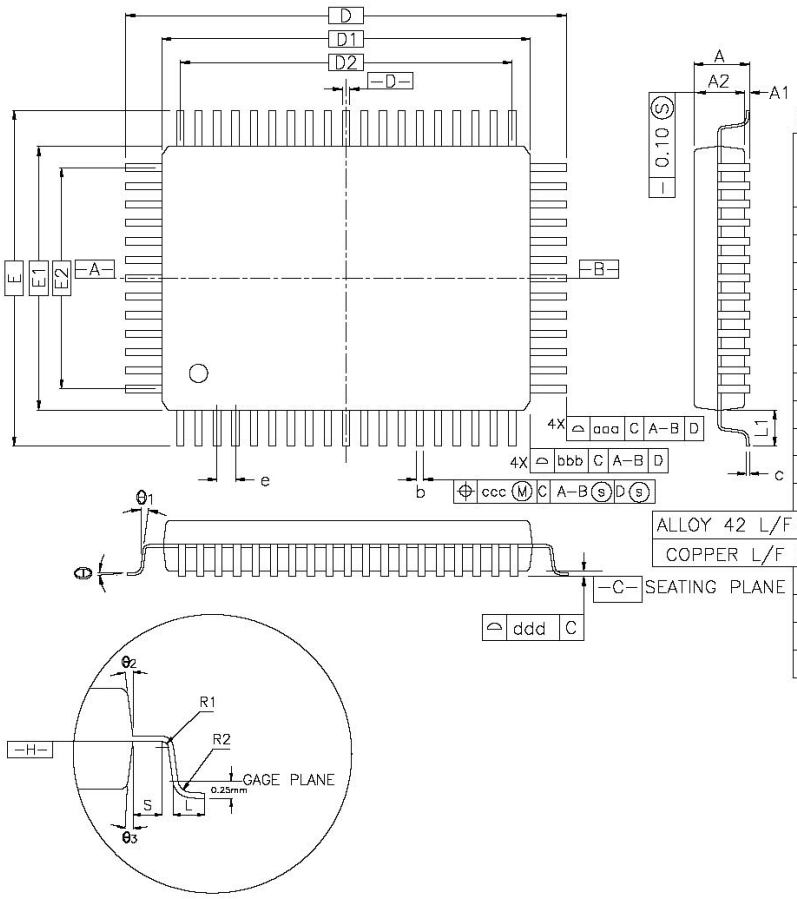
$$\mathrm{Ra} = \mathrm{Rb} \times \left(\frac{0.952 \times \mathrm{R3}}{\mathrm{R2} \,||\, 25\mathrm{K}} - 0.048 \right)$$

where R2||25k is the parallel combination of R2 and 25k Ohms. In a single ended (half bridge) system, the component value relationships would be, stated in terms of the components in the feedback section:

$$\mathrm{Ra} = \mathrm{Rb} \times \left(\frac{1.90 \times \mathrm{R3}}{\mathrm{R1} \,||\, \mathrm{R2} \,||\, 25\mathrm{K}} + 0.90 \right)$$

where Rd = 0.176 x Ra, and R1||R2||25k is the parallel combination of R1, R2, and 25k Ohms.

Package Information (QFP 100)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	3.40	—	—	0.134
A1	0.25	—	—	0.010	—	—
A2	2.50	2.72	2.90	0.098	0.107	0.114
D	23.20 BASIC			0.913 BASIC		
D1	20.00 BASIC			0.787 BASIC		
E	17.20 BASIC			0.677 BASIC		
E1	14.00 BASIC			0.551 BASIC		
R2	0.13	—	0.30	0.005	—	0.012
R1	0.13	—	—	0.005	—	—
θ	0°	—	7°	0°	—	7°
θ1	0°	—	—	0°	—	—
ALLOY 42 L/F θ2 , θ3	7° REF			7° REF		
COPPER L/F θ2 , θ3	15° REF			15° REF		
c	0.11	0.15	0.23	0.004	0.006	0.009
L	0.73	0.88	1.03	0.029	0.035	0.041
L1	1.60 REF			0.063 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	64L						80L						100L						128L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.35	0.40	0.50	0.014	0.016	0.020	0.30	0.35	0.45	0.012	0.014	0.018	0.22	0.30	0.38	0.009	0.012	0.015	0.170	0.200	0.270	0.007	0.008	0.011
e	1.00 BSC.			0.039 BSC.			0.80 BSC.			0.031 BSC.			0.65 BSC.			0.026 BSC.			0.50 BSC.			0.020 BSC.		
D2	18.00 REF			0.709 REF			18.40 REF			0.724			18.85 REF			0.742			18.50			0.728		
E2	12.00 REF			0.472 REF			12.00 REF			0.472			12.35 REF			0.486			12.50			0.492		
TOLERANCES OF FORM AND POSITION																								
aaa	0.25			0.010			0.25			0.010			0.25			0.010			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.20			0.008			0.20			0.008			0.13			0.005			0.08			0.003		
ddd	0.10			0.004			0.10			0.004			0.10			0.004			0.08			0.003		

NOTES :

1. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.

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