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GEC PLESSEY
SEMICONDUCTORS

SP8630

600MHz÷10

The SP8630 is an asynchronous emitter coupled logic divider which provides an ECLIII/10K compatible output when used with an external pulldown resistor. It requires an AC coupled input of 600mV p-p.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: −5·2V
- Power Consumption: 350mW
- Temperature Range: −30°C to +70°C

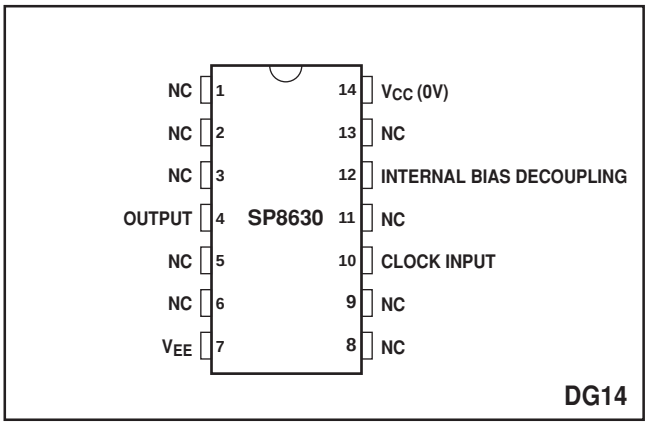


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{EE}	−8V
Output current	15mA
Storage temperature range	−65°C to +150°C
Max. junction temperature	+175°C
Max. clock input voltage	2·5V p-p

ORDERING INFORMATION

SP8630 B DG
5962-92003 (SMD)

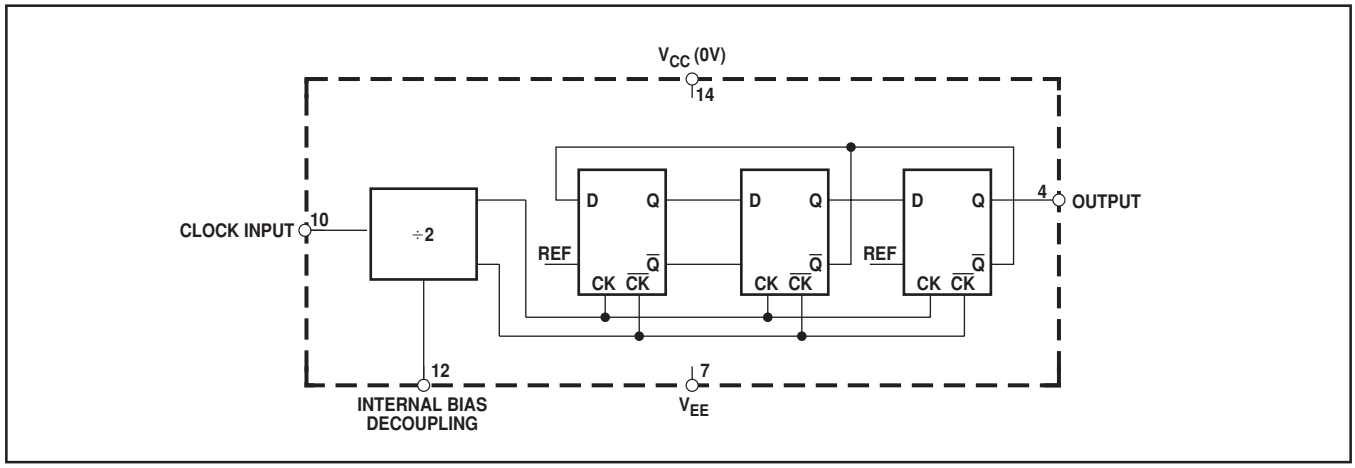


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range

Supply voltage, V_{CC} = 0V, V_{EE} = −5·2V ± 0·25V
Temperature, T_{AMB} = −30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{MAX}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{MIN}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		70	mA	V_{EE} = −5·2V	
Output low voltage	V_{OL}	−1·8	−1·5	V	V_{EE} = −5·2V	3
Output high voltage	V_{OH}	−0·85	−0·7	V	V_{EE} = −5·2V	3
Minimum output swing	V_{OUT}	400		mV	V_{EE} = −5·2V	

NOTES
1. The temperature coefficients of V_{OH} = +1·63mV/°C, and V_{OL} = +0·94mV/°C but these are not tested.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Tested at 25°C only.

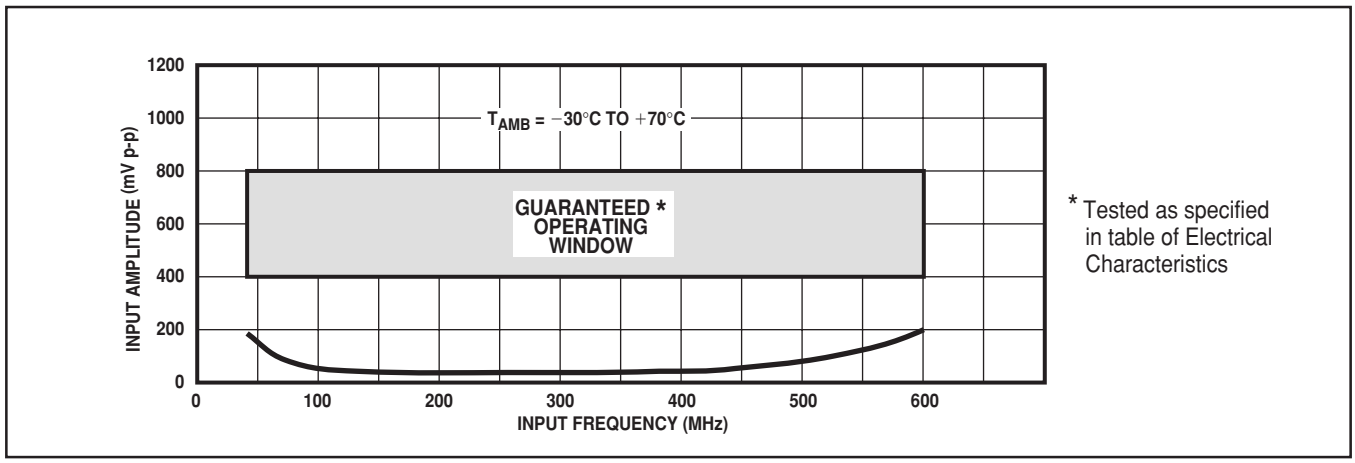


Fig. 3 Typical input characteristic

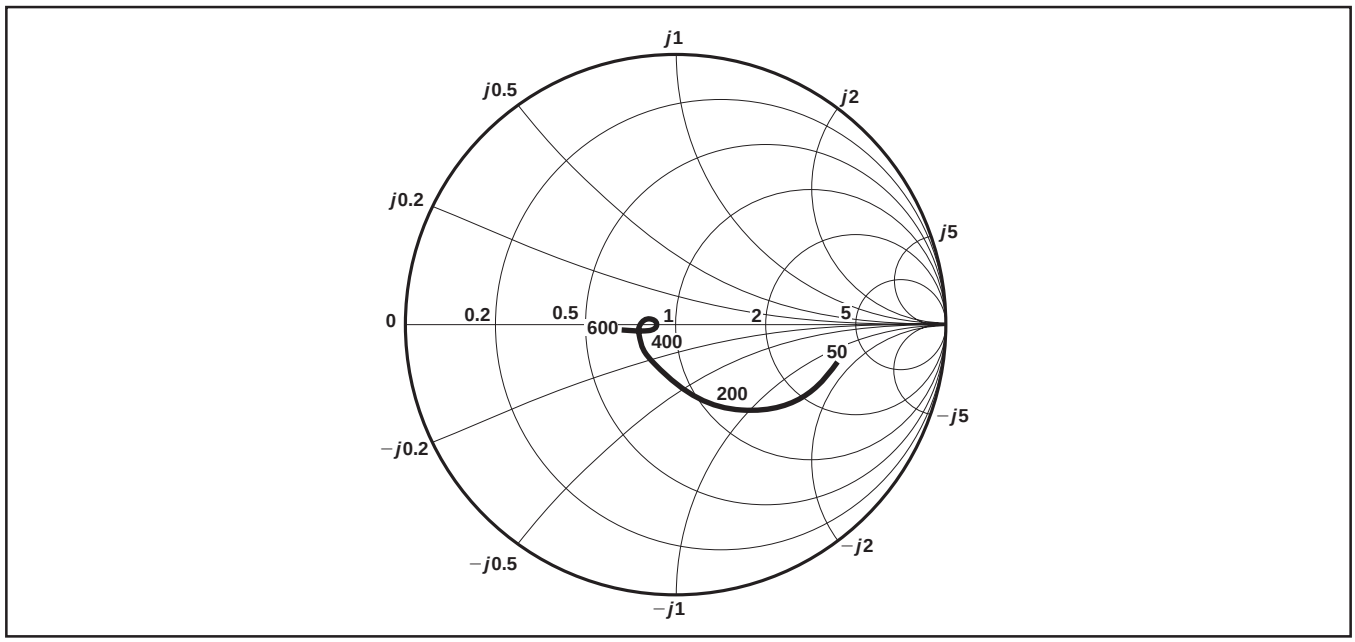


Fig. 4 Typical input impedance. Test conditions: supply voltage = −5·2V, ambient temperature = 25°C, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. The circuit will operate down to DC but slew rate must be better than 100V/μs.
3. The output is compatible with ECLII. There is an internal load of 3kΩ at the output. The output can be interfaced to ECLIII/10K by the addition of 1·5kΩ to the output to increase the output voltage swing.
4. Input impedance is a function of frequency, see Fig. 4.
5. All components should be suitable for the frequency in use.

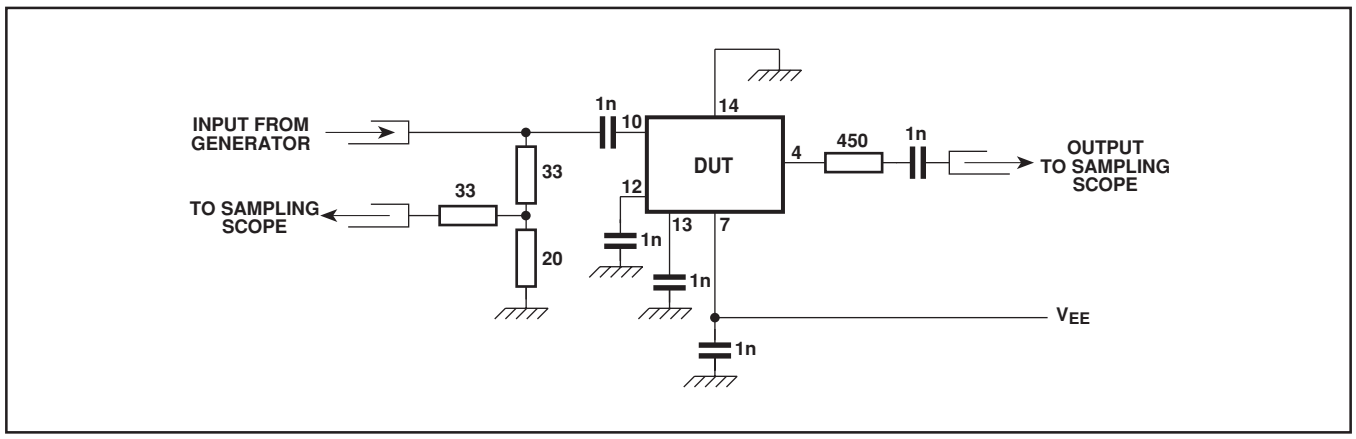


Fig. 5 Test circuit

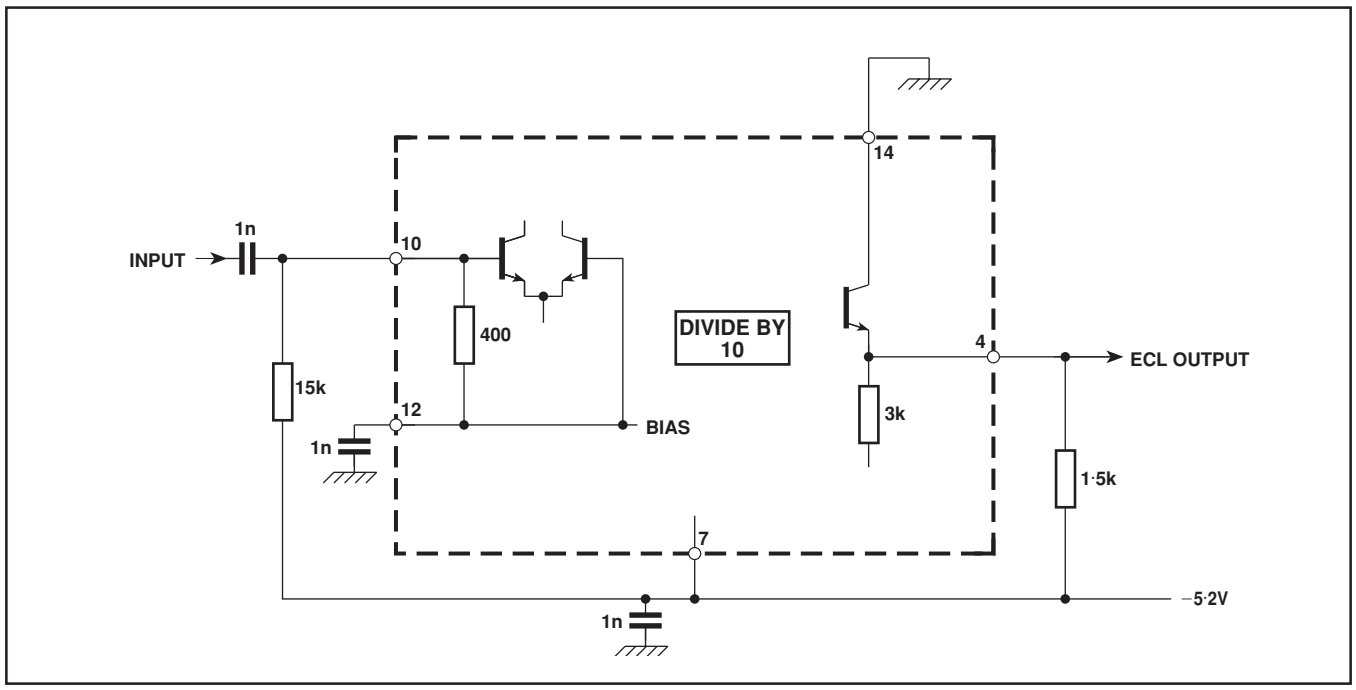
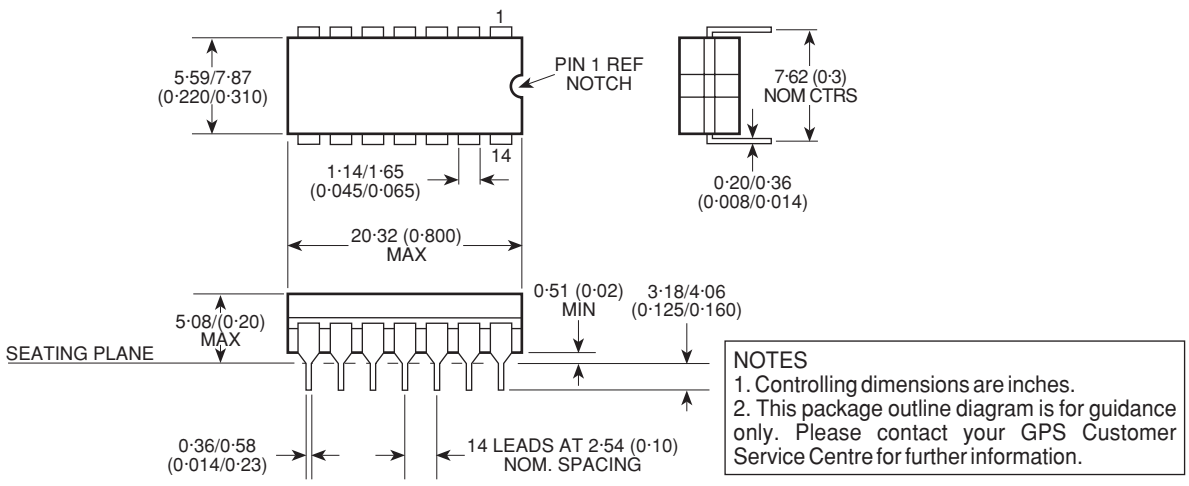


Fig. 6 Typical application showing interfacing

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are inches.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

14-LEAD CERAMIC DIL – DG14

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