

FEATURES

350 MHz Small Signal Bandwidth
130 MHz Large Signal BW (4 V p-p)
High Slew Rate: 1200 V/ μ s
Fast Settling: 11 ns to 0.01%/7 ns to 0.1%
 ± 3 V Supply Operation

APPLICATIONS

ADC Input Driver
Differential Amplifiers
IF/RF Amplifiers
Pulse Amplifiers
Professional Video
DAC Current-to-Voltage
Baseband and Video Communications
Pin Diode Receivers
Active Filters/Integrators/Log Amps

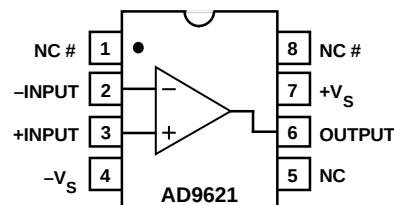
GENERAL DESCRIPTION

The AD9621 is one of a family of very high speed and wide bandwidth amplifiers utilizing a voltage feedback architecture. These amplifiers define a new level of performance for voltage feedback amplifiers, especially in the categories of large signal bandwidth, slew rate, settling, and low noise.

Proprietary design architectures have resulted in an amplifier family that combines the most attractive attributes of both current feedback and voltage feedback amplifiers. The AD9621 exhibits extraordinarily accurate and fast pulse response characteristics (7 ns settling to 0.1%) as well as extremely wide small and large signal bandwidth previously found only in current feedback amplifiers. When combined with balanced high impedance inputs and low input noise current more common to voltage feedback architectures, the AD9621 offers performance not previously available in a monolithic operational amplifier.

*Protected by U.S. Patent 5,150,074 and others pending.

CONNECTION DIAGRAM



OPTIONAL CAPACITOR CB CONNECTED HERE
DECREASES SETTLING TIME

Other members of the AD962X amplifier family are the AD9622 (G = +2), AD9623 (G = +4), and the AD9624 (G = +6). A separate data sheet is available from Analog Devices for each model. Each generic device has been designed for a different minimum stable gain setting, allowing users flexibility in optimizing system performance. Dynamic performance specifications such as slew rate, settling time, and distortion vary from model to model. The table below summarizes key performance attributes for the AD962X family and can be used as a selection guide.

The AD9621 is offered in industrial and military temperature ranges. Industrial versions are available in plastic DIP, SOIC, and cerdip; MIL versions are packaged in cerdips.

PRODUCT HIGHLIGHTS

1. Wide Large Signal Bandwidth
2. High Slew Rate
3. Fast Settling
4. Output Short-Circuit Protected

Parameter	AD9621	AD9622	AD9623	AD9624	Units
Minimum Stable Gain	+1	+2	+4	+6	V/V
Harmonic Distortion (20 MHz)	-52	-66	-64	-66	dB
Large Signal Bandwidth (4 V p-p)	130	160	190	200	MHz
SSBW (0.5 V p-p)	350	220	270	300	MHz
Slew Rate	1200	1500	2100	2200	V/ μ s
Rise/Fall Time (0.5 V Step)	2.4	1.7	1.6	1.5	ns
Settling Time (to 0.1%/0.01%)	7/11	8/14	8/14	8/14	ns
Input Noise (0.1 MHz – 200 MHz)	80	49	36	32	μ V rms

REV. 0

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AD9621—SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS ($\pm V_S = \pm 5\text{ V}$, $R_{\text{LOAD}} = 100\ \Omega$; $A_V = 1$, unless otherwise noted)

Parameter	Conditions	Temp	Test Level	AD9621AN/AQ/AR			AD9621SQ			Units
				Min	Typ	Max	Min	Typ	Max	
DC SPECIFICATIONS ¹										
Input Offset Voltage		+25°C	I	−12	±2	+12	−12	±2	+12	mV
		Full	VI	−15		+15	−15		+15	mV
Input Bias Current		+25°C	I		7	16		7	16	μA
		Full	VI	−20		+20	−20		+20	μA
Input Bias Current TC		Full	V		35			35		nA/°C
Input Offset Current		+25°C	I	−2.0	±0.3	+2.0	−2.0		+2.0	μA
		Full	VI	−3.0		+3.0	−3.0		+3.0	μA
Offset Current TC		Full	V		2.5			2.5		nA/°C
Input Resistance		+25°C	V		500			500		kΩ
Input Capacitance		+25°C	V		1.2			1.2		pF
Common-Mode Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Common-Mode Rejection Ratio	ΔV _{CM} = 1 V	+25°C	I	46	49		46	49		dB
Open Loop Gain	V _{OUT} = ±2 V p-p	+25°C	V		56			56		dB
Output Voltage Range		Full	VI	±3.0	±3.4		±3.0	±3.4		V
Output Current		Full	VI	60	70		60	70		mA
Output Resistance		+25°C	V		0.3			0.3		Ω
FREQUENCY DOMAIN										
Bandwidth (−3 dB)										
Small Signal	V _{OUT} ≤ 0.4 V p-p	Full	II	230	350		230	350		MHz
Large Signal	V _{OUT} ≤ 4.0 V p-p	Full	V		130			130		MHz
Amplitude of Peaking	Full Spectrum	Full	II		0.1	1.2		0.1	1.2	dB
Amplitude of Roll-off	≤ 100 MHz	Full	II		0	0.6		0	0.6	dB
Phase Nonlinearity	DC to 100 MHz	+25°C	V		1.1			1.1		Degree
2nd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−55	−44		−55	−44	dBc
3rd Harmonic Distortion	2 V p-p; 20 MHz	Full	II		−52	−43		−52	−43	dBc
Common-Mode Rejection Mode	@ 20 MHz	+25°C	V		+28			+28		dB
Spectral Input Noise Voltage	1 to 200 MHz	+25°C	V		5.6			5.6		nV/√Hz
Spectral Input Noise Current	1 to 200 MHz	+25°C	V		3.6			3.6		pA/√Hz
Average Equivalent Integrated Input Noise Voltage	0.1 to 200 MHz	+25°C	V		80			80		μV rms
TIME DOMAIN										
Slew Rate	V _{OUT} = 5 V Step	Full	IV	850	1200		850	1200		V/μs
Rise/Fall Time	V _{OUT} = 0.5 V Step	+25°C	V		2.4			2.4		ns
	V _{OUT} = 5 V Step	Full	IV		4.8	7		4.8	7	ns
Overshoot	V _{OUT} = 2 V Step	Full	IV		0	15		0	15	%
Settling Time										
To 0.1%	V _{OUT} = 2 V Step	+25°C	V		7			7		ns
To 0.01%	V _{OUT} = 2 V Step	Full	IV		11	15		11	15	ns
To 0.1% ²	V _{OUT} = 4 V Step	+25°C	V		9			9		ns
To 0.01 ²	V _{OUT} = 4 V Step	+25°C	V		13			13		ns
Overdrive Recovery	1.5x to ±2 mV	+25°C	V		50			50		ns
Differential Gain (4.3 MHz)	R _L = 150 Ω	+25°C	V		0.01			0.01		%
Differential Phase (4.3 MHz)	R _L = 150 Ω	+25°C	V		<0.01			<0.01		Degree
POWER SUPPLY REQUIREMENTS ¹										
Supply Voltage (±V _S)		Full	IV	3.0	5.0	5.5	3.0	5.0	5.5	V
Quiescent Current										
+I _S	+V _S = +5 V	Full	VI		23	29		23	29	mA
−I _S	−V _S = −5 V	Full	VI		23	29		23	29	mA
Power Supply Rejection Ratio	ΔV _S = 0.5 V	+25°C	I	54	66		54	66		dB

NOTES

¹Measured at $A_V = 21$.

²Measured with a 0.001 μF C_B capacitor connected across Pins 1 and 8.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltages ($\pm V_S$)	± 6 V
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	6 V
Continuous Output Current ²	90 mA
Operating Temperature Ranges	
AN, AQ, AR	-40°C to +85°C
SQ	-55°C to +125°C
Storage Temperature	
Ceramic	-65°C to +150°C
Plastic	-65°C to +125°C
Junction Temperature	
Ceramic ³	+175°C
Plastic ³	+150°C
Lead Soldering Temperature (1 minute) ⁴	+220°C

NOTES

¹Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

²Output is short-circuit protected; for maximum reliability, 90 mA continuous current should not be exceeded.

³Typical thermal impedances (part soldered onto board; no air flow):

Ceramic DIP: $\theta_{JA} = 100^\circ\text{C/W}$; $\theta_{JC} = 30^\circ\text{C/W}$

Plastic SOIC: $\theta_{JA} = 125^\circ\text{C/W}$; $\theta_{JC} = 45^\circ\text{C/W}$

Plastic DIP: $\theta_{JA} = 90^\circ\text{C/W}$; $\theta_{JC} = 45^\circ\text{C/W}$

⁴Temperature shown is for surface mount devices, mounted by vapor phase soldering. Throughhole devices (ceramic and plastic DIPs) can be soldered at +300°C for 10 seconds.

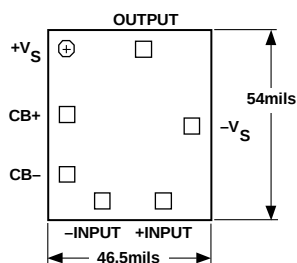
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9621AN	-40°C to +85°C	8-Pin Plastic DIP	N-8
AD9621AQ	-40°C to +85°C	8-Pin Cerdip	Q-8
AD9621AR	-40°C to +85°C	8-Pin SOIC	R-8
AD9621SQ	-55°C to +125°C	8-Pin Cerdip	Q-8

EXPLANATION OF TEST LEVELS

Test Level

- I – 100% production tested.
- II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing of “A” grade devices done on sample basis.
- III – Sample tested only.
- IV – Parameter is guaranteed by design and characterization testing.
- V – Parameter is a typical value only.
- VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.



Chip Layout

THEORY OF OPERATION

The AD9621 is a wide bandwidth, unity gain stable voltage feedback amplifier. Since its open-loop frequency response follows the conventional 6 dB/octave roll-off, its gain bandwidth product is basically constant. Increasing its closed-loop gain results in a corresponding decrease in small signal bandwidth. The AD9621 typically maintains a 55 degree unity loop gain phase margin. This high margin minimizes the effects of signal and noise peaking.

Feedback Resistor Choice

At minimum stable gain (+1), the AD9621 provides optimum dynamic performance with $R_F \approx 51 \Omega$. This resistor acts only as a parasitic suppressor against damped R_F oscillations that can occur due to lead (input, feedback) inductance and parasitic capacitance. For settling accuracy to 0.1% or less, this resistor should not be required if layout guidelines are closely followed. This value for R_F provides the best combination of wide bandwidth, low parasitic peaking, and fast settling time.

When the AD9621 is used in the transimpedance (I-to-V) mode, such as for photo-diode detection, the value for R_F and diode capacitance (C_I) are usually known. See Figure 1. Generally, the value of R_F selected will be in the k Ω range, and a shunt capacitor (C_F) across R_F will be required to maintain good amplifier stability. The value of C_F required to maintain < 1 dB of peaking can be estimated as:

$$C_F \approx [(2\omega_o C_I R_F - 1)\omega_o^2 R_F^2]^{1/2} \Big|_{R_F \geq 1 \text{ k}\Omega}$$

where ω_o is equal to the unity gain bandwidth product of the amplifier in RAD/sec, and C_I is the equivalent total input capacitance at the inverting input. Typically ω_o is 700×10^6 RAD/sec (See Open Loop Frequency Response curve).

As an example, choosing R_F of 10 k Ω and C_I of 5 pF, requires C_F to be 1.1 pF (Note: C_I includes both the source and parasitic circuit capacitance). The bandwidth of the amplifier can be estimated using the C_F calculated as:

$$f_3 \text{ dB} \approx \frac{1.6}{2 \pi R_F C_F}$$

For general voltage gain applications, the amplifier bandwidth can be estimated as:

$$f_3 \text{ dB} \approx \frac{\omega_o}{1 + \left(\frac{R_F}{R_G} \right)}$$

This estimation loses accuracy for gains approaching +2/-1 or lower due to the amplifier's damping factor. For these “low gain” cases, the bandwidth will actually extend beyond the calculated value. See Closed Loop BW plots.

As a rule of thumb, capacitor C_F will not be required if:

$$(R_F \parallel R_G) C_I \leq \frac{NG}{4\omega_o}$$

where NG is the Noise Gain ($1 + R_F/R_G$) of the circuit. For most voltage gain applications, this should be the case.

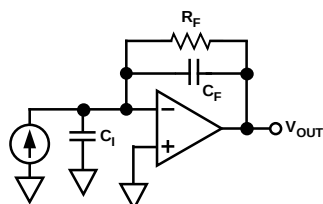


Figure 1. Transimpedance Configuration

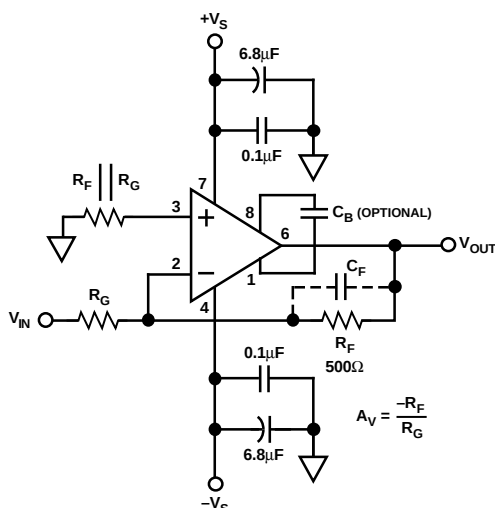


Figure 2. Inverting Gain Connection Diagram

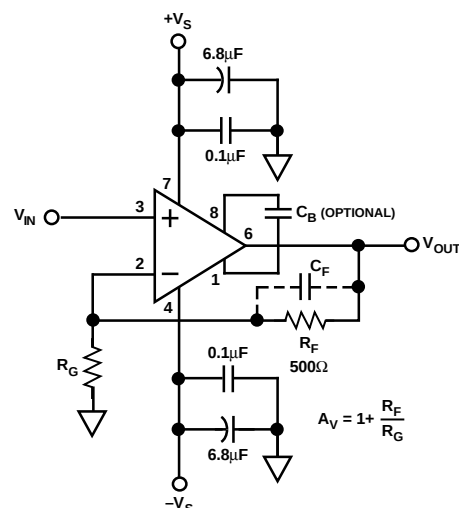


Figure 3. Noninverting Gain Connection Diagram

Pulse Response

Unlike a traditional voltage feedback amplifier in which slew speed is dictated by its front end dc quiescent current and gain bandwidth product, the AD9621 provides “on demand” trans-conductance current that increases proportionally to the input “step” signal amplitude. This results in slew speeds (1200 V/μs) comparable to wideband current feedback designs. This, combined with relatively low input noise current (3.6 pA/√Hz), gives the AD9621 the best attributes of both voltage and current feedback amplifiers.

Bootstrap Capacitor (C_B)

In most applications, the C_B capacitor will not be required. Under certain conditions, it can be used to further enhance settling time performance.

The C_B capacitor (0.001 μF) connects to the internal high impedance nodes of the amplifier. Using this capacitor will reduce the large signal (4 V) step output settling time by 3 to 5 ns for 0.05% or greater accuracy. For settling accuracy less than 0.05% or for smaller step sizes, its effect will be less apparent.

Under heavy slew conditions, this capacitor forces the internal signal (initial step) amplitude to be controlled by the “on” (slewed) transistor, preventing its complement from completely turning off. This allows for faster settling time of these internal nodes and also the output.

In the frequency domain, total (high frequency) distortion will be approximately the same with or without C_B. Typically, the 3rd harmonic will be greater than the 2nd without C_B. This will be reversed with C_B in place.

APPLICATIONS

The AD9621 is a voltage feedback amplifier and is well suited for such applications as photo-detector preamp, active filters, and log amplifiers. The device’s wide bandwidth (350 MHz),

phase margin (55°), low noise current (3.6 pA/√Hz), and slew rate (1200 V/μs) give higher performance capabilities to these applications over previous voltage feedback designs.

With a settling time of 11 ns to 0.01% and 7 ns to 0.1%, the device is an excellent choice for DAC I/V conversion. The same characteristics, along with low harmonic distortion, make it a good choice for ADC buffering/amplification. With its superb linearity at relatively high signal frequencies, it is an ideal driver for ADCs up to 14 bits.

Layout Considerations

As with all wide bandwidth components, printed circuit layout is critical to obtain best dynamic performance with the AD9621. The ground plane in the area of the amplifier and its associated components should cover as much of the component side of the board as possible (or first interior layer of a multi layer surface mount board).

The ground plane should be removed in the area of the inputs and R_F and R_G to minimize stray capacitance at the input. The same precaution should be used for C_B, if used. Each power supply trace should be decoupled close to the package with a 0.1 μF ceramic capacitor, plus a 6.8 μF tantalum nearby.

All lead lengths for input, output, and feedback resistor should be kept as short as possible. All gain setting resistors should be chosen for low values of parasitic capacitance and inductance, i.e., microwave resistors and/or carbon resistors.

Microstrip techniques should be used for lead lengths in excess of one inch. Sockets should be avoided if at all possible because of their high series inductance. If sockets are necessary, individual pin sockets such as AMP p/n 6-330808-3 should be used. These contribute far less stray reactance than molded socket assemblies.

An evaluation board is available from Analog Devices for a nominal charge.

Typical Performance ($R_L = 100\ \Omega$; $A_V = +1$, unless otherwise noted)—AD9621

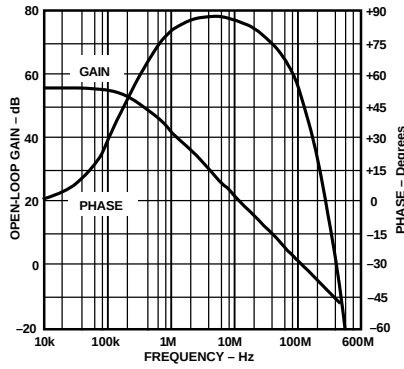


Figure 4. Open-Loop Gain and Phase

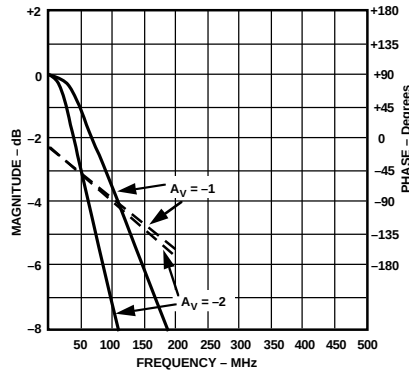


Figure 5. Inverting Frequency Response

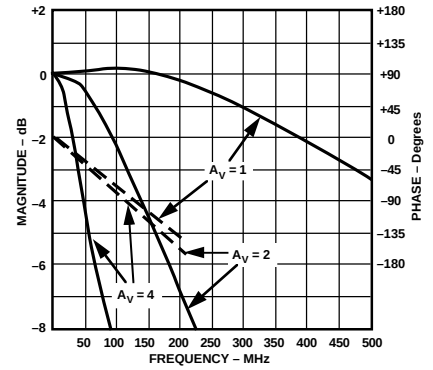


Figure 6. Noninverting Frequency Response

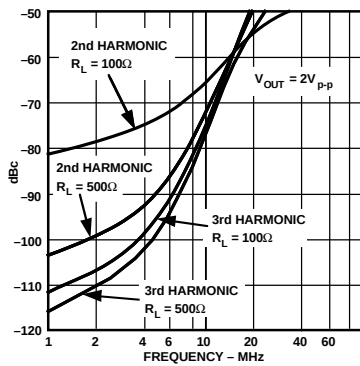


Figure 7. Harmonic Distortion vs. Frequency

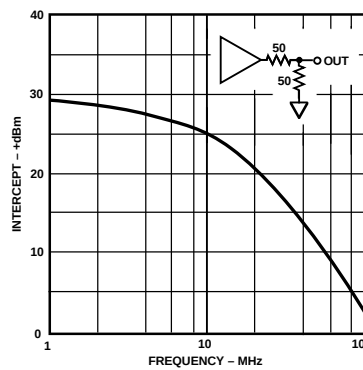


Figure 8. Third Order Intercept

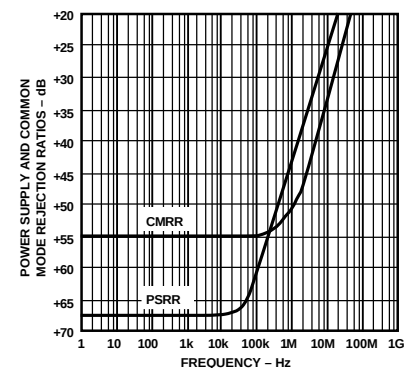


Figure 9. CMRR and PSRR vs. Frequency

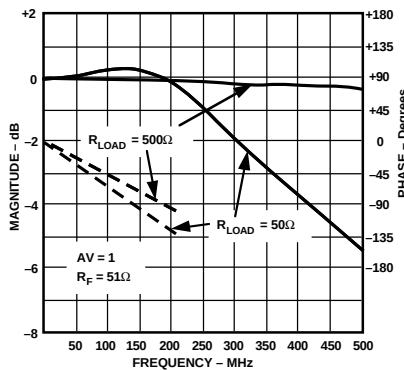


Figure 10. Frequency Response vs. R_{LOAD}

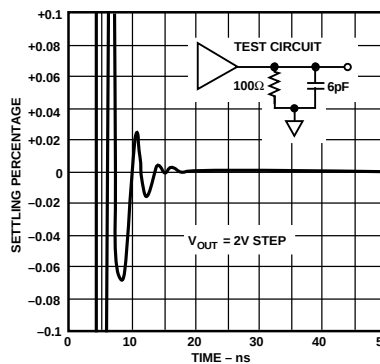


Figure 11. Short-Term Settling Time

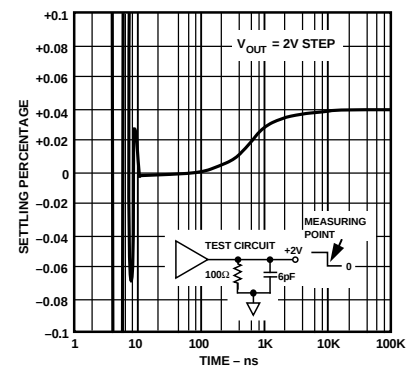


Figure 12. Long-Term Settling Time

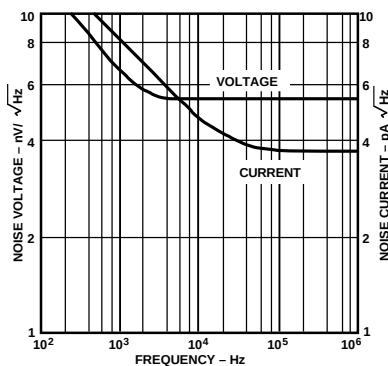


Figure 13. Input Spectral Noise Density

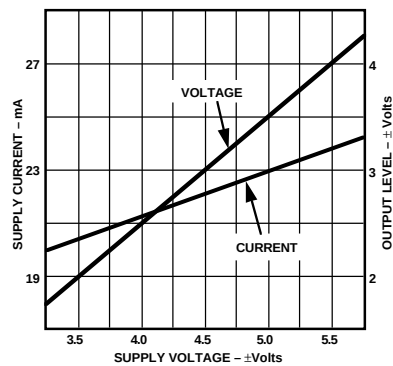


Figure 14. Output Level and Supply Current vs. Supply Voltage

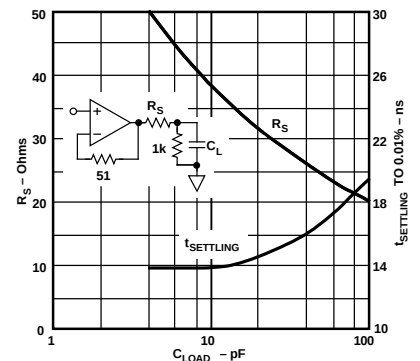
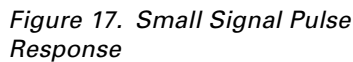
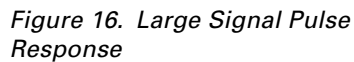


Figure 15. Settling Time vs. Capacitive Load



Dimensions shown in inches and (mm).

Plastic DIP (Suffix N)

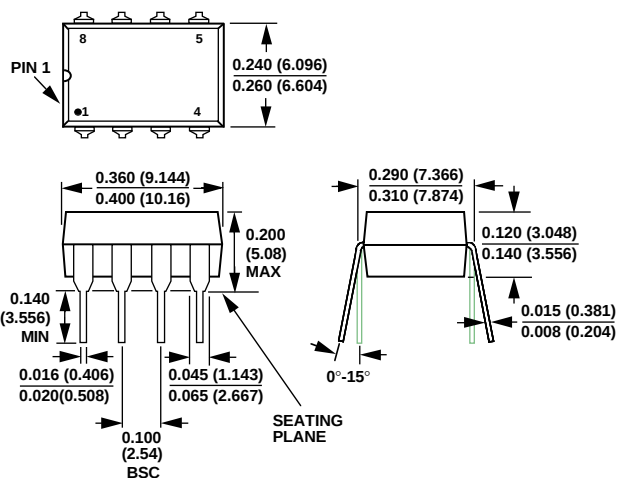


Figure 1: Dimensions of the test structure. The figure includes three views: a top view, a side view, and a cross-sectional view. The top view shows a central rectangular area labeled 'TOP VIEW' with dimensions 0.196 (5.00) and 0.188 (4.75) for the top width, 0.244 (6.20) and 0.228 (5.80) for the left height, and 0.158 (4.00) and 0.150 (3.80) for the right height. The bottom width is 0.180 (0.46) and 0.014 (0.36). The bottom height is 0.050 (1.27) TYP. The side view shows a central rectangular area with dimensions 0.069 (1.75) and 0.053 (1.35) for the right height. The bottom width is 0.010 (0.25) and 0.004 (0.10). The cross-sectional view shows a central rectangular area with dimensions 0.206 (5.20) and 0.181 (4.60) for the top width, 0.015 (0.38) and 0.007 (0.18) for the bottom width, and 0.045 (1.15) and 0.020 (0.50) for the bottom height.