MSM6950B

ANALOG FRONT END LSI

GENERAL DESCRIPTION

The MSM6950B is an analog front-end LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology for modem chip set based on Bell 212A. CCITT V. 22 and CCITT V. 22 bis standard. The MSM6950B consists of two BPFs, for low band and high band, an A/D converter with 8-bit parallel output, a D/A converter with 8-bit parallel input, an AGC circuit controlled by external digital signals, a guard tone generator (550 Hz/1800 Hz selectable) and some analogue signal control switches for various applications.

The MSM6950B communicates with a modulator and a demodulator via each 8 bits parallel digital line.
This chip does not contain a carrier detect function but it will be performed with a digital signal processor dedicated to implement a demodulator by using digital signals from the A/D converter.

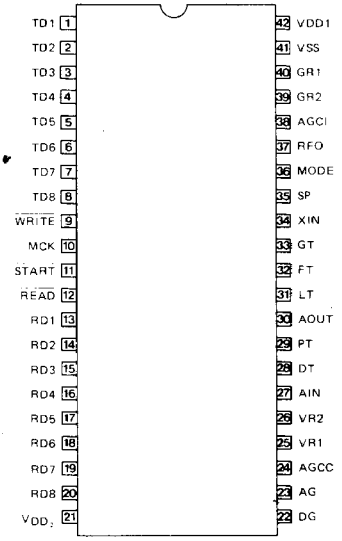
This device provides an analog signal input, an analog signal output and some signal-loop control inputs, and requires a 3.6864 MHz clock input to generate the operating time-base.

FEATURES

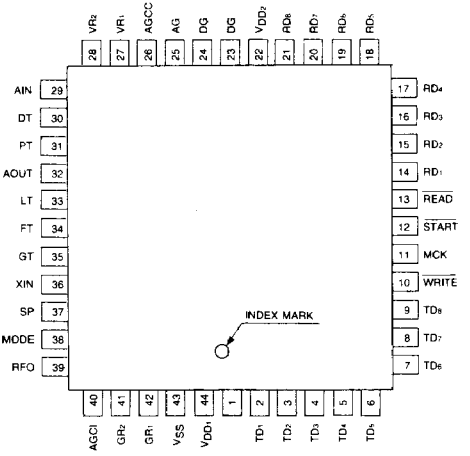
- Conforms to bell 212A, 103 and CCITT V. 22 and V. 22 bis.
- 8-bit parallel output A/D converter and 8-bit parallel input D/A converter on chip.
- On-chip voltage reference.
- On-chip AGC circuit controlled by 8-bit external digital signal, over the received signal level range of 48 dB with 0.19 dB step.
- Dynamic range, 70 dB.
- Guard tone mixing function, 550 Hz or 1800 Hz.
- On-chip multi-purpose LPF for tone transmitting and call progress detection.
- Provides AC loop test function, a transmitting analog signal can be looped back as a receive analog signal within the chip.
- Supply voltage, ±5V.
- Low power dissipation, 115 mW.
- 3.6864 MHz external clock for operation.
- 42-pin plastic DIP MSM6950BRS
  56-pin plastic FLAT
  . . . . . MSM6950BGS-VK
  44-pin PLCC. MSM6950BJS

PIN CONFIGURATION (Top view)

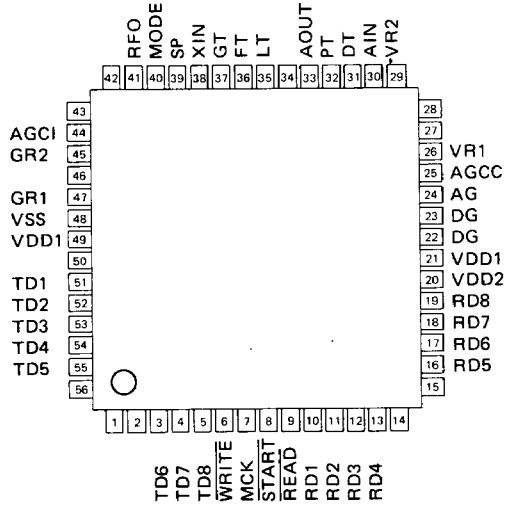
42 pin DIP (MSM6950BRS)



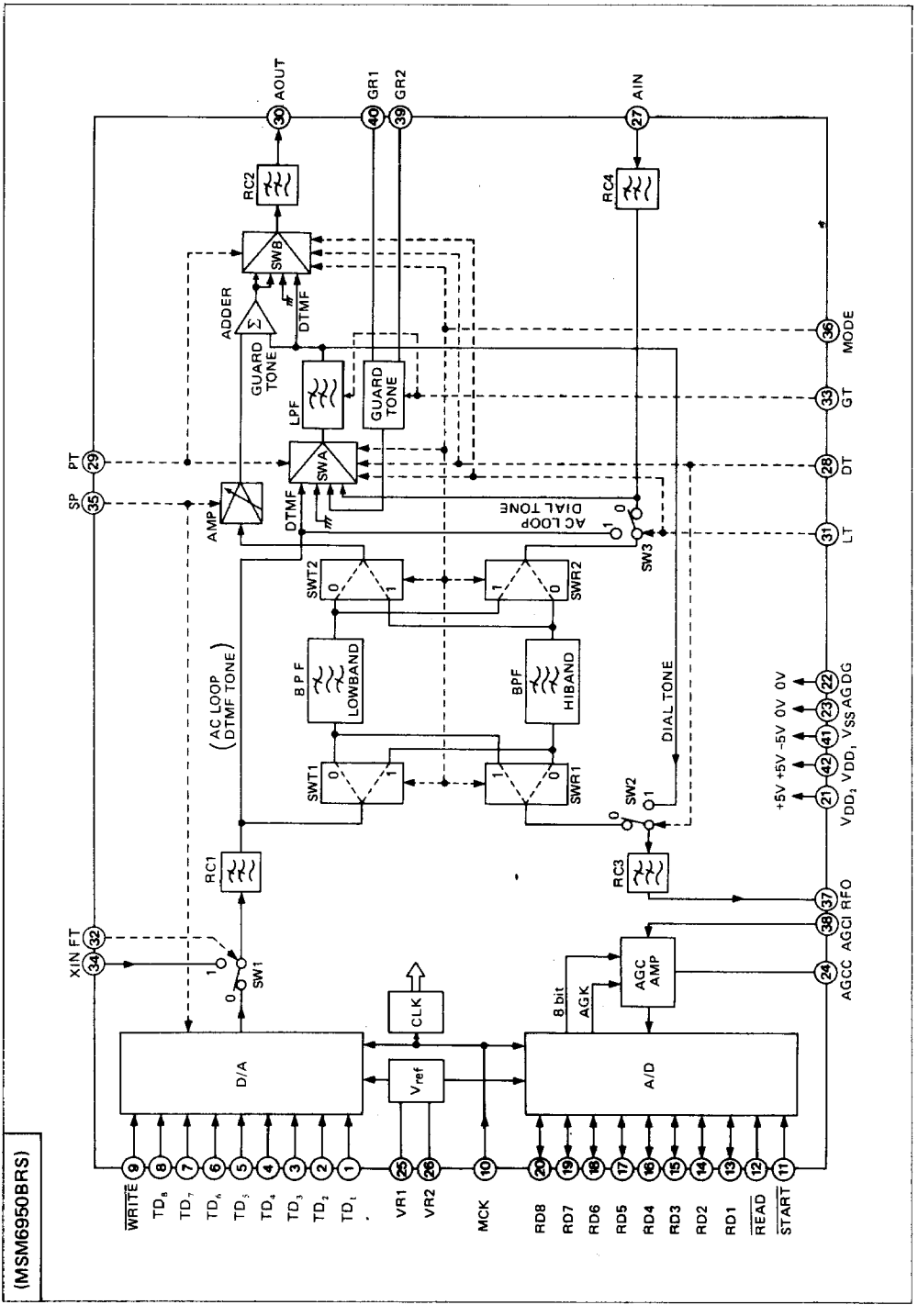
44 pin PLCC (MSM6950BJS)



56 pin FLAT (MSM6950BGS-VK)



BLOCK DIAGRAM



Pin Assignment

Pin Name	Pin No.			In/Out	Function
	RS	GS	JS		
TD1	1	51	2	Input	Transmit signal digital data input to DA (LSB)
TD2	2	52	3	Input	Transmit signal digital data input to DA
TD3	3	53	4	Input	Transmit signal digital data input to DA
TD4	4	54	5	Input	Transmit signal digital data input to DA
TD5	5	55	6	Input	Transmit signal digital data input to DA
TD6	6	3	7	Input	Transmit signal digital data input to DA
TD7	7	4	8	Input	Transmit signal digital data input to DA
TD8	8	5	9	Input	Transmit signal digital data input to DA (MSB)
$\overline{\text{WRITE}}$	9	6	10	Input	TD writing control signal for DA
MCK	10	7	11	Input	Master clock input 3.6864 MHz
$\overline{\text{START}}$	11	8	12	Input	Control signal for starting of AD conversion
$\overline{\text{READ}}$	12	9	13	Input	RD reading control signal for AD
RD1	13	10	14	In/Out	Receive signal digital data output from AD (LSB)
RD2	14	11	15	In/Out	Receive signal digital data output from AD
RD3	15	12	16	In/Out	Receive signal digital data output from AD
RD4	16	13	17	In/Out	Receive signal digital data output from AD
RD5	17	16	18	In/Out	Receive signal digital data output from AD
RD6	18	17	19	In/Out	Receive signal digital data output from AD
RD7	19	18	20	In/Out	Receive signal digital data output from AD
RD8	20	19	21	In/Out	Receive signal sigital data output from AD (MSB)
VDD2	21	20	22		Positive power supply (+5 V)
DG	22	22, 23	23, 24		Digital ground (0 V)
AG	23	24	25		Analog ground (0 V)
AGCC	24	25	26		External capacitor terminal for AGC
VR1	25	26	27	Input	External resistor terminal for reference voltage
VR2	26	29	28	Output	External resistor terminal for reference voltage
AIN	27	30	29	Input	Receive analog signal input
DT	28	31	30	Input	Dial tone detecting loop
PT	29	32	31	Input	DTMF signal transmitting loop
AOUT	30	33	32	Output	Transmit analog signal output
LT	31	35	33	Input	AC loop test
FT	32	36	34	Input	XIN enable (Filter test or External input)
GT	33	37	35	Input	Guard tone select (1800/550 Hz)
XIN	34	38	36	Input	External transmit analog signal input
SP	35	39	37	Input	DA output PAM width select
MODE	36	40	38	Input	Originate/Answer mode select
RFO	37	41	39	Output	Receive filter output
AGCI	38	44	40	Input	AGC circuit input
GR2	39	45	41	Output	External resistor terminal for Guard tone level
GR1	40	47	42	Input	External resistor terminal for Guard tone level
VSS	41	48	43		Negative power supply (-5 V)
VDD1	42	21,49	44		Positive power supply (+5 V)

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	VDD	Ta = 25°C with respect to AG or DG	-0.3 ~ +7	V
	VSS		+0.3 ~ -7	
Analog input voltage	VIA		VSS - 0.3 ~ VDD + 0.3	
Digital input voltage	VID		-0.3 ~ VDD + 0.3	
Operating temperature	T_{OP}	—	-40 ~ + 85	°C
Storage temperature	T_{STG}	—	-55 ~ +150	

2. Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	With Respect to AG or DG	4.75	5.00	5.25	V
	V_{SS}		-5.25	-5.00	-4.75	
	AG, DG	–	–	0	–	
Operating temperature	T_{OP}	–	0	–	70	°C
R_0	–	–	–	51	–	KΩ
R_1	–	Transformer Impedance (Hybrid) $\left[\frac{600\ \Omega}{600\ \Omega}\right]$: 600 Ω	–	600	–	Ω
R_2	–		–	600	–	
R_3	–		–	300	–	
R_4	–	–	–	51	–	KΩ
R_5	–		–	51	–	
R_6	–		–	51	–	
R_7	–		–	51	–	
R_8	–		10	33	–	
R_9	–		–	36	–	
R_{10}	–		–	100	–	
R_{11}	–		–	51	–	
R_{12}	–		–	51	–	
C_0	–	–	–	0.1	–	μF
C_1	–		–	2.2	–	
C_2	–		–	1	–	
C_3	–		–	0.1	–	
C_4	–		–	1	–	
C_5, C_7, C_9	–		–	10	–	
C_6, C_8	–		–	1	–	
$R_{13} \sim R_{20}$	–	–	–	20	–	KΩ
Reference Voltage	V_R	Adjusted by External Resistors	–	+2.50	–	V
Master Clock Frequency	F_{MCK}	–	3.6860	3.6864	3.6867	MHz
MCK Duty Cycle	D_{MCK}	50% to 50%	30	50	70	%
Digital Input Rise Time	T_R	$T_{D_1} \sim T_{D_8}$, $\overline{WRITE}$, $\overline{START}$, $\overline{READ}$, $R_{D_1} \sim R_{D_8}$, See Figure 1	0	–	50	nS
Digital Input Fall Time	T_F		0	–	50	nS

Parameter	Symbol	Condition	Min	Typ	Max	Unit
$\overline{\text{WRITE}}$ Period *1	T_{PW}	See Figure 2, 3	115	1/ 0.0072	143	μS
$\overline{\text{WRITE}}$ Width	T_{WW}		0.55	–	100	μS
$\overline{\text{START}}$ Period	T_{PS}		98.2	1/ 0.0072	143	μS
$\overline{\text{START}}$ Width	T_{WS}		1.1	–	79	μS
$\overline{\text{READ}}$ Width	T_{WR}		3.2	–	*	μS
$\overline{\text{START}} \rightarrow \overline{\text{READ}}$ Timing	T_{SR}		80	–	*	μS
$\overline{\text{READ}} \rightarrow \overline{\text{START}}$ Timing	T_{RS}		15	–	*	μS
Allowable XIN Input DC Offset Voltage	V_{OSXIN}	–	-100	–	+100	mV
Allowable AIN Input DC Offset Voltage	V_{OSAIN}	–	-100	–	+100	mV

* $T_{WR\ MAX} = T_{PS} - T_{SR} - T_{RS}$
$T_{SR\ MAX} = T_{PS} - T_{WR} - T_{RS}$
$T_{RS\ MAX} = T_{PS} - T_{WR} - T_{SR}$

3. Power Dissipation

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, V_R = +2.5 V, T_a = 0 ∼ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Positive Power Supply Current	I_{DD}	–	–	12	20	mA
Negative Power Supply Current	I_{SS}	–	–	11	20	mA

Note: $I_{DD} = I_{DD1}$ (V_{DD1} pin) + I_{DD2} (V_{DD2} pin).

4. Digital Interface

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, T_a = 0 ~ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Low Voltage	V_{IL}	–	–	–	0.6	V
Input High Voltage	V_{IH}	–	2.2	–	–	V
Output Low Voltage	V_{OL}	I_{OL} = 0.36 mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = 20 μA	2.4	–	–	V
Input Low Current	I_{IL}	$DG \leq V_{IN} \leq V_{IL}$	-10	–	10	μA
Input High Current	I_{IH}	$V_{IH} \leq V_{IN} \leq V_{DD}$	-10	–	10	μA
DA Data Set-up Time	T_{SD}	See Figure 3	0	–	–	μS
DA Data Hold Time	T_{HD}		1.1	–	–	μS
AGC Data Set-up Time	T_{SA}	See Figure 2	0	–	–	μS
AGC Data Hold Time	T_{HA}		2.2	–	–	μS
AD Data Output Delay Time	T_{D1}	Pull-up Resistor = 20 KΩ See Figure 2	0.4	–	3	μS
	T_{D2}		0.5	–	3	μS

5. ANALOG INTERFACE (VDD = +5V ± 5%, −5V ± 5%, Ta = 0~70°C)

Reference Voltage (VR2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reference Voltage	VR	R8 = Opened	1.03	1.16	1.30	V

Transmit Modem Signal Characteristics (XIN, AOUT)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Input Resistance		RXIN	XIN $f_{XIN} \leqq$ 5KHz		500			KΩ
Input Voltage		VXIN	XIN				5	V_{PP}
Output Voltage		VAOUT	RAOUT ≧ 20KΩ, CAOUT ≦ 100PF		5			V_{PP}
Load Resistance		RAOUT			20			KΩ
Load Capacitance		CAOUT					100	PF
DC Offset Voltage		VOST	AOUT, XIN = 0V		−500	0	+500	mV
*1 Absolute Voltage Gain	Bell 212A/ V.22/V.22bis	GT1	Originate	1200Hz, 0dBm	+0.5	+2.0	+3.5	dB
		GT2	Answer	2400Hz, 0dBm	+0.5	+2.0	+3.5	dB
	Tone Transmit	GT3	GT = 1, 1020Hz, 0dBm		+0.5	+2.0	+3.5	dB
Gain Tracking		TGT1	GT1 − GT2		−1.0	0	+1.0	dB
*2 Idle Channel Noise	Bell 212A/ V.22/V.22bis	NIDLT1	Originate	0.3~ 3.4KHz		−60/ −55	−55/ −50	dBm
		NIDLT2	Answer			−56/ −50	−50/ −45	dBm
		NIDLT3	Originate	1.8~ 3KHz		−76/ −74	−65/ −65	dBm
		NIDLT4	Answer	0.6~ 1.8KHz		−73/ −71	−65/ −65	dBm
	Tone Transmit	NIDLT5	GT = 1	0.3~ 3.4KHz		−71/ −70	−60/ −60	dBm

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Clock Noise		NCLKT	All modes, at 57.6KHz				– 50	dBm
Total Harmonic Distor-tion	Bell 212A/ V.22/V.22bis	THDT1	Originate	1200Hz, 0dBm		– 55	– 50	dB
		THDT2	Answer	2400Hz, 0dBm		– 48	– 43	dB
	Tone Transmit	THDT3	GT = 1, 1020Hz, 0dBm			– 60	– 55	dB

*1 GT = 20 log (VAOUT/VXIN)

*2 Idle Channel Noise is defined with no weighted filter.

① / ②	①; $\overline{\text{WRITE}}$ = 7.2KHz, ②; $\overline{\text{WRITE}}$ = 8.4KHz

Note) 0dBm = 0.775Vrms

Guard Tone (AOUT)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Tone Frequency	FGT1	GT = 0	530	553.8	570	Hz
	FGT2	GT = 1	1780	1800	1820	Hz
Tone Amplitude	VGT1	GT = 0, R11 = Opened	– 13.5	– 15.0	– 16.5	dBm
	VGT2	GT = 1, R11 = Opened	– 13.0	– 14.5	– 16.0	dBm
Total Harmonic Distortion (2nd and 3rd) *	THDGT1	GT = 0, VGT1 = – 4dBm		– 63	– 57	dB
	THDGT2	GT = 1, VGT2 = – 4dBm		– 51	– 45	dB

* Harmonics above 3rd harmonic are negligible.

Receive Modem Signal Characteristics (AIN, RFO)

Parameter		Symbol	Condition		Min	Typ	Max	Unit
Input Resistance		RAIN	AIN $f_{XIN} \leqq 5KHz$		500			KΩ
Input Voltage Swing		VAIN	AIN				5	V_{PP}
Output Voltage		VRFO	RRFO ≧ 20KΩ, CRFO ≦ 100PF		5			V_{PP}
Load Resistance		RRFO	RFO		20			KΩ
Load Capacitance		CRFO	RFO				100	PF
DC Offset Voltage		VOSR	RFO		− 500	0	+ 500	mV
*1 Absolute Voltage Gain	Bell 212A/ V.22/V.22bis	GR1	Answer	1200Hz, 3dBm	− 1.5	0	+ 1.5	dB
		GR2	Originate	2400Hz, 3dBm	− 1.5	0	+ 1.5	dB
	Tone Receive	GR3	GT = 0, 300Hz, 3dBm		− 1.5	0	+ 1.5	dB
Gain Tracking		TGR	GR1-GR2		− 1.0	0	+ 1.0	dB
*2 Idle Channel Noise	Bell 212A/ V.22/V.22bis	NIDLR1	Answer	0.3~ 3.4KHz		− 63/ − 60	− 57/ − 55	dBm
		NIDLR2	Originate			− 63/ − 60	− 57/ − 55	dBm
	Tone Receive	NIDLR3	GT = 0			− 75/ − 73	− 60/ − 60	dBm
Clock Noise		NCLKR1	All modes, at 57.6KHz				− 45	dBm
		NCLKR2	GT = 0, at N × 14.4KHz				− 35	dBm
Total Harmonic Distor- tion	Bell 212A/ V.22/V.22bis	THDR1	Answer	1200Hz, + 3dBm		− 47	− 43	dB
		THDR2	Originate	2400Hz, + 3dBm		− 41	− 37	dB
		THDR3	Originate	1200Hz, 0dBm		− 58	− 53	dB
	Tone Receive	THDR4	GT = 0, 300Hz, + 3dBm			− 53	− 49	dB

*1 GR = 20 log (VRFO/VAIN)

*2 Idle Channel Noise is defined with no weighted filter.

① / ② ①; $\overline{WRITE}$ = 7.2KHz, ②; $\overline{WRITE}$ = 8.4KHz

6. Filter Transfer Characteristics

Low-band BPF

(V_{DD} = +5 V ±5%, V_{SS} = -5 V ±5%, V_R = +2.5 V, T_a = 0 ∿ 70°C)

Relative Voltage Gain to G_{FL_4}	G_{FL_1}	508 Hz	–	-44	-40	dB
	G_{FL_2}	555 Hz	–	-60	-45	dB
	G_{FL_3}	898 Hz	-1.5	–	+1.5	dB
	G_{FL_4}	1,008 Hz	Referred Gain 0			dB
	G_{FL_5}	1,148 Hz	-1.5	–	+1.5	dB
	G_{FL_6}	1,352 Hz	-1.5	–	+1.5	dB
	G_{FL_7}	1,508 Hz	-2	–	+1	dB
	G_{FL_8}	1,805 Hz	–	-65	-45	dB
	G_{FL_9}	2400 Hz	–	-55	-50	dB
Group Delay Distortion	G_{DL}	900 ~ 1,500 Hz	–	–	100	μS

High-band BPF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Relative Voltage Gain to G_{FH_4}	G_{FH_1}	1,195 Hz	–	-55	-50	dB
	G_{FH_2}	1,641 Hz	–	-55	-50	dB
	G_{FH_3}	2,055 Hz	-1.5	–	+1.5	dB
	G_{FH_4}	2,195 Hz	Referred Gain 0			dB
	G_{FH_5}	2,398 Hz	-1.5	–	+1.5	dB
	G_{FH_6}	2,602 Hz	-1.5	–	+1.5	dB
	G_{FH_7}	2,742 Hz	-0.5	–	+2.5	dB
	G_{FH_8}	3,211 Hz	–	-43	-38	dB
	G_{FH_9}	3,398 Hz	–	-35	-29	dB
Group Delay Distortion	G_{DH}	2,100 ~ 2,700 Hz	–	–	200	μS

Multi-purpose LPF

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Relative Voltage Gain to G_{FLF_2}	G_{FLF_1}	211 Hz	GT = 0	-1	0	+1	dB
	G_{FLF_2}	305 Hz		Referred Gain 0			dB
	G_{FLF_3}	727 Hz		-4	-3	-2	dB
	G_{FLF_4}	1,508 Hz		–	–	-30	dB
Relative Voltage Gain to G_{FHF_2}	G_{FHF_1}	211 Hz	GT = 1	-1	0	+1	dB
	G_{FHF_2}	305 Hz		Referred Gain 0			dB
	G_{FHF_3}	2,906 Hz		-4	-3	-2	dB
	G_{FHF_4}	3,898 Hz		–	–	-10	dB

7. AGC Circuit and DA, AD Converters

(V_{DD} = +5 V ±5%, V_{SS} = −5 V ±5%, V_R = +2.5 V, T_a = 0 ∿ 70°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
AGC Amplifier						
Input Resistance	R_{AGCI}	–	–	1	–	MΩ
Variable Voltage Gain Range	G_{AGC}	–	-4	–	+43.8	dB
Voltage Gain Accuracy	G_E	–	-0.4	+0.03 ~ -0.17	+0.4	dB
Output DC Offset Voltage	V_{OSAGC}	AGC1 = 0 V	-60 (-3)	–	+60 (+3)	mV (LSB)
Transmit Digital to Analog Converter						
Bits of Resolution	B_{REST}	–	–	8	–	bit
End-point Linearity	NL_{DA}	–	–	0.36	0.5	%
Differential Non-linearity	DNL_{DA}	–	–	1/5	1/2	LSB
Full Scale – Plus Full Scale	PFV_{DA}	–	–	+2,481	–	mV
Full Scale – Minus Full Scale	NFV_{DA}	–	–	-2,500	–	mV
DC Offset Voltage	V_{OSDA}	–	-10	-1.5	+10	mV
Receive Analog to Digital Converter						
Bits of Resolution	B_{RESR}	–	–	8	–	bit
End-point Linearity	NL_{AD}	–	–	0.24	0.5	%
Differential Non-linearity	DNL_{AD}	–	–	1/5	1/2	LSB
Full Scale – Plus Full Scale	PFV_{AD}	–	–	+2,481	–	mV
Full Scale – Minus Full Scale	NFV_{AD}	–	–	-2,500	–	mV
DC Offset Voltage*	V_{OSAD}	–	-1/2	–	+1/2	LSB

* This specification does not include the DC offset voltage at the input of the AD converter.

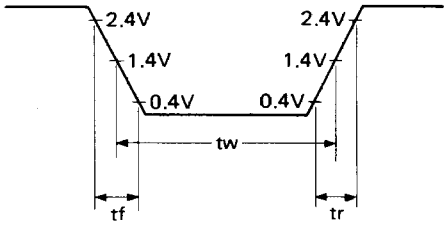


Figure 1 Definition of Rise/Fall Time

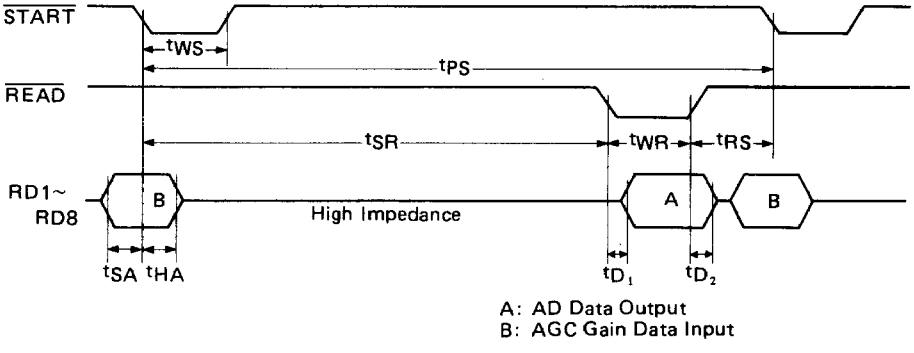


Figure 2 Receive Data Timing Chart

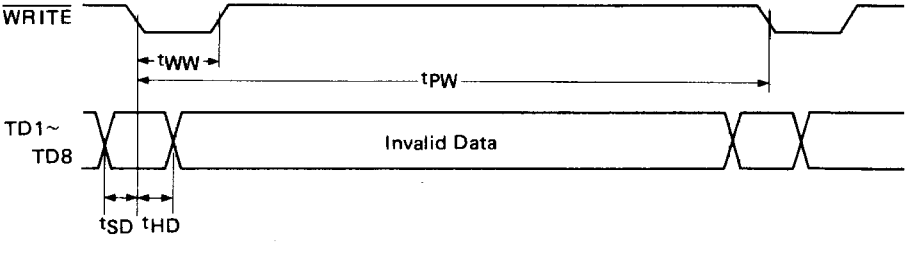


Figure 3 Transmit Data Timing Chart

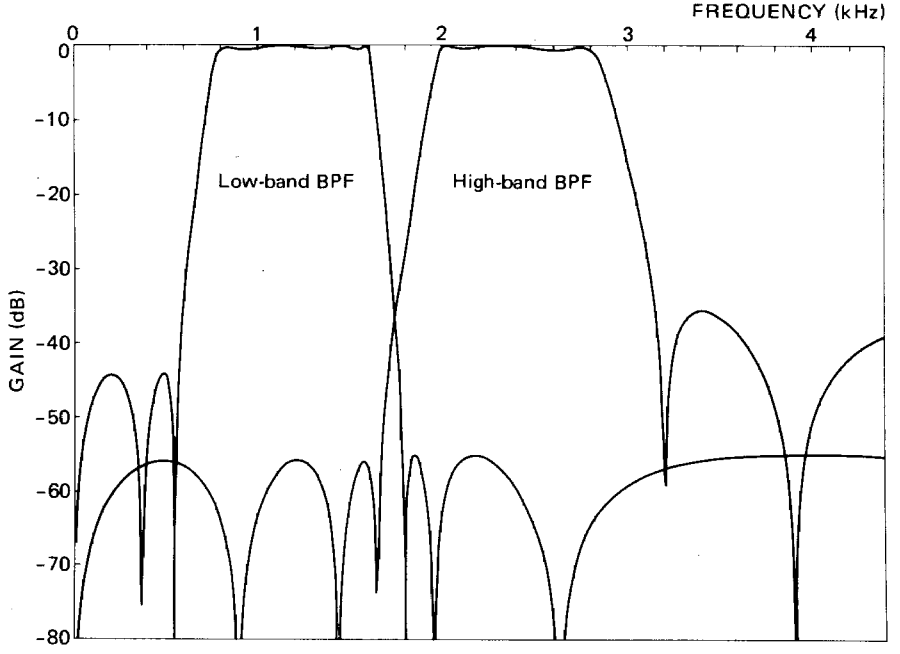


Figure 4 Low/High – band BPF FREQUENCY CHARACTERISTICS

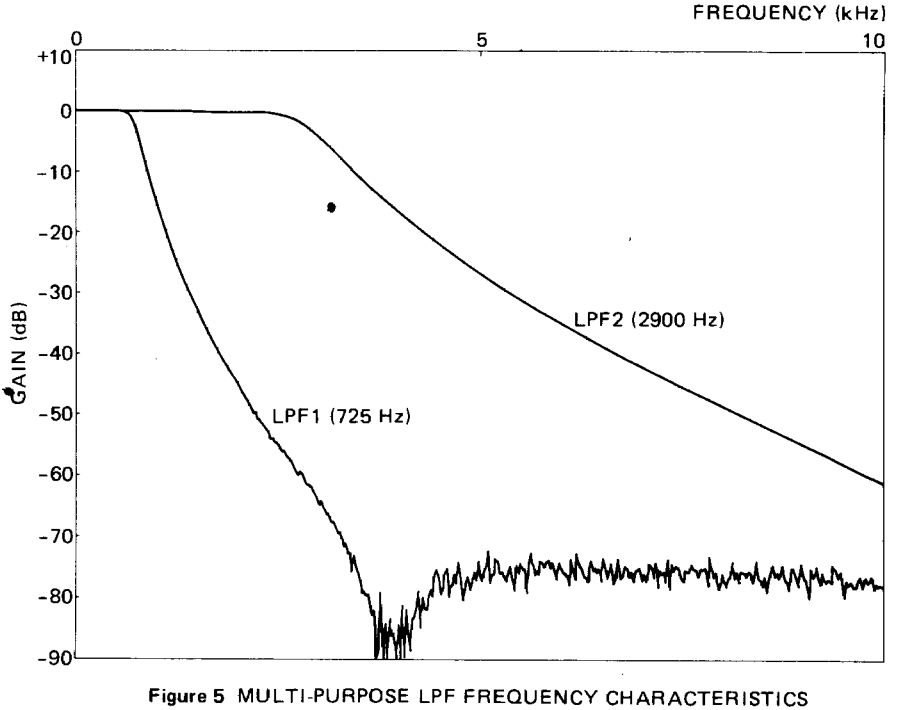
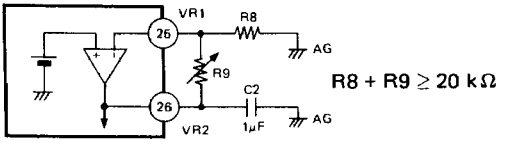


Figure 5 MULTI-PURPOSE LPF FREQUENCY CHARACTERISTICS

PIN DESCRIPTION

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th><th>JS</th></tr>
<tr><td>TD1 ~ TD8</td><td>1∿8</td><td>3∿5,
51∿
55</td><td>2∿9</td><td>Transmit signal digital data input for DA conversion. These pins are 8 bit parallel two's complement data input pins. The data is loaded to the DA converter at the falling edge of $\overline{\text{WRITE}}$. TD1 is the LSB and TD8 is the MSB. Refer to Table 1 below.
<table>
<tr><th>TD</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>Total Value</th><th>Nominal Output Voltage*</th></tr>
<tr><td>Plus Full Scale</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+127</td><td>+2,172.1 mV</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>+126
~ 1</td><td></td></tr>
<tr><td>Plus 0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Minus 0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-1</td><td>-17.1 mV</td></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>-2
~ 127</td><td></td></tr>
<tr><td>Minus Full Scale</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-128</td><td>-2,189.2 mV</td></tr>
</table>
Table 1 *The reference voltage for DA conversion is +2.5 V. This output voltage is defined at A_{OUT}.</td></tr>
<tr><td>$\overline{\text{WRITE}}$</td><td>9</td><td>6</td><td>10</td><td>This signal enables TD1 ~ TD8 pins to write data into DA converter.
The digital input from TD1 ~ TD8 is latched to the DA converter at the falling edge of $\overline{\text{WRITE}}$ signal, and then converted to analog signal.
The analog output signal is renewed about 9 μsec after the falling edge of $\overline{\text{WRITE}}$ signal. The cycle of this signal can be chosen out of 115 μsec ~ 143 μsec.</td></tr>
<tr><td>MCK</td><td>10</td><td>7</td><td>11</td><td>A 3.6864 MHz clock signal should be applied to this pin. This is the time base for the operation of the MSM6950B.</td></tr>
<tr><td>$\overline{\text{START}}$</td><td>11</td><td>8</td><td>12</td><td>This signal enables MSM6950B to start the AD conversion. This signal is also used to latch the input data used for setting the amplitude of the AGC circuit. The input data is supplied from a demodulating chip, the general performance of which is digital signal processing.
These two operations are performed at the falling edge of $\overline{\text{START}}$.
The cycle of this signal can be chosen out of 98 μsec ~ 143 μsec.</td></tr>
<tr><td>$\overline{\text{READ}}$</td><td>12</td><td>9</td><td>13</td><td>This is a control signal for 3-state output data bus line, RD1 ~ RD8. While this pin is at digital 0 state, the output bus is activated and the result of the AD conversion is output from RD1 ~ RD8 terminals.
While this pin is at digital 1 state, the output bus is inactivated and RD1 ~ RD8 become input terminals.</td></tr>
</table>

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th><th>JS</th></tr>
<tr><td>RD1 ~ RD8</td><td>13~20</td><td>10~23, 16~19</td><td>14~21</td><td>These are I/O terminals controlled by $\overline{START}$ and $\overline{READ}$ terminals.
When $\overline{READ}$ is set at digital 0 state, RD1 ~ RD8 become output terminals and the AD conversion result is output from these pins with 8 bit parallel two's compliment format. Refer to Table 2.
When $\overline{READ}$ is set at digital 1 state, RD1 ~ RD8 become input terminals. The data input to these pins is loaded into the registers at the falling edge of $\overline{START}$ signal. In this case, this data is used at the gain setting data for AGC circuit.
Nominal absolute voltage gain of AGC circuit is described in Table 3. The dynamic range of the AGC circuit is about 48 dB as shown in Table 3.
$\overline{READ}$ = Digital 0
<table>
<tr><th>RD8</th><th>RD7</th><th>RD6</th><th>RD5</th><th>RD4</th><th>RD3</th><th>RD2</th><th>RD1</th><th>Nominal Corresponding Voltage on the Input of AGC Circuit (AGCI)</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+2,480.5 mV</td></tr>
<tr><td colspan="8">⋮</td><td>~ 19.5 mV Step</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>+19.5 mV</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>-19.5 mV</td></tr>
<tr><td colspan="8">⋮</td><td>~ 19.5 mV Step</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-2,500 mV</td></tr>
</table>
Table 2
$\overline{READ}$ = Digital 1
<table>
<tr><th>RD8</th><th>RD7</th><th>RD6</th><th>RD5</th><th>RD4</th><th>RD3</th><th>RD2</th><th>RD1</th><th>Nominal Absolute Voltage Gain of AGC Circuit (dB)</th></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+43.8</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>+43.6</td></tr>
<tr><td colspan="8">⋮</td><td>0.1875 dB Step</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-3.63</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-3.81</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-4.00</td></tr>
</table>
Table 3</td></tr>
<tr><td>V_{DD_2}</td><td>21</td><td>20</td><td>22</td><td>Positive power supply, +5 V.
This power supply is internally connected to the digital output logical circuitry RD1 ~ RD8 to avoid the deterioration to the noise performance. Same power supply as to V_{DD_1} should be used.</td></tr>
<tr><td>DG</td><td>22</td><td>22, 23</td><td>23, 24</td><td>Digital ground, 0 V.</td></tr>
<tr><td>AG</td><td>23</td><td>24</td><td>25</td><td>Analog ground, 0 V.</td></tr>
<tr><td>AGCC</td><td>24</td><td>25</td><td>26</td><td>An external capacitor of 1 μF should be connected between AGCC and AG. This capacitor is necessary to compensate the DC offset voltage generated in the AGC circuit.</td></tr>
</table>

Pin Name	Pin No. RS	GS	JS	Function
VR1, VR2	25, 26	26, 29	27, 28	The MSM6950B provides the voltage reference which is used for AD and DA convertions. The electrical potential is stabilized to variations of temperature or supply voltages, but tends to be different from chip to chip. Therefore, an external adjustment is necessary. The resistors used to adjust the reference voltage are connected to these pins as shown in Figure 6.  **Figure 6** (MSM6950BRS) A bypass capacitor is required to keep this reference electrical in the silent condition. A capacitor with the value of 1 μF is recommended. The reference voltage on VR2 is determined by the following equation and the typical value is +2.5 V. $V_{REF} = 1.2 \times \frac{R_8 + R_9}{R_8}$ [volts]
AIN	27	30	29	Receive analog signal input pin. The maximum input level is about +7.2 dBm (5 Vp-p).
DT, PT	28, 29	31, 32	30, 31	These pins control the transmit and receive analog signal paths for AC loop test, DTMF tone, guard tone and call progress tone. For details, refer to Table 8.
AOUT	30	33	32	This is the transmit analog signal output terminal. The output resistance is about 10 Ω and the load resistance should be more than 20 kΩ. The higher the road resistor is, the lower the power dissipation of MSM6950B becomes. When the full scale digital data is input to DA, the output voltage on AOUT becomes as follows. **Table 4**

Input Data to DA	Reference Voltage	Output Voltage (AOUT)
Plus Full Scale	+2.5 V	+2.17 V
Minus Full Scale		-2.19 V

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th><th>JS</th></tr>
<tr><td>LT</td><td>31</td><td>35</td><td>33</td><td>LT is used to provide the local AC loop test function.
When digital 1 is input to LT, the transmit analog signal bypasses the transmit analog filter and is directly routed to the receive analog filter. At this time, the transmit analog signal must be of the same channel with the receiver. The passband of the receive analog filter is selected by LT and MODE as shown in Table 5.

<table>
<tr><th>LT</th><th>MODE</th><th>Receive BPF's Passband</th><th>AIN</th><th>AOUT</th></tr>
<tr><td rowspan="2">1</td><td>0</td><td>2,000 ~ 2,800 Hz</td><td rowspan="2">Open</td><td rowspan="2">Shorted to AG (0V)</td></tr>
<tr><td>1</td><td>800 ~ 1,600 Hz</td></tr>
<tr><td>0</td><td>*</td><td colspan="3">Normal Operating State</td></tr>
</table>
Table 5</td></tr>
<tr><td>FT</td><td>32</td><td>36</td><td>34</td><td>FT controls the external transmit signal to be input to the MSM6950B and to send it over telephone line through the AOUT terminal. When FT is in digital 1 state, XIN is connected to the transmit filter input and external analog tones, such as DTMF tone, can be input to the MSM6950B through the XIN terminal.
When digital 0 is applied to FT, the output signal from DA converter is routed to the transmit filter input. This is the normal application for the MSM6950B.</td></tr>
<tr><td>GT</td><td>33</td><td>37</td><td>35</td><td>GT controls the signal to select the frequency of the guard tone and this is a necessary function to be used internationally.
At the same time, the passband width of LPF is decided according to the frequency.

<table>
<tr><th>GT</th><th>Guard Tone Frequency</th><th>LPF's Passband</th></tr>
<tr><td>0</td><td>550 Hz</td><td>0 ~ 725 Hz</td></tr>
<tr><td>1</td><td>1,800 Hz</td><td>0 ~ 2,900 Hz</td></tr>
</table>
Table 6

LPF plays a role of rejecting harmonic components from the originated guard tone. In addition to it, this LPF can be also used in the receiver as the band limiting filter during call progress tone detection.</td></tr>
<tr><td>XIN</td><td>34</td><td>38</td><td>36</td><td>XIN is an external analog signal input. As described in the paragraph for FT, XIN is activated when FT is in digital 1 state. The maximum input level is about +7.2 dBm (5 Vp-p).</td></tr>
</table>

<table>
<tr><th rowspan="2">Pin Name</th><th colspan="3">Pin No.</th><th rowspan="2">Function</th></tr>
<tr><th>RS</th><th>GS</th><th>JS</th></tr>
<tr><td>SP</td><td>35</td><td>39</td><td>37</td><td>SP should be connected to digital 0 for the actual applications.</td></tr>
<tr><td>MODE</td><td>36</td><td>40</td><td>38</td><td>MODE determines the role of each BPF by controlling SWT and SWR as shown in the circuit configuration.
When digital 0 is applied to this pin, the low channel BPF is assigned to the transmitter and the high channel BPF is assigned to the receiver. This condition is called as "Originate mode". When digital 1 is input to MODE, the positions of BPFs are reversed and this is called as "Answer mode".
During the AC loop back test, the frequency band used for this test becomes the receiver's channel determind by MODE.

<table>
<tr><th>MODE</th><th>Mode</th><th>Transmit Filter</th><th>Receive Filter</th></tr>
<tr><td>0</td><td>Originate</td><td>L · BPF (800 ~ 1,600 Hz)</td><td>H · BPF (2,000 ~ 2,800 Hz)</td></tr>
<tr><td>1</td><td>Answer</td><td>H · BPF (2,000 ~ 2,800 Hz)</td><td>L · BPF (800 ~ 1,600 Hz)</td></tr>
</table>
Table 7</td></tr>
<tr><td>RFO</td><td>37</td><td>41</td><td>39</td><td>RFO is the analog signal output of the receive filter.
This signal is to be connected to the AGC circuit through an external capacitor of 0.1 μF. The load resistance should be more than 20 kΩ. The maximum voltage swing is about 5 Vp-p.</td></tr>
<tr><td>AGCI</td><td>38</td><td>44</td><td>40</td><td>AGCI is the input pin of the AGC circuit and is connected to RFO through an external capacitor as shown in Figure 7. The role of the capacitor is to avoid a bad influence for the DC offset voltage generated in the receive filter. The input resistance is high and the maximum input voltage swing is about 5 Vp-p.

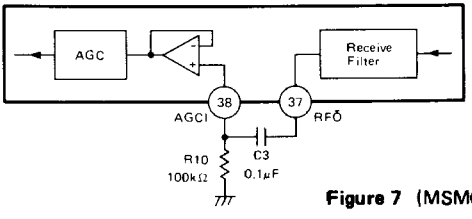
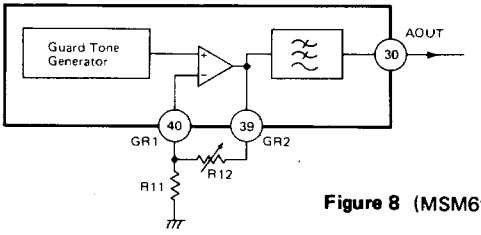
 

Figure 7 (MSM6950BRS)</td></tr>
</table>

Pin Name	Pin No. RS	GS	JS	Function
GR2, GR1	39, 40	45, 47	41, 42	The output guard tone level can be adjusted by using external resistors as shown in Figure 8.  **Figure 8** (MSM6950BRS) The approximate output tone level is determined by the following equation. $$V_{AOUT} = 20 \cdot \log \frac{R_{11} + R_{12}}{R_{11}} - 15 \text{ [dBm]}$$ In Bell's standard sets, the guard tone function is not applied.
VSS	41	48	43	Negative power supply, -5 V.
V_{DD1}	42	21, 49	44	Positive power supply +5 V.

III

MSM6950BRS CIRCUIT WIRING ILLUSTRATION

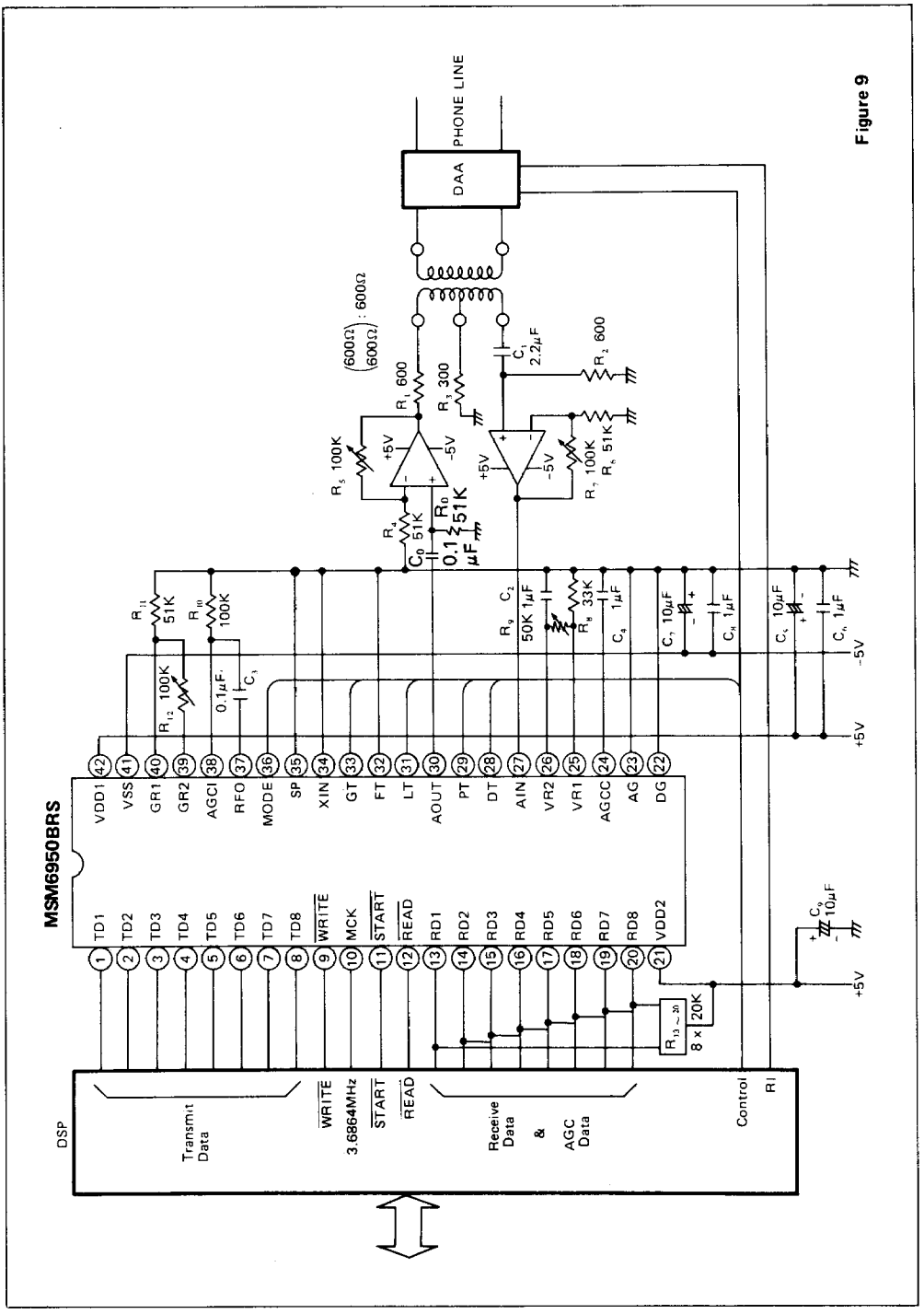


Figure 9

APPLICATION INFORMATIONS

1. Typical Master Clock (MCK) Frequency and $\overline{\text{WRITE}}$, $\overline{\text{START}}$, $\overline{\text{READ}}$ signals.

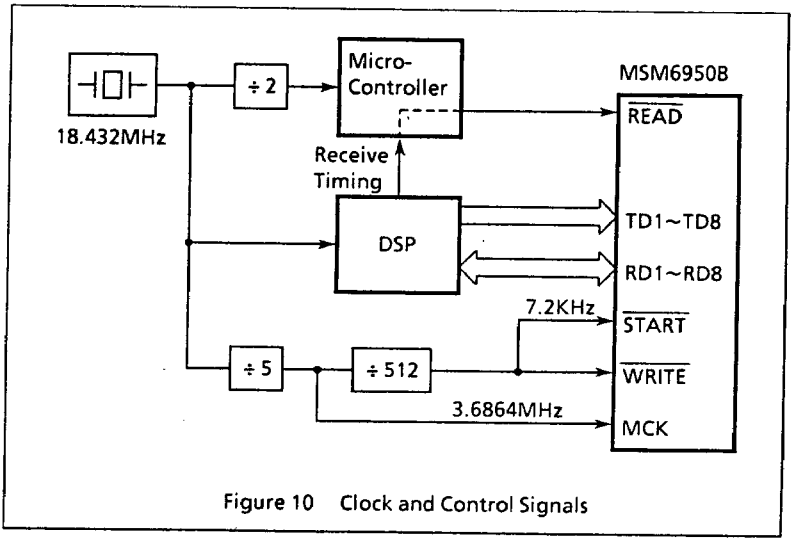


Figure 10 Clock and Control Signals

Figure 10 shows the typical design for the operating clock and control signals.

It is desirable to use one time base for the noise performance of the modem system.

2 Originate Transmission Mode

The signal pass in this mode is shown in Figure 11.

The low band signal must be transmitted and the high band signal must be received. MODE determines the positions of two BPFs by controlling SWT1, SWT2, SWR1 and SWR2. When MODE is in digital 0 state, the low channel BPF is assigned to the transmitter and the high channel BPF is assigned to the receiver. Both DT and PT should be in digital 1 state so that the guard tone function should be disabled.

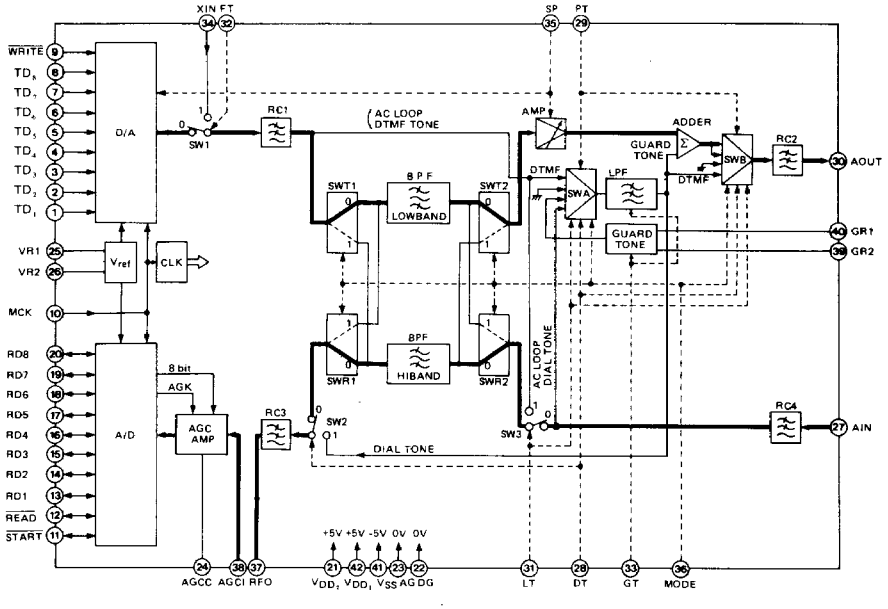


Figure 11 (MSM6950BRS)

3 Answer Transmission Mode

The signal pass in this mode is shown in Figure 12.

The high band signal must be transmitted and the low band signal must be received. When MODE is in digital 1 state, the high channel BPF is assigned to the transmitter and the low channel BPF is assigned to the receiver. In some applications, it is required to mix a guard tone to the high channel transmit signal in the answer mode. The control signals on DT, PT and GT determine the guard tone function. When DT and PT are in digital 1 state, the guard tone function is disabled and only the high channel transmitter is enabled. When DT, PT and GT are in digital 0 state, the guard tone, the frequency of which is 550 Hz, is mixed to the transmit signal.

When GT is changed to digital 1 keeping DT and PT in digital 0 state, another guard tone, the frequency of which is 1800 Hz, is mixed to the transmit signal.

The original guard tone is filtered through LPF and only its fundamental component is extracted and mixed to the transmit signal. The cut-off frequency of LPF is about 725 Hz while GT is in digital 0 state and becomes about 2900 Hz while GT is in digital 1 state.

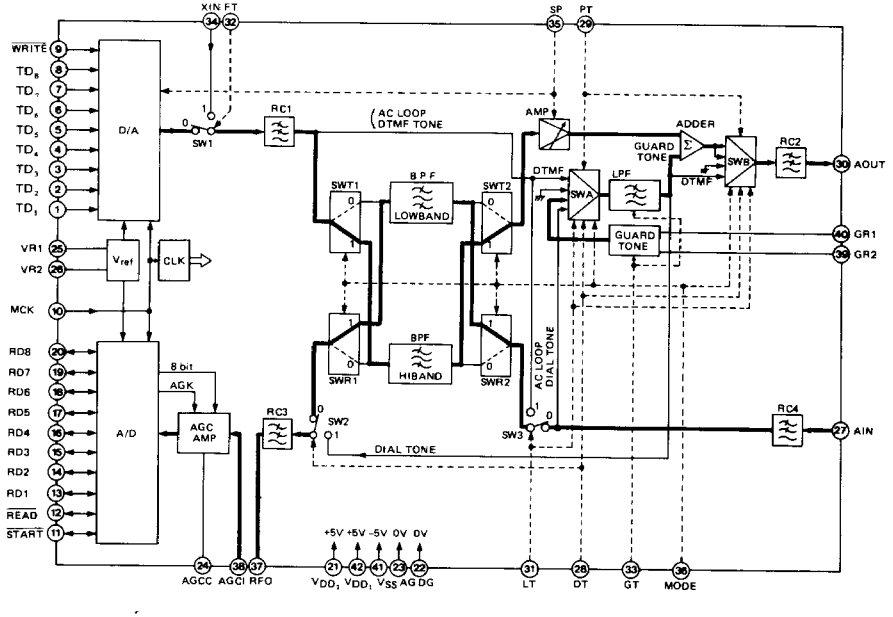


Figure 12 (MSM6950BRS)

4 Tone Transmit Mode

The signal path in this mode is shown in Figure 13.

LPF put on this path has two kinds of its cut-off frequency (725 Hz/2900 Hz). So, This mode is useful for DTMF signaling and so forth. Refer to Table 9.

When transmit signal is passed from DA converter to low cut-off frequency (725 Hz) LPF, AOUT signal level is changed less than ±2.5 dB by the timing of $\overline{\text{WRITE}}$ signal and internal clock.

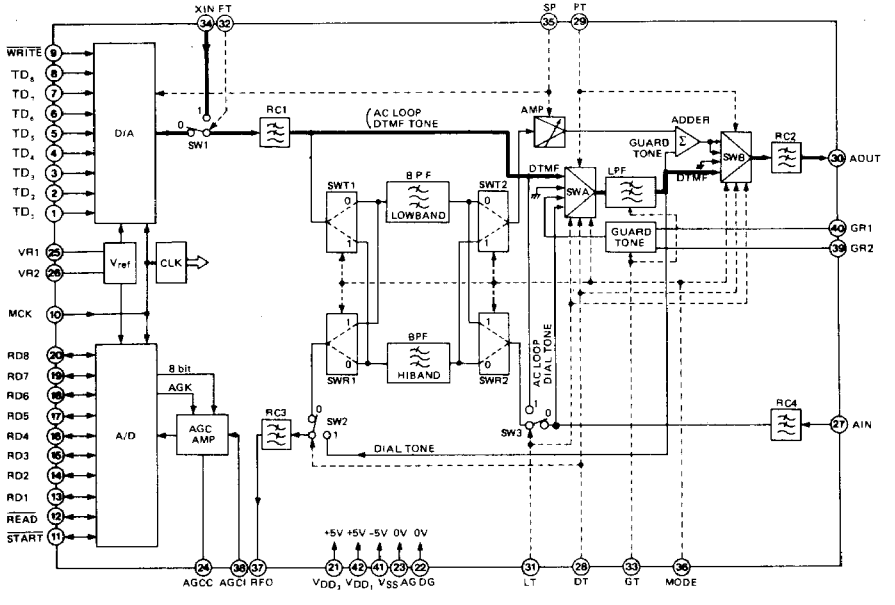


Figure 13 (MSM6950BRS)

5 Tone Receive Mode

The signal path in this mode is shown in Figure 14.

As LPF put on this path has two kinds of cut-off frequency – 725 Hz and 2900Hz. This mode is useful for call progress tone monitoring, such as for dial tone. Refer to Table 8. In this mode, AOUT is connected to AG (0 V) internally.

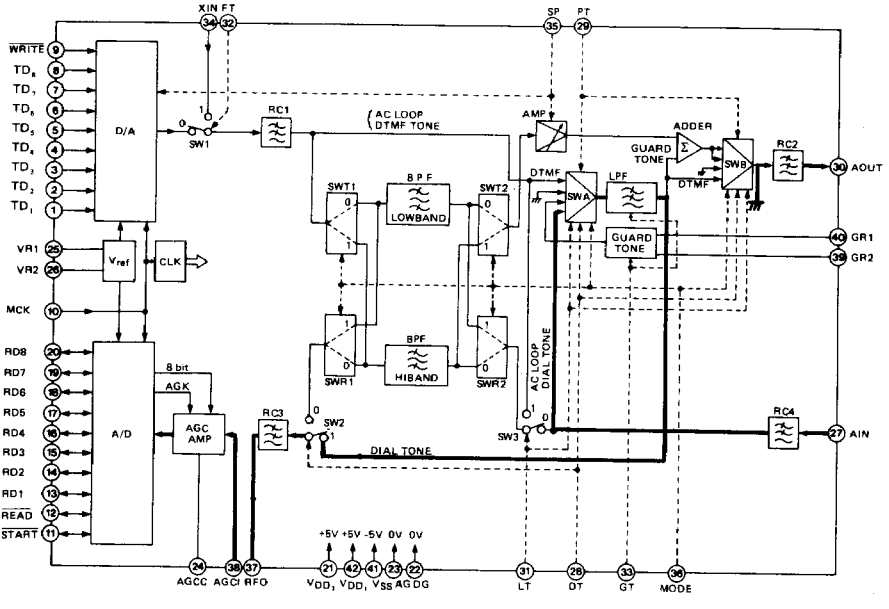


Figure 14 (MSM6950BRS)

6 AC Loop-back Test Mode

The signal path in this mode is shown in Figure 15.

The modem system has to receive its own transmit signal to check the modem operation.

In this mode, the transmit BPF is skipped from the signal route and the channel used for AC Loop-back test is determined by the reveiver's channel assigned by MODE. Refer to Table 8.

AOUT is connected to AG (0V) internally.

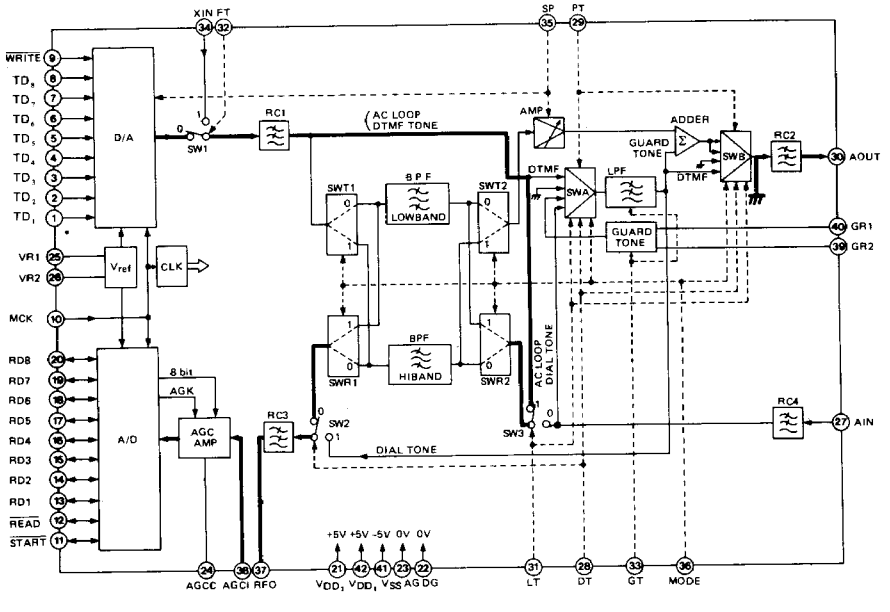


Figure 15 (MSM6950BRS)

Control Signal						Transmitter			Receiver		Note	
DT	PT	MODE	GT	SP	LT	Pass Band*1	Gain*1	Guard Tone	Pass Band*2	Gain*2		
1	1	0	X	0	0	800~1600Hz	+2.0dB		2000~2800Hz	0dB	Originate	FSK DPSK QAM
1	1	1	X	0	0	2000~2800Hz	+2.0dB		800~1600Hz	0dB	Answer	
0	0	1	0	0	0	2000~2800Hz	+2.0dB	550Hz	800~1600Hz	0dB	Answer with Guard Tone	
0	0	1	1	0	0	2000~2800Hz	+2.0dB	1800Hz	800~1600Hz	0dB		
0	1	0	0	0	0	0~ 725Hz	+1.0dB		2000~2800Hz	0dB	Extra Tone/DTMF Tone Transmitting	
0	1	1	0	0	0	0~ 725Hz	+1.0dB		800~1600Hz	0dB		
0	1	0	1	0	0	0~2900Hz	+2.0dB		2000~2800Hz	0dB		
0	1	1	1	0	0	0~2900Hz	+2.0dB		800~1600Hz	0dB		
1	0	X	0	X	0	*3			0~ 725Hz	-1.0dB	Filtering for Call Progress Tone	
1	0	X	1	X	0	*3			0~2900Hz	0dB		
1	1	0	X	0	1	*3			2000~2800Hz	0dB	AC Loop-back Test	FSK DPSK QAM
0	0	0	X	0	1	*3			2000~2800Hz	0dB		
1	1	1	X	0	1	*3			800~1600Hz	0dB		
0	0	1	X	0	1	*3			800~1600Hz	0dB		

*1 XIN → AOUT
*2 AIN → RFO
*3 AOUT is connected to Ground.

Table 8 Various Operating Modes