# Advanced Power MOSFET

# IRLS530A

## FEATURES

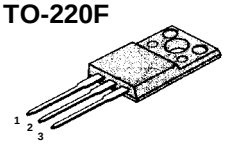
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10μA (Max.) @ $V_{DS}$ = 100V
- Lower $R_{DS(ON)}$ : 0.101Ω (Typ.)

$BV_{DSS}$ = 100 V

$R_{DS(on)}$ = 0.12Ω

$I_D$ = 10.7 A

**TO-220F**




**1.Gate 2. Drain 3. Source**

## Absolute Maximum Ratings

| Symbol | Characteristic | Value | Units |
|---|---|---|---|
| $V_{DSS}$ | Drain-to-Source Voltage | 100 | V |
| $I_D$ | Continuous Drain Current ($T_C$=25℃) | 10.7 | A |
| | Continuous Drain Current ($T_C$=100℃) | 7.5 | |
| $I_{DM}$ | Drain Current-Pulsed ① | 49 | A |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $E_{AS}$ | Single Pulsed Avalanche Energy ② | 228 | mJ |
| $I_{AR}$ | Avalanche Current ① | 10.7 | A |
| $E_{AR}$ | Repetitive Avalanche Energy ① | 3.6 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 6.5 | V/ns |
| $P_D$ | Total Power Dissipation ($T_C$=25℃) | 36 | W |
| | Linear Derating Factor | 0.24 | W/℃ |
| $T_J$ , $T_{STG}$ | Operating Junction and Storage Temperature Range | - 55 to +175 | ℃ |
| $T_L$ | Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds | 300 | |

## Thermal Resistance

| Symbol | Characteristic | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | -- | 4.2 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient | -- | 62.5 | |

## Electrical Characteristics ($T_C$=25℃ unless otherwise specified)

| Symbol | Characteristic | Min. | Typ. | Max. | Units | Test Condition |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | 100 | -- | -- | V | $V_{GS}$=0V,$I_D$=250μA |
| $\Delta BV/\Delta T_J$ | Breakdown Voltage Temp. Coeff. | -- | 0.1 | -- | V/℃ | $I_D$=250μA ***See Fig 7*** |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | -- | 2.0 | V | $V_{DS}$=$V_{GS}$, $I_D$=250μA |
| $I_{GSS}$ | Gate-Source Leakage , Forward | -- | -- | 100 | nA | $V_{GS}$=20V |
| | Gate-Source Leakage , Reverse | -- | -- | -100 | | $V_{GS}$=-20V |
| $I_{DSS}$ | Drain-to-Source Leakage Current | -- | -- | 10 | μA | $V_{DS}$=100V |
| | | -- | -- | 100 | | $V_{DS}$=80V,$T_C$=150℃ |
| $R_{DS(on)}$ | Static Drain-Source On-State Resistance | -- | -- | 0.12 | Ω | $V_{GS}$=5V,$I_D$=5.35A ④ |
| $g_{fs}$ | Forward Transconductance | -- | 10.2 | -- | S | $V_{DS}$=40V,$I_D$=5.35 ④ |
| $C_{iss}$ | Input Capacitance | -- | 580 | 755 | pF | $V_{GS}$=0V,$V_{DS}$=25V,f =1MHz ***See Fig 5*** |
| $C_{oss}$ | Output Capacitance | -- | 140 | 175 | | |
| $C_{rss}$ | Reverse Transfer Capacitance | -- | 60 | 75 | | |
| $t_{d(on)}$ | Turn-On Delay Time | -- | 10 | 30 | ns | $V_{DD}$=50V,$I_D$=14A, $R_G$=6Ω ***See Fig 13*** ④ ⑤ |
| $t_r$ | Rise Time | -- | 11 | 30 | | |
| $t_{d(off)}$ | Turn-Off Delay Time | -- | 29 | 70 | | |
| $t_f$ | Fall Time | -- | 15 | 40 | | |
| $Q_g$ | Total Gate Charge | -- | 16.9 | 24 | nC | $V_{DS}$=80V,$V_{GS}$=5V, $I_D$=14A ***See Fig 6 & Fig 12*** ④ ⑤ |
| $Q_{gs}$ | Gate-Source Charge | -- | 2.7 | -- | | |
| $Q_{gd}$ | Gate-Drain("Miller") Charge | -- | 9.7 | -- | | |

## Source-Drain Diode Ratings and Characteristics

| Symbol | Characteristic | Min. | Typ. | Max. | Units | Test Condition |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current | -- | -- | 14 | A | Integral reverse pn-diode in the MOSFET |
| $I_{SM}$ | Pulsed-Source Current ① | -- | -- | 49 | | |
| $V_{SD}$ | Diode Forward Voltage ④ | -- | -- | 1.5 | V | $T_J$=25℃,$I_S$=10.7A,$V_{GS}$=0V |
| $t_{rr}$ | Reverse Recovery Time | -- | 109 | -- | ns | $T_J$=25℃,$I_F$=14A di$_F$/dt=100A/μs ④ |
| $Q_{rr}$ | Reverse Recovery Charge | -- | 0.41 | -- | μC | |

**Notes ;**

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=3mH, $I_{AS}$=10.7A, $V_{DD}$=25V, $R_G$=27Ω, Starting $T_J$=25℃

③ $I_{SD}$≤14A, di/dt≤350A/μs, $V_{DD}$≤$BV_{DSS}$, Starting $T_J$=25℃

④ Pulse Test : Pulse Width = 250μs, Duty Cycle ≤ 2%

⑤ Essentially Independent of Operating Temperature

**Fig 1. Output Characteristics**

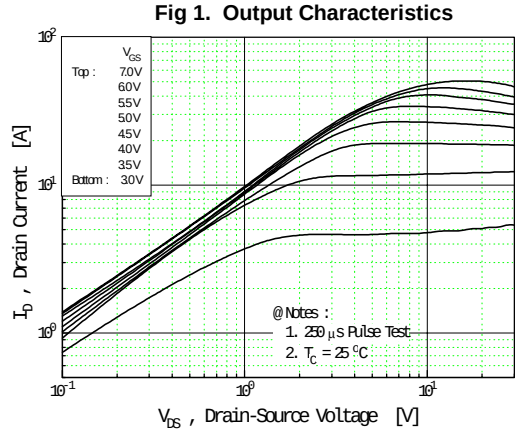



**Fig 2. Transfer Characteristics**

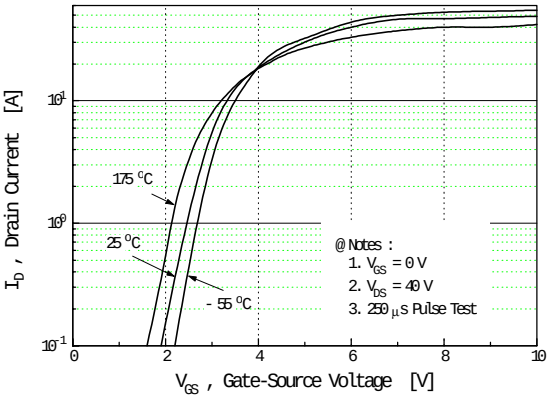



**Fig 3. On-Resistance vs. Drain Current**

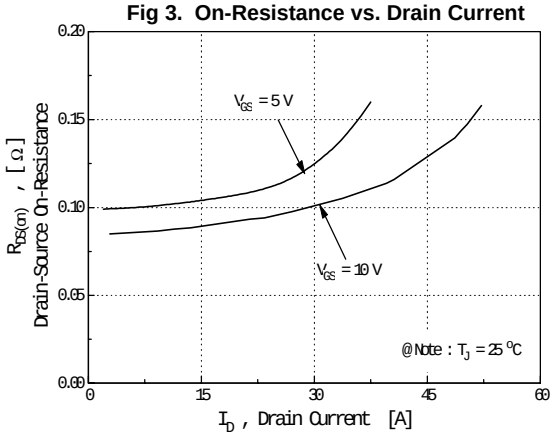



**Fig 4. Source-Drain Diode Forward Voltage**

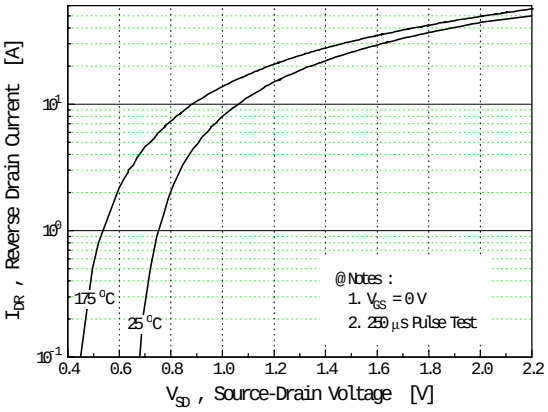



**Fig 5. Capacitance vs. Drain-Source Voltage**

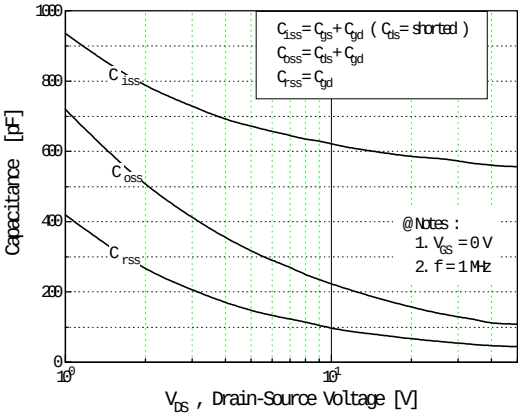



**Fig 6. Gate Charge vs. Gate-Source Voltage**

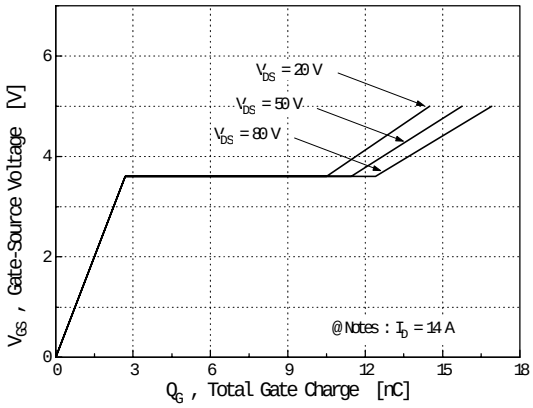


**Fig 7. Breakdown Voltage vs. Temperature**

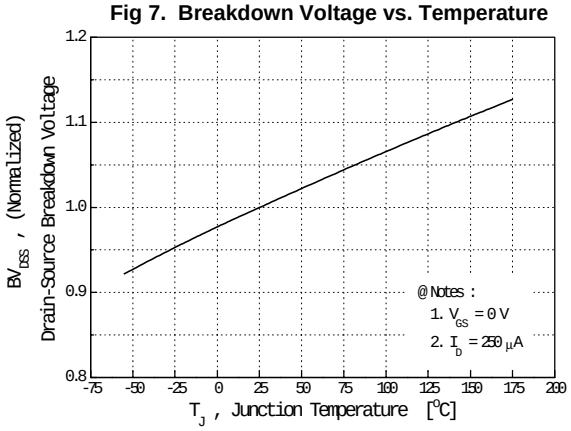



**Fig 8. On-Resistance vs. Temperature**

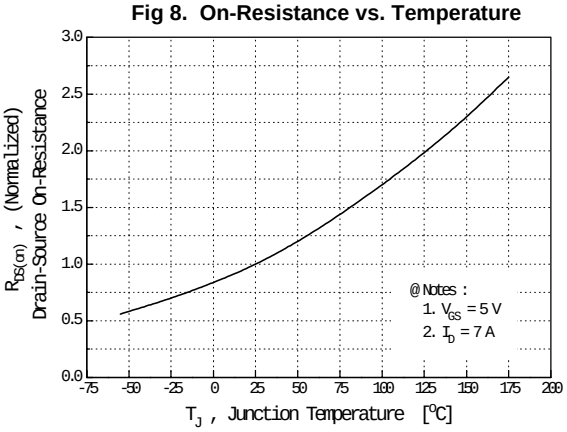



**Fig 9. Max. Safe Operating Area**

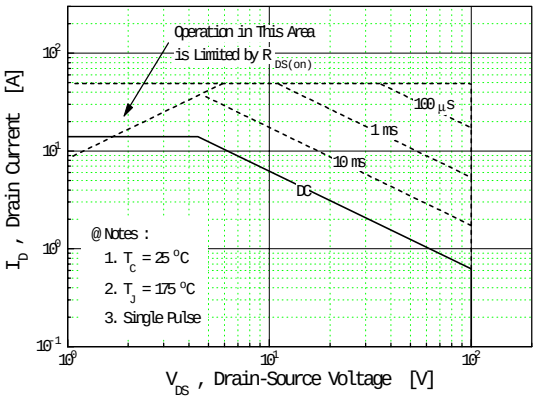



**Fig 10. Max. Drain Current vs. Case Temperature**

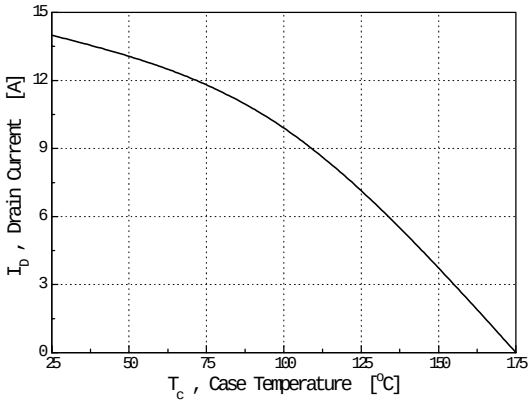



**Fig 11. Thermal Response**

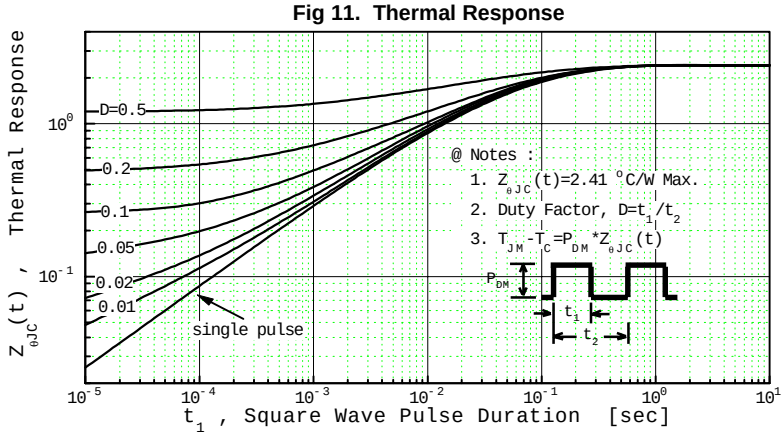


**Fig 12. Gate Charge Test Circuit & Waveform**

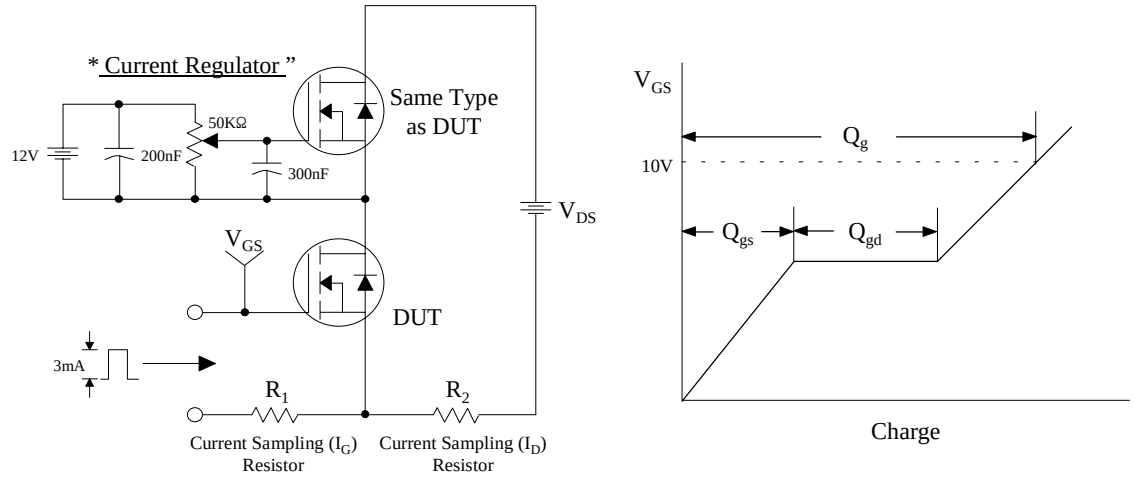



**Fig 13. Resistive Switching Test Circuit & Waveforms**

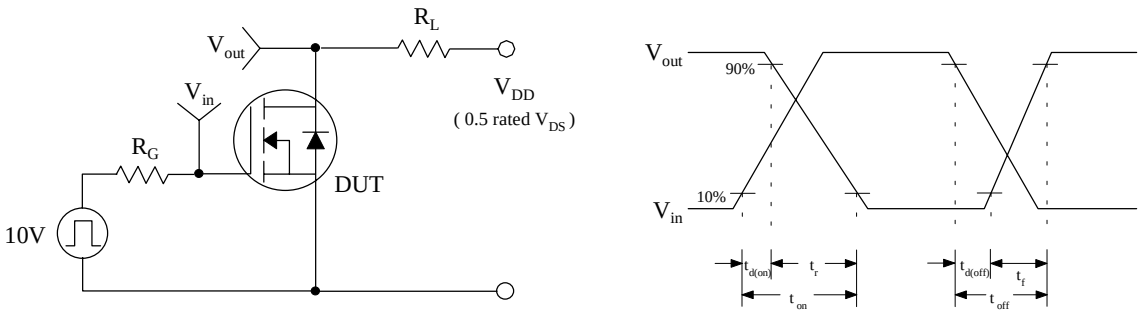



**Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms**

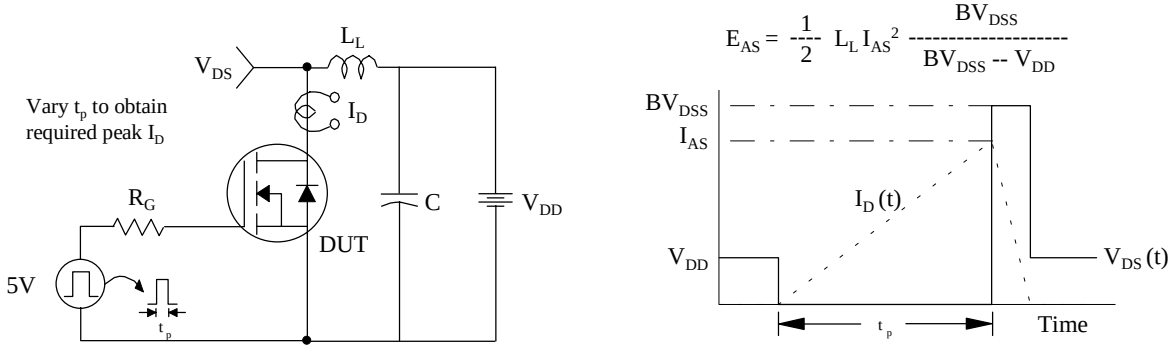
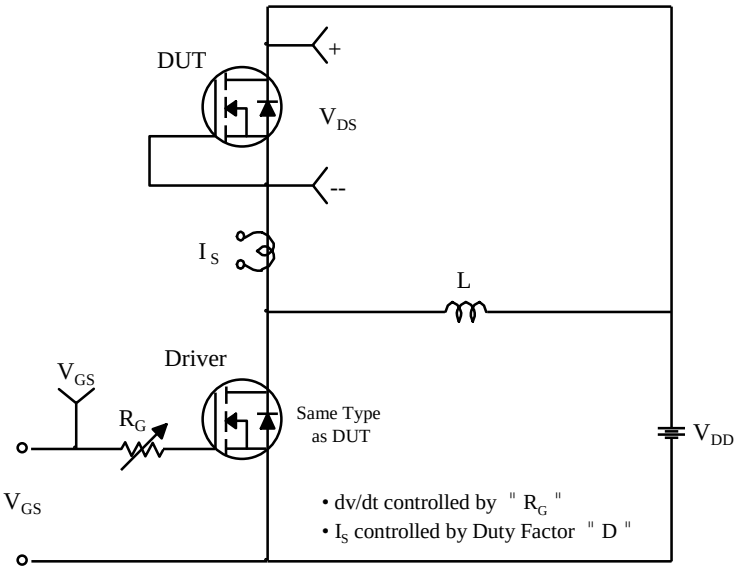
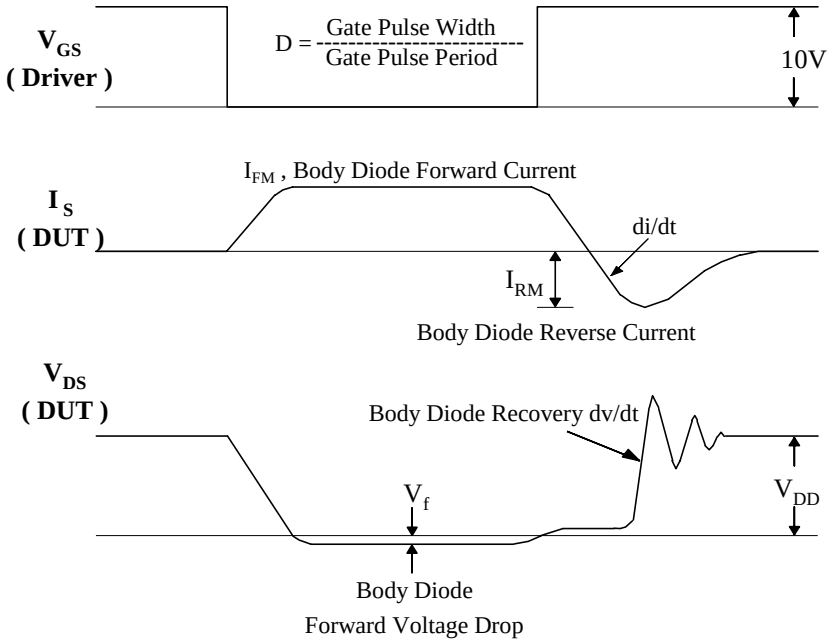


**Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms**



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