National Semiconductor

PRELIMINARY
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SCAN50C400
1.25/2.5/5.0 Gbps Quad Multi-rate Backplane Transceiver

General Description

The SCAN50C400 is a four-channel high-speed backplane transceiver (SERDES) designed to support multiple line data rates at 1.25, 2.5 or 5.0 Gbps over a printed circuit board backplane. It provides a data link of up to 20 Gbps total through-put in each direction.

Each transmit section of the SCAN50C400 takes a 4-bit differential LVDS source synchronous data bus, serializing it to a differential high-speed serial bit stream and output from a CML driver. The receive section of the SCAN50C400 consists of a differential input stage, a clock/data recovery PLL, a serial-to-parallel converter, and a LVDS output bus. De-emphasis at the high-speed driver outputs and a limiting amplifier circuit at the receiver inputs are used to reduce ISI distortions to enable error-free data transmission over more than 26 inches point-to-point link with a low cost FR4 backplane.

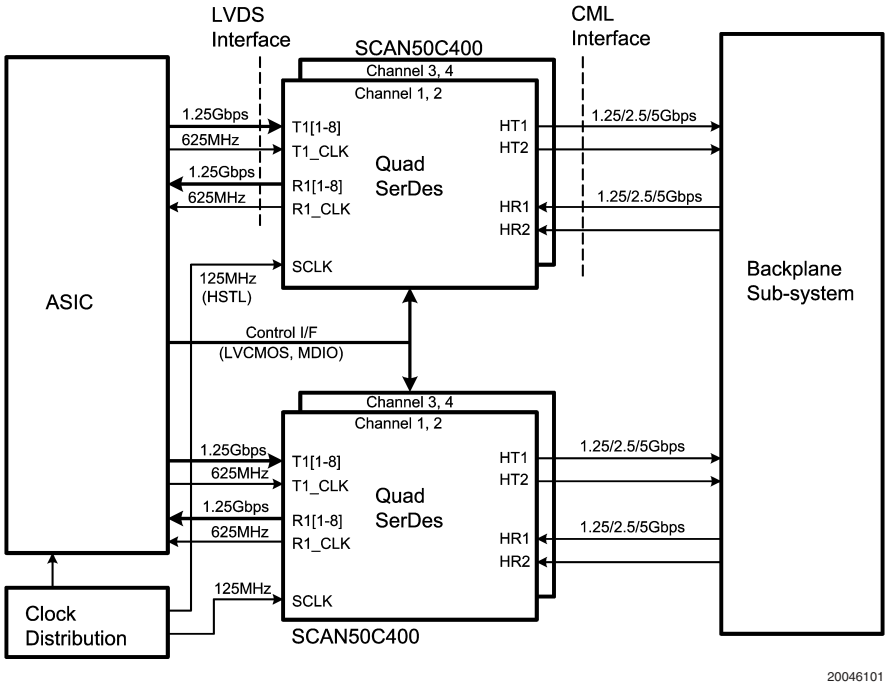
Internal low jitter PLLs are used to derive the high-speed serial clock from a differential reference clock source. Two channels share common transmit and receive LVDS clocks.

The SCAN50C400 has built-in self-test (BIST) circuitry and also loopback test modes to support at-speed self-testing.

Features

- Quad Backplane SERDES transceiver
- Multiple data rates at 1.25, 2.5 or 5 Gbps
- 40 Gbps total full duplex throughput
- Better than 10^{-15} bit error rate
- Test Modes: On-chip at-speed BIST circuitry, Loopbacks
- On-chip LVDS and CML terminations
- High-speed CML driver with optional signal conditioning
- 4-bit differential source synchronous LVDS parallel I/O
- Low-jitter PLL reference to external differential HSTL clock at 125 MHz
- Designed for use with low cost FR4 backplane
- TIA/EIA 644-A compatible LVDS IO
- IEEE Draft P802.3ae D4.0 - MDIO management interface protocol compatible
- IEEE 1149.1 (JTAG) compliant test mode
- 1.35V for core, high-speed circuitry and MDIO
- 3.3V ±5% for LVDS IO, Control and JTAG interface
- Low power, 4.5W (TYP)
- 23 mm x 23 mm thermally enhanced BGA package

Typical Application



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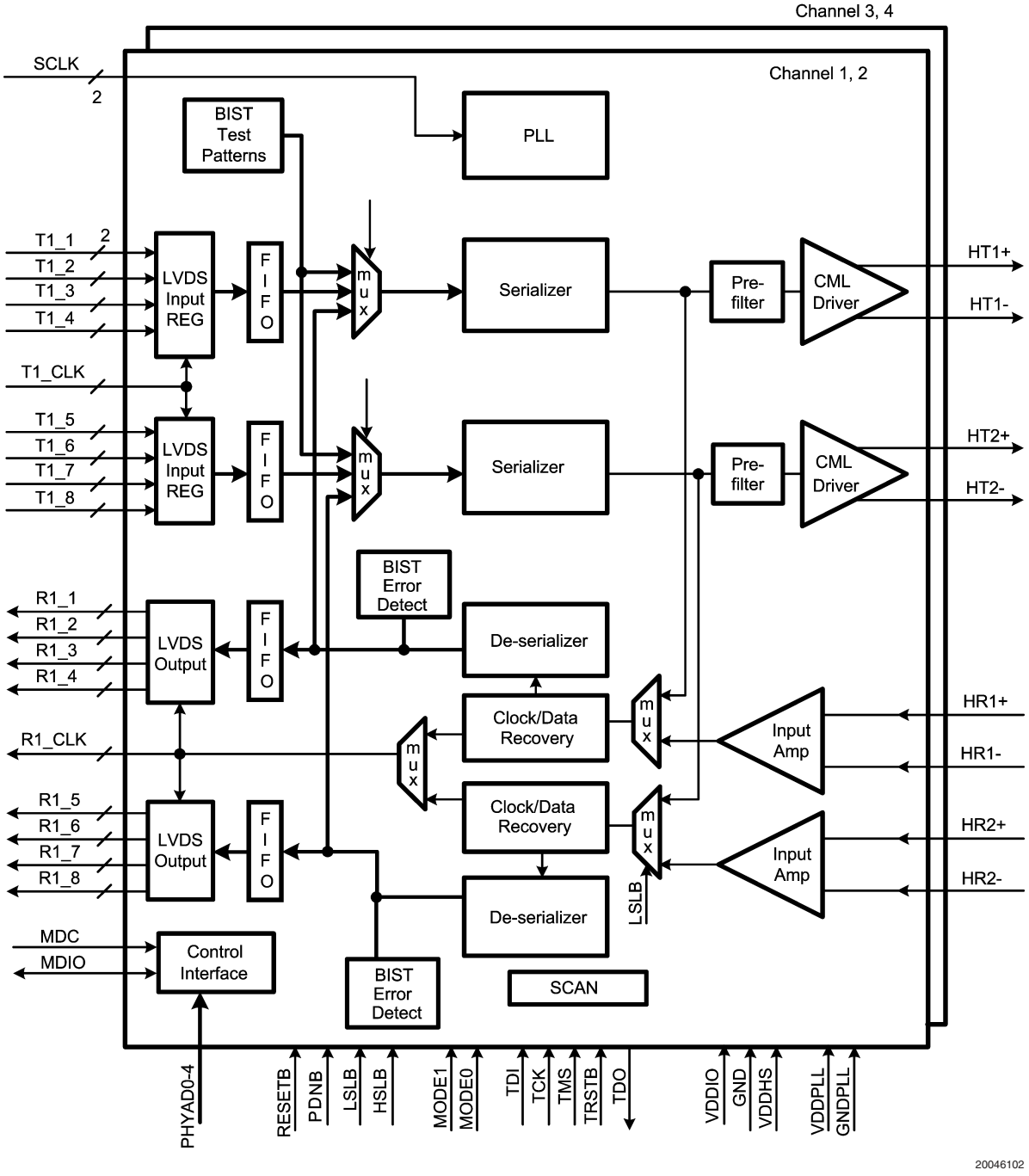
Equivalent Functional Diagram



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Ordering Information

NSID / Marking	Data Rate Support
(logo) # SCAN50C400UT Lot#, Wafer#	1.25/2.5/5.0 Gbps Operation

Connection Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	NC	NC	TDO	TDI	LSLB	TRSTB	T2_1+	GND	T2_3+	T2_4+	NC	GND	T2_7+	T2_8+	NC	SCLK+	NC	NC	NC	NC	NC	NC	A
B	NC	NC	TCK	TMS	HSLB	MODE1	T2_1-	NC	T2_3-	T2_4-	NC	NC	T2_7-	T2_8-	NC	SCLK-	NC	GND	RES0	NC	NC	NC	B
C	T1_8+	T1_8-	GND	NC	GND	T2_CLK+	GND	T2_2+	NC	GND	T2_5+	T2_6+	GND	NC	NC	NC	NC	NC	NC	NC	NC	NC	C
D	T1_7+	T1_7-	GND	NC	NC	T2_CLK-	NC	T2_2-	NC	NC	T2_5-	T2_6-	NC	VDDHS	GND	NC	VDDHS	NC	VDDHS	NC	VDDHS	GND	D
E	GND	NC	T1_6+	T1_6-	VDDIO	VDDIO	VDDIO	VDDIO	NC	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	NC	NC	HT4-	HT4+	E
F	GND	NC	T1_5+	T1_5-	VDDIO													NC	VDDHS	NC	VDDHS	GND	F
G	T1_4+	T1_4-	NC	NC	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	NC	NC	HT3-	HT3+	G
H	T1_3+	T1_3-	GND	NC	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	VDDHS	NC	VDDHS	GND	H
J	GND	NC	T1_2+	T1_2-	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	NC	NC	HT2-	HT2+	J
K	T1_CLK+	T1_CLK-	T1_1+	T1_1-	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	VDDHS	NC	NC	GND	K
L	GND	NC	GND	NC	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	RES1	NC	HT1-	HT1+	L
M	GND	NC	GND	NC	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	NC	NC	NC	GND	M
N	R1_CLK+	R1_CLK-	R1_1+	R1_1-	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	NC	NC	HR1-	HR1+	N
P	GND	NC	R1_2+	R1_2-	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	RES2	NC	VDDHS	GND	P
R	R1_3+	R1_3-	GND	NC	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	NC	NC	HR2-	HR2+	R
T	R1_4+	R1_4-	GND	VDDHS	VDDIO		GND	GND	GND	GND	GND	GND	GND	GNDPLL	GNDPLL	GNDPLL		VDDPLL	NC	NC	VDDHS	GND	T
U	GND	NC	R1_5+	R1_5-	VDDIO													NC	NC	NC	HR3-	HR3+	U
V	GND	NC	R1_6+	R1_6-	VDDIO	VDDIO	VDDIO	VDDIO	NC	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	VDDHS	NC	NC	VDDHS	GND	V
W	R1_7+	R1_7-	GND	NC	NC	R2_CLK-	NC	R2_2-	NC	NC	R2_5-	R2_6-	NC	VDDHS	NC	RES3	NC	NC	NC	NC	HR4-	HR4+	W
Y	R1_8+	R1_8-	GND	RESETB	PDNB	R2_CLK+	GND	R2_2+	GND	GND	R2_5+	R2_6+	GND	NC	GND	NC	NC	GND	NC	NC	NC	GND	Y
AA	NC	NC	MDC	MDIO	PHYAD4	MODE0	R2_1-	NC	R2_3-	R2_4-	NC	NC	R2_7-	R2_8-	NC	RES4	NC	NC	NC	NC	NC	NC	AA
AB	NC	NC	PHYAD1	PHYAD2	PHYAD3	PHYAD0	R2_1+	GND	R2_3+	R2_4+	NC	GND	R2_7+	R2_8+	GND	NC	NC	GND	RES5	NC	NC	NC	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

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TOP VIEW
Order Number SCAN50C400UT
See NS Package Number UFJ440A

Pin Descriptions

Pin Name	Ball Number	I/O, Type	Description
HIGH-SPEED DIFFERENTIAL I/O			
HT1+ HT1–	L22 L21	O, CML	Inverting and non-inverting high-speed CML differential outputs of the serializer, channel 1. Data is sourced from T1_1±, T1_2±, T1_3± and T1_4±. On-chip 50Ω termination resistors connect from HT1+ and HT1– to V_{DDHS}.
HT2+ HT2–	J22 J21	O, CML	Inverting and non-inverting high-speed CML differential outputs of the serializer, channel 2. Data is sourced from T1_5±, T1_6±, T1_7± and T1_8±. On-chip 50Ω termination resistors connect from HT2+ and HT2– to V_{DDHS}.
HT3+ HT3–	G22 G21	O, CML	Inverting and non-inverting high-speed CML differential outputs of the serializer, channel 3. Data is sourced from T2_1±, T2_2±, T2_3± and T2_4±. On-chip 50Ω termination resistors connect from HT3+ and HT3– to V_{DDHS}.
HT4+ HT4–	E22 E21	O, CML	Inverting and non-inverting high-speed CML differential outputs of the serializer, channel 4. Data is sourced from T2_5±, T2_6±, T2_7± and T2_8±. On-chip 50Ω termination resistors connect from HT4+ and HT4– to V_{DDHS}.
HR1+ HR1–	N22 N21	I, CML	Inverting and non-inverting high-speed differential inputs of the deserializer, channel 1. Data is de-serialized and output at R1_1±, R1_2±, R1_3± and R1_4±. On-chip 50Ω termination resistors connect from HR1+ and HR1– to an internal bias.
HR2+ HR2–	R22 R21	I, CML	Inverting and non-inverting high-speed differential inputs of the deserializer, channel 2. Data is de-serialized and output at R1_5±, R1_6±, R1_7± and R1_8±. On-chip 50Ω termination resistors connect from HR2+ and HR2– to an internal bias.
HR3+ HR3–	U22 U21	I, CML	Inverting and non-inverting high-speed differential inputs of the deserializer, channel 3. Data is de-serialized and output at R2_1±, R2_2±, R2_3± and R2_4±. On-chip 50Ω termination resistors connect from HR3+ and HR3– to an internal bias.
HR4+ HR4–	W22 W21	I, CML	Inverting and non-inverting high-speed differential inputs of the deserializer, channel 4. Data is de-serialized and output at R2_5±, R2_6±, R2_7± and R2_8±. On-chip 50Ω termination resistors connect from HR4+ and HR4– to an internal bias.
REFERENCE CLOCK			
SCLK+ SCLK–	A16 B16	I, HSTL	Inverting and non-inverting differential reference clock to the PLL for generating internal high-speed clocks. A low jitter 125 MHz ±100 ppm clock should be connected to SCLK±. All four serializers and deserializers are frequency-locked to SCLK±. A 50 Ω termination to Ground is present on each input pin.
TRANSMIT INPUT DATA			
T1_1+ T1_1– T1_2+ T1_2– T1_3+ T1_3– T1_4+ T1_4–	K3 K4 J3 J4 H1 H2 G1 G2	I, LVDS	Differential transmit input data for channel 1. An on-chip 100 Ω resistor is connected between each pair of complimentary inputs. T1[1–4]± are synchronous to clock T1_CLK±. Data at T1[1–4]± are serialized and output at HT1±. T1_1 is shifted out first, see *Figure 2*. Data is strobed on both rising and falling edges of T1_CLK±.
T1_5+ T1_5– T1_6+ T1_6– T1_7+ T1_7– T1_8+ T1_8–	F3 F4 E3 E4 D1 D2 C1 C2	I, LVDS	Differential transmit input data for channel 2. An on-chip 100 Ω resistor is connected between each pair of complimentary inputs. T1[5–8]± are synchronous to clock T1_CLK±. Data at T1[5–8]± are serialized and output at HT2±. T1_5 is shifted out first, see *Figure 2*. Data is strobed on both rising and falling edges of T1_CLK±.
T1_CLK+ T1_CLK–	K1 K2	I, LVDS	Differential 625 MHz transmit nibble clock for channels 1 and 2. Data at T1[1–4]± and T1[5–8]± are strobed-in at both rising and falling edges of T1_CLK±, forming an 8-bit input data bus at 1.25 Gbps. T1_CLK± should be frequency-locked to reference clock SCLK±. An on-chip 100 Ω resistor is connected between each pair of complimentary inputs.

Pin Descriptions (Continued)

Pin Name	Ball Number	I/O, Type	Description
TRANSMIT INPUT DATA			
T2_1+ T2_1– T2_2+ T2_2– T2_3+ T2_3– T2_4+ T2_4–	A7 B7 C8 D8 A9 B9 A10 B10	I, LVDS	Differential transmit input data for channel 3. An on-chip 100 Ω resistor is connected between each pair of complimentary inputs. T2[1–4]± are synchronous to clock T2_CLK±. Data at T2[1–4]± are serialized and output at HT3±. T2_1 is shifted out first, see *Figure 2*. Data is strobed on both rising and falling edges of T2_CLK±.
T2_5+ T2_5– T2_6+ T2_6– T2_7+ T2_7– T2_8+ T2_8–	C11 D11 C12 D12 A13 B13 A14 B14	I, LVDS	Differential transmit input data for channel 4. An on-chip 100 Ω resistor is connected between each pair of complimentary inputs. T2[5–8]± are synchronous to clock T2_CLK±. Data at T2[5–8]± are serialized and output at HT4±. T2_5 is shifted out first, see *Figure 2*. Data is strobed on both rising and falling edges of T2_CLK±.
T2_CLK+ T2_CLK–	C6 D6	I, LVDS	Differential 625 MHz transmit nibble clock for channels 3 and 4. Data at T2[1–4]± and T2[5–8]± are strobed-in at both rising and falling edges of T2_CLK±, forming an 8-bit input data bus at 1.25 Gbps. T2_CLK± should be frequency-locked to reference clock SCLK±. An on-chip 100 Ω resistor is connected between each pair of complimentary inputs.
RECEIVE OUTPUT DATA			
R1_1+ R1_1– R1_2+ R1_2– R1_3+ R1_3– R1_4+ R1_4–	N3 N4 P3 P4 R1 R2 T1 T2	O, LVDS	Channel 1 deserialized recovered data. Data at HR1± is de-serialized and output at R1[1–4]±, clocked by both rising and falling edges of R1_CLK±.
R1_5+ R1_5– R1_6+ R1_6– R1_7+ R1_7– R1_8+ R1_8–	U3 U4 V3 V4 W1 W2 Y1 Y2	O, LVDS	Channel 2 deserialized recovered data. Data at HR2± is de-serialized and output at R1[5–8]±, clocked by both rising and falling edges of R1_CLK±.
R1_CLK+ R1_CLK–	N1 N2	O, LVDS	Differential recovered nibble clock for channel 1 and 2. R1_CLK± is a 625 MHz clock sourced from the clock recovery PLL. R1_CLK±, together with R1[1–4]± and R1[5–8]±, form a source synchronous 8-bit output data bus at 1.25 Gbps.
R2_1+ R2_1– R2_2+ R2_2– R2_3+ R2_3– R2_4+ R2_4–	AB7 AA7 Y8 W8 AB9 AA9 AB10 AA10	O, LVDS	Channel 3 deserialized recovered data. Data at HR3± is de-serialized and output at R2[1–4]±, clocked by both rising and falling edges of R2_CLK±.

Pin Descriptions (Continued)

Pin Name	Ball Number	I/O, Type	Description
RECEIVE OUTPUT DATA			
R2_5+ R2_5– R2_6+ R2_6– R2_7+ R2_7– R2_8+ R2_8–	Y11 W11 Y12 W12 AB13 AA13 AB14 AA14	O, LVDS	Channel 4 deserialized recovered data. Data at HR4± is de-serialized and output at R2[5–8]±, clocked by both rising and falling edges of R2_CLK±.
R2_CLK+ R2_CLK–	Y6 W6	O, LVDS	Differential recovered nibble clock for channel 3 and 4. R2_CLK± is a 625 MHz clock sourced from the clock recovery PLL. R2_CLK±, together with R2[1–4]± and R2[5–8]±, form a source synchronous 8-bit output data bus at 1.25 Gbps.
SERIAL INTERFACE — 1.35V Levels (1.5V Tolerant)			
MDC	AA3	I, LVCMOS	Synchronous clock to the management serial data input/output interface. The clock rate can be 0 MHz–2.5 MHz. MDC can be asynchronous to transmit or receive clocks (SCLK±, T1_CLK±, T2_CLK±, R1_CLK±, R2_CLK±). This pin includes an internal 30kΩ pull-up to the 1.35V rail.
MDIO	AA4	IO, LVCMOS	Bi-directional management data line where control data is transferred between station management and SCAN50C400 transceiver. This pin includes an internal 30 kΩ pull-up resistor to the 1.35V rail. An external pull-up resistor is typically connected from MDIO to the 1.35V rail.
PHYAD0 PHYAD1 PHYAD2 PHYAD3 PHYAD4	AB6 AB3 AB4 AB5 AA5	I, LVCMOS	PHYAD0–4 define the 5-bit PHY address to the SCAN50C400 transceiver. PHYAD4 is the MSB. These pins include an internal 30kΩ pull-up to the 1.35V rail.
CONTROL INTERFACE — 3.3V Levels			
RESETB	Y4	I,LVCMOS	A logic low at RESETB initiates hardware reset function. RESETB must be low for more than 1ms with SCLK running. This pin includes an internal pull-up.
LSLB	A5	I, LVCMOS	A logic low at LSLB enables LVDS loopback test mode for all four channels. The serialized bit stream is internally connected to the high-speed serial input of each channel's deserializer. It forms a diagnosis data path from the LVDS parallel transmit inputs (T1[1-8]±, T2[1-8]±), through the SCAN50C400, and back to the LVDS parallel LVDS outputs (R1[1-8]±, R2[1-8]±). The data inputs at HR± are ignored, but the input terminations at HR+ and HR– remain active. During normal operation, LSLB should be tied high. See *Figure 6*. This pin includes an internal pull-up. **LSLB HSLB** 1 1 Normal SERDES mode. 1 0 High-Speed Loopback enabled. 0 1 LVDS Loopback enabled. 0 0 Not recommended. SCAN50C400 defaulted to LVDS loopback.
HSLB	B5	I, LVCMOS	A logic low at HSLB enables High-speed loopback test mode for all four channels. The deserialized data at the LVDS side are internally connected to the transmit input data of each channel's serializer. It forms a diagnosis data path from the high-speed serial inputs (HR±), through the SCAN50C400, and back to the high-speed serial outputs (HT±). The data inputs at T1[1-8]± and T2[1-8]± are ignored, but the on-chip differential terminations remain active. During normal operation, HSLB should be tied high. See *Figure 7* and truth table in LSLB description. This pin includes an internal pull-up.

Pin Descriptions (Continued)

Pin Name	Ball Number	I/O, Type	Description
CONTROL INTERFACE — 3.3V Levels			
MODE0 MODE1	AA6 B6	I, LVCMOS	MODE0–1 selects the line data rate. These pins include internal pull-ups. **MODE1** **MODE0** 0 0 Serializer outputs at 5 Gbps, Deserializer inputs at 5 Gbps. 1 0 Serializer outputs at 2.5 Gbps, Deserializer inputs at 2.5 Gbps. 0 1 Serializer outputs at 1.25 Gbps, Deserializer inputs at 1.25 Gbps. 1 1 Serializer outputs at 5 Gbps, Deserializer inputs at 5 Gbps.
PDNB	Y5	I, LVCMOS	A logic low at PDNB activates the hardware power down mode. In power down mode, the MDIO Management interface is not functioning. This pin includes an internal **pull-down** (default is OFF).
SCAN INTERFACE — 3.3V Levels			
TRSTB	A6	I, LVCMOS	Test Reset Input per IEEE 1149.1. There is an internal pull-up that defaults this input to a logic high. Test Reset is active low.
TMS	B4	I, LVCMOS	Test Mode Select per IEEE 1149.1. There is an internal pull-up that defaults this input to a logic high.
TDI	A4	I, LVCMOS	Test Data Input per IEEE 1149.1. There is an internal pull-up that defaults this input to a logic high.
TCK	B3	I, LVCMOS	Test Clock Input per IEEE 1149.1. There is an internal weak pull-down on this pin.
TDO	A3	O, LVCMOS	Test Data Output per IEEE 1149.1. Default is TRI-STATE.
RESERVED / TEST PINS			
RES0 RES1 RES2 RES3 RES4 RES5	B19 L19 P19 W16 AA16 AB19		Reserved for testing purposes. Do not connect.
POWER			
V_{DDIO}		I, Power	V_{DDIO} = 3.3V ±5%. It powers the LVDS parallel IO interface, LVCMOS control logic and SCLK input stage.
V_{DDHS}		I, Power	V_{DDHS} = 1.35V. It powers the high-speed CML I/O circuitry and MDIO serial control logic.
GND		I, Power	Ground reference. GND should be tied to a solid ground plane through a low impedance path. GND and GND_PLL should both be at the same potential.
V_{DDPLL}		I, Power	V_{DDPLL}– GND_PLL = 1.35V. It powers PLL circuitry of the device.
GND_PLL		I, Power	Ground reference to PLL circuitry. GND_PLL should be tied to a solid plane through a low inductance path. GND and GND_PLL should both be at the same potential.
NO CONNECT			
NC			Not used by SCAN50C400.

Pin Descriptions - Power Pin / Type / Ball Number

Pin Name	Voltage	Ball Numbers
V_{DDIO}	3.3V	E5, E6, E7, E8, F5, G5, H5, J5, K5, L5, M5, N5, P5, R5, T5, U5, V5, V6, V7, V8
V_{DDPLL}	1.35V	G18, H18, J18, K18, L18, M18, N18, P18, R18, T18
V_{DDHS}	1.35V	E10, E11, E12, E13, E14, E15, E16, E17, E18 V10, V11, V12, V13, V14, V15, V16, V17, V18, T4 D14, D17, D19, F19, H19, K19, W14, D21, F21, H21, P21, T21, V21
GND	0V	E1, F1, J1, L1, M1, P1, U1, V1 C3, D3, H3, L3, M3, R3, T3, W3, Y3 C5, C7, Y7, A8, AB8, Y9, C10, Y10, A12, AB12, C13, Y13 D15, Y15, AB15, B18, Y18, AB18, D22, F22, H22, K22, M22, P22, T22, V22, Y22 G7, H7, J7, K7, L7, M7, N7, P7, R7, T7 G8, H8, J8, K8, L8, M8, N8, P8, R8, T8 G9, H9, J9, K9, L9, M9, N9, P9, R9, T9 G10, H10, J10, K10, L10, M10, N10, P10, R10, T10 G11, H11, J11, K11, L11, M11, N11, P11, R11, T11 G12, H12, J12, K12, L12, M12, N12, P12, R12, T12 G13, H13, J13, K13, L13, M13, N13, P13, R13, T13
GND_PLL	0V	G14, H14, J14, K14, L14, M14, N14, P14, R14, T14 G15, H15, J15, K15, L15, M15, N15, P15, R15, T15 G16, H16, J16, K16, L16, M16, N16, P16, R16, T16
NC	Float	A1, B1, AA1, AB1, A2, B2, E2, F2, J2, L2, M2, P2, U2, V2, AA2, AB2 G3, C4, D4, G4, H4, L4, M4, R4, W4, D5, W5, D7, W7, B8, AA8 C9, D9, E9, V9, W9, D10, W10, A11, B11, AA11, AB11, B12, AA12, D13, W13 C14, Y14, A15, B15, C15, W15, AA15 C16, D16, Y16, AB16, A17, B17, C17, W17, Y17, AA17 A18, C18, D18, F18, U18, W18, AA18 A19, C19, E19, G19, J19, M19, N19, R19, T19, U19, V19, W19, Y19, AA19 A20, B20, C20, D20, E20, F20, G20, H20, J20, K20, L20, M20, N20, P20, R20, T20, U20, V20, W20, Y20, AA20, AB20 A21, B21, C21, K21, M21, Y21, AA21, AB21 A22, B22, C22, AA22, AB22 AB17

Note: I = Input O = Output IO = Input/Output

Functional Descriptions

REFERENCE CLOCK

The reference clock SCLK± is a differential input clock that synchronizes the transmitters of the SCAN50C400. Internal low-jitter PLLs are used to frequency-lock to the lower speed SCLK± at 125 MHz, multiply and generate the internal clocks that sample the input LVDS transmit data, and the high-speed bit-clock that shifts out the transmit serial data at HT±. The input stage at SCLK± accepts HSTL differential clock signals and provides a 50 Ω termination to Ground on each input. It should be connected to a low-jitter clock source free from periodic jitter with less than 2ps-rms random jitter. *Figure 1* illustrates a possible connection to SCLK. LVDS input data and transmit clocks (T1_CLK± and T2_CLK±) should be frequency-locked to SCLK±. *Figure 1* illustrates the SCLK input stage.

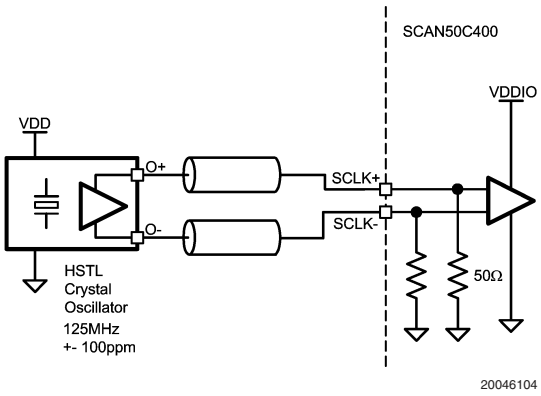


FIGURE 1. SCLK± Driven by HSTL Clock Driver / Crystals

Functional Descriptions (Continued)

DATA RATE / DEVICE CONFIGURATION

SCAN50C400 supports multiple data rates at 1.25, 2.50 or 5.0 Gbps selected by two control pins, MODE0 and MODE1. SCLK± is fixed at 125 MHz, and the transfer rate at the parallel LVDS side is also fixed at 1.25 Gbps, regardless of the line data rate selected. The SCAN50C400 is a selectable 1:1, 2:1 or 4:1 serializer/deserializer at line data rate of 1.25, 2.5, or 5.0 Gbps. See *Figure 2*.

Mode control is set at power-up via the MODE0 and MODE1 pins. These pins include internal pull-up devices, thus default to (1,1) 5 Gbps Mode if undriven. After power-up the mode of the device may be changed at any time. When mode is changed data integrity is not guaranteed until after each active channel has re-locked. Lock time is dependant upon the data pattern.

MODE1	MODE0	Description
0	0	**5.0 Gbps, 4:1 Serializer/Deserializer**
1	1	T1[1-4]± to HT1±. LSB T1_1± is the first bit transmitted. T1[5-8]± to HT2±. LSB T1_5± is the first bit transmitted. T2[1-4]± to HT3±. LSB T2_1± is the first bit transmitted. T2[5-8]± to HT4±. LSB T2_5± is the first bit transmitted. HR1± to R1[1-4]±. LSB R1_1± is the first bit received. HR2± to R1[5-8]±. LSB R1_5± is the first bit received. HR3± to R2[1-4]±. LSB R2_1± is the first bit received. HR4± to R2[5-8]±. LSB R2_5± is the first bit received.
1	0	**2.5 Gbps, 2:1 Serializer/Deserializer** (T1_1±, T1_3±) to HT1±. LSB T1_1± is the first bit transmitted. T1_2± and T1_4± are ignored. (T1_5±, T1_7±) to HT2±. LSB T1_5± is the first bit transmitted. T1_6± and T1_8± are ignored. (T2_1±, T2_3±) to HT3±. LSB T2_1± is the first bit transmitted. T2_2± and T2_4± are ignored. (T2_5±, T2_7±) to HT4±. LSB T2_5± is the first bit transmitted. T2_6± and T2_8± are ignored. HR1± to (R1_1±, R1_3±). LSB R1_1± is the first bit received. R1_2±, R1_4± replicate R1_1± and R1_3±. HR2± to (R1_5±, R1_7±). LSB R1_5± is the first bit received. R1_6±, R1_8± replicate R1_5± and R1_7±. HR3± to (R2_1±, R2_3±). LSB R2_1± is the first bit received. R2_2±, R2_4± replicate R2_1± and R2_3±. HR4± to (R2_5±, R2_7±). LSB R2_5± is the first bit received. R2_6±, R2_8± replicate R2_5± and R2_7±.
0	1	**1.25 Gbps, Feed-through 1:1** Serializer/Deserializer. T1_1± to HT1±. T1[2-4]± are ignored. T1_5± to HT2±. T1[6-8]]± are ignored. T2_1± to HT3±. T2[2-4]± are ignored. T2_5± to HT4±. T2[6-8]± are ignored. HR1± to R1_1±. R1[2-4]± replicate R1_1±. HR2± to R1_5±. R1[6-8]± replicate R1_5±. HR3± to R2_1±. R2[2-4]± replicate R2_1±. HR4± to R2_5±. R2[6-8]± replicate R2_5±.

Functional Descriptions (Continued)

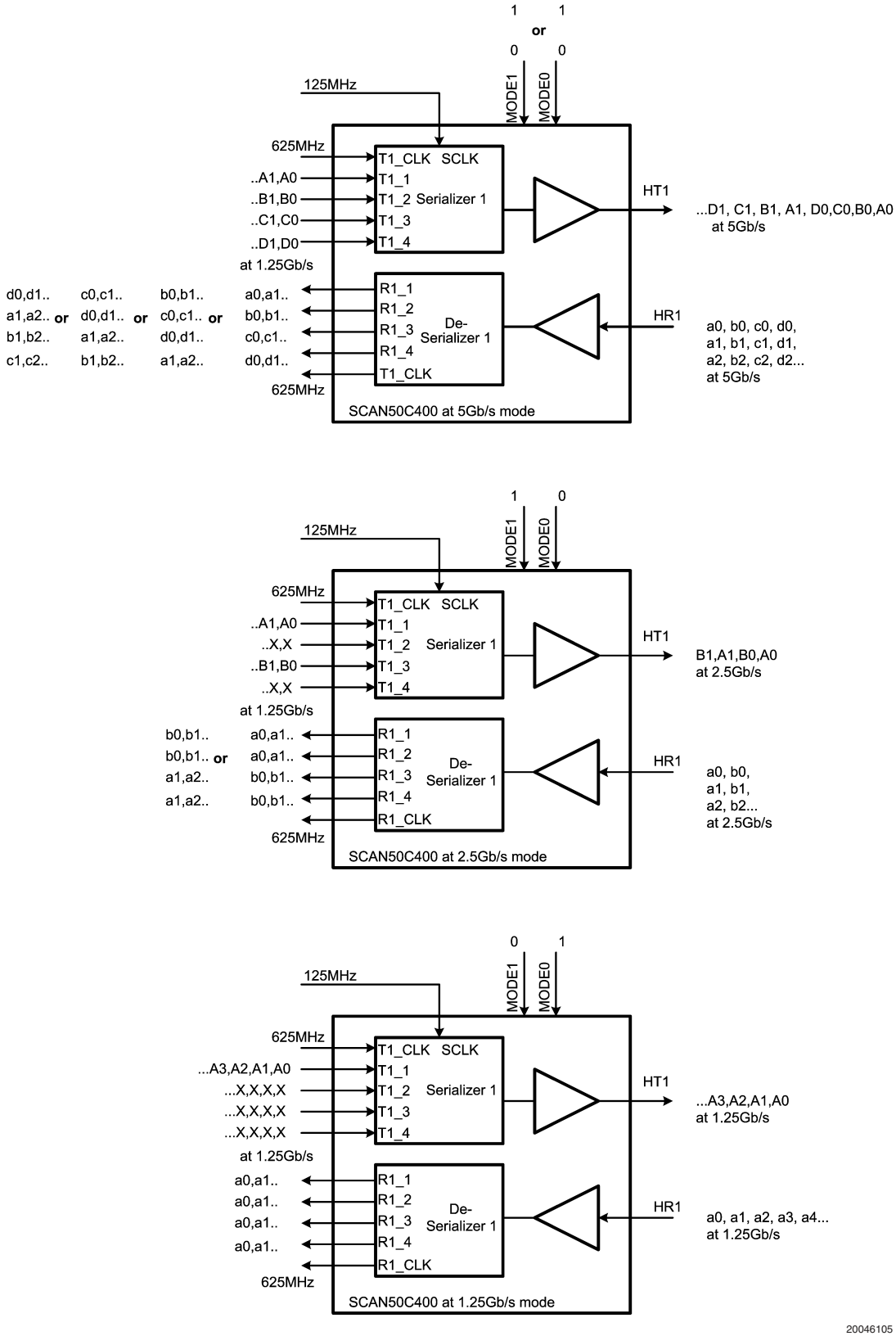


FIGURE 2. SCAN50C400 at 5, 2.5 and 1.25 Gbps Modes, Channel 1 Shown (x = don't care)

Functional Descriptions (Continued)

LVDS TRANSMIT DATA BUS

The 4-bit LVDS transmit data bus of channels 1 and 2, are registered by both the rising and falling edges of T1_CLK±. Similarly, the 4-bit LVDS transmit data bus of channels 3 and 4, are registered by T2_CLK±. The LVDS data bus has a fixed transfer rate of 1.25 Gbps. T1_CLK± and T2_CLK± are 625 MHz and must be frequency-locked to the reference clock SCLK±. Internal FIFO's are used to compensate against the phase skew between T1_CLK± or T2_CLK± and the internal clock that samples the input transmit data. Channels 1 and 2 share the same transmit clock T1_CLK±, while channels 3 and 4 share the same transmit clock T2_CLK±. The two channels, 1 and 2, or 3 and 4, effectively form an 8-bit LVDS transmit data bus that are serialized into two high-speed serial bit streams, providing an aggregated through-put of up to 10 Gbps in either direction. Each serializer follows a bit interleaving order with the LSB of the 4-bit LVDS transmit data being the first bit to be transmitted at HT±.

Figure 9 shows the timing diagram of the transmit LVDS interface.

HIGH-SPEED DATA OUTPUT

The high-speed serialized bit stream is output at HT±, driven by a current-mode-logic (CML) driver with optional signaling conditioning and optional VOD adjustment to optimize performance over a wide range of transmission length and attenuation distortion result from a low cost FR4 backplane. The CML I/O is designed for AC coupling.

Internal 50Ω resistors connected from HT+ and HT– to V_{DDHS} terminate the outputs of each driver. The output level can be programmed from 650 mV_{p-p} to 315mV_{p-p} in 8 steps. It is programmed through the serial control interface (See *Table 2. User Registers Implemented in the SCAN50C400 and Defaults*).

CML VOD Adjust Typical Levels

STEP Setting MDIO Register (offset 30.49)	AC Coupled VOD (mV) TYP
(0x0000)	650
(0x0492) - Default	550
(0x0924)	430
(0x0DB6)	420
(0x1248)	405
(0x16DA)	380
(0x1B6C)	350
(0x1FFE)	315

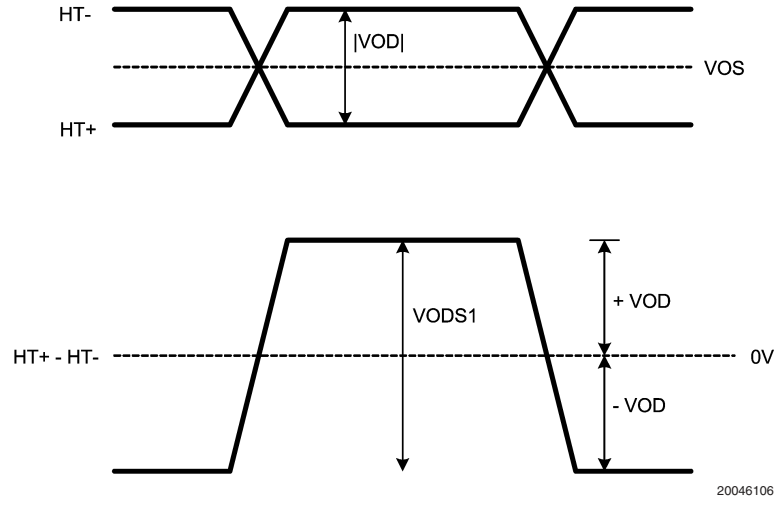


FIGURE 3. High-Speed CML Output Waveforms with de-emphasis disabled (Full VOD)

Each high-speed CML driver of the SCAN50C400 includes a de-emphasis filter. It is a user-programmable 2-tap FIR filter used to equalize the transmission channel to reduce inter-symbol interference. The FIR filter is designed to reduce the output level of lower frequency components of the data bit stream. *Figure 4* shows the HT waveform of 2 continuous 1's (or 2 continuous 0's), in which the output level of the 2nd bit (and subsequent bits of the continuous 1's) is reduced. The configuration of the FIR filter is user programmable through registers 30.5 and 30.6 which are accessible through the Serial control Interface.

Functional Descriptions (Continued)

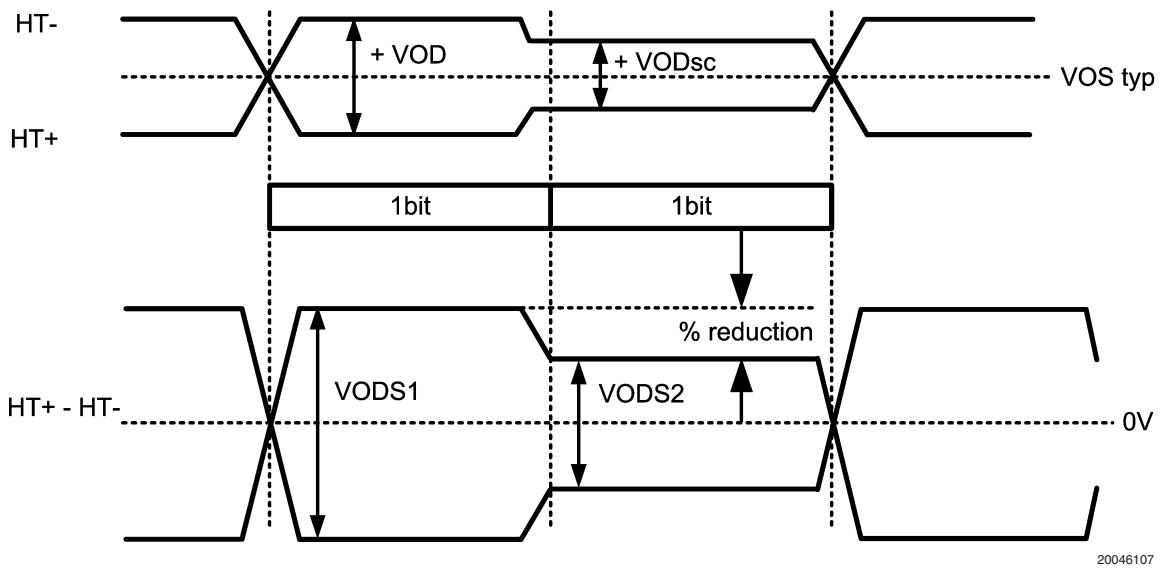


FIGURE 4. High-Speed CML Output Waveforms with signal conditioning enabled

Functional Descriptions (Continued)

DESERIALIZER

Serial bit stream is received at HR± terminals. The input stage is designed for AC-coupling. Internal 50Ω termination resistors connect HR+ and HR– to an internal bias. At power-up, in the absence of data, the clock/data recovery circuit will be frequency-locked to SCLK. A clock/data recovery circuit locks to the incoming bit stream to recover the high-speed receive bit clock and re-time incoming data. The clock/data recovery circuit expects a coded input bit stream with no more than 20 bits (@5Gbps) of continuous one's or continuous zero's. Similarly, at 2.5 Gbps with 2 multiplexed 8b/10b bit streams, the receiver expects no more than 10 bits of continuous 1's or continuous 0's, and at 1.25 Gbps, the receiver expects no more than 5 bits of continuous 1's or 0's, as guaranteed by 8b/10b coding.

The recovered bit clock is used to re-time the incoming data, after which the serial bit stream is deserialized. The recovered nibble clock from either Channel 1 or Channel 2 is automatically selected as the recovered clock at R1_CLK± and used to strobe the recovered data R1[1-4]± and R1[5-8]±. An internal FIFO is used to compensate against phase skew between the recovered clocks of the two channels. In the absence of data transitions at one of the two channels (for example, a loss of the link), user intervention is recommended to power-down the deserializer (through register 30.1) that has lost the link. This will ensure use of the recovered clock from the channel with valid data. Similarly, one recovered nibble clock from either Channel 3 or Channel 4 is selected as the recovered clock at R2_CLK±. *Figure 10* shows a timing diagram of the recovered LVDS data bus.

The de-serializing process does not rely on any framing protocol. As a result, at 5 Gbps, any one particular bit in the serial bit stream may appear in any one of the 4 LVDS output data bits at start-up; and at 2.5 Gbps, any one particular bit in the serial bit stream may appear in any one of the 2 LVDS output data bits at start up. Subsequent de-serialization follows a bit de-interleaving order. This bit de-interleaving process is illustrated in *Figure 2*.

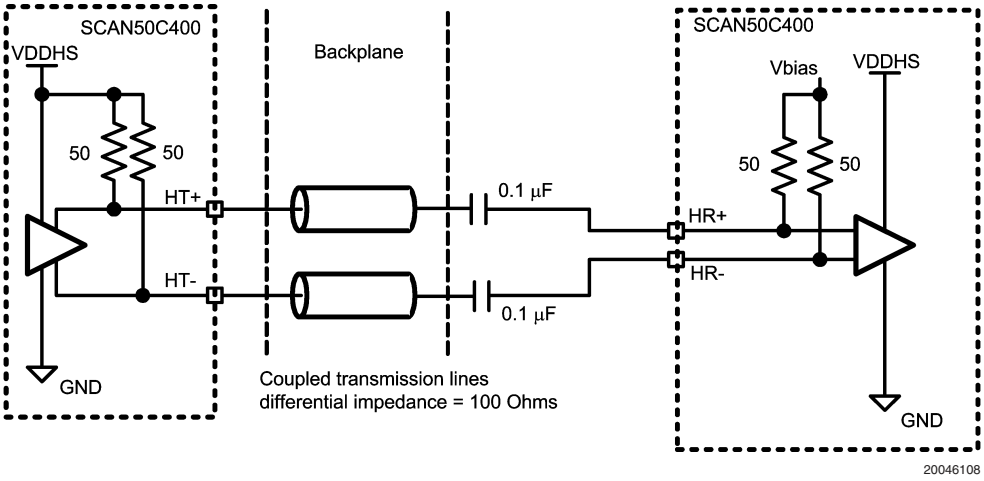


FIGURE 5. High-Speed IO, AC Coupled

Functional Descriptions (Continued)

LVDS LOOPBACK (Local Serial Loopback)

To support local self-testing, the SCAN50C400 is equipped with LVDS loopback test mode, activated by pulling LSLB low. LSLB affects all four channels. It enables an internal loopback path from each serializer's high-speed bit stream to its deserializer inputs. It provides a diagnosis path from the LVDS transmit data bus at T1[1-8]± and T2[1-8]±, through the serializers, loopback to the deserializers, and output at the deserializer's LVDS receive data bus at R1[1-8]± and R2[1-8]±. The recovered LVDS receive data can be compared to the LVDS transmit data for self-testing through the host. This loopback mode is also commonly referred as local serial loopback. For normal operation, LSLB and HSLB should be driven high. In this loopback mode the HT outputs are disabled. See **Loopback Mode** table. LSLB pin includes an internal pull-up and defaults to normal SERDES mode.

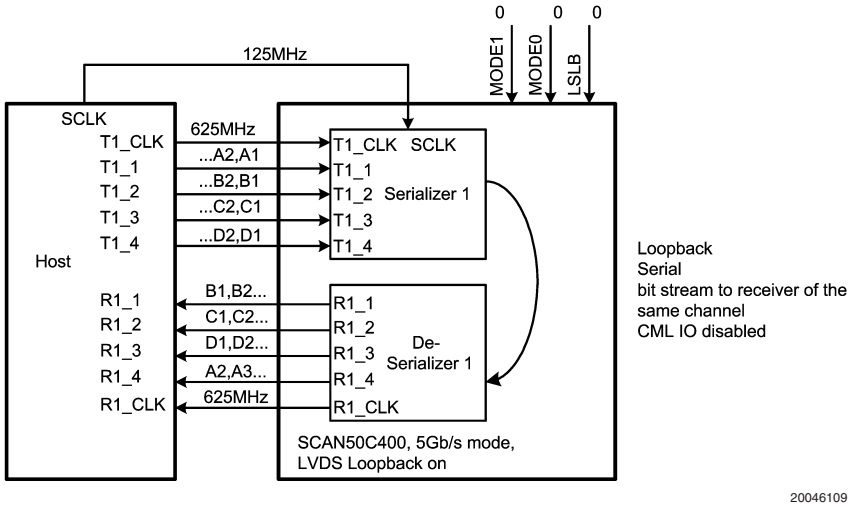


FIGURE 6. SCAN50C400 in LVDS Loopback (Channel 1 at 5 Gbps Shown)

HIGH-SPEED LOOPBACK (Remote Loopback or Line Loopback

To support remote self-testing, the SCAN50C400 is equipped with High-Speed Loopback test mode, activated by pulling HSLB low. HSLB affects all four channels. It enables an internal loopback path from each deserializer's low -speed LVDS receive data bus to its transmitter LVDS inputs. It provides a diagnosis path from the high-speed serial bit stream at HR±, through the deserializer, loopback to the transmit inputs of the serializer and output at the CML outputs HT±. When the test is originated from an upstream device, the High-Speed Loopback test mode supports self-testing of 2 transceivers and the transmission channel. The SCAN50C400 supports high-speed loopback for a synchronous system in which both the local and remote SCAN50C400 transceivers are frequency-locked to the same system clock SCLK.

The high-speed loopback is also commonly referred as remote loopback, or line loopback.

When both LSLB and HSLB are driven low, the SCAN50C400 will be defaulted to the LVDS Loopback test mode.

For normal operation, HSLB and LSLB should be driven high. See **Loopback Mode** table. HSLB pin includes an internal pull-up and defaults to normal SERDES mode.

Functional Descriptions (Continued)

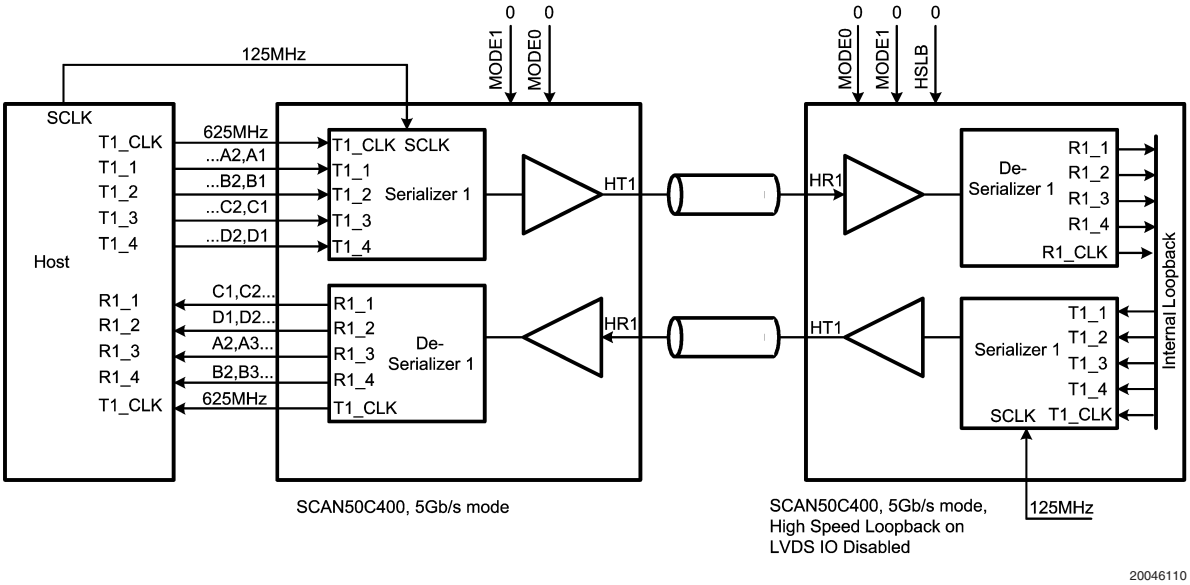


FIGURE 7. SCAN50C400 in High-Speed Loopback (5 Gbps Shown)

Loopback Mode Table

LSLB	HSLB	Mode
1	1	Normal SERDES Mode (default state)
1	0	High-Speed Loopback Mode (HR looped to HT)
0	1	LVDS Loopback Mode (T data looped to R)
0	0	Not Recommended. Defaults to LVDS Loopback Mode.

POWER DOWN

When PDNB is pulled low, the SCAN50C400 is put into the hardware power down mode. Most internal circuitry is shut down to conserve power. All high-speed CML IO's are at static high due to the internal termination resistor (pulled-high to 1.35V). All LVDS inputs are at high impedance state with internal 100Ω termination resistor connecting between each complimentary input pair. All LVDS outputs are floating. The MDIO management bus is inactive. If powered down by the PDNB pin, it must then be enabled by the PDNB pin. Software power down can also be activated through the Serial Control Interface. During software power down, the MDIO management bus remains functional. See Control Register 1 (offset=30.1) for details. If powered down by the software, the device must be reenabled through the software power down bit. PDNB pin includes an internal pull-down and defaults to Power Down mode, device is disabled until actively driven (enabled).

RESET

When RESETB is driven low, the SCAN50C400 is put into the reset state. In this state, all MDIO registers are set to the default values, and the MDIO management bus is inhibited. RESETB should be driven low for more than 1ms while SCLK is running. When RESETB goes high, the SCAN50C400 exits the reset state, the MDIO management bus is enabled, and the transmit PLL starts to acquire lock, typically within 100us. After RESETB goes high, the receiver PLL's are initially frequency locked to SCLK. When valid data is presented at the receiver inputs, HR±, the receiver's PLL's are phase-locked to the incoming data. RESETB pin includes an internal pull-up.

Software reset can be activated through the Serial Control Interface. See Control Register 1 (offset=30.1) for details. During software reset, the Serial Control Interface remains functional, but all registers are preset to their default values. Software reset can only be activated in normal mode when both LSLB and HSLB are at a logic high..

Functional Descriptions (Continued)

UN-USED INPUTS AND FAILSAFE CONDITIONS

When LVDS inputs are open, internal fail-safe circuitry will force both of them low, and the high-speed CML drivers will output a logic low. (See specific conditions in table below).

When CML inputs are open, the internal clock/data recovery circuitry will be frequency-locked to the SCLK clock. The LVDS output drivers will be forced to static logic high.

LVCMOS inputs (MODE0, MODE1, LSLB, HSLB, RESETB) have internal pull-up resistors to 3.3V rail. 5 Gbps normal SERDES mode is the default state.

LVCMOS input PDNB has an internal pull-down resistors. This must be driven or tied high to enable the device.

All Serial Management Interface pins (MDC, MDIO, PHYADn) have internal pull-high resistors. Typical pull-up is 30 kΩ to the 1.35V rail.

Failsafe Condition Table — Serializer

INPUTS				OUTPUTS		
SCLK	TCLK	LVDS DATA INPUTS		CML OUTPUTS		Notes
		Tn+	Tn–	HTn+	HTn–	
running	running	floating	floating	Low	High	Logic Low
running	floating since power-up	X	X	Low	High	Logic Low
running	Static since power-up	X	X	Low	High	Logic Low
running	Running, then float or static	X	X	Last valid state	Last valid state	Logic High or Low
floating	X	X	X	High	High	Both High, 0V Differential

X = either High or Low

Failsafe Condition Table — Deserializer

INPUTS			OUTPUTS			
SCLK	CML INPUTS		LVDS DATA OUTPUTS		Rn-CLK	Notes
	HR+	HR–	Rn+	Rn–		
running	floating	floating	High	Low	Running (625 MHz)	Logic High
floating	X	X	High	Low	Running (<600 MHz)	Logic High

X = either High or Low

JTAG - IEEE 1149.1

The TDI, TDO, TMS, TCK, and TRSTB pins provide the JTAG interface. Per IEEE 1149.1 TDI, TMS, and TRSTB include internal pull-up devices. TCK pin provides a weak pull-down device. All JTAG inputs are 3.3V compatible. The TDO pin default state is TRI-STATE. Additional JTAG details to be published at a later date.

Functional Descriptions (Continued)

AT-SPEED BIST

The SCAN50C400 is equipped with extensive features to support at-speed built-in self-test (BIST) for use in both manufacturing as well as field diagnosis purposes.

Each serializer can be individually put into TX_BIST mode, in which one of the many built-in test patterns is activated, serialized and output at the high-speed CML drivers. Several test patterns are supported, including pseudo-random word (PRW) pattern (2^7-1), memory-based 256-bit user-defined fix pattern, PRW with preamble and post-amble of continuous zero's or continuous one's.

Each deserializer can be individually put into RX_BIST mode, in which the deserializer waits for a valid synchronization header from the transmitter, after which the on-chip BIST Error Detector is activated to compare recovered data against the expected data pre-programmed by user. The BIST test result is reported in the BIST Status Register of each deserializer. A one-bit BIST_OK status is provided to indicate pass/fail. An 8-bit counter is used to store the number of error detected (0 to 255 max). Seven different test patterns are provided, some of which are user defined or customizable. These are:

TP-A Pseudo Random Word, which is 127 bits long and then repeats (2^7-1)

TP-E User Defined 256-bit memory based pattern, default is 10101....[AA....AA] 'h

TP-F Special Pattern with a "0" preamble, a PRW payload, and a "1" post-amble all of which are selectable length

TP-G Special Pattern with a "1" preamble, a PRW payload, and a "0" post-amble all of which are selectable length

More detailed information on AT-SPEED BIST Operation can be found in the **Functional Descriptions - Serial Control Interface** section of this datasheet.

Both the BIST modes of the serializer and deserializer, as well as the BIST status are accessed through the Serial Control Interface (MDIO). Multiple registers are used for the control, pattern selection, and customization of the At-speed BIST function. Register 30.11 is the main control register to enable the individual channel for BIST mode. Registers 30.57 through 30.60 are read-only registers which report the result of the BIST run. The test pattern (TP-A though G) is selected and customized in registers 30.12 and 30.13. The memory based 256-bit pattern for the serializer (TX) is stored in registers 30.16 to 30.31 and the deserializer (RX) memory based pattern is stored in registers 30.32 to 30.47. A more detailed description can be found under the Register Section of this datasheet.

To operate the At-Speed BIST function the following steps should be taken:

1. Select and or customize the test pattern
2. Enable both the Serializer and Deserializer BIST functions synchronously
3. Run the test for a user-defined amount of time
4. Disable the Deserializer BIST function
5. Disable the Serializer BIST function
6. Read result of the test from the BIST Status Registers

Note that the duration of the test is user defined and is controlled by the time duration between step #2 and #4 above. To establish a BER of 10^{14} at 5 Gbps, a minimum run time of 20,000 seconds is required (almost 6 hours).

The LVDS loopback and High-Speed loopback further enhance the self-test capabilities of the SCAN50C400. With LVDS loopback activated together with TX_BIST and RX_BIST modes, the SCAN50C400 provides a self-diagnosis data path through almost the entire chip, with the exception of LVDS IO and high-speed IO.

At-speed BIST only operates in the native 5 Gbps mode. By loading special patterns into TP-E lower speed operation can be emulated. A 1010101010101010 [AAAA'h] represents a maximum transition 5 Gbps pattern. A 1100110011001100 [CCCC'h] represents a maximum transition 2.5 Gbps pattern. A 1111000011110000 [F0F0'h] represents a maximum transition 1.25 Gbps pattern.

At-speed BIST provides a simple and low-cost diagnosis function, relieving the host ASIC processor from the heavy burden of processing data for test purposes.

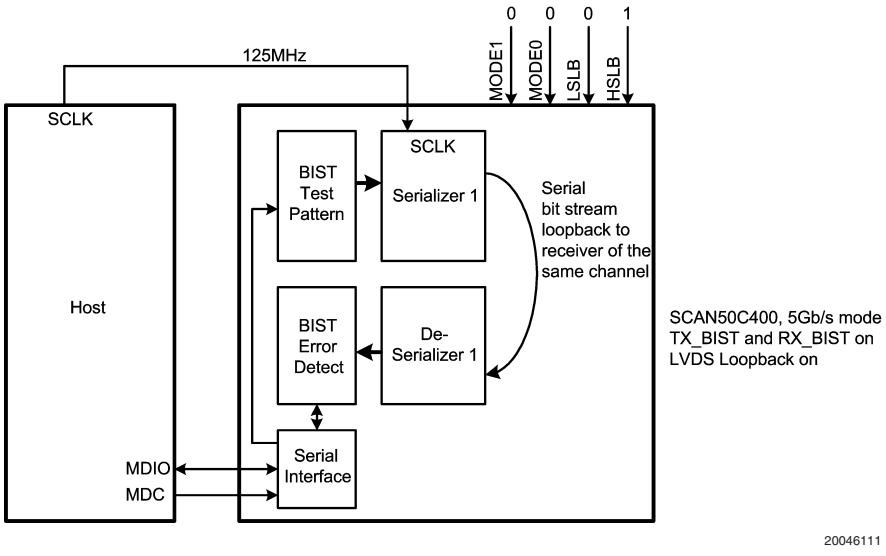


FIGURE 8. At-speed BIST Modes Used with Local Loopback

Functional Descriptions (Continued)

SERIAL CONTROL INTERFACE (MDIO)

The serial control interface allows communication between a station management controller and the SCAN50C400 devices. It can be used to configure the CML drivers' output level, enable BIST and obtain test results from BIST. It is protocol compatible to the station management bus defined in IEEE Draft P802.3ae/D4.0. The serial control interface consists of two pins, the data clock MDC and bi-directional data MDIO. MDC has a maximum clock rate of 2.5 MHz and no minimum limit. The MDIO is bi-directional and can be shared by up to 32 PHY's.

Note that with many SCAN50C400 devices in parallel, the internal pull-up will be in the range of 937Ω (30kΩ/32). The parallel equivalence of the internal resistance and the external pull up should not be less than 250Ω. Signal quality on the net should provide incident wave switching. It may be desirable to control the edge rate of MDC and MDIO from the station management controller to optimize signal quality depending upon the trace net and any resulting stub lengths.

The MDIO pin typically uses an external pull-up resistor (5 kΩ), which during IDLE and bus turn-around, will pull MDIO high. In order to initialize the MDIO interface, the station management sends a sequence of 32 contiguous logic ones on MDIO with MDC clocking. This preamble may be generated either by driving MDIO high for 32 consecutive MDC clock cycles, or by simply allowing the MDIO pull-up resistor to pull the MDIO high for 32 MDC clock cycles. A preamble is required for every operation (64-bit frames, do not suppress preambles).

MDC is an aperiodic signal. Its high or low duration is 160 ns minimum and has no maximum limit. Its period is 400 ns maximum. MDC can be asynchronous to SCLK±, T1_CLK±, T2_CLK±, R1_CLK± or R2_CLK±.

Table 1. Protocol of Management Bus shows the management frame structure in according to IEEE Draft P802.3ae/D4.0.

<1…1> is a sequence of 32 contiguous one's at MDIO used as Preamble for synchronization purpose.

<PPPPP> is the PHY address of the device, defined by the logic states of PHYAD0-4. The MSB bit is the first bit transmitted or received. The PHY address is read at power-up or after a RESET event.

<EEEEE> is the device (register) address. The MSB bit is the first bit transmitted or received. SCAN50C400 supports device address of 30 for accessing vendor specific registers (<EEEEE>=30 decimal, 1E hex).

<AAAA AAAA AAAA AAAA> is the 16-bit address field of the register to be accessed. The first bit transmitted or received is bit 15.

<DDDD DDDD DDDD DDDD> is the 16-bit data field. It is the data to be written into the SCAN50C400 when performing a Write operation. During the Read or Read-Increment-Address operation, it is the read-back data from the SCAN50C400. The first bit transmitted or received is bit 15.

The MDIO Interface is not active when the SCAN50C400 is in hardware RESET mode or powerdown mode.

TABLE 1. Protocol of Management Bus

Management bus protocol	<Preamble><Start><OpCode><PHY addr><dev addr><turnaround><data><idle>
Address	<1...1><00><00><PPPPP><EEEEE><10><AAAA AAAA AAAA AAAA><idle>
Write	<1...1><00><01><PPPPP><EEEEE><10><DDDD DDDD DDDD DDDD><idle>
Read	<1...1><00><11><PPPPP><EEEEE><Z0><DDDD DDDD DDDD DDDD><idle>
Read-increment-Address	<1...1><00><10><PPPPP><EEEEE><Z0><DDDD DDDD DDDD DDDD><idle>

OPERATIONS

The MDIO interface will be active with PDNB = High, RESETB = High for normal mode. It should return the following data:

- Correct PHY ADD, Correct DEV ADD — expected content
- Incorrect PHY ADD, Correct DEV ADD — FFFF'h
- Correct PHY ADD, Incorrect DEV ADD — 0000'h
- RESETB = Low — FFFF'h

Additional information on the Serial Control Interface is provided in National's Application Note AN-1242.

REGISTERS

The SCAN50C400 implements the Device Identifier and its device-specified features in the vendor specific registers. *Table 2. User Registers Implemented in the SCAN50C400 and Defaults* shows the user registers implemented in the SCAN50C400. There are also reserved registers not listed which are used for in-house testing on the SCAN50C400. To prevent putting the device into unspecified operating states, users must not write to reserved registers not listed in *Table 2. User Registers Implemented in the SCAN50C400 and Defaults*. The SCAN50C400 will ignore any write to registers not supported, and return 0 for any read from non-supported registers. The SCAN50C400 will also ignore any management access using the Start-code of <01> as defined in IEEE 802.3 section 22.2.4.5 (Clause 22 Protocol). In this datasheet, registers used in the SCAN50C400 are designated as Reg <30.offset>.

Functional Descriptions (Continued)

TABLE 2. User Registers Implemented in the SCAN50C400 and Defaults

Register Offset	Access	Description
30.1	RW	Control Register 1.
30.2	RO	Device Identifier Register 1.
30.3	RO	Device Identifier Register 2.
30.4	RW	Loopback Control Register.
30.5	RW	TX Signal Conditioning Control Register 1.
30.6	RW	TX Signal Conditioning Control Register 2.
30.8	RO	Status Register.
30.11	RW	Control Register 2.
30.12	RW	BIST TX Control Register.
30.13	RW	BIST RX Control Register.
30.14	RO	Package Identifier (Copy of 30.2).
30.15	RO	Package Identifier (Copy of 30.3).
30.16-31	RW	TX BIST Fixed Pattern Registers.
30.32-47	RW	RX BIST Fixed Pattern Registers.
30.49	RW	TX CML VOD Control Register.
30.57	RO	BIST Status Register for Channel 1.
30.58	RO	BIST Status Register for Channel 2.
30.59	RO	BIST Status Register for Channel 3.
30.60	RO	BIST Status Register for Channel 4.

Functional Descriptions (Continued)

Control Register 1 (Offset=30.1)

Bit	Bit Name	Access	Default	Description
15:8	SW_PDNB	RW	FF 'h	SW_PDNB is the active low software power-down for individual serializers or deserializers. During software power-down, the MDIO serial interface remains functional. The user must program SW_PDNB HIGH to exit power-down mode. The PDNB pin overrides SW_PWDNB. D15=0: Activates software power-down on Channel 4 Deserializer. D14=0: Activates software power-down on Channel 3 Deserializer. D13=0: Activates software power-down on Channel 2 Deserializer. D12=0: Activates software power-down on Channel 1 Deserializer. D11=0: Activates software power-down on Channel 4 Serializer. D10=0: Activates software power-down on Channel 3 Serializer. D9=0: Activates software power-down on Channel 2 Serializer. D8=0: Activates software power-down on Channel 1 Serializer.
7:0	SW_RSTB	RW	FF 'h	SW_RSTB is the active low software reset for individual serializers or deserializers. SW_RSTB should be LOW for more than 10us. During software reset, the MDIO serial interface remains functional. Software reset can be activated only during normal operating mode (i.e. LSLB and HSLB are both HIGH). The user is required to program SW_RSTB high to exit software reset. The RESETB pin overrides SW_RSTB. D7=0: Activates software reset on Channel 4 Deserializer. D6=0: Activates software reset on Channel 3 Deserializer. D5=0: Activates software reset on Channel 2 Deserializer. D4=0: Activates software reset on Channel 1 Deserializer. D3=0: Activates software reset on Channel 4 Serializer. D2=0: Activates software reset on Channel 3 Serializer. D1=0: Activates software reset on Channel 2 Serializer. D0=0: Activates software reset on Channel 1 Serializer.

Device Identifier Register 1 (Offset=30.2)
Package Identifier Register 1 (Offset=30.14)

Bit	Bit Name	Access	Default	Description
15:0	OUI_MSB	RO	A000 'h	OUI (Organizationally Unique Identifier) MSB Bits 3 to 18 of the OUI are stored in bits 15 to 0 of this register. National's OUI is 080017 'h

Functional Descriptions (Continued)

Device Identifier Register 2 (Offset=30.3)
Package Identifier Register 2 (Offset=30.15)

Bit	Bit Name	Access	Default	Description
15:10	OUI_LSB	RO	01 0000 'b	OUI LSB Bits 19 to 24 of the OUI are mapped to bits 15 to 10 of this register.
9:4	VNDR_MDL	RO	10 0000 'b	Vendor Model Number Bits 9 to 4 contain the 6-bit vendor model number. Bit 9 is the MSB.
3:0	REV_NUM	RO	1001 'b	Model Revision Number Bits 3 to 0 contain the 4-bit model revision number. This field will be incremented for all major device changes.

Loopback Control Register (Offset=30.4)

Bit	Bit Name	Access	Default	Description
15:2	Reserved	NA		Reserved
1:0	LP_BK	RW	11 'b	Software control for internal loopback test modes. The user is required to set LP_BK to high to exit loopback mode and return to the normal operating mode. The LSLB and HSLB pins override the software loopback control bits. **D1 D0** 1 1 Normal operating mode. 1 0 LVDS loopback (also called Local serial loopback). 0 1 High-speed loopback (also called Line Loopback). 0 0 Not recommended, defaulted to the LVDS loopback.

TX Signal Conditioning Control Register 1 (Offset=30.5)

Bit	Bit Name	Access	Default	Description
15:12	DE_EMP_CH	RW	0000'b	Select the individual serializer for driver de-emphasis programming. D15=1: Ch.4 serializer D14=1: Ch.3 serializer D13=1: Ch.2 serializer D12=1: Ch.1 serializer
11	Reserved	NA	0'b	Reserved
10:7	A1_LSB	RW	000'b	A1_LSB is a 3-bit number mapped into bits 3:0 of coefficient A1 for the Transmit de-emphasis filter.
6:1	A0	RW	000000'b	A0 is a 6-bit number mapped into bits 5:0 of coefficient A0 for the Transmit de-emphasis filter
0	Reserved	NA	0'b	Reserved

Functional Descriptions (Continued)

TX Signal Conditioning Control Register 2 (Offset=30.6)

Bit	Bit Name	Access	Default	Description
15:12	Reserved	NA	0000'b	Reserved
11:4	A2	RW	00'h	A2 is an 8-bit number mapped into bits 7:0 of coefficient A2 for the Transmit de-emphasis filter.
3:1	A1_MSB	RW	000'b	A1_MSB is a 3-bit number mapped into bits 6:4 of coefficient A0 for the Transmit de-emphasis filter.

Status Register (Offset=30.8)

Bit	Bit Name	Access	Default	Description
15:14	DEV_PRESENT	RO	8000 'h	**D15 D14** 1 0 Device responding at this address. 1 1 No device responding. 0 1 No device responding. 0 0 No device responding.
13:0	Reserved	Do not Access		

Functional Descriptions (Continued)

Control Register 2 (Offset=30.11)

Bit	Bit Name	Access	Default	Description
15:12	DISABLE_LVDS	RW	0 'h	Disable the LVDS output stages of individual deserializer, during which the LVDS outputs are held at logic high (+VOD). D15=1: Disable LVDS outputs of CH 4 DES (R2[5–8]±). D14=1: Disable LVDS outputs of CH 3 DES (R2[1–4]±). D13=1: Disable LVDS outputs of CH 2 DES (R1[5–8]±). D12=1: Disable LVDS outputs of CH 1 DES(R1[1–4]±). The user is required to set D15:12 to 0'h for normal operating mode.
11:8	DISABLE_HT	RW	0 'h	Disable the high-speed CML output stage of individual serializer, during which both the high-speed outputs HT+ and HT– are forced to static high. During LVDS loopback (local loopback) test mode, DISABLE_HT is the default mode. When EN_BIST_TX is activated, DISABLE_HT is automatically overridden. D11=1: Disable high-speed CML outputs of CH 4 SER (HT4±). D10=1: Disable high-speed CML outputs of CH 3 SER (HT3±). D9=1: Disable high-speed CML outputs of CH 2 SER (HT2±). D8=1: Disable high-speed CML outputs of CH 1 SER (HT1±). The user must set D11:8 to 0'h for normal operating mode.
7:4	EN_BIST_RX	RW	0 'h	Enables built-in-self-test (BIST) of individual deserializer. The receiver will start looking for synchronization header from the incoming bit stream. When header is detected, the error detection function is activated. Any error detected will be reported to bits 7:0 of BIST Status Registers. To avoid synchronization problems, the user must activate the deserializer's BIST mode (EN_BIST_RX) and the serializer's BIST mode (EN_BIST_TX) synchronously. It is important for user to deactivate the BIST mode of the deserializer (de-assert EN_BIST_RX), then deactivate the BIST mode of the serializer (de-assert EN_BIST_TX) in order to properly exit from self-test. Duration (total bits sent) is controlled by the user and is calculated based on operating data rate and duration of test. Note - the BIST function overrides output enable controls. D7=1: Enables BIST for Channel 4 Deserializer. D6=1: Enables BIST for Channel 3 Deserializer. D5=1: Enables BIST for Channel 2 Deserializer. D4=1: Enables BIST for Channel 1 Deserializer. The user is required to set EN_BIST_RX to 0'h for normal operating mode.

Functional Descriptions (Continued)

Bit	Bit Name	Access	Default	Description
3:0	EN_BIST_TX	RW	0 'h	Enables built-in-self-test (BIST) of individual serializer. The selected test pattern will be sent out at HT± of the serializer. When EN_BIST_TX is de-asserted, the last data word is sent out before terminating the self-test test mode. Duration (total bits sent) is controlled by the user and is calculated based on operating data rate and duration of test. Please see the EN_BIST_RX section for the appropriate steps to properly synchronize the serializer and deserializer. Note - the BIST function overrides output enable controls. D3=1: Enable BIST of Channel 4 Serializer. D2=1: Enable BIST of Channel 3 Serializer. D1=1: Enable BIST of Channel 2 Serializer. D0=1: Enable BIST of Channel 1 Serializer. The user is required to set EN_BIST_TX to 0'h for normal operating mode.

BIST TX Control Register (Offset=30.12)
BIST RX Control Register (Offset=30.13)

Bit	Bit Name	Access	Default	Description
15:14		NA		Reserved
13:9	SET_ONE	RW	1F 'h	The 5-bit value of SET_ONE (0 to 31) programs the duration of the continuous one's that come before or after PRW pattern used in test patterns ZERO-PRW-ONE or ONE-PRW-ZERO. Duration = (SET_ONE+1) * 1.6 ns. A SET_ONE value of 0 is the same as a SET_ONE value of 31.
8:4	SET_ZERO	RW	1F 'h	The 5-bit value of SET_ZERO (0 to 31) programs the duration of the continuous zero's that come before or after PRW pattern used in test patterns ZERO-PRW-ONE or ONE-PRW-ZERO. Duration = (SET_ZERO+1) * 1.6 ns. A SET_ZERO value of 0 is the same as a SET_ZERO value of 31.
3:2	PRW_SEL	RW	00 'b	Selects the built-in pseudo-random word patterns. **D3 D2** 0 0 PRW (2^7 –1) 0 1 Not used. 1 0 Not used. 1 1 Not used.
1:0	PAT_SEL	RW	01 'b	Selects test patterns for running built-in-self-test. **D1 D0** 0 0 Selects memory-based fixed test pattern. See Registers 30.16–31 and 30.32–47 for details. 0 1 Selects PRW patterns 1 0 Selects ZERO-PRW-ONE test pattern. Continuous zero's followed by PRW, then continuous one's. 1 1 Selects ONE-PRW-ZERO test pattern. Continuous one's, followed by PRW, then continuous zero's.

Functional Descriptions (Continued)

TX Fixed Pattern Registers (Offset=30.16–30.31)

Bit	Bit Name	Access	Default	Description
15:0	TX_PAT	RW	AAAA 'h	There are 16 registers (30.16 to 30.31) for users to store 256 bits of user-defined data bits to be transmitted at HT when the serializer's built-in-self-test mode is turned on. All 256 bits are transmitted sequentially. D0 of register 30.16 is the first bit transmitted. After the last bit (D15 of register 30.31) is transmitted, the SCAN50C400 will loop the test pattern and restart at D0 of register 30.16, forming a repeating fix pattern.

RX Fixed Pattern Registers (Offset=30.32–30.47)

Bit	Bit Name	Access	Default	Description
15:0	RX_PAT	RW	AAAA 'h	There are 16 registers (30.32 to 30.47) for users to store 256 bits of user-defined data bits that are used as the expected received bits for the incoming bit stream. When the deserializer's BIST mode is turned on and fix pattern is selected, the on-chip BIST Error Detector will compare the recovered data bits against the user-defined expected data stored in registers 30.32–30.47, once valid synchronization header is detected. D0 of register 30.32 is the first bit received.

TX CML VOD Control Register (Offset=30.49)

Bit	Bit Name	Access	Default	Description	
15:13	Reserved	NA		Reserved.	
12:10	VOD4	RW	001'b	VOD4 is a 3-bit control that selects one of the 8 output levels at HT4.	
9:7	VOD3	RW	001'b	VOD3 is a 3-bit control that selects one of the 8 output levels at HT3.	
6:4	VOD2	RW	001'b	VOD2 is a 3-bit control that selects one of the 8 output levels at HT2.	
3:1	VOD1	RW	001'b	VOD1 is a 3-bit control that selects one of the 8 output levels at HT1.	
				VOD4/ VOD3/ VOD2/ VOD1	Differential output level in mVp-p
				000	1300
				001	1100
				010	860
				011	840
				100	810
				101	760
				110	700
				111	630
0	Reserved	NA			Reserved.

Functional Descriptions (Continued)

BIST Status Registers **Channel 1 (Offset=30.57)**
Channel 2 (Offset=30.58)
Channel 3 (Offset=30.59)
Channel 4 (Offset=30.60)

Bit	Bit Name	Access	Default	Description
15:12	Reserved.	NA		Reserved.
11	BIST_HDR	RO	0'b	Transmitter sends a header and then will stay High until BIST is deactivated.
10	BIST_ST	RO	0 'b	BIST_ST=1 indicates detection of synchronization header.
9	BIST_END	RO	0 'b	On receipt of user's command to terminate the deserializer's BIST mode (D7–4 of Control Register 2, offset 30.11), the SCAN50C400 will complete processing the last data word, before exiting the self-test test mode. BIST_END is set high to indicate completion of receiver's BIST error detection.
8	BIST_OK	RO	0 'b	BIST_OK=0 indicates no error has been detected. BIST_OK is valid only after both BIST_ST and BIST_END are at logic 1 states.
7:0	BIST_ERR	RO	FF 'h	BIST_ERR is an 8-bit error counter that contains the number of error detected by the internal BIST error detector. When the error counter overflow, it will stay at FF'h. BIST_ERR is valid only if both BIST_ST and BIST_END are at logic 1 states. BIST_ERR is cleared to zero after reset, or after BIST has been restarted. BIST_ERR has a value of 0–255.

Referenced Figures

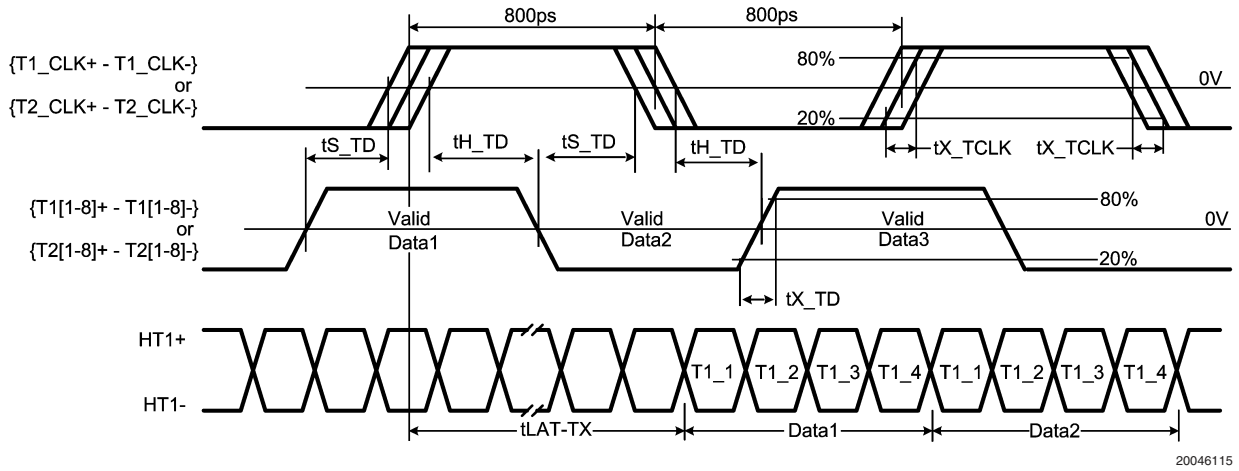


FIGURE 9. Transmit Data Timing

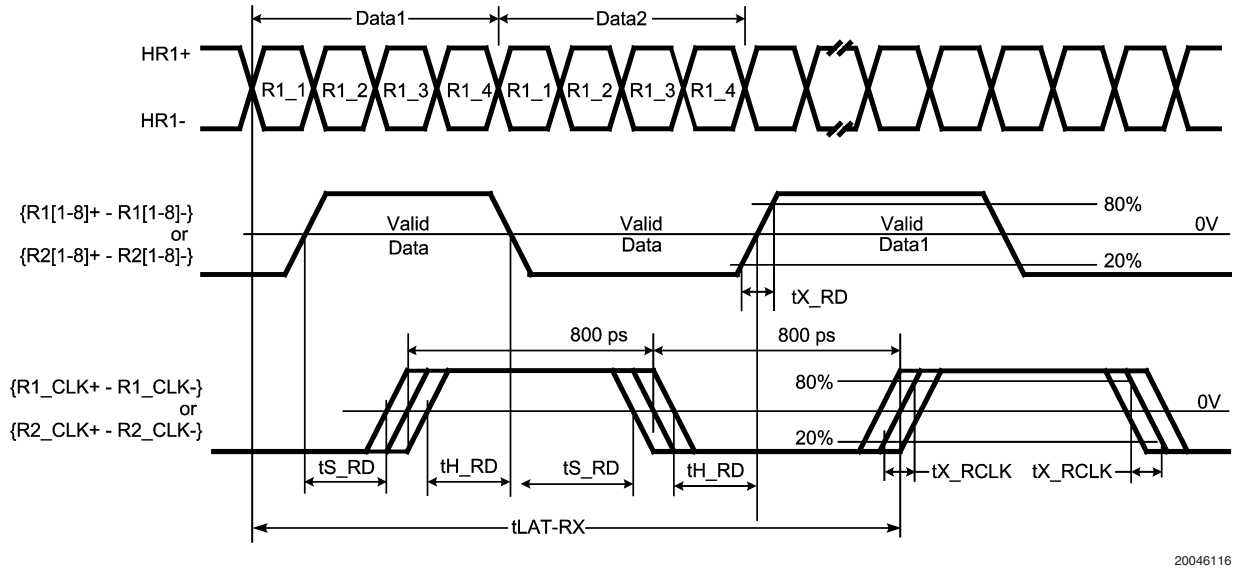
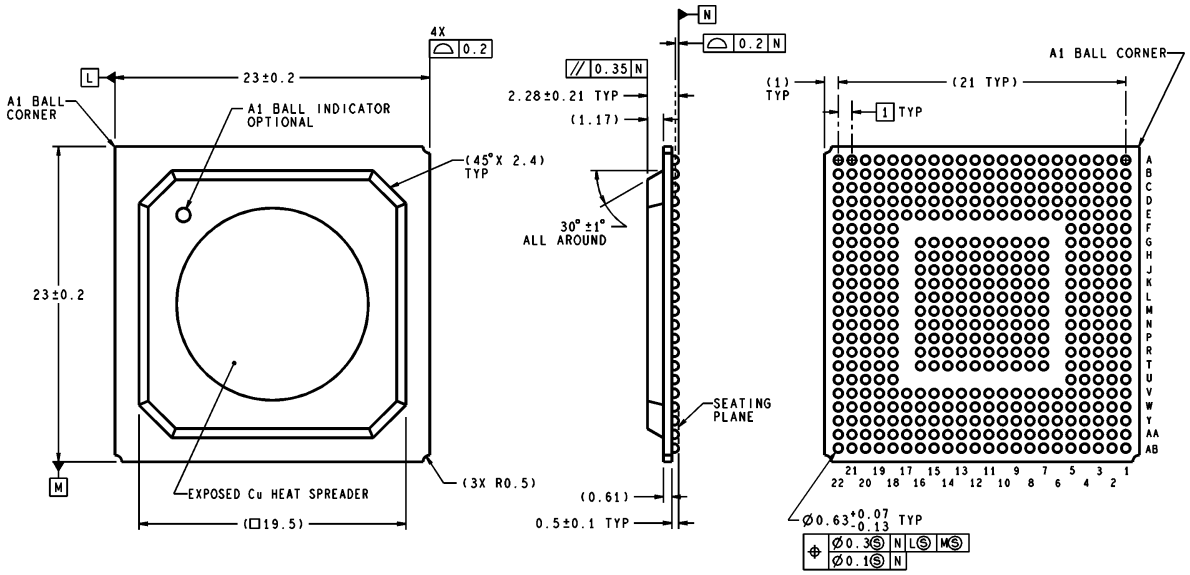


FIGURE 10. Receive Data Timing

Physical Dimensions inches (millimeters) unless otherwise noted



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UFJ440A (Rev A)

Order Number SCAN50C400UT
NS Package Number UFJ440A

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