ML4876*

LCD Backlight Lamp Driver with Contrast

GENERAL DESCRIPTION

The ML4876 is an ideal solution for driving small cold cathode fluorescent tubes (CCFL) used in liquid crystal display (LCD) backlight applications. It provides the dimming ballast control and the contrast control for the LCD display.

By utilizing differential drive the ML4876 can deliver the same light output with significantly less input power compared to existing single ended drive schemes. Improvements as high as 30% can be realized when using low power lamps and advanced LCD screen housings. This increased light output is achieved because the differential drive configuration is much less sensitive, and therefore less power is wasted in the capacitive parasitics that exist in the backlight housing. An additional benefit of this configuration is an even distribution of light.

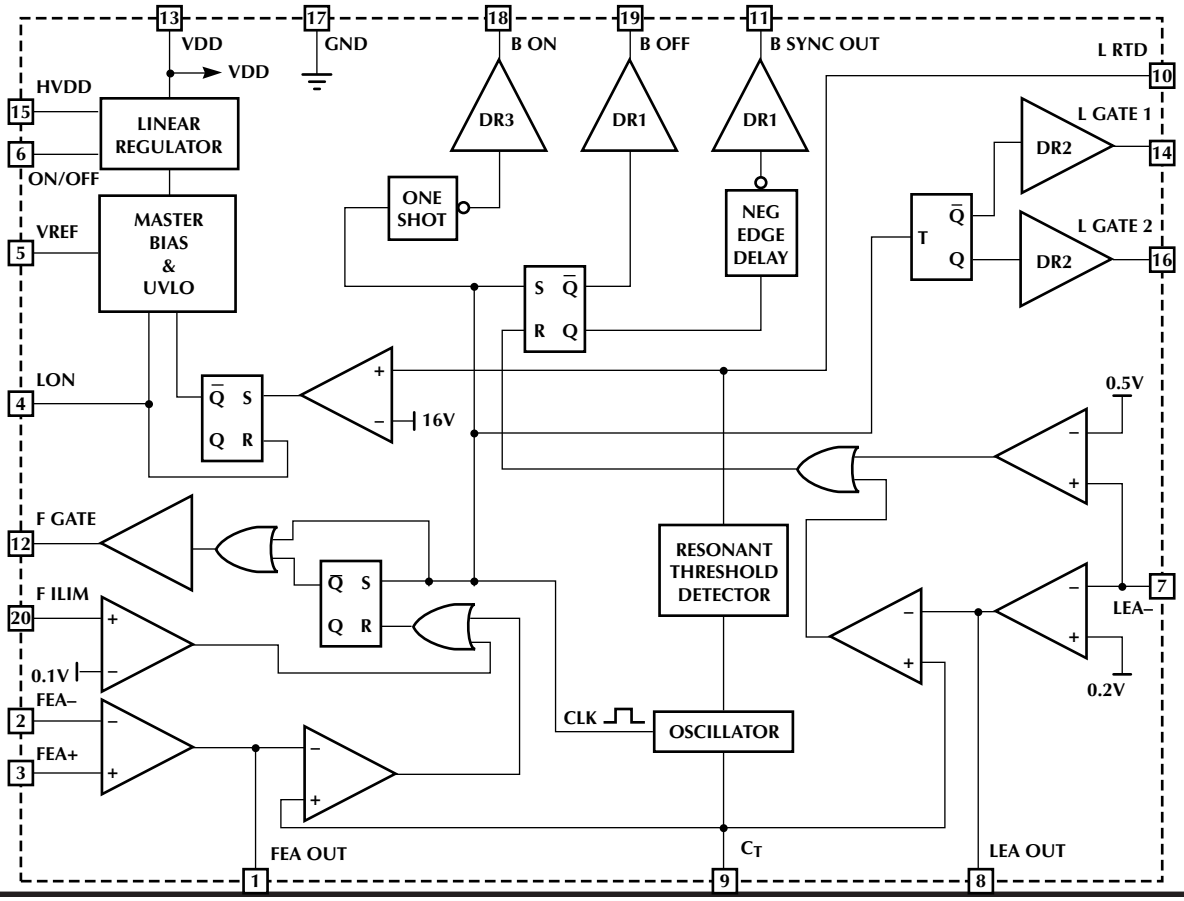
The ML4876 is optimized for portable applications where high efficiency is critical to maximize battery life. The high efficiency is achieved by a resonant scheme with zero voltage switching.

FEATURES

- Backlight lamp driver with differential drive
- Up to 30% lower power for same light output
- Low standby current (< 10µA)
- Improved efficiency (≈95%)
- Allows all N-channel MOSFET drive
- Low switching losses
- Resonant threshold detection
- Buck regulator uses synchronous rectification

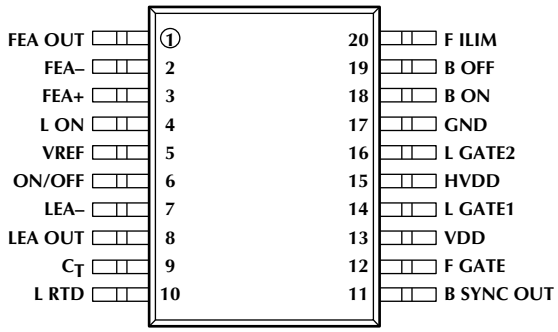
* THIS PART IS END OF LIFE AS OF JULY 1, 2000

BLOCK DIAGRAM



PIN CONFIGURATION

ML4876
20-Pin SSOP (R20)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	FEA OUT	Output of flyback (contrast) error amplifier
2	FEA–	Negative input of flyback (contrast) error amplifier
3	FEA+	Positive input of flyback (contrast) error amplifier
4	L ON	Logic input. A ″0″ on this pin disables the lamp driver section only
5	VREF	Voltage reference output
6	ON/OFF	Logic input. A ″0″ on this pin disables the linear regulator
7	LEA–	Negative input for lamp error amplifier
8	LEAOUT	Output of lamp error amplifier
9	C_T	Oscillator timing capacitor
10	L RTD	Input to resonant threshold detector
11	B SYNC OUT	Output of MOSFET driver. Connects to gate of synchronous FET catch diode.
12	F GATE	Connects to gate of MOSFET in primary side of contrast control
13	VDD	Output of linear regulator. Positive power for IC.
14	L GATE1	Output of MOSFET driver. Connection to gate of one side of inverter FET drive pair
15	HVDD	Battery power input to linear regulator
16	L GATE2	Output of MOSFET driver. Connection to gate of one side of inverter FET drive pair
17	GND	Ground
18	B ON	Connection to primary side of gate pulse transformer
19	B OFF	Output of MOSFET driver. Connection to gate of FET that disables the input power.
20	F ILIM	Input to current limit comparator

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Supply Current (I_{CC}) 75mA
Output Current, Source or Sink 250mA
Voltage on HVDD 20V
Current into L RTD ..... ±10mA
Transient Voltage on B ON 9V
Voltage on Any Other Pin ..... –0.3V to VDD +0.3V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering 10 sec.) ..... 260°C
Thermal Resistance (q_{JA}) Plastic SSOP ..... 100°C/W

OPERATING CONDITIONS

Temperature Range
ML4876C ..... 0°C to 70°C
ML4876E ..... –20°C to 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, VDD = 5V ±5%, C_T = 47pF, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT REGULATOR						
Error Amplifier						
	Open Loop Gain		60	70		dB
	Bias Point	Closed loop	0.18	0.2	0.22	V
	Output High	I_{LOAD} = 5µA	2.8	3.0		V
	Output Low	I_{LOAD} = 25µA		0.4	0.7	V
	Bandwidth (–3dB)			1		MHz
	Input Voltage Range		–0.3	0.2	VREF	V
	Input Bias Current			50	100	nA
Current Limit Comparator						
	Current Threshold		450	500	550	mV
	Input Bias Current	V_{LILIM} = 0.1V		50	100	nA
	Propagation Delay	(Note 2)		30		ns
Output Drivers						
	Output High - B SYNC OUT, B OFF	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
	Output Low - B SYNC OUT, B OFF	I_{LOAD} = 12mA		0.2	0.375	V
	Rise & Fall time - B SYNC OUT, B OFF	C_{LOAD} = 100pF		20	50	ns
	Output High - B ON	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
	Output Low - B ON	I_{LOAD} = 50mA		0.2	0.375	V
	Fall Time - B ON	C_{LOAD} = 2400pF (Note 2)		45	80	ns
	ONE SHOT Pulse Width		100	150	200	ns
	DELAY TIMER Delay Time		20	35	55	ns
FLYBACK REGULATOR						
Error Amplifier						
	Open Loop Gain		60	70		dB
	Offset Voltage		–15		15	mV
	Output High	I_{LOAD} = 5µA	2.8	3.0		V
	Output Low	I_{LOAD} = 25µA		0.4	0.7	V

ELECTRICAL CHARACTERISTICS (Continued)

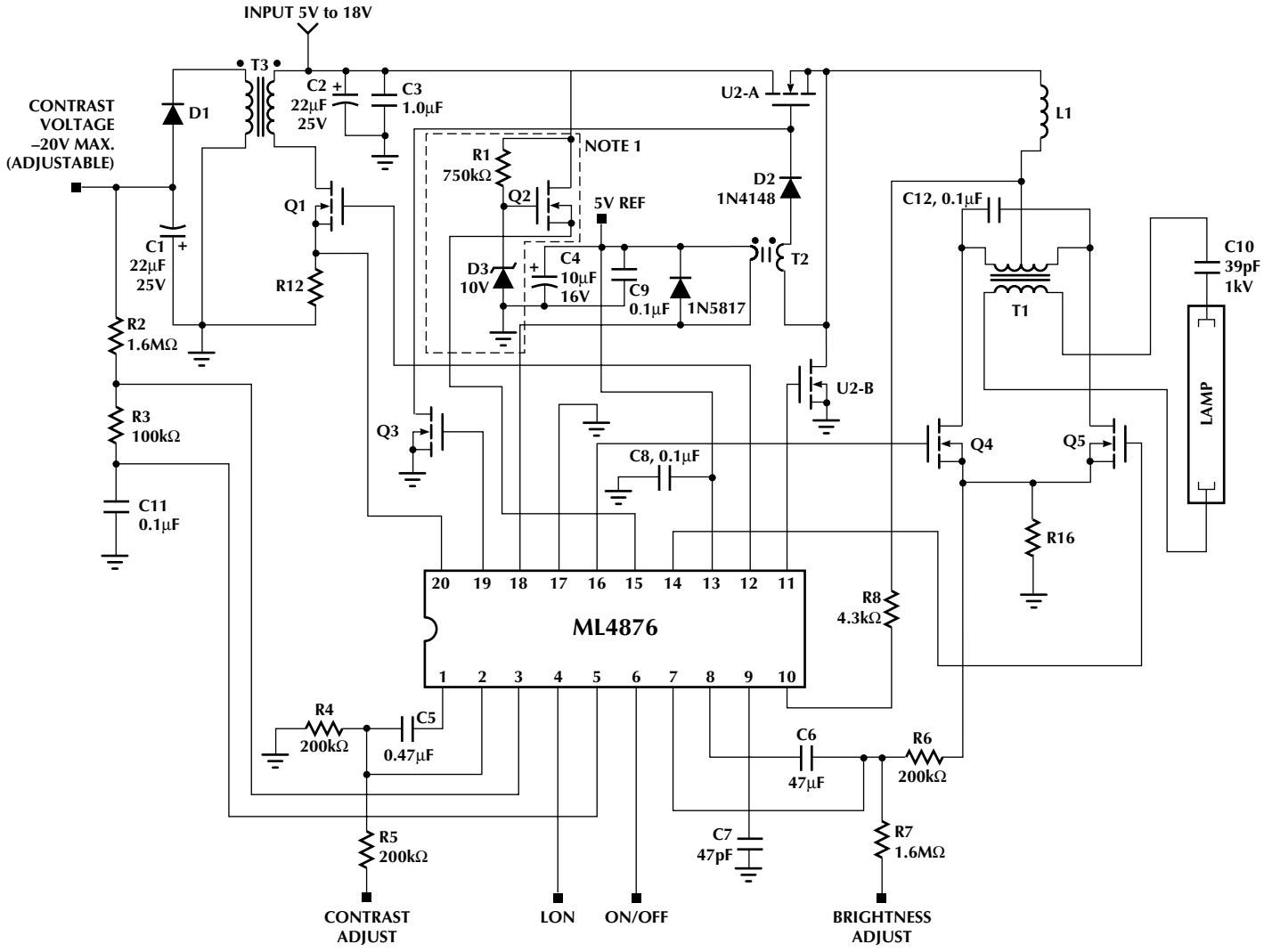
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
FLYBACK REGULATOR (Continued)						
Current Limit Comparator						
	Threshold		70	100	130	mV
	Input Bias Current	V_{LILIM} = 0.1V		50	100	nA
	Propagation Delay			125	250	ns
Output Drivers						
	Output High - F Gate	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
	Output Low - F Gate	I_{LOAD} = 50mA		0.2	0.375	V
	Rise & Fall Time	C_{LOAD} = 1000pF		20	50	ns
HIGH VOLTAGE INVERTER						
Oscillator						
	Nominal Frequency		59	70	81	kHz
	Discharge Current	V_{CT} = 2V	500	700	900	µA
	Peak Voltage		2.3	2.5	2.7	V
	Valley Voltage		0.8	1	1.2	V
	Output Drivers					
	Output High - L GATE 1, 2	VDD = 5V, I_{LOAD} = 12mA	4.625	4.8		V
	Output Low - L GATE 1, 2	I_{LOAD} = 50mA		0.2	0.375	V
	Rise & Fall Time - L GATE 1, 2	C_{LOAD} = 1000pF		20	50	ns
Resonant threshold Detector						
	Threshold		0.75	1.1	1.45	V
	Hysteresis		250	500	750	mV
Lamp Out Detect						
	Threshold		16	18	20	V
Under Voltage Detector						
	Start Up Threshold		3.8	4.1	4.4	V
	Hysteresis		150	300	450	mV
Logic Interface (On/Off, L ON)						
	VIH		2.6			V
	VIL				0.5	V
	Input Bias Current	V_I = 3V		10	25	µA
Linear Regulator						
	Regulator Voltage (VDD)	HVDD = 12V	4.75	5.0	5.35	V
	Regulator Source Current	External to device		10		mA
	Drop Out Voltage	I_{HVDD} = 1mA		30	90	mV
	Drop Out Voltage	I_{HVDD} = 5mA		125	275	mA
	HVDD Input Voltage Range		5		18	V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
	VDD Supply Current (No Load)	On/Off = 3V, L_{ON} = 3V		0.45	0.6	mA
	VDD Supply Current	On/Off = 3V, L_{ON} = 0V		200	350	µA
	VDD Supply Current	On/Off = "0", HVDD = 12V			10	µA
	VREF Output Voltage	T_A = 25°C	2.47	2.5	2.53	V
	VREF Load Regulation	I_{VREF} = 25µA		10	20	mV
	VREF Line Regulation			20	30	mV
	VREF Line, Load, Temp		2.465	2.5	2.535	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

Note 2: Actual load is 1200pF. The 2:1 transformer reflects an effective 2400pF.



NOTE 1
R1, D3, Q2 ARE OPTIONAL AND ALLOWS A BATTERY VOLTAGE RANGE FROM 7V TO 28V. REMOVING THESE COMPONENTS AND CONNECTING DIRECTLY TO THE INPUT VOLTAGE ALLOWS 5.0 TO 18V.

Figure 1. ML4876 Typical Application Schematic

FUNCTIONAL DESCRIPTION

The ML4876 consists of a PWM regulator, a lamp driver/ inverter, a linear regulator, a flyback regulator, and control circuits. This IC, in conjunction with external components, converts a DC battery voltage into the high voltage and high frequency ac signal required to start and drive miniature cold cathode fluorescent lamps. In addition it generates the DC voltage for the contrast requirements of LCD screens. A typical application circuit is shown in Figure 1. Please refer to Application Note 32 for detailed application information beyond what is presented here.

Note: Please read the Power Sequencing section below prior to using the ML4876.

LAMP DRIVER

The lamp driver, sometimes referred to as a lamp inverter, is comprised of a PWM regulator and a Royer type inverter circuit to drive the lamp. The PWM regulator, in a buck configuration, controls the magnitude of the lamp current to provide the dimming capability. Figure 2 shows a simplified circuit to more easily illustrate the operation of the circuit.

Due to the presence of the buck inductor, L1, the circuit shown in Figure 2 is essentially a current fed parallel loaded resonant circuit. Lm is the primary inductance of the output transformer, T1, which tunes with the resonant capacitor C_R to set the resonant frequency of the inverter. The oscillator frequency is always set lower than the natural resonant frequency to ensure synchronization. The current source IC models the current through the buck inductor L1.

The MOSFETs (Q4 and Q5) are alternately turned on with a constant 50% duty cycle signal (L GATE1, L GATE2) at one-half the frequency of the oscillator. In this way each transistor pulses, or excites, the resonant tank on each half cycle. The combination of these two signals appear across the primary winding of the output transformer as a sinusoidal waveform. This voltage is multiplied by the step-up turns ratio of the output transformer and impressed across the lamp.

The output transitions are controlled by feedback through the L RTD pin by sensing the voltage at the center tap of the output transformer. Each time this signal reaches the minimum resonant threshold detection point an internal clock pulse is generated to keep the system synchronized. Figure 3 shows some of these representative waveforms at the important nodes of the circuit.

The PWM regulator is comprised of a MOSFET (U2-A), inductor L1, and the gate control and drive circuitry as shown in Figure 1. A signal with a constant pulse width of 150ns is applied to the primary of the 2:1 pulse transformer T2, rectified by diode D2, and used to charge the gate capacitance of U2-A, thereby turning it on. The turn off is controlled by discharging this capacitance through MOSFET U2-B. The pulse width of the signal on the gate of U2-B (B OFF) varies according to the amplitude of the feedback signal on LEA–, which is proportional to the AC current flowing in the lamp. This feedback signal is developed by monitoring the current through resistor R6 in the common source connection of the inverter MOSFETs (Q4 and Q5). The lamp current, and therefore brightness, is adjusted by varying the voltage applied to R7 at the brightness adjust control point. Increasing this voltage decreases the brightness.

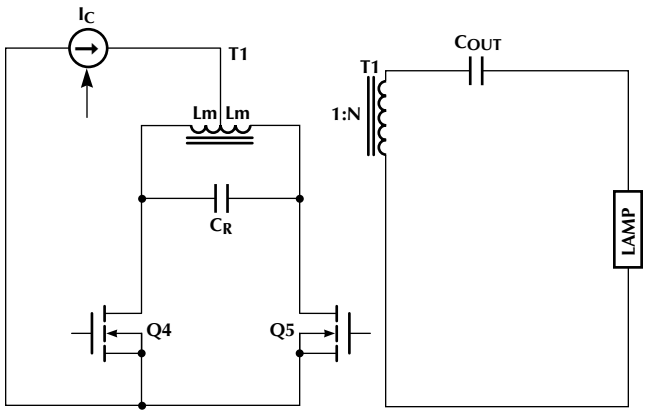


Figure 2. Simplified Lamp Driver Circuit

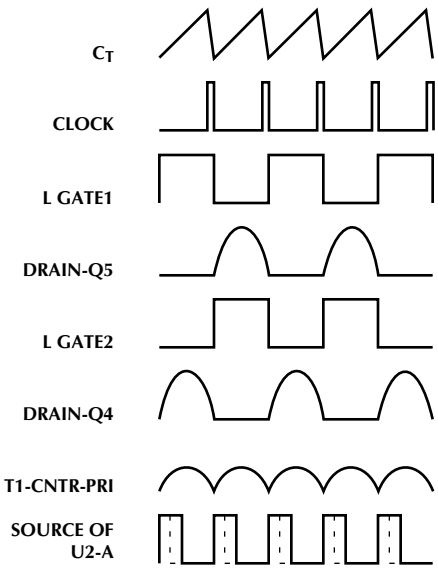


Figure 3. Operating Waveforms of the Lamp Driver Section

FUNCTIONAL DESCRIPTION (Continued)

CONTRAST CONTROL GENERATOR

The contrast voltage generator is a separate regulator in a flyback configuration. In conjunction with the external transformer (T3), MOSFET (Q1), diode (D1), and assorted capacitors and resistors, it provides an adjustable DC output contrast voltage necessary to drive LCD screens. The voltage is adjusted by controlling the voltage applied to R5 at the contrast adjustment point.

The contrast voltage can be made either positive or negative simply by changing the connection of the external components. The schematic shown in Figure 1 is connected for a negative voltage. Please refer to Application Note 32 for the circuit connection for a positive output voltage.

OSCILLATOR

The frequency of the oscillator in the ML4876 is set by selecting the value of C_T.

Figure 4 shows the oscillator frequency versus the value of C_T. This nomograph may be used to select the appropriate value of C_T to achieve the desired oscillator frequency.

LINEAR REGULATOR

A linear voltage regulator is provided to power the low voltage and low current control circuitry on the ML4876. This is typically used when there is no separate 5V supply available at the inverter board. For operation up to 18V the linear regulator is used by connecting HVDD to the input battery voltage. For operation over 18V, a MOSFET and a resistor (Q2 and R1, Figure 1) are connected as shown. The MOSFET is required to stand off the high voltage.

LAMP OUT DETECT

In those cases when there is no lamp connected, or the connection is faulty, the output voltage of the lamp driver circuit will tend to rise to a high level in an attempt to start the nonexistent lamp. The lamp out detect circuit on the ML4876 will detect this condition by sensing the center tap voltage on the primary of the output transformer (T1) on the L RTD pin. When this voltage exceeds 16V, an internal latch is set and the lamp driver goes into a shutdown mode. The logic control pin L ON must be cycled low, then high to reset the latch and return the lamp driver to the normal state.

LOGIC CONTROL

The ML4876 is controlled by a two logic inputs, L ON and ON/OFF. A logic level high on the L ON pin enables just the lamp driver. A logic zero on the L ON pin disable the lamp driver only. A logic level high on the ON/OFF pin enable the complete circuit. A logic level low on the ON/OFF pin puts the circuit into a very low power state.

POWER SEQUENCING

It is important to observe correct power and logic input sequencing when powering up the ML4876. The following procedure must be observed to avoid damaging the device.

1. Apply the battery power to HVDD

2. Apply the VDD voltage (if HVDD is not used). With HVDD connected this voltage is supplied by the internal regulator on the ML4876.

3. Apply a logic high to the ON/OFF input. This will enable the internal linear regulator to ensure the VDD supply is on (when HVDD is used).

4. Apply a logic high to the L ON input.

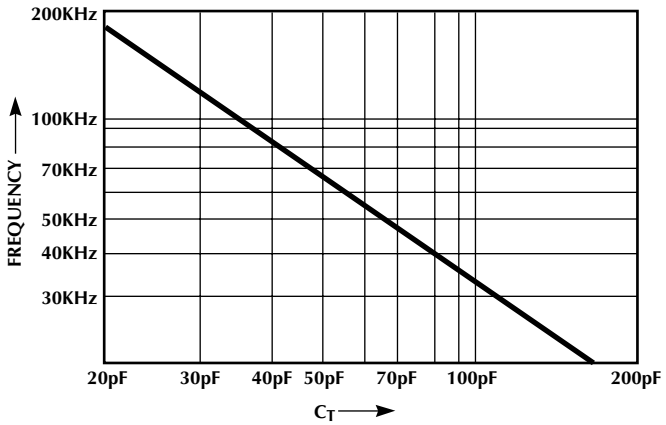
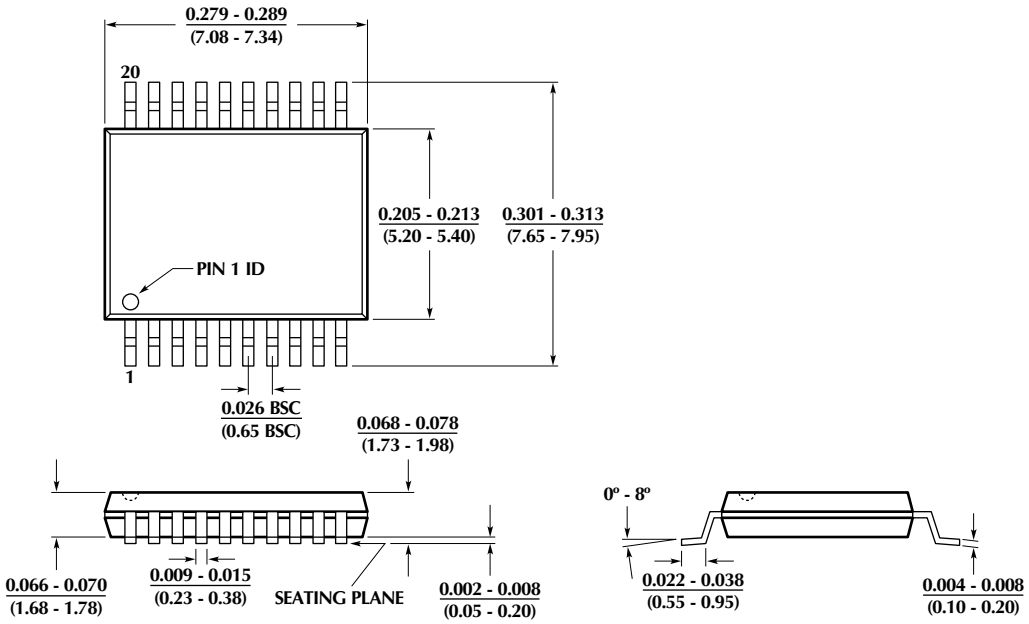


Figure 4. Frequency vs. C_T

PHYSICAL DIMENSIONS inches (millimeters)

Package: R20
20-Pin SSOP



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4876CR (END OF LIFE)	0°C to 70°C	20-Pin Molded SSOP (R20)
ML4876ER (OBSOLETE)	–20°C to 70°C	20-Pin Molded SSOP (R20)

2092 Concourse Drive
San Jose, CA 95131
Tel: (408) 433-5200
Fax: (408) 432-0295
www.microlinear.com