QE1M Device
Quad E1 Mapper
TXC-04252

DATA SHEET

FEATURES

- Add/drop four 2.048 Mbit/s signals from STM-1/VC-4, STS-3/AU-3 or STS-1 buses
- Independent add and drop bus timing modes
- Selectable HDB3 positive/negative rail or NRZ E1 interface. Performance counter provided for coding violations.
- Digital desynchronizer
- Drop buses are monitored for parity, loss of clock, upstream AIS and H4 multiframe errors
- Performance counters are provided for TU/VT pointer movements, BIP-2 errors and Far End Block Errors (FEBEs)
- TU/VTs are monitored for Loss Of Pointer, New Data Flags (NDFs), AIS, Remote Defect Indication (RDI), and size errors (S-bits)
- V5 Byte Signal Label Mismatch and Unequipped detection
- E1 facility and line loopbacks, generation of BIP-2 and FEBE errors, and send RDI capability
- Intel / Motorola / Multiplexed-compatible microprocessor bus interface with interrupt capability
- Programmable internal RISC processor implements VT-POH and VT-alarm handling
- J2 16-byte ETSI trail trace comparison
- Optional V4 receive and transmit byte access
- TU tandem connection processing (N2 byte)
- IEEE 1149.1 standard boundary scan
- Single +5 V ± 5 % power supply
- 160-lead plastic quad flat package or 208-lead PBGA (17 mm x 17 mm)

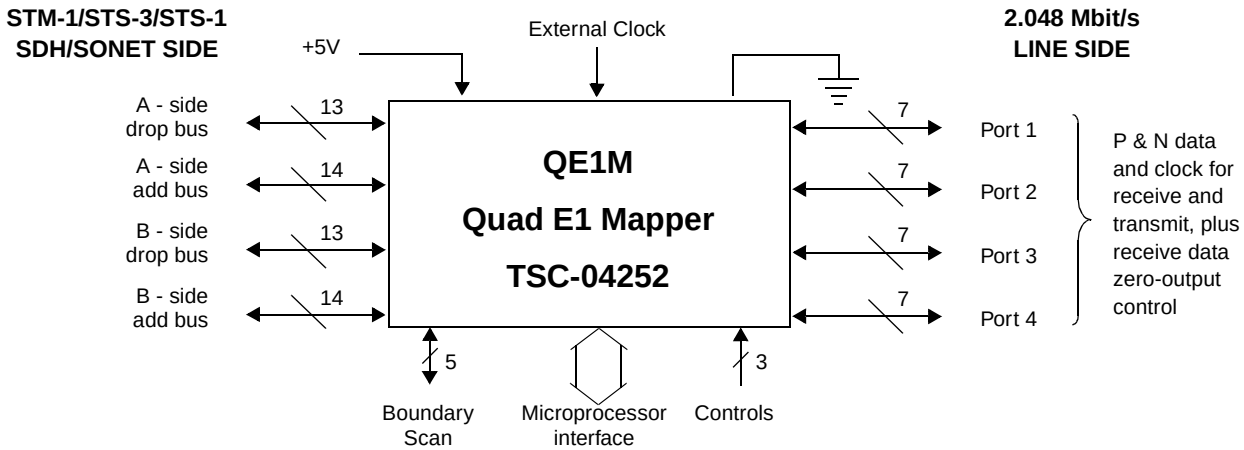
DESCRIPTION

The Quad E1 Mapper device is designed for add/drop multiplexer, terminal multiplexer, and dual and single unidirectional ring applications. Four E1 2.048 Mbit/s signals are mapped to and from asynchronous Tributary Unit-12 (TU-12) or Virtual Tributary 2 (VT2) formats. The QE1M interfaces to a multiple-segment, byte-parallel SDH/SONET-formatted bus at the 19.44 Mbit/s byte rate for STM-1/STS-3 operation or at the 6.48 Mbit/s byte rate for STS-1 operation. The E1 2.048 Mbit/s signals can be either HDB3 positive/negative rail- or NRZ-formatted signals. The QE1M provides performance counters, alarm detection, and the ability to generate errors and Alarm Indication Signals (AIS). E1 facility and line loopback capabilities are also provided.

The QE1M bus interface is used to connect to other TranSwitch devices such as the STM-1/STS-3/STS-3c Overhead Terminator (SOT-3), TXC-03003 or TXC-03003B, to form an STM-1/STS-3 add/drop or terminal system.

APPLICATIONS

- STM-1/STS-3/STS-1 to 2.048 Mbit/s add/drop mux/demux
- Unidirectional or bidirectional ring applications
- STM-1/STS-3/STS-1 termination terminal mode multiplexer
- STM-1/STS-3/STS-1 test equipment



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BLOCK DIAGRAM

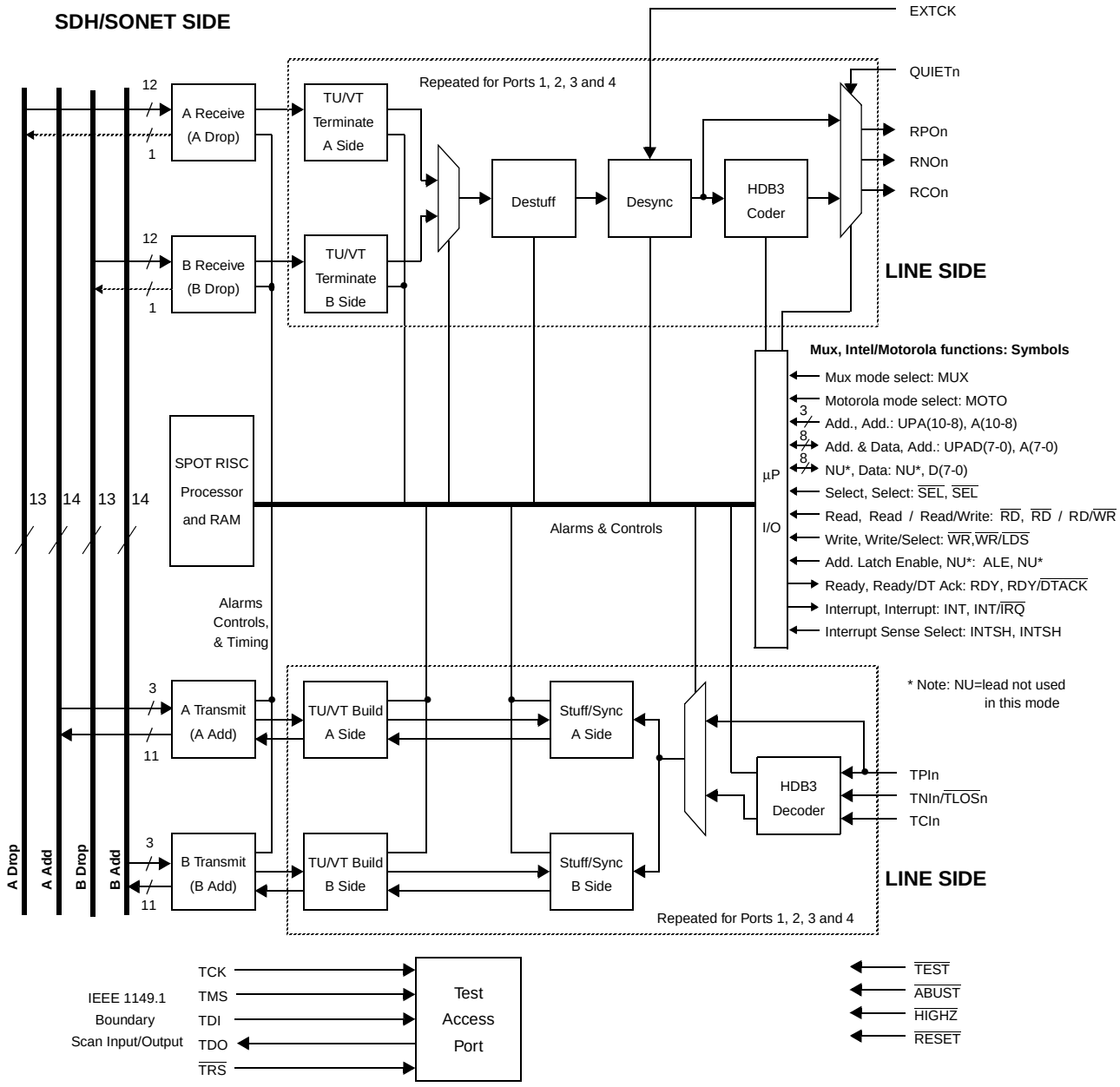


Figure 1. QE1M TXC-04252 Block Diagram

BLOCK DIAGRAM DESCRIPTION

The block diagram for the Quad E1 Mapper is shown in 1. The Quad E1 Mapper interfaces to four buses, designated as A Drop, B Drop, A Add, and B Add. The four buses run at the STM-1/STS-3 rate of 19.44 Mbyte/s, or at the STS-1 rate of 6.48 Mbyte/s. For North American applications, the asynchronous E1 signals are carried in floating Virtual Tributary 2 (VT2) format in a Synchronous Transport Signal - 1 (STS-1), or in an STS-1 that is carried in a Synchronous Transport Signal - 3 (STS-3). For ITU-T applications, the E1 signals are carried in floating mode Tributary Unit - 12 (TU-12) format in the STM-1 Virtual Container - 4 structure (VC-4) using Tributary Unit Group - 3 (TUG-3), or in the STM-1 Virtual Container - 3 structure (VC-3) using Tributary Unit Group -2 (TUG-2) mapping schemes. Four E1 signals can be dropped from one bus (A Drop or B Drop), or from both of the drop buses, to the E1 lines. Four asynchronous E1 signals are converted into TU-12 or VT2 format and are added to either of the add buses, or both, depending upon the mode of operation. When the Quad E1 Mapper is configured for drop bus timing, the add buses are, by definition, byte- and multiframe-synchronous with their like-named drop buses, but are delayed by one byte time because of internal processing. For example, if a byte in the STM-1 Virtual Container - 4 structure (VC-4) using Tributary Unit Group - 3 (TUG-3), TU-12/VT2 is to be added to the A Add bus, the time of its placement on the bus is derived from the A Drop bus timing, and from software instructions specifying which TU/VT number is being dropped/added. When the device is configured for add bus timing, the add bus, parity, and add indicator signals are derived from the add clock, C1J1V1 and SPE signals.

The A Receive block is identical to the B Receive block. The TU/VT Terminate block is repeated 8 times, two for each port (A and B sides). The Destuff, Desync, and HDB3 Coder blocks are repeated four times, one for each port. The interface between a drop bus and Receive block consists of 12 input leads, and an optional output lead: a byte clock, byte-wide data, a C1J1 indicator which may be carrying a V1 indication making the signal a C1J1V1 indicator, an SPE indicator, and an odd parity bit for the last-named three signals. Parity is selectable by control bits for even parity and for the data byte only. The output lead is an optional TU/VT select indicator signal. The Drop C1J1V1 signal is used in conjunction with the Drop SPE signal to determine the location of the various pulses. The C1 pulse identifies the location of the C1 byte when the SPE signal is low. A single J1 pulse identifies the starting location of the J1 byte in the VC-4 format, when the SPE signal is high. Three J1 pulses are provided for the STS-3 format, each identifying the starting location of the J1 byte in each of the STS-1 signals.

The Quad E1 Mapper can operate with a V1 pulse in the C1J1V1 signal, or it can use an internal H4 detector for determining the location of the V1 pulse. The V1 pulse location is used to determine the location of the pointer byte V1. For STM-1 VC-4 operation, if the C1J1V1 signal is used, a single V1 pulse must occur three drop bus clock cycles every four frames following the J1 pulse when the SPE signal is high. For STS-3 operation, three V1 pulses must be present every four frames. Each of the three V1 pulses must be present three clock cycles after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 A. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte location is six clock cycles after the V1 pulse.

For STS-1 operation, one V1 pulse must be present if the C1J1V1 signal is used. The V1 pulse must occur on the next clock cycle after the J1 pulse, and when the SPE signal is high. The J1 pulse identifies the J1 byte location (defined as the starting location for the STS-1) in the POH bytes. In the next column (first clock cycle) the TUs start. Thus, the V1 pulse identifies the starting location of the first V1 byte in the signal. The rest of the V1 bytes for the 21 TU-12/VT2s are also aligned with respect to the V1 pulse (please see the first diagram in the Operation - Multiplex Format and Mapping Information section).

Each bus is monitored for parity errors, loss of clock, H4 multiframe alignment if selected, and an upstream SDH/SONET AIS indication. The Quad E1 Mapper can monitor either the TOH E1 bytes or the H1/H2 bytes for an AIS indication. Which E1 byte and H1/H2 bytes are selected is a function of the TU/VT selected.

Each TU/VT Terminate block (A and B side) performs pointer processing based on the location of the V1 and V2 bytes. The pointer bytes are monitored for loss of pointer, TU AIS indication, and NDF. The pointer tracking process is based on the latest ETSI standard, which also meets ANSI/Bellcore requirements. Pointer increments and decrements are also counted, and the SS-bits are monitored for the correct value. This block also monitors the various alarms found in the V5 and K4 (formerly known as Z7) bytes, including signal label mismatch detection, unequipped status detection, BIP-2 parity error detection and error counter, FEBE counter, and the three RDI indications. The Quad E1 Mapper performs a 16-byte J2 trail trace comparison on the channels selected. For 64-byte messages, the bytes are stored in a memory map segment for a microprocessor read cycle. The device also provides the TU tandem connection feature and performs the 16-byte message comparison for the N2 (formerly known as Z6) byte message.

A control bit for each port selects the TU/VT from either the A Drop or B Drop bus. The TU/VT is destuffed in the Destuff block using majority logic rules for the three sets of three justification control bits to determine if the two S-bits are data bits or frequency justification bits.

The Desync block removes the effects on the E1 output of systemic jitter that might occur because of signal mappings and pointer movements in the network. The Desync block contains two parts, a pointer leak buffer, and a E1 loop buffer. The pointer leak buffer can accept up to five consecutive pointer movements, and can adjust the effect over time. The E1 Loop Buffer consists of a digital loop filter, which is designed to track the frequency of the received E1 signal and to remove both transmission and stuffing jitter.

An option for each port provides either NRZ data, or an HDB3-encoded positive and negative rail signal for the E1 interface. Receive data (towards the E1 line), for all four channels, can be clocked out on either rising or falling edges of the clock. In addition, control bits are provided for forcing the data and clock signals to a high impedance state (tristate). A control lead is provided for forcing the output leads to the 0 state.

In the add direction, the Quad E1 Mapper accepts clock and either NRZ data or HDB3-encoded positive and negative rail signals. Data, for all four channels, can be clocked in on either the falling or rising edge of the clock. In the NRZ mode, an external loss of clock indication input signal can be provided. For the rail signal, coding violations are counted, and there is monitoring for loss of signal. An E1AIS detector is also provided.

The data signal is written into a FIFO in one of the eight Stuff/Sync blocks. Threshold modulation is used for the frequency justification process. Timing information from the drop bus or add bus is used to read the FIFO and perform the TU/VT justification process. This block permits tracking of an incoming E1 signal having an average frequency offset as high as 120 ppm, and up to 1.5 UI of peak-to-peak jitter. Since the Quad E1 Mapper supports a ring architecture, two sets of blocks are provided for each port. The TU/VT selection is the same for both blocks. A control bit, and transmit line alarms, can generate an E1AIS.

The eight TU/VT Build blocks format the TU/VT into a STS-1, STS-3 or STM-1 structure for the asynchronous 2048 kbit/s signals, as shown in 2. The pointer value carried in the V1 and V2 bytes is transmitted with a fixed value of 105. Transmit access is provided for the 8 overhead communications channel bits (O-bits) via the microprocessor. The microprocessor also writes the signal label, and the value of the J2 message, either as a 16-byte or a 64-byte message. The Quad E1 Mapper provides the TU tandem connection feature for the TU, including the transmission of the 16-byte message and the various alarms associated with the tandem connection feature. The device provides three-bit RDI using the V5 and K4 (Z7) bytes. Local alarms, or the microprocessor, can generate the remote payload, server, or connectivity defect indications. The Far End Block Error (FEBE) is inserted from the BIP-2 errors detected on the receive side, and BIP-2 parity is generated for the V5 byte. Control bits are provided for generating unequipped status, generating TU/VT AIS, and inserting FEBE and BIP-2 errors. The ability to generate Null Pointer Indicators (NPIs) is also provided for the STM-1 VC-4 format.

The A Transmit block is identical to the B Transmit block. The interface between an add bus and a Transmit block consists of three input leads and eleven output leads, when the add bus timing mode is selected. The input leads are a byte clock, a C1J1V1 indicator, and an SPE indicator. The output leads are byte-wide data, a parity indicator, an add indicator, and an optional TU/VT selection indicator signal. The Add C1J1V1 signal is used in conjunction with the Add SPE signal to determine the location of the various pulses. An option is pro-

vided in which the drop side V1 reference pulse, either from the drop bus C1J1V1 indicator or from the H4 multiframe detector, may be used as the add side V1 reference pulse.

When drop bus timing is selected, the output leads are byte-wide data, a parity indicator, an add indicator, and an optional TU/VT selection indicator signal. The add bus clock, SPE and C1J1V1 signals are disabled.

The Microprocessor Input/Output Interface block consists of an Intel-, Motorola- or multiplexed address/data-compatible bus interface that provides access to assigned QE1M memory map addresses in the range from 000H to 7FFH (please see the Memory Map and Memory Map Description sections for further information). Interrupt capability is also provided. The alarms that cause the interrupt can be set on positive, negative, or both positive and negative transitions, or on positive levels. Interrupt mask bits are provided for register byte locations, and some defined bits.

Control bits are provided which enable an E1 facility or line loopback. Because of the complexity of the SDH/SONET interface and the two timing modes, SDH/SONET loopback of the TU/VTs is not supported.

The SPOT (SONET Processor for Overhead Termination) block is a RISC processor with associated instruction and data memory that performs selected low-speed functions, including all overhead processing and counter maintenance. The SPOT program must be loaded into the SPOT instruction memory after power-up. Executable microcode is provided by TranSwitch (see the Operations - Internal SPOT Processor section).

The Boundary Scan Interface Block provides a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

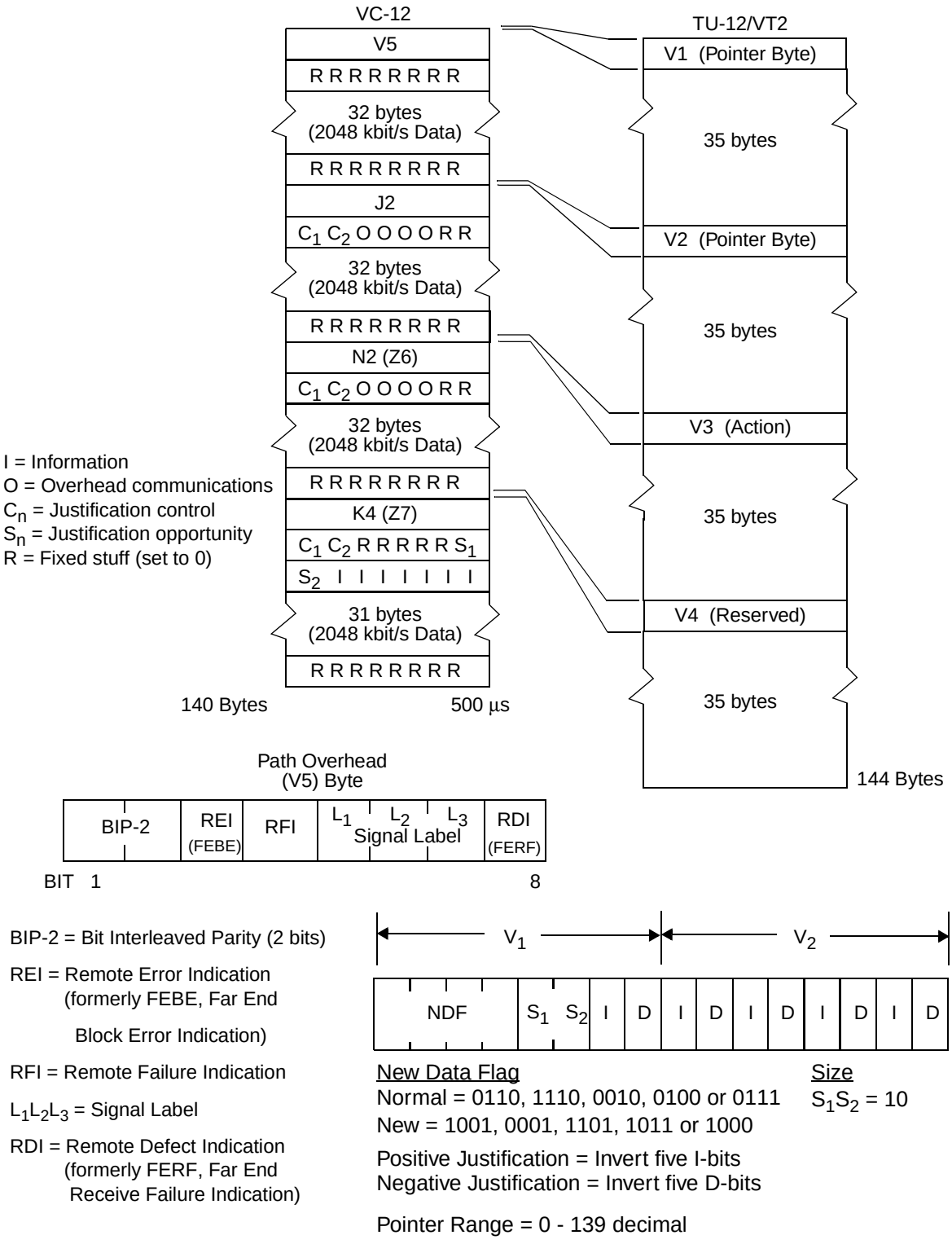
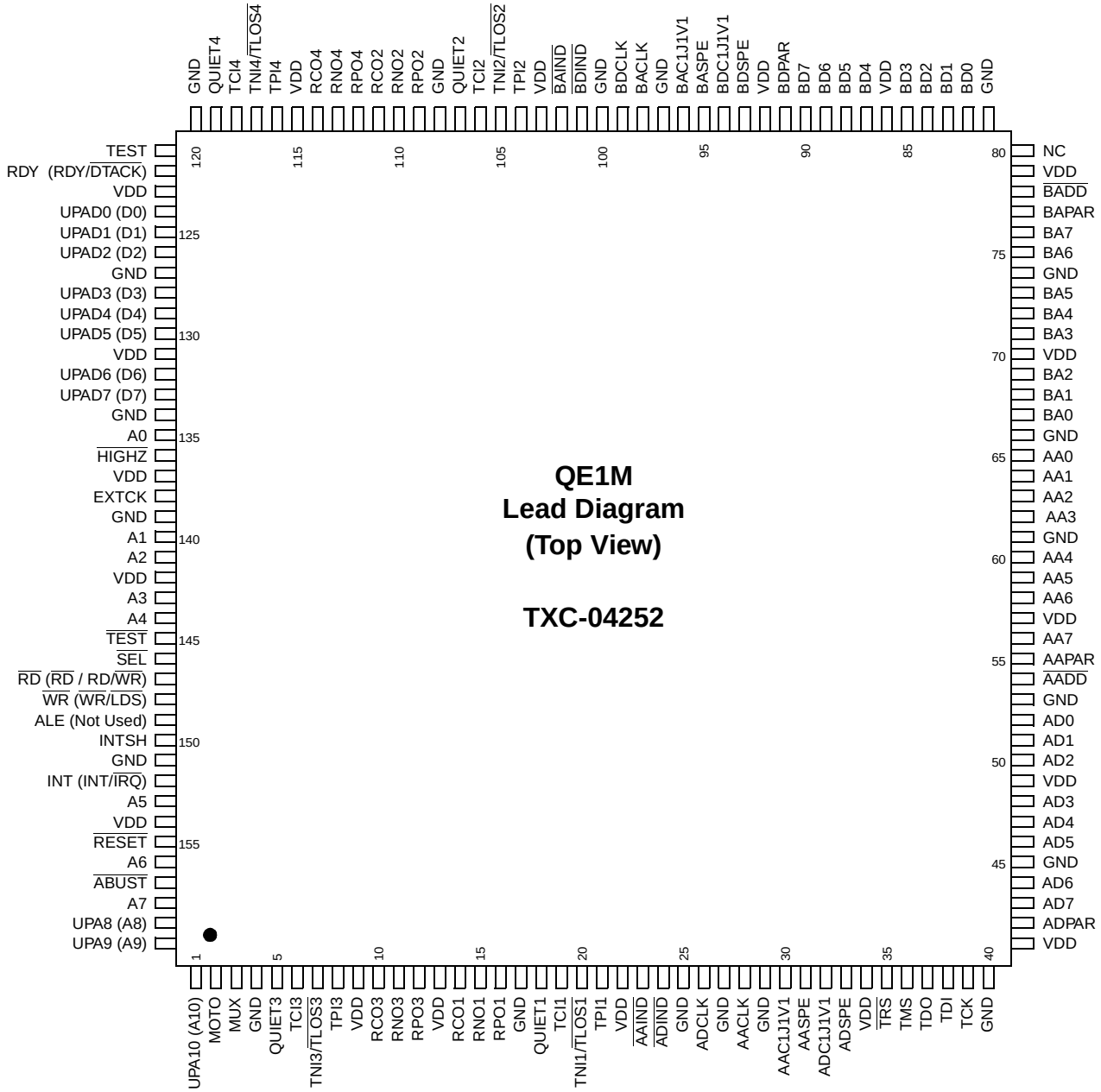


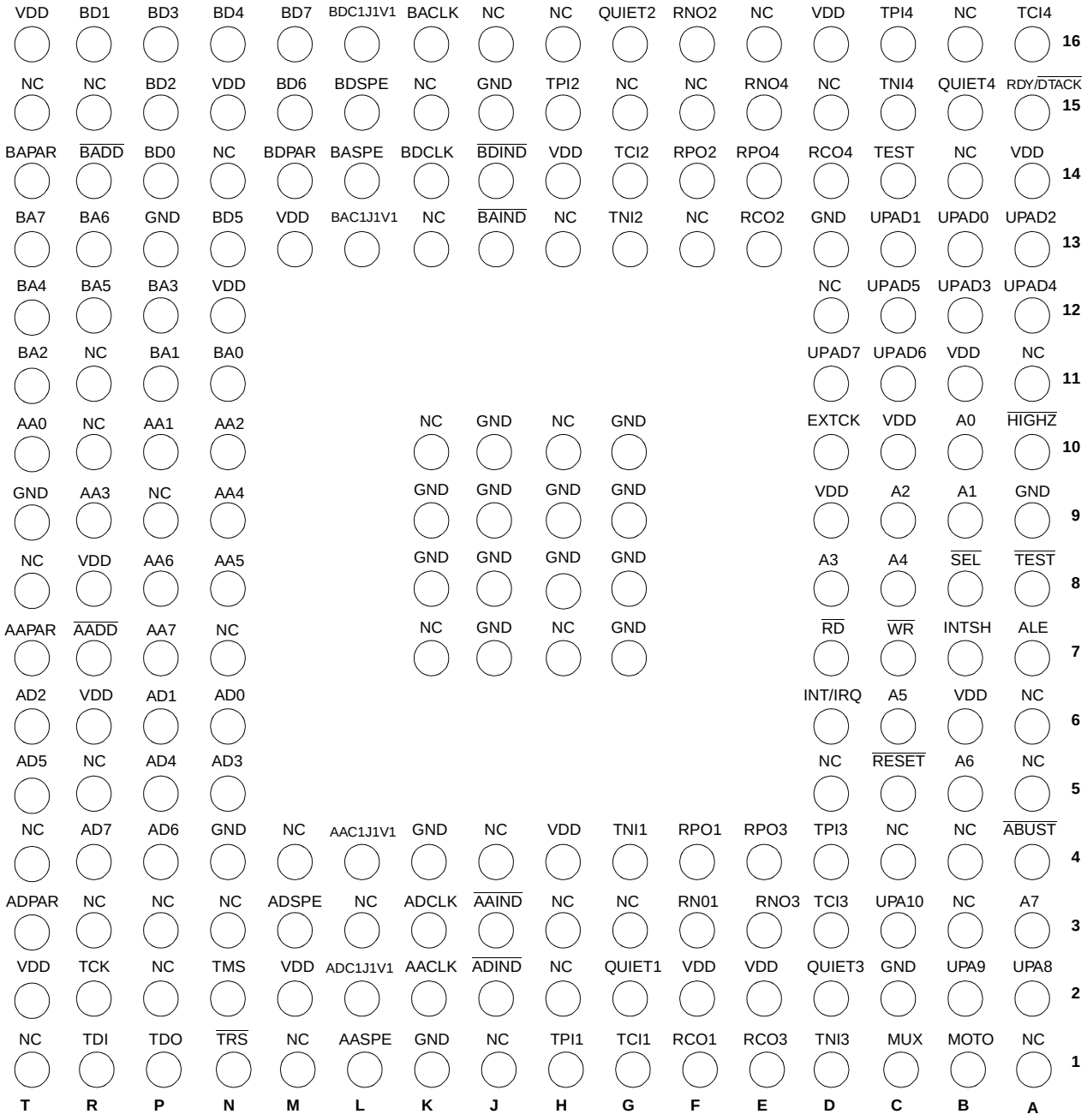
Figure 2. 2048 kbit/s Asynchronous Mapping

LEAD DIAGRAMS



Note: See Figure 28 for Package Information. X(Y/Z) format is used for microprocessor interface signals to identify Multiplex (Intel/Motorola) interface functions, where these are different.

Figure 3. QE1M TXC-04252 Plastic Quad Flat Package Lead Diagram



Note: This is the bottom view. The leads are solder balls. See Figure 29 for package information. Some signal Symbols have been abbreviated to fit the space available. The Symbols are shown in full in the Lead Descriptions section.

Figure 4. QE1M TXC-04252 Plastic Ball Grid Array Package Lead Diagram

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND AND NO CONNECT

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P *	Type	Name/Function
VDD	9, 13, 22, 34, 41, 49, 57, 70, 79, 86, 92, 103, 115, 123, 131, 137, 142, 154	A14, B6, B11, C10, D9, D16, E2, F2, H4, H14, M2, M13, N12, N15, R6, R8, T2, T16	P		**VDD:** +5 volt supply voltage, ±5%.
GND	4, 17, 25, 27, 29, 40, 45, 53, 61, 66, 74, 81, 97, 100, 108, 120, 127, 134, 139, 151	A9, C2, D13, G7, G8, G9, G10, H8, H9, J7, J8, J9, J10, J15, K1, K4, K8, K9, N4, P13, T9	P		**Ground:** 0 volt reference.
NC	80	A1, A5, A6, A11, B3, B4, B14, B16, C4, D5, D12, D15, E16, F13, F15, G3, G15, H2, H3, H7, H10, H13, H16, J1, J4, J16, K7, K10, K13, K15, L3, M1, M4, N3, N7, N14, P2, P3, P9, R3, R5, R10, R11, R15, T1, T4, T8, T15			**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of these leads may impair performance or cause damage to the device.

Note: I = Input; O = Output; P = Power; T=Tristate

A DROP AND A ADD BUS I/O

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type *	Name/Function
ADCLK	26	K3	I	TTL	**A Drop Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation, and at 6.48 MHz for STS-1 operation. A Drop bus byte-wide data (AD7-AD0), the parity bit (ADPAR), SPE indication (ADSPE), and the C1J1V1 indication (ADC1J1V1) are clocked in on falling edges of this clock. This clock may also be used for timing and deriving the like-named add bus byte-wide data, add and TU/VT indications, and parity bits. The add bus signals are clocked out on rising edges of the clock during the time slots that correspond to the selected TU/VT.
ADPAR	42	T3	I	TTL	**A Drop Bus Parity Bit:** An odd parity bit input signal representing the parity calculation for each data byte, SPE, and C1J1V1 signal from the drop bus. Control bits are provided in address 012H which enable parity to be calculated as even (control bit DPE is 1), and/or for the data byte only (control bit PDDO is 1).
AD(7-0)	43, 44, 46-48, 50-52	R4, P4, T5, P5, N5, T6, P6, N6	I	TTL	**A Drop Bus Data Byte:** Byte-wide data that corresponds to the STM-1/STS-3/STS-1 signal from the drop bus. The first bit received (dropped) corresponds to bit 7.
ADSPE	33	M3	I	TTL	**A Drop Bus SPE Indicator:** A signal that is active high during each byte of the STM-1/STS-3/STS-1 payload, and low during Transport Overhead times.
ADC1J1V1	32	L2	I	TTL	**A Drop Bus C1J1V1 Indications:** An active high timing signal that carries STM-1/STS-3/STS-1 starting frame and SPE information. This signal works in conjunction with the ADSPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1/STS-3 signal, and the C1 byte in the STS-1 signal, when ADSPE is low. The J1 signal identifies the starting location of the J1 signal when ADSPE is high. One or more V1 pulses may be present depending upon the format. The V1 pulses may be used in place of the H4 byte as the multiframe indication.
$\overline{\text{ADIND}}$	24	J2	O	CMOS 4mA	**A Drop Bus TU/VT Selection Indication:** Enabled when control bit ADnEN is written with a 1. An active low signal that is clocked out for the time slots determined by TU/VT selection (RTUNn register) for each port (n=port number, 1-4).

*See Input, Output and Input/Output Parameters section below for Type definitions.

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type *	Name/Function
AACLK	28	K2	I	TTL	**A Add Bus Clock:** When the add bus timing mode is selected, this input must be provided for add bus timing. This clock operates at 19.44 MHz for STM-1/STS-3 operation, and at 6.48 MHz for STS-1 operation. The add bus SPE indication (AASPE), and the C1J1V1 indication (AAC1J1V1) are clocked in on falling edges of this clock. Add bus byte-wide data (AA7-AA0), add indicator ($\overline{\text{AADD}}$), and parity bit (AAPAR) are clocked out on rising edges of the clock during the time slots that correspond to the selected TU/VT. When drop bus timing is selected, this input is disabled.
AAPAR	55	T7	O(T)	CMOS 4mA	**A Add Bus Parity Bit:** An odd parity output signal that is calculated over the byte-wide add data. This tristate lead is only active when there is data being added to the add bus. When control bit APE is 1, even parity is calculated.
AA(7-0)	56, 58, 59, 60, 62, 63, 64, 65	P7, P8, N8, N9, R9, N10, P10, T10	O(T)	CMOS 4mA	**A Add Bus Data Byte:** Byte-wide data that corresponds to the selected TU/VT.
AASPE	31	L1	I	TTL	**A Add Bus SPE Indicator:** When the add bus timing mode is selected, this signal must be provided for add bus timing. This signal must be high during each byte of the STM-1/STS-3/STS-1 payload, and low during Transport Overhead byte times.
AAC1J1V1	30	L4	I	TTL	**A Add Bus C1J1V1 Indications:** When the add bus timing mode is selected, this signal must be provided for add bus timing. An active high timing signal that carries STM-1/STS-3/STS-1 starting frame and SPE information. This signal works in conjunction with the AASPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1/STS-3 signal, and the C1 byte in the STS-1 signal, when AASPE is low. The J1 signal identifies the starting location of the J1 signal when AASPE is high. The J1 signal identifies the location of the J1 byte. One or more V1 pulses may be present depending upon the format. The V1 pulses are used in place of the H4 byte as the multiframe indication.
$\overline{\text{AAIND}}$	23	J3	O	CMOS 4mA	**A Add Bus TU/VT Selection Indication:** Enabled when control bit AAnEN is written with a 1. An active low signal that is clocked out for the time slots determined by TU/VT selection (TTUNn register) for each port (n=port number, 1-4).
$\overline{\text{AADD}}$	54	R7	O	CMOS 4mA	**A Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the A Add bus is valid. It identifies the location of all of the TU/VT time slots being selected. When control bit ADDI is 1, the indicator is active high instead of active low.

B DROP AND B ADD BUS I/O

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
BDCLK	99	K14	I	TTL	**B Drop Bus Clock:** This clock operates at 19.44 MHz for STM-1/STS-3 operation, and at 6.48 MHz for STS-1 operation. B Drop bus byte-wide data (BD7-BD0), the parity bit (BDPAR), SPE indication (BDSPE), and the C1J1V1 indication (BDC1J1V1) are clocked in on falling edges of this clock. This clock may also be used for timing and deriving the like-named add bus byte-wide data, add and TU/VT indications, and parity bits. The add bus signals are clocked out on rising edges of the clock during the time slots that correspond to the selected TU/VT.
BDPAR	91	M14	I	TTL	**B Drop Bus Parity Bit:** An odd parity bit input signal representing the parity calculation for each data byte, SPE, and C1J1V1 signal from the drop bus. Control bits are provided in address 012H which enable parity to be calculated as even (control bit DPE is 1), and/or for the data byte only (control bit PDDO is 1).
BD(7-0)	90-87, 85-82	M16, M15, N13, N16, P16, P15, R16, P14	I	TTL	**B Drop Bus Data Byte:** Byte-wide data that corresponds to the STM-1/STS-3/STS-1 signal from the drop bus. The first bit received (dropped) corresponds to bit 7.
BDSPE	93	L15	I	TTL	**B Drop Bus SPE Indicator:** A signal that is active high during each byte of the STM-1/STS-3/STS-1 payload, and low during Transport Overhead times.
BDC1J1V1	94	L16	I	TTL	**B Drop Bus C1J1V1 Indications:** An active high timing signal that carries STM-1/STS-3/STS-1 starting frame and SPE information. This signal works in conjunction with the BDSPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1/STS-3 signal, and the C1 byte in the STS-1 signal, when BDSPE is low. The J1 signal identifies the starting location of the J1 signal when BDSPE is high. One or more V1 pulses may be present depending upon the format. The V1 pulses may be used in place of the H4 byte as the multiframe indication.
$\overline{\text{BDIND}}$	101	J14	O	CMOS 4mA	**B Drop Bus TU/VT Selection Indication:** Enabled when control bit BDnEN is written with a 1. An active low signal that is clocked out for the time slots determined by TU/VT selection (RTUNn register) for each port (n=port number, 1-4).

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
BACLK	98	K16	I	TTL	**B Add Bus Clock:** When the add bus timing mode is selected, this input must be provided for add bus timing. This clock operates at 19.44 MHz for STM-1/STS-3 operation, and at 6.48 MHz for STS-1 operation. The add bus SPE indication (BASPE), and the C1J1V1 indication (BAC1J1V1) are clocked in on falling edges of this clock. Add bus byte-wide data (BA7-BA0), add indicator ($\overline{\text{BADD}}$), and parity bit (BAPAR) are clocked out on rising edges of the clock during the time slots that correspond to the selected TU/VT. When drop bus timing is selected, this input is disabled.
BAPAR	77	T14	O(T)	CMOS 4mA	**B Add Bus Parity Bit:** An odd parity output signal that is calculated over the byte-wide add data. This tristate lead is only active when there is data being added to the add bus. When control bit APE is 1, even parity is calculated.
BA(7-0)	76, 75, 73, 72, 71, 69, 68, 67	T13, R13, R12, T12, P12, T11, P11, N11	O(T)	CMOS 4mA	**B Add Bus Data Byte:** Byte-wide data that corresponds to the selected TU/VT.
BASPE	95	L14	I	TTL	**B Add Bus SPE Indicator:** When the add bus timing mode is selected, this signal must be provided for add bus timing. This signal must be high during each byte of the STM-1/STS-3/STS-1 payload, and low during Transport Overhead byte times.
BAC1J1V1	96	L13	I	TTL	**B Add Bus C1J1V1 Indications:** When the add bus timing mode is selected, this signal must be provided for add bus timing. An active high timing signal that carries STM-1/STS-3/STS-1 starting frame and SPE information. This signal works in conjunction with the BASPE signal. The C1 pulse identifies the location of the first C1 byte in the STM-1/STS-3 signal, and the C1 byte in the STS-1 signal, when BASPE is low. The J1 signal identifies the starting location of the J1 signal when BASPE is high. The J1 signal identifies the location of the J1 byte. One or more V1 pulses may be present depending upon the format. The V1 pulses are used in place of the H4 byte as the multiframe indication.
$\overline{\text{BAIND}}$	102	J13	O	CMOS 4mA	**B Add Bus TU/VT Selection Indication:** Enabled when control bit BAnEN is written with a 1. An active low signal that is clocked out for the time slots determined by TU/VT selection (TTUNn register) for each port (n=port number, 1-4).
$\overline{\text{BADD}}$	78	R14	O	CMOS 4mA	**B Add Bus Add Data Present Indicator:** This normally active low signal is present when output data to the B Add bus is valid. It identifies the location of all of the TU/VT time slots being selected. When control bit ADDI is 1, the indicator is active high instead of active low.

PORT n LINE INTERFACE (n = 1, 2, 3 or 4)

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
RCOn (n=1-4)	14, 111, 10, 114	F1, E13, E1, D14	O(T)	CMOS 4mA	**Receive Port n Output Clock:** A 2.048 MHz clock output. Data is normally clocked out on rising edges of this clock. When control bit RCKI is 1, data is clocked out on falling edges of this clock. When control bit RnEN is 0, this lead is forced to a high impedance state.
RPOn (n=1-4)	16, 109, 12, 112	F4, F14, E4, E14	O(T)	CMOS 4mA	**Receive Port n Data Positive Rail or NRZ:** When control bit BYPASn is 0, positive rail data is provided on this lead. When control bit BYPASn is 1, an NRZ signal is provided on this lead. When control bit RnEN is 0, this lead is forced to a high impedance state.
RNOn (n=1-4)	15, 110, 11, 113	F3, F16, E3, E15	O(T)	CMOS 4mA	**Receive Port n Data Negative Rail:** When control bit BYPASn is 0, negative rail data is provided on this lead. When control bit RnEN is 0, or control bit BYPASn is 1, this lead is forced to a high impedance state.
TCIn (n=1-4)	19, 106, 6, 118	G1, G14, D3, A16	I	TTL	**Transmit Port n Input Clock:** A 2.048 MHz clock input. Data is normally clocked in on falling edges of this clock. When control bit TCKI is 1, data is clocked in on the rising edges of this clock.
TPIn (n=1-4)	21, 104, 8, 116	H1, H15, D4, C16	I	TTL	**Transmit Port n Data Positive Rail or NRZ:** When control bit BYPASn is 0, positive rail input data is provided on this lead. When control bit BYPASn is 1, an NRZ signal is provided on this lead.
TNIn/ $\overline{\text{TLOS}}$n (n=1-4)	20, 105, 7, 117	G4, G13, D1, C15	I	TTL	**Transmit Port n Data Negative Rail/External Loss Of Signal:** When control bit BYPASn is 0, negative rail input data is provided on this lead. When control bit BYPASn is 1, this lead may be used to input an active low external loss of signal indicator from the line interface device.
QUIETn (n=1-4)	18, 107, 5, 119	G2, G16, D2, B15	I	TTL	**Quiet Port n:** A high forces the RPOn and RNOn leads to the 0 state for either a rail or NRZ interface, overriding control bit RnEN when it is 0. A low disables this feature.

MICROPROCESSOR BUS INTERFACE SELECTION

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
MUX	3	C1	I	TTL	**Multiplex Mode:** A high placed on this lead configures the microprocessor bus to a multiplexed address/data bus interface. A low configures the Intel or Motorola interfaces (see Symbol MOTO below).

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
MOTO	2	B1	I	TTL	**Motorola Mode**: Enabled when a low is placed on the MUX lead. The following table lists the bus selection options. MUX / MOTO / Action H / L or H / Multiplex bus interface L / L / Intel bus interface L / H / Motorola bus interface This selection modifies some bus interface lead functions, as described in the next two sections of this table.

MICROPROCESSOR BUS INTERFACE - MULTIPLEXED BUS

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
UPA(10-8)	1, 160, 159	C3, B2, A2	I (Note 1)	TTL (Note 1)	**Address Bus:** These are additional address lines for accessing QE1M memory locations (most significant three bits). UPA10 is the most significant bit. High is logic 1.
UPAD(7-0)	133, 132, 130, 129, 128, 126, 125, 124	D11, C11, C12, A12, B12, A13, C13, B13	I/O	TTL 8mA	**Address/Data Bus:** These leads are the time-multiplexed address (lower eight bits only) and data bus for accessing the QE1M memory locations. UPAD7 is the most significant bit. High is logic 1.
$\overline{SEL}$	146	B8	I	TTL	**Select:** An active low signal generated by the microprocessor for accessing the QE1M memory locations.
$\overline{RD}$	147	D7	I	TTL	**Read:** An active low signal generated by the microprocessor for reading the QE1M memory locations. The memory map is selected by placing a low on the select lead.
$\overline{WR}$	148	C7	I	TTL	**Write:** An active low signal generated by the microprocessor for writing to QE1M memory locations. The memory map is selected by placing a low on the select lead.
ALE	149	A7	I	TTL	**Address Latch Enable:** An active high signal generated by the microprocessor for holding an address stable during a read or write cycle.
RDY	122	A15	O(T)	TTL 8mA	**Ready:** A high is an acknowledgment from the addressed memory location that the transfer can be completed. A low indicates that the Mapper cannot complete the transfer cycle, and that microprocessor wait states must be generated.
INT	152	D6	O(T)	TTL 8mA	**Interrupt:** A high or low on this output lead signals an interrupt request to the microprocessor. The polarity of this signal is determined by the state of the INTSH lead.

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
INTSH	150	B7	I	TTL	**Interrupt Sense High Selection:** A high on this lead causes the interrupt sense to be high when an interrupt occurs. A low causes the interrupt sense to be low when an interrupt occurs.

Note 1: Leads UPA(10-8) are implemented as Input/Output type TTL 4mA to support production tests but are used as TTL inputs.

MICROPROCESSOR BUS INTERFACE - SPLIT BUS FOR MOTOROLA (M) OR INTEL (I)

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
A(10-0)	1, 160, 159, 158, 156, 153, 144, 143, 141, 140, 135	C3, B2, A2, A3, B5, C6, C8, D8, C9, B9, B10	I (Note 1)	TTL (Note 1)	**Address Bus (Motorola/Intel Buses):** These address line inputs are used for accessing a QE1M memory location for a read/write cycle. A10 is the most significant bit. High is logic 1.
D(7-0)	133, 132, 130, 129, 128, 126, 125, 124	D11, C11, C12, A12, B12, A13, C13, B13	I/O	TTL 8mA	**Data Bus (Motorola/Intel Buses):** Bidirectional data lines used for transferring data to or from a QE1M memory location. D7 is the most significant bit. High is logic 1.
$\overline{SEL}$	146	B8	I	TTL	**Select:** A low enables data transfers between the microprocessor and the QE1M memory during a read/write cycle.
$\overline{RD}$ / RD/$\overline{WR}$	147	D7	I	TTL	**Read (I mode) or Read/Write (M mode):** Intel Mode - An active low signal generated by the microprocessor for reading the QE1M memory locations. Motorola Mode - An active high signal generated by the microprocessor for reading the QE1M memory locations. An active low signal is used to write to memory locations.
$\overline{WR}$ / $\overline{LDS}$	148	C7	I	TTL	**Write (I mode) or Device Select (M mode):** Intel Mode - An active low signal generated by the microprocessor for writing to the QE1M memory locations. Motorola Mode - The $\overline{SEL}$ and $\overline{LDS}$ inputs are logically OR-gated inside the QE1M, generating an internal active low select signal ($\overline{CS}$) that is similar to $\overline{SEL}$. This internal signal is used to enable data transfer. This lead can be used for the interface with the Motorola 68302 microprocessor. If it is not used, it should be tied to ground, so that $\overline{CS}$ is the same signal as $\overline{SEL}$.

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
RDY / $\overline{\text{DTACK}}$	122	A15	O(T)	TTL 8mA	**Ready (I mode) or Data Transfer Acknowledge (M mode):** Intel Mode - A high is an acknowledgment from the addressed QE1M memory location that the transfer can be completed. A low indicates that the Mapper cannot complete the transfer cycle, and that microprocessor wait states must be generated. Motorola Mode - During a read bus cycle, a low signal indicates that the information on the data bus is valid. During a write bus cycle, a low signal acknowledges the acceptance of data. This lead is tristated.
INT/ $\overline{\text{IRQ}}$	152	D6	O(T)	TTL 8mA	**Interrupt:** When INTSH is high, a high on this output lead signals an interrupt request INT to the microprocessor, as required for Intel. When INTSH is low, a low signals an interrupt request $\overline{\text{IRQ}}$ to the microprocessor, as required for Motorola.
INTSH	150	B7	I	TTL	**Interrupt Sense High:** Interrupt polarity select. A high on this lead causes the interrupt sense to be high when an interrupt occurs. A low causes the interrupt sense to be low when an interrupt occurs. This lead must be set to meet the interrupt polarity requirement of the microprocessor.

Note 1: Leads A(10-0) are implemented as type Input/Output type TTL 4mA to support production tests but are used as TTL inputs.

CONTROLS, EXTERNAL CLOCK AND TEST LEADS

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
TEST	121	C14	I	CMOS	**TranSwitch Test Lead:** A low must be placed on this lead.
$\overline{\text{TEST}}$	145	A8	I	TTLp	**TranSwitch Test Lead:** This lead is pulled high internally by an internal pull-up to V_{DD}. It must be left floating or held high.
EXTCK	138	D10	I	CMOS	**External Reference Clock:** This clock is used for desynchronizer operation and other purposes. The clock frequency must be 58.32 MHz (+/- 30 ppm over life) and the clock duty cycle must be (50 +/- 10) %.
$\overline{\text{RESET}}$	155	C5	I	TTL	**Hardware Reset:** When an active low pulse is applied to this lead for a minimum duration of 150 nanoseconds after power is applied, this pulse clears all performance counters and alarms, resets the control bits (except those bits that force a high impedance state for the add buses), and initializes the internal FIFOs and internal SPOT processor. The microprocessor must write the control bit states for normal operation.

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
$\overline{\text{HIGHZ}}$	136	A10	I	TTL	**High Impedance Select:** A low forces all output leads to the high impedance state for testing purposes (except TDO).
$\overline{\text{ABUST}}$	157	A4	I	TTL	**Add Bus Timing Select:** A low selects the A and B Add bus clock, SPE and C1J1V1 input signals for deriving timing for the A and B Add buses. A high selects the like-named drop bus for deriving timing (e.g., A Drop bus for A Add bus). This control lead is disabled when a 1 is written to control bit SBTEN.

BOUNDARY SCAN INTERFACE SIGNALS

Symbol	160-Lead PQFP Lead No.	208-Lead PBGA Lead No.	I/O/P	Type	Name/Function
TCK	39	R2	I	TTL	**IEEE 1149.1 Test Port Serial Scan Clock:** This signal is used to shift data into TDI on the rising edge, and out of TDO on the falling edge. The maximum clock frequency is 10 MHz.
TMS	36	N2	I	TTLp	**IEEE 1149.1 Test Port Mode Select:** TMS is sampled on the rising edge of TCK, and is used to place the Test Access Port controller into various states as defined in IEEE 1149.1. This lead is set high internally by an internal pull-up to V_{DD} for normal framer operation.
TDI	38	R1	I	TTLp	**IEEE 1149.1 Test Port Serial Scan Data In:** Serial test instructions and data are clocked into this lead on the rising edge of TCK. This input has an internal pull-up to VDD.
TDO	37	P1	O(T)	TTL 4mA	**IEEE 1149.1 Test Port Serial Scan Data Out:** Serial test instructions and data are clocked out of this lead on the falling edge of TCK. When inactive, this 3-state output will be put into its high impedance state.
$\overline{\text{TRS}}$	35	N1	I	TTLp	**IEEE 1149.1 Test Port Reset Lead:** This lead will asynchronously reset the Test Access Port (TAP) controller. This lead is to be held low, asserted low or pulsed low (for a minimum duration of 20 ns) to reset the TAP controller on QE1M power-up. This input has an internal pull-up to V_{DD}.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{DD}	-0.5	+6.0	V	Note 1
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	Note 1
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient Operating Temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	Absolute value 2000		V	Note 3
Latch-up	LU				JEDEC STD-17

Notes:

1. Conditions exceeding the Min or Max values may cause permanent failure. Exposure to conditions near the Min or Max values for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Absolute value tested per MIL-STD-883D, Method 3015.7.

THERMAL CHARACTERISTICS

The thermal characteristics of the PQFP and PBGA versions of the QE1M device are shown in the table below:

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance: junction to ambient for PQFP	--	--	41.4	$^oC/W$	0 ft/min linear airflow
Thermal resistance: junction to ambient for PBGA	--	--	38	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
I_{DD}		110	143	mA	STS-1
Power dissipation, P_{DD}		550	750	mW	STS-1
I_{DD}		136	170	mA	STM-1 or STS-3
Power dissipation, P_{DD}		680	900	mW	STM-1 or STS-3

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

INPUT PARAMETERS

Input Parameters For CMOS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	0.7 * V_{DD}			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.3 * V_{DD}	V	$4.75 \le V_{DD} \le 5.25$
Input capacitance		7.5		pF	

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input capacitance		7.5		pF	

Input Parameters For TTLp

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input capacitance		7.5		pF	
Input Resistance		70		kΩ	

OUTPUT PARAMETERS

Output Parameters For CMOS 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.7			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
Input capacitance		7.5		pF	

Output Parameters For TTL 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -4.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
Input capacitance		7.5		pF	

Output Parameters For TTL 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	V_{DD} = 4.75; I_{OH} = -8.0
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
Input capacitance		7.5		pF	

INPUT/OUTPUT PARAMETERS

Input/output Parameters For TTL 4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
Input capacitance		5.5		pF	
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -4.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 4.0$
I_{OL}			4.0	mA	
I_{OH}			-4.0	mA	
Input capacitance		7.5		pF	

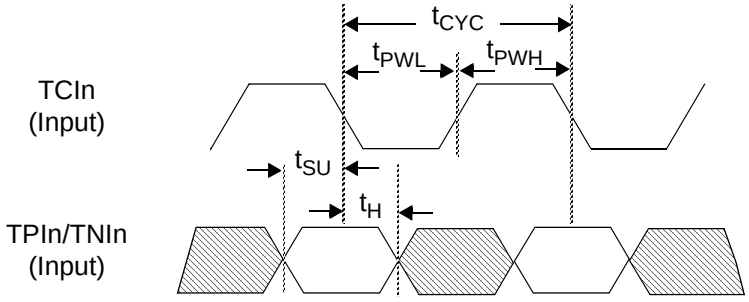
Input/output Parameters For TTL 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \le V_{DD} \le 5.25$
V_{IL}			0.8	V	$4.75 \le V_{DD} \le 5.25$
V_{OH}	2.4			V	$V_{DD} = 4.75$; $I_{OH} = -8.0$
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 8.0$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
Input capacitance		7.5		pF	

TIMING CHARACTERISTICS

Detailed timing diagrams for the QE1M device are illustrated in Figures 5 through 17, with values of the timing intervals tabulated below the waveform diagrams. The tristate condition of a signal waveform is shown as midway between high and low. The timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals, unless otherwise indicated. Where a waveform diagram describes both A and B bus signals, their symbols are combined in labeling the waveform (e.g., $\overline{A/BADD}$ for $\overline{AADD}$ and $\overline{BADD}$).

Figure 5. Ports 1, 2, 3 and 4 E1 Transmit Timing



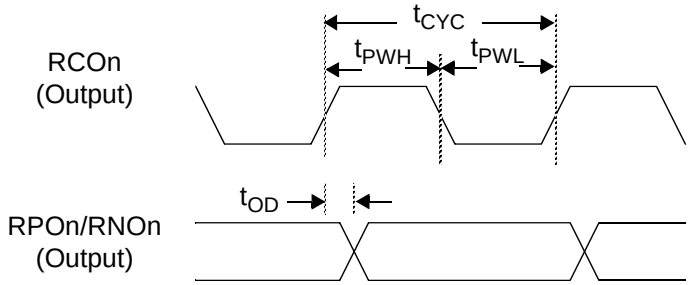
Note: n = 1 - 4

Notes:

1. TCIn is shown for TCLKI = 0, where data is clocked in on falling edges. Data is clocked in on rising edges when TCLKI =1.
2. For NRZ operation, TNIn is not used for data input and may instead be used as the input for an external active low loss of signal indication $\overline{TLOSn}$. Otherwise, this lead must be held high.

Parameter	Symbol	Min	Typ	Max	Unit
TCIn Clock period	t_{CYC}		488.28		ns
TCIn clock low time	t_{PWL}	150			ns
TCIn clock high time	t_{PWH}	150			ns
TPIn/TNIn data setup time before TCIn↓	t_{SU}	10			ns
TPIn/TNIn data hold time after TCIn↓	t_H	2.0			ns

Figure 6. Ports 1, 2, 3 and 4 E1 Receive Timing



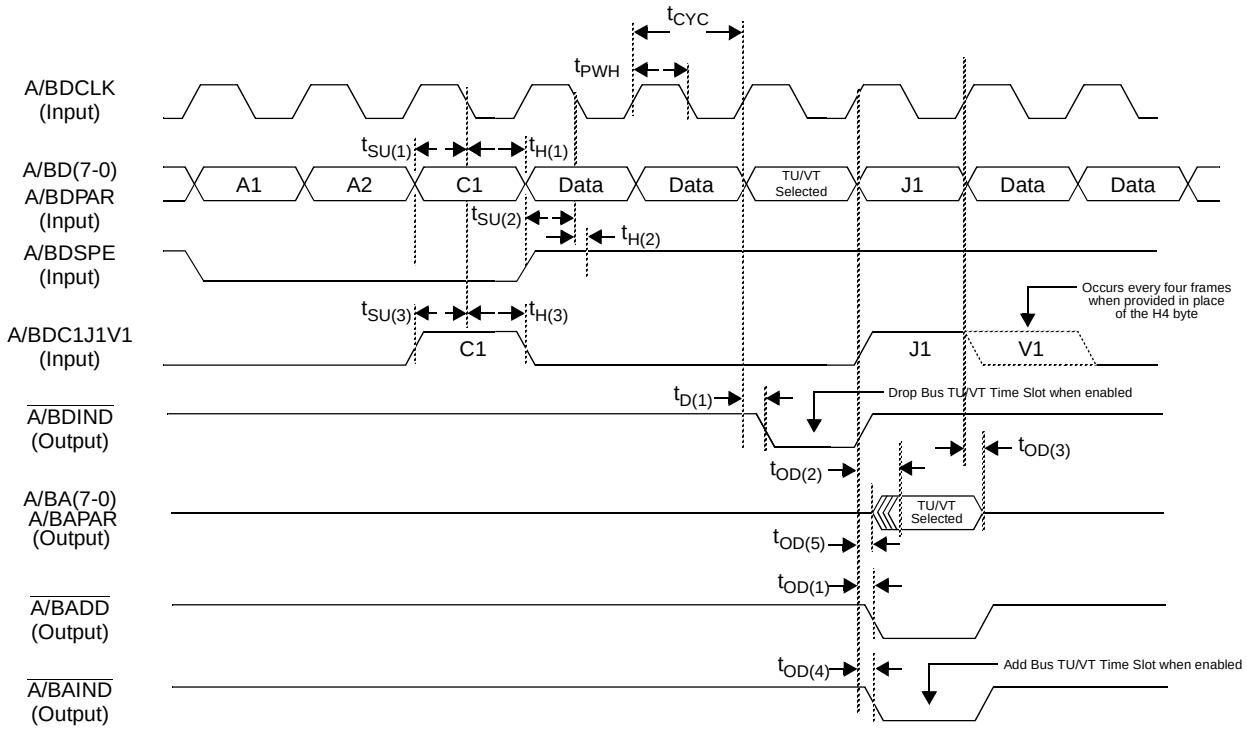
Note: n = 1 - 4

Note: RCOn is shown for RCLKI=0, where data is clocked out on rising edges. Data is clocked out on falling edges when RCLKI=1.

Parameter	Symbol	Min	Typ	Max	Unit
RCOn clock period	t_{CYC}	480		498	ns
RCOn clock low time (RCLKI = 0)	t_{PWL}		257		ns
RCOn clock high time (RCLKI = 0)	t_{PWH}	222		241	ns
RCOn clock low time (RCLKI = 1)	t_{PWL}	222		241	ns
RCOn clock high time (RCLKI = 1)	t_{PWH}		257		ns
RPOn/RNOn data delay after RCOn↑	t_{OD}	2.0		5.0	ns

Note: All output times are measured with a maximum 75 pF load capacitance.

Figure 7. STS-1 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus

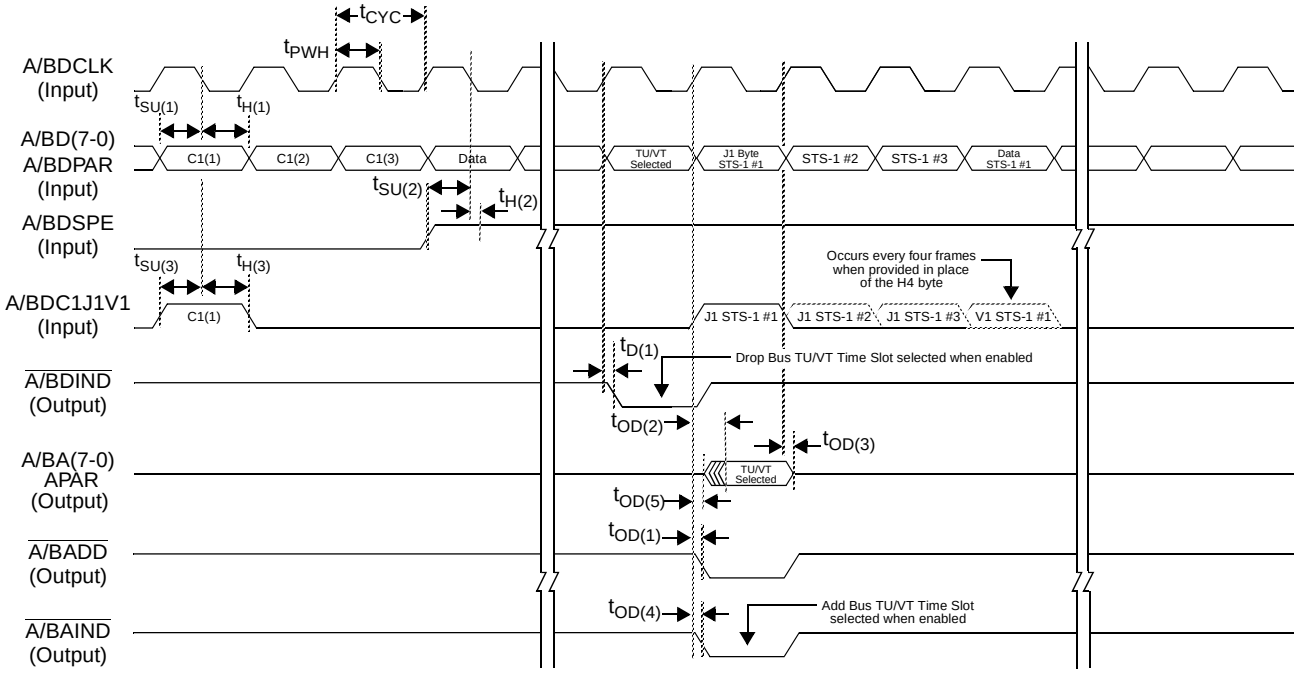


Note: For illustration purposes, a single TU/VT (TU number 21) is shown. The V1 pulse may or may not be present. If it is not present, the H4 byte must be provided. An additional byte time of delay in A/BA(7-0) is provided when control bit ABD is written with a 1. The table omits A/B parameter prefixes. DSPE edges are at payload boundaries.

Parameter	Symbol	Load	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}			154.32		ns
DLCK duty cycle t_{PWH}/t_{CYC}			40	50	60	%
D(7-0)/DPAR data /parity setup time before DCLK↓	$t_{SU(1)}$		10			ns
D(7-0)/DPAR data /parity hold time after DCLK↓	$t_{H(1)}$		5.0			ns
DSPE setup time before DCLK↓	$t_{SU(2)}$		10			ns
DSPE hold time after DCLK↓	$t_{H(2)}$		5.0			ns
DC1J1V1 setup time before DCLK↓	$t_{SU(3)}$		10			ns
DC1J1V1 hold time after DCLK↓	$t_{H(3)}$		5.0			ns
$\overline{\text{DIND}}$ drop bus indication output delay from DCLK↑	$t_{D(1)}$	25pF	7.0		30	ns
A(7-0)/APAR data /parity out valid delay from DCLK↑	$t_{OD(2)}$	75pF	9.0		39	ns
A(7-0)/APAR data /parity to tristate delay from DCLK↑	$t_{OD(3)}$		8.0		20	ns
$\overline{\text{ADD}}$ add indicator delay from DCLK↑	$t_{OD(1)}$	25pF	9.0		30	ns
$\overline{\text{AIND}}$ add bus indication output delay from DCLK↑	$t_{OD(4)}$		9.0		30	ns
A(7-0)/APAR data /parity out tristate to driven delay from DCLK↑	$t_{OD(5)}$	75pF	7.0		9.0	ns

Note: All output times are measured with the specified load capacitance.

Figure 8. STM-1/STS-3 A/B Drop and Add Bus Signals, Timing Derived from Drop Bus

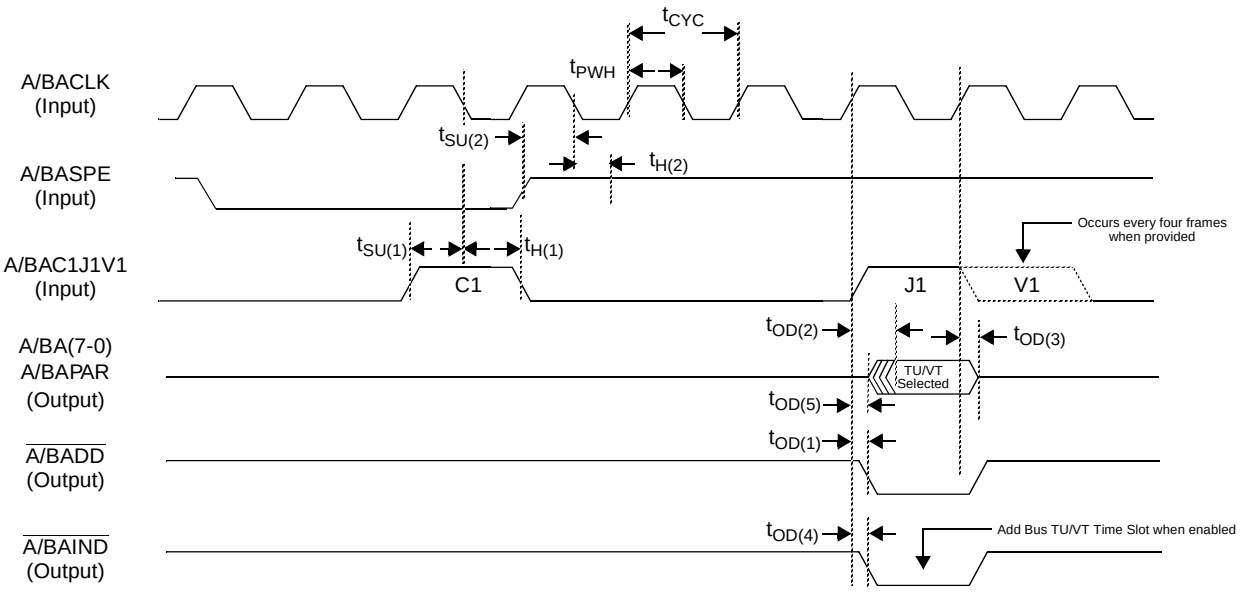


Note: A single TU/VT is shown for illustration purposes. It also shows the TU/VT selection for the drop bus and add bus (number 21 in STS-1 number 3). The format is an AU-3/STS-3. For VC-4 operation, one J1 pulse and one optional V1 pulse are present. An additional byte time of delay in A/BA(7-0) is provided when control bit ABD is written with a 1. The table omits A/B parameter prefixes. DSPE edges are at payload boundaries.

Parameter	Symbol	Load	Min	Typ	Max	Unit
DCLK clock period	t_{CYC}			51.44		ns
DCLK duty cycle t_{PWH}/t_{CYC}			40	50	60	%
D(7-0)/DPAR data /parity setup time before DCLK↓	$t_{SU(1)}$		10			ns
D(7-0)/DPAR data /parity hold time after DCLK↓	$t_{H(1)}$		5.0			ns
DSPE setup time before DCLK↓	$t_{SU(2)}$		10			ns
DSPE hold time after DCLK↓	$t_{H(2)}$		5.0			ns
DC1J1V1 setup time before DCLK↓	$t_{SU(3)}$		10			ns
DC1J1V1 hold time after DCLK↓	$t_{H(3)}$		5.0			ns
$\overline{\text{DIND}}$ drop bus indication output delay from DCLK↑	$t_{D(1)}$	25pF	7.0		30	ns
A(7-0)/APAR data /parity out valid delay from DCLK↑	$t_{OD(2)}$	75pF	9.0		39	ns
A(7-0)/APAR data /parity to tristate delay from DCLK↑	$t_{OD(3)}$		8.0		20	ns
$\overline{\text{ADD}}$ add indicator delay from DCLK↑	$t_{OD(1)}$	25pF	9.0		30	ns
$\overline{\text{AIND}}$ add bus indication output delay from DCLK↑	$t_{OD(4)}$		9.0		30	ns
A(7-0)/APAR data /parity out tristate to driven delay from DCLK↑	$t_{OD(5)}$	75pF	7.0		9.0	ns

Note: All output times are measured with the specified load capacitance.

Figure 9. STS-1 A/B Add Bus Signals, Timing Derived from Add Bus

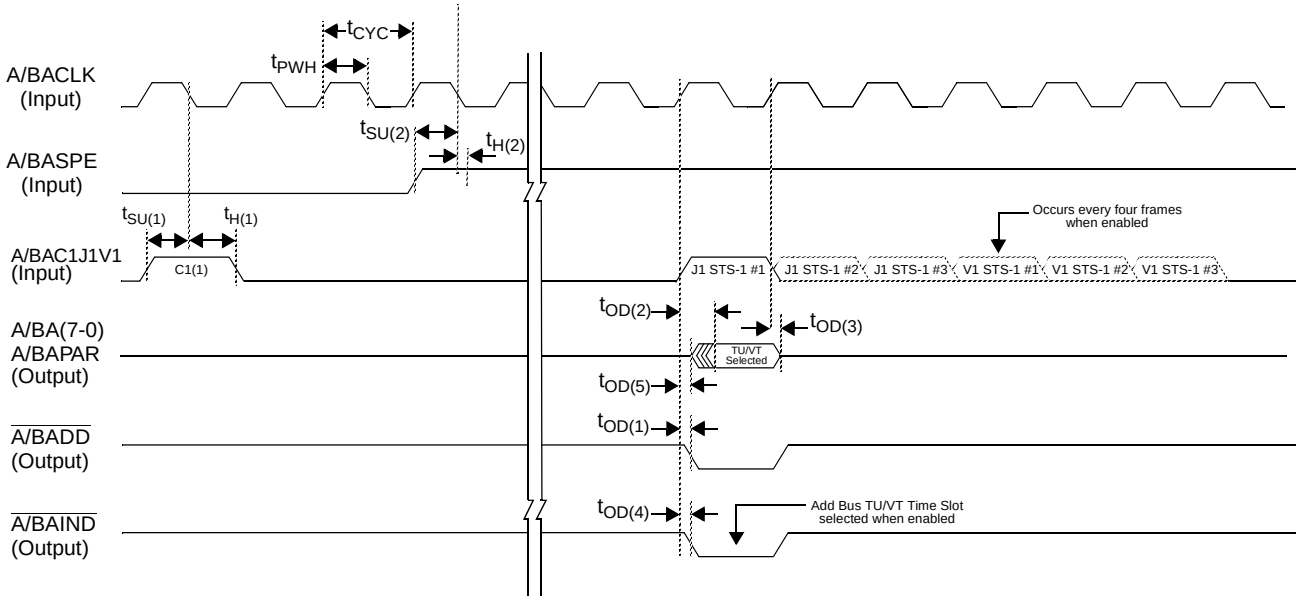


Notes: For illustration purposes, a single TU/VT is shown. The location of this TU/VT corresponds to TU/VT number 21. An additional byte time of delay in A/BA(7-0) is provided when control bit ABD is written with a 1. The table omits A/B parameter prefixes. ASPE edges are at payload boundaries.

Parameter	Symbol	Load	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}			154.32		ns
ACLK duty cycle, t_{PWH}/t_{CYC}			40	50	60	%
AC1J1V1 setup time before ACLK↓	$t_{SU(1)}$		10			ns
AC1J1V1 hold time after ACLK↓	$t_{H(1)}$		5.0			ns
ASPE setup time before ACLK↓	$t_{SU(2)}$		10			ns
ASPE hold time after ACLK↓	$t_{H(2)}$		5.0			ns
A(7-0)/APAR data /parity out valid delay from ACLK↑	$t_{OD(2)}$	75pF	7.0		31	ns
A(7-0)/APAR data /parity to tristate delay from ACLK↑	$t_{OD(3)}$		7.0		16	ns
$\overline{ADD}$ add indicator delayed from ACLK ↑	$t_{OD(1)}$	25pF	7.0		24	ns
$\overline{AIND}$ add bus indication output delay from ACLK↑	$t_{OD(4)}$		7.0		24	ns
A(7-0)/APAR data /parity out tristate to driven delay from ACLK↑	$t_{OD(5)}$	75pF	5.0		7.0	ns

Note: All output times are measured with the specified load capacitance.

Figure 10. STM-1/STS-3 A/B Add Bus Signals, Timing Derived from Add Bus

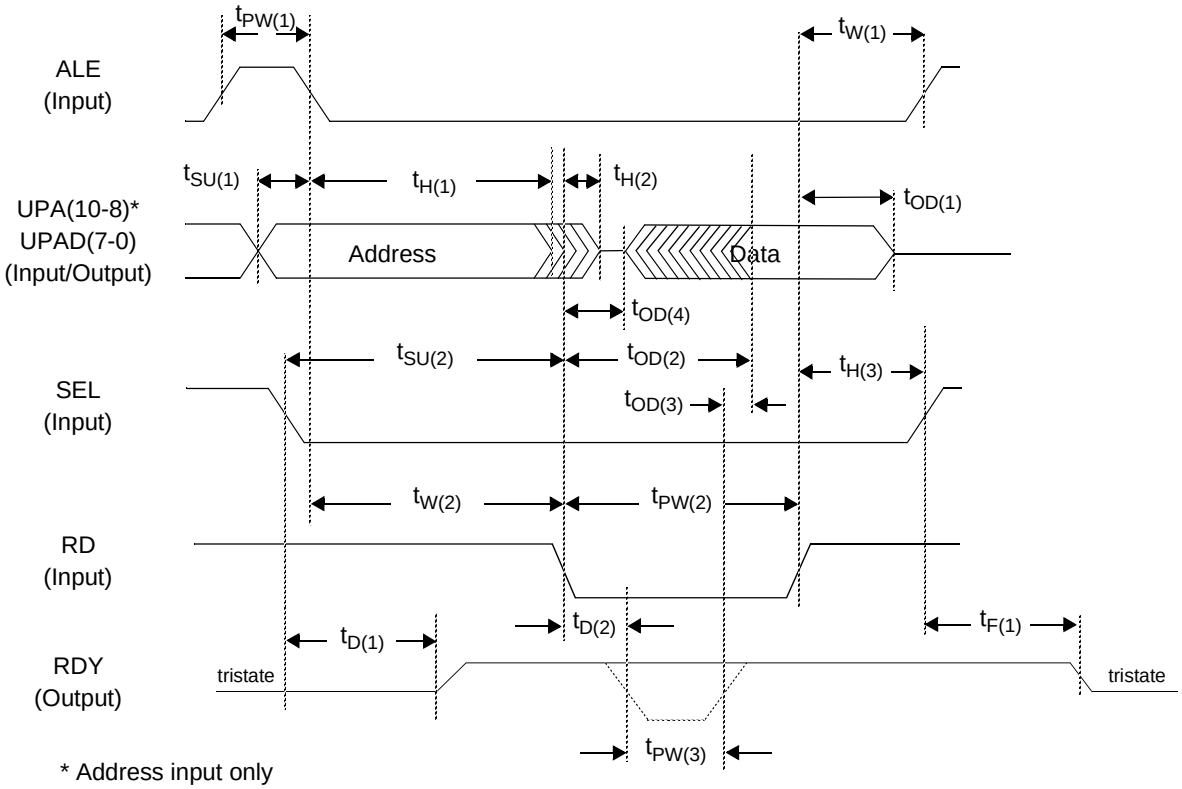


Note: A single TU/VT is shown for illustration purposes. It also shows the TU/VT selection for the drop bus and add bus (number 21 in STS-1 number 3). The format is an AU-3/STS-3. For VC-4 operation, one J1 pulse and one optional V1 pulse are present. An additional byte time of delay in A/BA(7-0) is provided when control bit ABD is written with a 1. The table omits A/B parameter prefixes. ASPE edges are at payload boundaries.

Parameter	Symbol	Load	Min	Typ	Max	Unit
ACLK clock period	t_{CYC}			51.44		ns
ACLK duty cycle, t_{PWH}/t_{CYC}			40	50	60	%
AC1J1V1 setup time before ACLK↓	$t_{SU(1)}$		10			ns
AC1J1V1 hold time after ACLK↓	$t_{H(1)}$		5.0			ns
ASPE setup time before ACLK↓	$t_{SU(2)}$		10			ns
ASPE hold time after ACLK↓	$t_{H(2)}$		5.0			ns
A(7-0)/APAR data /parity out valid delay from ACLK↑	$t_{OD(2)}$	75pF	7.0		31	ns
A(7-0)/APAR data /parity to tristate delay from ACLK↑	$t_{OD(3)}$		7.0		16	ns
$\overline{ADD}$ add indicator delayed from ACLK↑	$t_{OD(1)}$	25pF	7.0		31	ns
$\overline{AIND}$ add bus indication output delay from ACLK↑	$t_{OD(4)}$		7.0		31	ns
A(7-0)/APAR data /parity out tristate to driven delay from ACLK↑	$t_{OD(5)}$	75pF	5.0		7.0	ns

Note: All output times are measured with the specified load capacitance.

Figure 11. Microprocessor Read Cycle Timing - Multiplex Bus



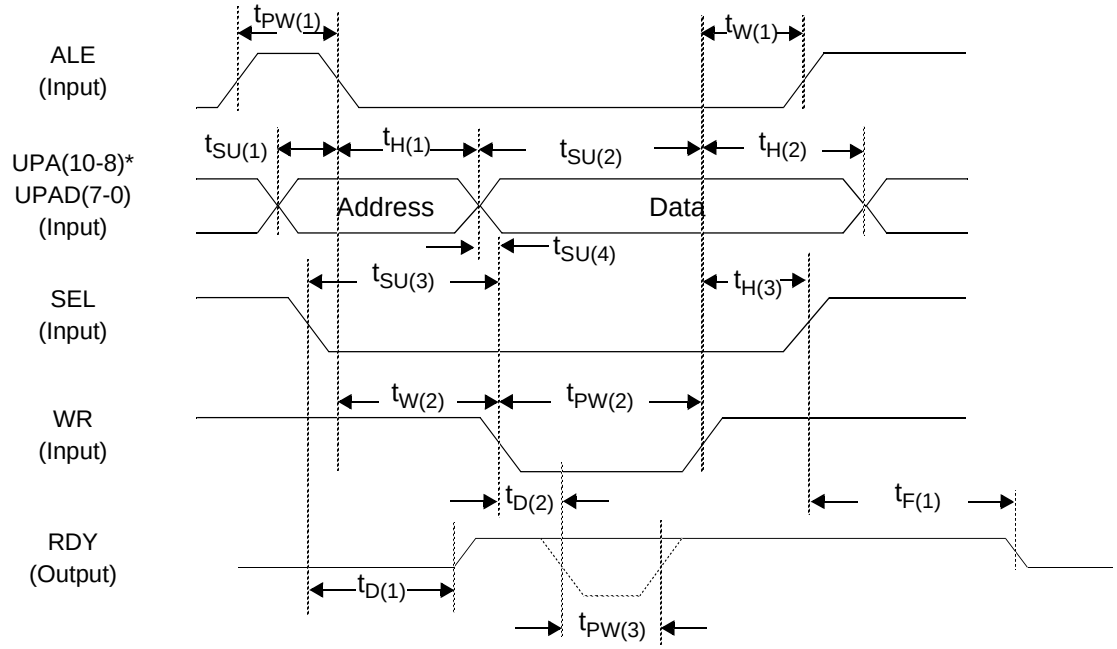
Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20			ns
UPA(10-8) and UPAD(7-0) address setup time before ALE↓	$t_{SU(1)}$	5.0			ns
UPA(10-8) and UPAD(7-0) address hold time after ALE↓	$t_{H(1)}$	3.0			ns
UPA(10-8) and UPAD(7-0) address hold time after $\overline{RD}$↓	$t_{H(2)}$			2.0	ns
UPAD(7-0) data output delay to tristate after $\overline{RD}$↑	$t_{OD(1)}$	2.0		11	ns
ALE wait time after $\overline{RD}$↑	$t_{W(1)}$	0.0			ns
$\overline{SEL}$ setup before $\overline{RD}$↓	$t_{SU(2)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{RD}$↑	$t_{H(3)}$	0.0			ns
$\overline{RD}$ wait after ALE↓	$t_{W(2)}$	20			ns
$\overline{RD}$ pulse width	$t_{PW(2)}$	40			ns
RDY↑ delay after $\overline{SEL}$↓	$t_{D(1)}$	2.0		10	ns
RDY↓ delay after $\overline{RD}$↓	$t_{D(2)}$	4.0		20	ns
RDY float time after $\overline{SEL}$↑	$t_{F(1)}$	2.0		10	ns

Parameter		Symbol	Min	Typ	Max	Unit
RDY pulse width	Register cycle	$t_{PW(3)}$			0.0	ns
	SPOT instruction read (Note 2)		6 * SPcyc		7 * SPcyc	ns
	Data RAM read (Note 3)		9 * SPcyc		33 * SPcyc	ns
UPAD(7-0) data output delay after $\overline{RD}\downarrow$	Register read only	$t_{OD(2)}$	8.0		28	ns
UPAD(7-0) data output delay after RDY$\uparrow$	SPOT instruction read and data RAM read only	$t_{OD(3)}$			0.0	ns
UPAD(7-0) data output tristate to driven delay after $\overline{RD}\downarrow$		$t_{OD(4)}$	2.0			ns

Notes:

1. All output times are measured with a maximum 75 pF load capacitance.
2. One SPcyc equals two EXTCK clock cycles.
   (The EXTCK clock frequency is 58.32 MHz. One SPcyc is about 34.29 ns.)
3. Excessive external microprocessor data RAM access could interfere with the QE1M internal data processing, resulting in data corruption. To prevent such a situation, when excessive external microprocessor data RAM access is detected, QE1M tries to slow down the external microprocessor access rate by lengthening the RDY pulse width to as high as 97 * SPcyc.

Figure 12. Microprocessor Write Cycle Timing - Multiplex Bus



* Address input only

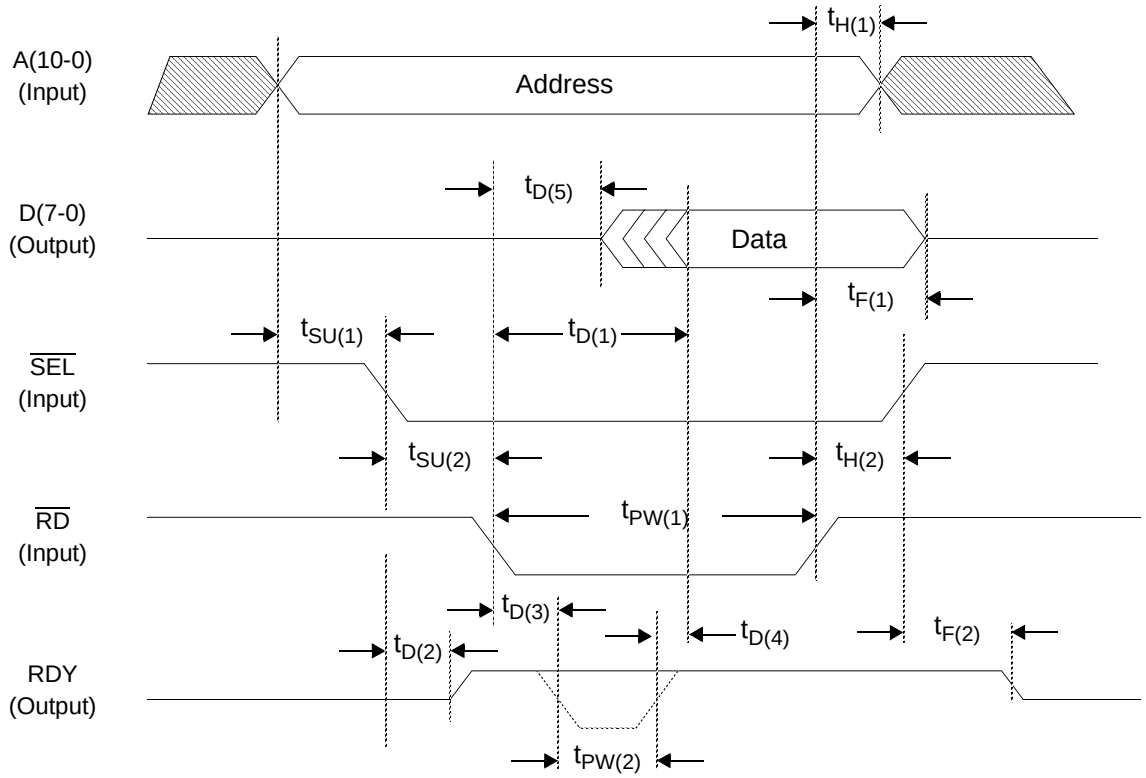
Parameter	Symbol	Min	Typ	Max	Unit
ALE pulse width	$t_{PW(1)}$	20			ns
ALE wait after $\overline{WR}\uparrow$	$t_{W(1)}$	0.0			ns
UPA(10-8) and UPAD(7-0) address setup time before ALE$\downarrow$	$t_{SU(1)}$	5.0			ns
UPA(10-8) and UPAD(7-0) address hold time after ALE$\downarrow$	$t_{H(1)}$	3.0			ns
UPAD(7-0) data input setup time before $\overline{WR}\uparrow$	$t_{SU(2)}$	12			ns
UPAD(7-0) data input hold time after $\overline{WR}\uparrow$	$t_{H(2)}$	6.0			ns
$\overline{SEL}$ setup time before $\overline{WR}\downarrow$	$t_{SU(3)}$	0.0			ns
$\overline{SEL}$ hold time after $\overline{WR}\uparrow$	$t_{H(3)}$	0.0			ns
$\overline{WR}$ wait after ALE$\downarrow$	$t_{W(2)}$	20			ns
$\overline{WR}$ pulse width	$t_{PW(2)}$	40			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(1)}$	2.0		10	ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$	$t_{D(2)}$	4.0		20	ns
RDY float time after $\overline{SEL}\uparrow$	$t_{F(1)}$	2.0		10	ns

Parameter		Symbol	Min	Typ	Max	Unit
RDY pulse width	Register write	$t_{PW(3)}$			0.0	ns
	SPOT instruction write (Note 2)		5 * SPcyc		7 * SPcyc	ns
	Data RAM write (Note 3)		9 * SPcyc		29 * SPcyc	ns
Data valid set up time to $\overline{WR}\uparrow$	SPOT instruction write and data RAM write only	$t_{SU(4)}$	-1 * SPcyc			ns

Notes:

1. All output times are measured with a maximum 75 pF load capacitance.
2. One SPcyc equals two EXTCK clock cycles.
   (The EXTCK clock frequency is 58.32 MHz. One SPcyc is about 34.29 ns.)
3. Excessive external microprocessor data RAM access could interfere with the QE1M internal data processing, resulting in data corruption. To prevent such a situation, when excessive external microprocessor data RAM access is detected, QE1M tries to slow down the external microprocessor access rate by lengthening the RDY pulse width to as high as 97 * SPcyc.

Figure 13. Microprocessor Read Cycle Timing - Intel



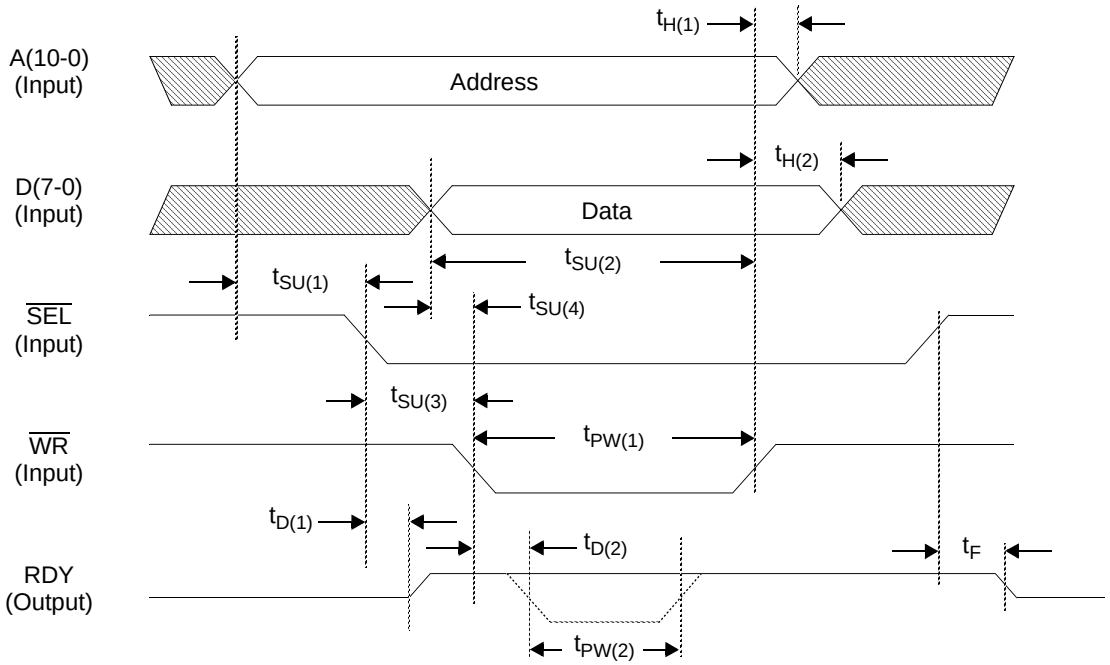
Parameter	Symbol	Min	Typ	Max	Unit
A(10-0) address setup time to $\overline{SEL}\downarrow$	$t_{SU(1)}$	0.0			ns
A(10-0) address hold time after $\overline{RD}\uparrow$	$t_{H(1)}$	3.0			ns
D(7-0) data output float time after $\overline{RD}\uparrow$	$t_{F(1)}$	2.0		11	ns
$\overline{SEL}\downarrow$ setup time to $\overline{RD}\downarrow$	$t_{SU(2)}$	10			ns
$\overline{RD}$ pulse width	$t_{PW(1)}$	40			ns
$\overline{SEL}\downarrow$ hold time after $\overline{RD}\downarrow$	$t_{H(2)}$	0.0			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$	$t_{D(2)}$	2.0		10	ns
RDY$\downarrow$ delay after $\overline{RD}\downarrow$	$t_{D(3)}$	4.0		20	ns
RDY float time after $\overline{SEL}\uparrow$	$t_{F(2)}$	2.0		10	ns

Parameter		Symbol	Min	Typ	Max	Unit
RDY pulse width	Register read	$t_{PW(2)}$			0.0	ns
	SPOT instruction read (Note 2)		6 * SPcyc		7 * SPcyc	ns
	Data RAM read (Note 3)		9 * SPcyc		33 * SPcyc	ns
Data output valid delay after $\overline{RD}\downarrow$	Register read only	$t_{D(1)}$	8.0		28	ns
Data output valid delay after RDY$\uparrow$	SPOT instruction read and data RAM read only	$t_{D(4)}$			0.0	ns
Data output tristate to driven delay after $\overline{RD}\downarrow$		$t_{D(5)}$	2.0			ns

Notes:

1. All output times are measured with a maximum 75 pF load capacitance.
2. One SPcyc equals two EXTCK clock cycles.
   (The EXTCK clock frequency is 58.32 MHz. One SPcyc is about 34.29 ns.)
3. Excessive external microprocessor data RAM access could interfere with the QE1M internal data processing, resulting in data corruption. To prevent such a situation, when excessive external microprocessor data RAM access is detected, QE1M tries to slow down the external microprocessor access rate by lengthening the RDY pulse width to as high as 97 * SPcyc.

Figure 14. Microprocessor Write Cycle Timing - Intel

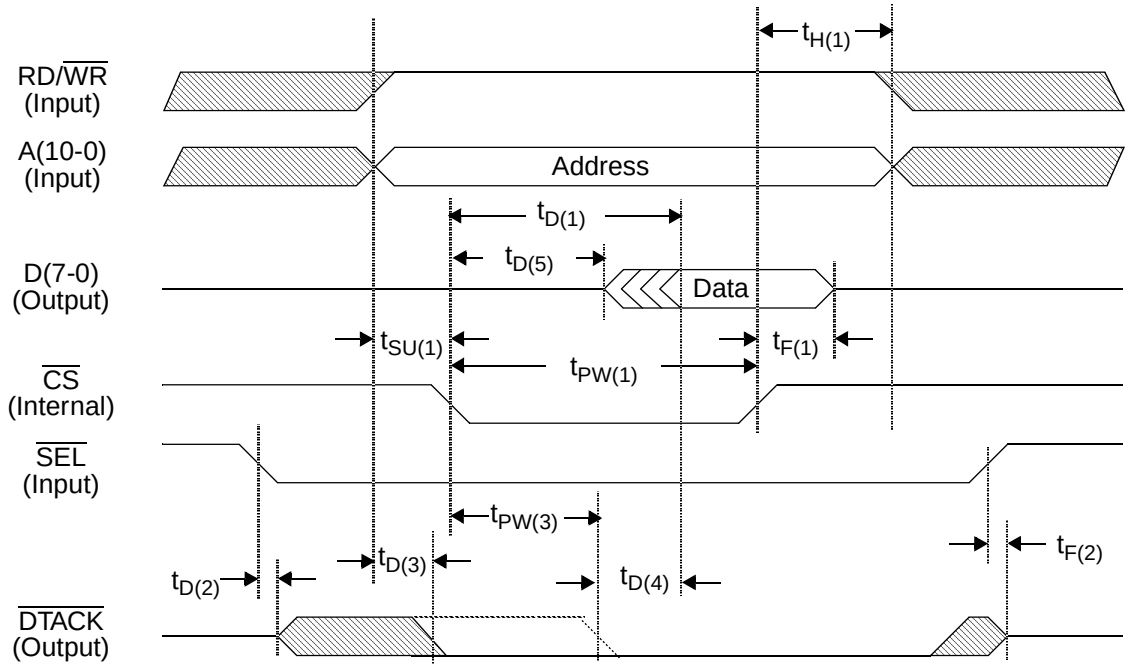


Parameter		Symbol	Min	Typ	Max	Unit
A(10-0) address setup time to $\overline{SEL}\downarrow$		$t_{SU(1)}$	0.0			ns
A(10-0) address hold time after $\overline{WR}\uparrow$		$t_{H(1)}$	3.0			ns
D(7-0) data input valid setup time to $\overline{WR}\uparrow$		$t_{SU(2)}$	12			ns
D(7-0) data input hold time after $\overline{WR}\uparrow$		$t_{H(2)}$	6.0			ns
$\overline{SEL}$ setup time to $\overline{WR}\downarrow$		$t_{SU(3)}$	10			ns
$\overline{WR}$ pulse width		$t_{PW(1)}$	40			ns
RDY$\uparrow$ delay after $\overline{SEL}\downarrow$		$t_{D(1)}$	2.0		10	ns
RDY$\downarrow$ delay after $\overline{WR}\downarrow$		$t_{D(2)}$	4.0		20	ns
RDY float time after $\overline{SEL}\uparrow$		t_F	2.0		10	ns
RDY pulse width	Register write	$t_{PW(2)}$			0.0	ns
	SPOT instruction write (Note 2)		5 * SPcyc		7 * SPcyc	ns
	Data RAM write (Note 3)		9 * SPcyc		29 * SPcyc	ns
D(7-0) data valid setup time to $\overline{WR}\downarrow$	SPOT instruction write and data RAM write only	$t_{SU(4)}$	-1 * SPcyc			ns

Notes:

1. All output times are measured with a maximum 75 pF load capacitance.
2. One SPcyc equals two EXTCK clock cycles.
   (The EXTCK clock frequency is 58.32 MHz. One SPcyc is about 34.29 ns.)
3. Excessive external microprocessor data RAM access could interfere with the QE1M internal data processing, resulting in data corruption. To prevent such a situation, when excessive external microprocessor data RAM access is detected, QE1M tries to slow down the external microprocessor access rate by lengthening the RDY pulse width to as high as 97 * SPcyc.

Figure 15. Microprocessor Read Cycle Timing - Motorola



Note: $\overline{CS}$ is an internal signal which is the logical OR of the $\overline{SEL}$ and $\overline{LDS}$ lead input signals.
Its timing parameters refer to whichever of these signals controls the associated transition.

Parameter		Symbol	Min	Typ	Max	Unit
A(10-0) address setup time and RD/$\overline{WR}\uparrow$ setup time before $\overline{CS}\downarrow$		$t_{SU(1)}$	10			ns
A(10-0) address hold time and RD/$\overline{WR}\downarrow$ delay time after $\overline{CS}\uparrow$		$t_{H(1)}$	3.0			ns
D(7-0) data output float time after $\overline{CS}\uparrow$		$t_{F(1)}$	2.0		11	ns
$\overline{CS}$ pulse width		$t_{PW(1)}$	40			ns
$\overline{DTACK}$ driven delay after $\overline{SEL}\downarrow$		$t_{D(2)}$	2.0		10	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$		$t_{F(2)}$	2.0		10	ns
$\overline{DTACK}\downarrow$ stable delay after address becomes stable (Note 4)		$t_{D(3)}$	6.0		26	ns
$\overline{DTACK}$ pulse width	Register read	$t_{PW(3)}$			0.0	ns
	SPOT instruction read (Note 2)		6 x SPcyc		7 x SPcyc	ns
	Data RAM read (Note 3)		9 x SPcyc		33 x SPcyc	ns
D(7-0) data output delay after $\overline{CS}\downarrow$	Register read only	$t_{D(1)}$	8.0		28	ns
D(7-0) data output delay after $\overline{DTACK}\downarrow$	SPOT instruction read and data RAM read only	$t_{D(4)}$			0.0	ns
D(7-0) data output tristate to drive delay after $\overline{CS}\downarrow$		$t_{D(5)}$	2.0			ns

Notes:

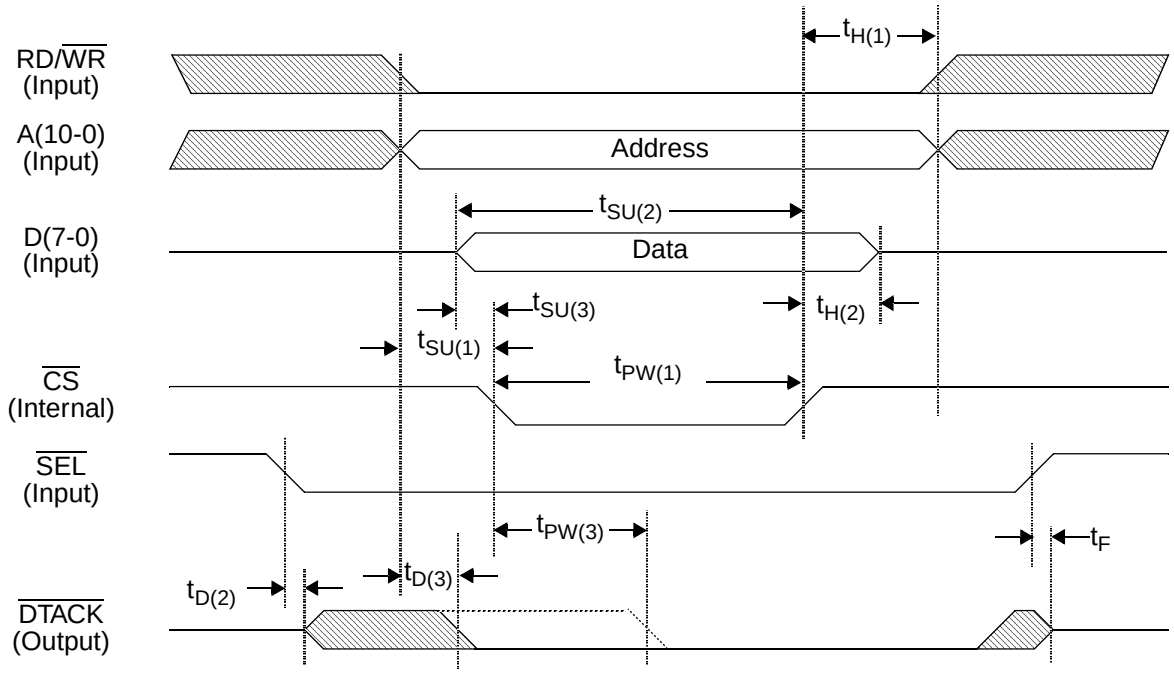
1. All output times are measured with a maximum 75 pF load capacitance.
2. One SPcyc equals two EXTCK clock cycles.
   (The EXTCK clock frequency is 58.32 MHz. One SPcyc is about 34.29 ns.)
3. Excessive external microprocessor data RAM access could interfere with the QE1M internal data processing, resulting in data corruption. To prevent such a situation, when excessive external microprocessor data RAM access is detected, QE1M tries to slow down the external microprocessor access rate by lengthening the $\overline{\text{DTACK}}$ pulse width to as high as 97 x SPcyc. To avoid such delays the following are TranSwitch recommendations for access frequency for the QE1M SPOT data RAM (addresses are shaded in the memory map at the end of the data sheet).

   a. Use 16 wait states for a read or write access if the $\overline{\text{DTACK}}$ signal is not being used. Forcing a longer wait state for every access may create unwanted delays in the internal process for the QE1M. Using the 16 wait states will provide reliability without causing excessive process delays (at the 25 MHz microprocessor frequency). For other frequencies, use an equivalent number of wait states that equals approximately 640 ns.

   b. Maintain no more than 16 microprocessor accesses per 125 µs frame period.

   c. Maintain a minimum of 600 ns between microprocessor accesses.
4. During a SPOT instruction read or data RAM read cycle, $\overline{\text{DTACK}}$ stays high after $t_{D(3)}$. During a register read cycle, $\overline{\text{DTACK}}$ settles to low after $t_{D(3)}$. $\overline{\text{DTACK}}$ may go directly from a low to a high impedance state.

Figure 16. Microprocessor Write Cycle Timing - Motorola



Note: $\overline{CS}$ is an internal signal which is the logical OR of the $\overline{SEL}$ and $\overline{LDS}$ lead input signals.
Its timing parameters refer to whichever of those signals controls the associated transition.

Parameter		Symbol	Min	Typ	Max	Unit
A(10-0) address setup time and RD/$\overline{WR}\downarrow$ setup time before $\overline{CS}\downarrow$		$t_{SU(1)}$	10			ns
A(10-0) address hold time and RD/$\overline{WR}\uparrow$ delay time after $\overline{CS}\uparrow$		$t_{H(1)}$	3.0			ns
D(7-0) data input setup time before $\overline{CS}\uparrow$		$t_{SU(2)}$	12			ns
D(7-0) data input hold time after $\overline{CS}\uparrow$		$t_{H(2)}$	6.0			ns
$\overline{CS}$ pulse width		$t_{PW(1)}$	40			ns
$\overline{DTACK}$ driven delay after $\overline{SEL}\downarrow$		$t_{D(2)}$	2.0		10	ns
$\overline{DTACK}$ float time after $\overline{SEL}\uparrow$		t_F	2.0		10	ns
$\overline{DTACK}\downarrow$ stable delay after address becomes stable (Note 4)		$t_{D(3)}$	6.0		26	ns
$\overline{DTACK}$ pulse width	Register write	$t_{PW(3)}$			0.0	ns
	SPOT instruction write (Note 2)		5 x SPcyc		7 x SPcyc	ns
	Data RAM write (Note 3)		9 x SPcyc		29 x SPcyc	ns
D(7-0) data valid setup time to $\overline{CS}\downarrow$	SPOT instruction write and data RAM write only	$t_{SU(3)}$	-1 x SPcyc			ns

Notes:

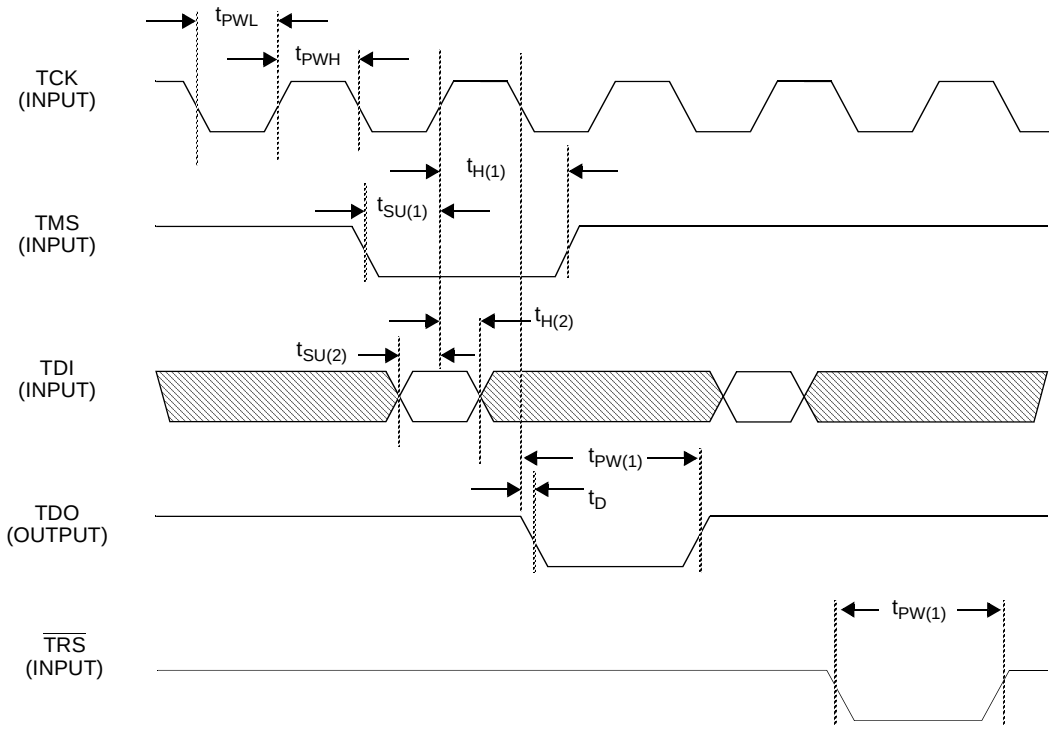
1. All output times are measured with a maximum 75 pF load capacitance.
2. One SPcyc equals two EXTCK clock cycles.
   (The EXTCK clock frequency is 58.32 MHz. One SPcyc is about 34.29 ns.)
3. Excessive external microprocessor data RAM access could interfere with the QE1M internal data processing, resulting in data corruption. To prevent such a situation, when excessive external microprocessor data RAM access is detected, QE1M tries to slow down the external microprocessor access rate by lengthening the $\overline{\text{DTACK}}$ pulse width to as high as 97 x SPcyc. To avoid such delays the following are TranSwitch recommendations for access frequency for the QE1M SPOT data RAM (addresses are shaded in the memory map at the end of the data sheet).

   a. Use 16 wait states for a read or write access if the $\overline{\text{DTACK}}$ signal is not being used. Forcing a longer wait state for every access may create unwanted delays in the internal process for the QE1M. Using the 16 wait states will provide reliability without causing excessive process delays (at the 25 MHz microprocessor frequency). For other frequencies, use an equivalent number of wait states that equals approximately 640 ns.

   b. Maintain no more than 16 microprocessor accesses per 125 µs frame period.

   c. Maintain a minimum of 600 ns between microprocessor accesses.
4. During a SPOT instruction write or data RAM write cycle, $\overline{\text{DTACK}}$ stays high after $t_{D(3)}$. During a register write cycle, $\overline{\text{DTACK}}$ settles to low after $t_{D(3)}$. $\overline{\text{DTACK}}$ may go directly from a low to a high impedance state.

Figure 17. Boundary Scan Timing



Parameter	Symbol	Min	Max	Unit
TCK clock high time	t_{PWH}	50		ns
TCK clock low time	t_{PWL}	50		ns
TMS setup time before TCK↑	$t_{SU(1)}$	3.0	-	ns
TMS hold time after TCK↑	$t_{H(1)}$	2.0	-	ns
TDI setup time before TCK↑	$t_{SU(2)}$	3.0	-	ns
TDI hold time after TCK↑	$t_{H(2)}$	2.0	-	ns
TDO delay from TCK↓ (Note 1)	t_D	-	22	ns
$\overline{TRS}$ Pulse Width	$t_{PW(1)}$	20	-	ns

Note 1: The output time (TDO) is measured with a maximum of 75 pF load capacitance.

OPERATION

The following sections detail the internal operation of the Quad E1 Mapper.

BUS INTERFACE MODES

The Quad E1 Mapper supports the following bus modes of operation:

- Drop Mode
- Single Unidirectional Ring Mode
- Multiplexer Mode
- Dual Unidirectional Ring Mode

Drop Mode

In the drop mode of operation, a TU/VT is terminated from either the A or B Drop bus to the receive output of one of the four ports, without a return path in the transmit direction.

Single Unidirectional Ring Mode

In the single unidirectional ring mode of operation, a TU/VT is dropped from the A (or B) Drop bus, with the return path the A (or B) Add bus. Timing for the TU/VT to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

Multiplexer Mode

In the multiplexer mode of operation, a TU/VT is dropped from the A (or B) Drop bus, with the return path the B (or A) Add bus. Timing for the TU/VT to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

Dual Unidirectional Ring Mode

In the dual unidirectional ring mode of operation, a TU/VT is dropped from the A (or B) Drop bus, with the return path both the A and B Add buses. Timing for the TU/VT to be added to the A (or B) Add bus is derived from either the A (or B) Drop bus, or from the A (or B) Add bus.

BUS MODE SELECTION

TU/VT bus mode selection is performed by the control bits defined in the table shown below. The n represents the port number (1-4). Note: Both the A and B Add buses power up in the high impedance state. A 0 must be written to control bits AAHZE and BAHZE for normal add bus operation.

Mode Type	TnSEL1	TnSEL0	RnSEL	DROP from Bus	ADD to Bus
Dropping only, from A	0	0	0	A	Drop-only (1)
Dropping only, from B	0	0	1	B	Drop-only (1)
Adding only, to A	0	1	0	Add-only (2)	A
Adding only, to B	0	1	1	Add-only (2)	B
Single unidirectional ring	0	1	0	A	A
Single unidirectional ring	0	1	1	B	B
Multiplexer, A in, B out	1	0	0	A	B
Multiplexer, B in, A out	1	0	1	B	A
Dual unidirectional ring	1	1	0	A	A and B
Dual unidirectional ring	1	1	1	B	B and A

Notes:

1. When the drop-only mode is selected, the ability to add a TU/VT is disabled, and the add bus is tri-stated.
2. The add-only feature is enabled by writing a 1 to control bit FRDISn. The FEBE value and RDI states are transmitted as zero. However, the microprocessor can send an RDI, if required.

Bus Mode Selection for Port n

SDH/SONET ADD/DROP MULTIPLEXING FORMAT SELECTIONS

The control bit settings for format selection are given in the table shown below. When the STS-1 format is selected, the buses are configured to operate at a bus rate of 6.48 Mbyte/s, instead of 19.44 Mbyte/s for VC-4/AU-3/STS-3 formats.

Format	MOD1	MOD0
STS-1 Format	0	0
STS-3 Format	0	1
STM-1 AU-3 Format	1	0
STM-1 TUG-3/VC-4 Format	1	1

Format Selection

DROP TU/VT SELECTION

The TU-12 (VT2) number selection register labels (RTUNn), which consist of seven bits, are given in the following table. An out of range value forces a high impedance state at the E1 receive interface. In addition, the FEBE and RDI states will be transmitted as zeros.

Locations 04CH (port 1), 07CH (port 2), 0ACH (port 3), 0DCH (port 4)

Bit	6	5	4	3	2	1	0	
AU-3/TUG-3 or STS-1 ID			TU/VT Group Number			TU/VT Number		Meaning
0	0		0	0	0	0	0	No TU/VT Selected
0	0							STS-1
0	1							AU-3/TUG-3 A, STS-1 #1
1	0							AU-3/TUG-3 B, STS-1 #2
1	1							AU-3/TUG-3 C, STS-1 #3
			0	0	1			TU/VT Group Number 1
			0	1	0			TU/VT Group Number 2
			0	1	1			TU/VT Group Number 3
			1	0	0			TU/VT Group Number 4
			1	0	1			TU/VT Group Number 5
			1	1	0			TU/VT Group Number 6
			1	1	1			TU/VT Group Number 7
						0	0	No TU/VT Selected
						0	1	TU/VT Number 1
						1	0	TU/VT Number 2
						1	1	TU/VT Number 3

TU/VT Selection

ADD TU/VT SELECTION

The TU-12 (VT2) number selection register labels (TTUNn), which consist of seven bits, are given in the following table. An out of range value forces a high impedance state on the add bus.

Locations 04DH (port 1), 07DH (port 2), 0ADH (port 3), 0DDH (port 4)

Bit	6	5	4	3	2	1	0	
AU-3/TUG-3 or STS-1 ID			TU/VT Group Number			TU/VT Number		Meaning
0	0		0	0	0	0	0	No TU/VT Selected
0	0							STS-1
0	1							AU-3/TUG-3 A, STS-1 #1
1	0							AU-3/TUG-3 B, STS-1 #2
1	1							AU-3/TUG-3 C, STS-1 #3
			0	0	1			TU/VT Group Number 1
			0	1	0			TU/VT Group Number 2
			0	1	1			TU/VT Group Number 3
			1	0	0			TU/VT Group Number 4
			1	0	1			TU/VT Group Number 5
			1	1	0			TU/VT Group Number 6
			1	1	1			TU/VT Group Number 7
						0	0	No TU/VT Selected
						0	1	TU/VT Number 1
						1	0	TU/VT Number 2
						1	1	TU/VT Number 3

TU/VT Selection

BUS TIMING

Timing for adding a TU/VT to the add bus is derived from the like-named drop bus, or from the like-named add bus. Bus timing may be selected by using a lead, or through software. Upon power-up or a device reset, the SBTEN (Software Bus Timing Enable) control bit is reset to 0 and the $\overline{\text{ABUST}}$ lead controls bus timing selection. To enable the software to control timing, the SBTEN control bit must be first written with a 1, which will override the state placed on the $\overline{\text{ABUST}}$ lead. When SBTEN is 1, bus timing (add or drop bus timing) is controlled by the DRPBT control bit. The various states associated with the bus timing selection are shown in the table below.

$\overline{\text{ABUST}}$ lead	SBTEN	DRPBT	Action
Low	0	X	Add bus timing selected by $\overline{\text{ABUST}}$ lead.
High	0	X	Drop bus timing selected by $\overline{\text{ABUST}}$ lead.
X	1	0	Add bus timing selected by DRPBT bit.
X	1	1	Drop bus timing selected by DRPBT bit.

Note: X = Don't Care

Bus Timing Selection

UNEQUIPPED OPERATION

The QE1M is capable of sending an unequipped channel or unequipped supervisory channel in all add modes of operation. Generally a channel which has either the UCHnE bit or both the UCHnE and USCHnE bits set in the port provisioning registers will add an unequipped channel or unequipped supervisory channel for the TU/VT selected. An unequipped channel has a TU/VT pointer consisting of a valid NDF, size bits equal to 01, and a fixed pointer value of 105. The remaining VT overhead bytes and the payload are sent as zeros. The unequipped supervisory channel has an identical pointer to the unequipped channel, but sends a valid J2 byte, and valid BIP-2 bits and RDI-bit in V5, and valid RDI-bits in Z7. The QE1M also sends a valid Z6 byte. The V5, RDI, Z7 RDI, and Z6 bytes can be set to zero by other control bits if they are not required. There are some differences in operation based on the UEAME bit in register 014H. The following table describes these differences.

Unequipped Channel Generation

UCHnE/USCHnE	UEAME	Add/Drop Mode	Drop From	A add	B add
0	X[1]	Mux	A	High-Z	Normal
			B	Normal	High-Z
		Single Unidirectional Ring	A	Normal	High-Z
			B	High-Z	Normal
		Bidirectional Ring	A	Normal	Normal
			B	Normal	Normal
		Drop Only	A	High-Z	High-Z
			B	High-Z	High-Z
1	0	Mux	A	Unequipped[2]	Normal
			B	Normal	Unequipped[2]
		Single Unidirectional Ring	A	Unequipped	High-Z
			B	High-Z	Unequipped
		Bidirectional Ring	A	Unequipped	Unequipped
			B	Unequipped	Unequipped
		Drop Only	A	High-Z	High-Z
			B	High-Z	High-Z
	1	Mux	A	High-Z	Unequipped[2]
			B	Unequipped[2]	High-Z
		Single Unidirectional Ring	A	Unequipped	High-Z
			B	High-Z	Unequipped
		Bidirectional Ring	A	Unequipped	Unequipped
			B	Unequipped	Unequipped
		Drop Only	A	High-Z	High-Z
			B	High-Z	High-Z

Notes:

1. X = Don't Care (0 or 1).
2. Only Multiplexed Mode is effected by the UEAME control bit. All other modes operate the same way regardless of the state of the UEAME control bit.

DROP BUS MULTIFRAME ALIGNMENT

V1 byte alignment in the receive direction (from the drop bus) is established by using the H4 byte or the V1 reference pulse in the ADC1J1V1 and BDC1J1V1 signal. Depending on the format, one or three V1 pulses will be present in this signal. When the H4 byte is used to establish V1 byte alignment, the V1 pulse does not have to be present in the ADC1J1V1 or BDC1J1V1 signal. Writing a 1 to control bit DV1SEL selects the V1 pulse in the ADC1J1V1 and BDC1J1V1 signal to be used to establish the V1 byte location reference, while a 0 selects the H4 byte as the multiframe detector for establishing the V1 reference. The H4 multiframe detection circuits are disabled when the V1 pulse is used in place of the H4 byte.

For STM-1 VC-4 operation, a single V1 pulse must occur three drop bus clock cycles every four frames following the J1 pulse. For STM-1 AU3/STS-3 operation, three V1 pulses must be present every four frames. Each V1 pulse must be present three clock cycles after the corresponding J1 pulse, when the SPE signal is high. For example, in a VC-4 signal, the J1 pulse identifies the J1 byte location (defined as the starting location for the VC-4) in the POH bytes. In the next column (first clock cycle) all the rows are assigned as fixed stuff. Similarly, in the next column (second clock cycle) all the rows are assigned as fixed stuff. The next column (third clock cycle) defines the start of TUG-3 A. This column is where the V1 pulse occurs every four frames. However, the actual V1 byte occurs six clock cycles after the V1 pulse.

For STS-1 operation, one V1 pulse must be present. The V1 pulse must occur on the next clock cycle after J1, and when the SPE signal is high. The J1 pulse identifies the J1 byte location (defined as the starting location for the STS-1) in the POH bytes. The next column (first clock cycle) defines the VTs starting location. Thus, the V1 pulse identifies the starting location of the first V1 byte in the signal. The rest of the V1 bytes for the 21 VT2s are also aligned with respect to the V1 pulse. The timing relationships between J1, V1, and other signals are shown in the Timing Characteristics section.

The H4 byte is used to identify the location of the V1 byte as shown in 18 below:

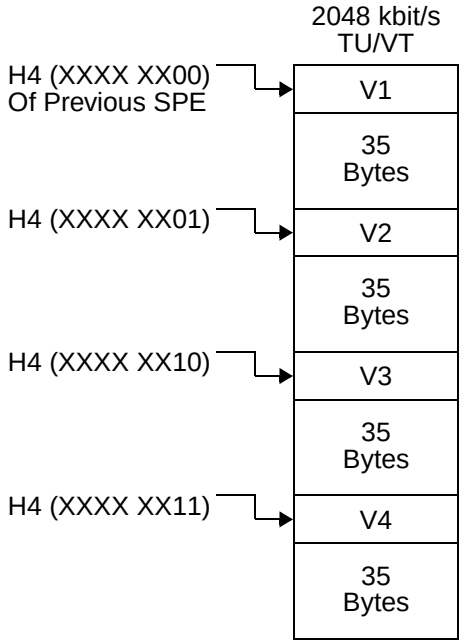


Figure 18. H4 Byte Floating VT Mode Bit Allocation

The H4 byte is monitored for multiframe alignment when enabled. Loss of multiframe alignment is declared (AsDH4E, BsDH4E) if two or more H4 byte values differ from those of a 2-bit counter for two consecutive multiframes. Recovery occurs when four consecutive sequential H4 byte values are detected once.

ADD BUS MULTIFRAME ALIGNMENT

When drop bus timing is selected, add bus V1 alignment is based on the drop bus V1 pulse (A/BDC1J1V1) if DV1SEL is 1, or on the V1 reference signal that is generated by the H4 multiframe detectors in the drop bus side if DV1SEL is 0.

When add bus timing is selected and a 0 is written to control bit DV1REF, V1 byte alignment for the add bus is established by using the V1 pulses that must be present in the A/BAC1J1V1 signal. When add bus timing is selected and a 1 is written to control bit DV1REF, V1 byte alignment for the add bus is determined by the drop bus V1 reference from either the A/BDC1J1V1 signal (if DV1SEL is 1), or from the internal V1 reference signal generated by the H4 multiframe detector in the drop bus direction (if DV1SEL is 0). The V1 pulse that is present in the A/BAC1J1V1 signal is ignored. Extreme care must be taken when using this V1 selection mode to prevent add bus V1 byte alignment slips.

The control bit selection for both V1 add and drop bus byte alignment is described in the table below.

Bus Timing Mode	DV1REF	DV1SEL	Action
Drop bus timing selected	0	0	Drop bus A/B H4 multiframe detector determines dropped TU/VT V1 byte starting location, and added TU/VT V1 byte starting location. V1 pulse in drop bus A/BDC1J1V1 signal ignored.
Drop bus timing selected	0	1	Drop bus V1 pulse in the A/BDC1J1V1 signal determines dropped TU/VT V1 byte starting location, and added TU/VT V1 byte starting location. A/B drop bus H4 multiframe detector disabled.
Add bus timing selected	0	0	Drop bus A/B H4 multiframe detector determines dropped TU/VT V1 byte starting location. V1 pulse in drop bus A/BDC1J1V1 signal ignored. Add bus V1 alignment determined by the V1 pulse in the add bus A/BAC1J1V1 signal.
Add bus timing selected	0	1	Drop bus V1 pulse in the A/BDC1J1V1 signal determines dropped TU/VT starting location. Drop bus H4 multiframe detector disabled. Add bus V1 alignment determined by the V1 pulse in the add bus A/BAC1J1V1 signal.
Add bus timing selected	1	0	Drop bus A/B H4 multiframe detector determines dropped TU/VT V1 byte starting location. V1 pulses in drop bus A/BDC1J1V1 and add bus A/BAC1J1V1 signals are ignored. Add bus V1 alignment determined by the internal V1 pulse generated by the drop bus A/B H4 byte detector.
Add bus timing selected	1	1	Drop bus V1 pulse in the A/BDC1J1V1 signal determines dropped TU/VT V1 byte starting location, A/B drop bus H4 multiframe detector disabled. V1 pulse in add bus A/BAC1J1V1 signal is ignored. Add bus V1 alignment determined by the V1 pulse in the drop bus A/BDC1J1V1 signal.

Note: X = Don't Care. Bus timing mode is selected via lead $\overline{\text{ABUST}}$ and control bits SBTEN, DRPBT, as described earlier.

Add and Drop Bus V1 Reference Selection

PERFORMANCE COUNTERS

All performance counters are saturating, with the counters stopping at their maximum count. A counter is reset to zero by a hardware or software device reset, and when it is read by the microprocessor. The performance counters for port n are also reset when a 1 is written to control bit RnSETC. This bit is self-clearing, and does not require the microprocessor to write a 0 into its location. Counts that occur during the read cycle are held and updated afterwards. For a 16-bit counter, the low order byte must be read first, followed by reading the high order byte before the corresponding low order byte for another port is read.

ALARM STRUCTURE

All alarm indications are reported as unlatched and latched status bits. The latched bit of an alarm can be set on the positive transitions, negative transitions, both positive and negative transitions, or positive levels of the alarm. Reading a latched alarm bit clears the bit to 0.

When control bit LATEN (address 011H, bit 4) is written with a 1, the latching of alarm transitions is enabled. Control bits IPOS and INEG (address 012H, bits 5 and 4) should be programmed to select the transition(s) on which latched bits are set. When LATEN is written with a 0, the latched bits are set on positive levels of the alarms. The IPOS and INEG bits are disabled when LATEN is set to 0.

Alarm Hierarchy Mask

Since multiple alarms at various levels can be detected simultaneously, a hierarchical masking scheme is employed in the QE1M. The QE1M hierarchical mask effectively eliminates the confusion caused by the simultaneous reporting of multiple alarms and speeds up the identification of the alarm origins.

The following table shows the hierarchical masking of unlatched low level alarms by high order alarms (depending on the Drop Bus selected and the Port selected). Masked cells indicate the lower level alarm masked by the high order alarms. For example: low level alarms J2LOL and J2TIM are masked when any of the following high order alarms/conditions are active: DLOC, OOR, UAISI, DH4E, AIS, LOP or SLER.

High Order Alarms or Conditions	Low Level Alarms masked by High Order Alarms							
	UAISI DH4E	LOP AIS NDF SIZE	SLER	RFI UNEQ	J2LOL J2TIM	RDIS RDIP RDIC	TCUQ TCAIS TCLM	TCLL TCTM TCODI TCRDI
DLOC	•	•	•	•	•	•	•	•
OOR[1]		•	•	•	•	•	•	•
UAISI[2], DH4E[3]		•	•	•	•	•	•	•
AIS, LOP			•	•	•	•	•	•
Signal Label =001 or =000			•					
SLER[5]					•			
TCLM[4]								•

Notes:

1. OOR: Receive TU/VT Out Of Range is the condition when the receive TU/VT select bits (registers 0x4C, 7C, AC, DC) are set to an invalid value in which no TU/VT is selected (e.g. 0x00). There is no alarm bit to indicate this condition.
2. When control bit HEAISE is 1
3. When control bit DV1SEL is 0
4. When control bit TCnEN is 1
5. When control bit 1BnRDI = 0

   When control bit 1BnRDI = 1, then J2 Message Tracking is still enabled and SLER alarm will not mask J2LOL and J2TIM.

INTERRUPT STRUCTURE

The interrupt indication register (address 020H) contains the global software interrupt bit INT and other interrupt indication bits. Each interrupt indication bit has an associated set of latched alarm bits. A mask bit is provided to enable the set of latched alarms to trigger their interrupt indication bit. For port alarms, the latched alarms of each port are further divided into several groups. A second level of mask bit is provided for each of these groups to mask out the interrupt indication bit of the port. For each interrupt indication bit, if its interrupt mask bits are 1, and one or more of its associated latched alarm bits are set, the interrupt indication bit will become 1; which in turn causes the software interrupt indication bit INT to become 1. The QE1M also generates a hardware interrupt at the tristate 8mA interrupt lead INT(INT/$\overline{\text{IRQ}}$), lead 152 or D6, provided the hardware interrupt enable bit (HWDIE) is 1.

Addresses 016H and 021H are the first set of interrupt mask registers. The additional mask registers for the port alarms are contained in addresses 017H, 018H and 019H. Upon power-up, when the RESET bit (bit 7 in address 015H) is written with a 1, or an active low is placed on the RESET lead (lead 155 or C5), all the interrupt mask bits are cleared to 0. They must be initialized to 1 in order to enable the interrupt indication bits. Control bits IPOS, INEG and LATEN should also be programmed to determine how the latched alarms are to be set.

Consider alarm AnAIS. Assume that HWDIE is 1, the interrupt masks for AnAIS are 1, the control bits IPOS and LATEN are 1, and control bit INEG is 0. Since AnAIS is a port alarm, interrupt mask bit PnMSK and the second level mask bit RPTnA should be set to 1. A positive transition on AnAIS causes the latched bit of AnAIS to be set, which in turn sets the interrupt indication bit PORTn. Then, both software and hardware interrupts occur.

When an interrupt occurs, the external microprocessor can determine the alarm that caused the interrupt by reading the latched alarm registers that correspond to the interrupt indication bit and interrupt mask bit. The read cycles allow the microprocessor to determine what alarm has been set. When the register containing the latched alarm (e.g., AnAIS) has been read, the latched alarm bit is cleared, releasing the software interrupt (INT and PORTn returning to 0) and hardware interrupt. If there is more than one alarm in more than one alarm register, each of the corresponding latched alarm registers must be read before the interrupt is released. In addition, the hardware and software interrupt may be released by writing a 0 to the mask bits that correspond to the interrupt indication register. For AnAIS, the interrupt can be masked by writing 0 to PnMSK or to the RPTnA bits.

Interrupt Registers

Address

Interrupt Indication Register (Address 020H)

020H	INT	EXTCK	ASIDE	BSIDE	PORT4	PORT3	PORT2	PORT1

Interrupt Mask Register (Address 016H, 021H)

016H	0	0	0	0	0	0	0	SPTMSK
021H	0	ECKMSK	ASMSK	BSMSK	P4MSK	P3MSK	P2MSK	P1MSK

Additional Interrupt Mask Registers (Addresses 017H, 018H, 019H)

017H	RPT4A	RPT4B	RPT3A	RPT3B	RPT2A	RPT2B	RPT1A	RPT1B
018H	TFIFO4A	TFIFO4B	TFIFO3A	TFIFO3B	TFIFO2A	TFIFO2B	TFIFO1A	TFIFO1B
019H	TPORT4	TPORT3	TPORT2	TPORT1	RFIFO4	RFIFO3	RFIFO2	RFIFO1

Interrupt Indication ASIDE Registers (Addresses 022H, 024H)

A Side Drop/Add Alarms (ASIDE)

022H	ADLOC	AALOC	ADPAR	0	0	A3UAISI	A2UAISI	A1UAISI
024H	LEXTC	0	0	0	0	A3DH4E	A2DH4E	A1DH4E

Interrupt Indication BSIDE Registers (Addresses 026H, 028H)

B Side Drop/Add Alarms (BSIDE)

026H	BDLOC	BALOC	BDPAR	0	0	B3UAISI	B2UAISI	B1UAISI
028H	SPTLOC	WDTEXP	0	PERR	0	B3DH4E	B2DH4E	B1DH4E

Interrupt Indication PORTn Registers (Addresses 030H, 04EH, 05AH, 03AH, 05EH, 05CH, 044H for Port 1)

Port n Alarms (PORTn)

030H 060H 090H 0C0H	AnAIS	AnLOP	AnSIZE	AnNDF	AnRDIS	AnRFI	AnUNEQ	AnSLER
04EH 07EH 0AEH 0DEH	AnRDIP	AnRDIC	0	0	AnJ2LOL	AnJ2TIM	0	0
05AH 08AH 0BAH 0EAH	AnTCUQ	AnTCAIS	AnTCLM	AnTCLL	AnTCTM	AnTCODI	AnTCRDI	0
03AH 06AH 09AH 0CAH	BnAIS	BnLOP	BnSIZE	BnNDF	BnRDIS	BnRFI	BnUNEQ	BnSLER
05EH 08EH 0BEH 0EEH	BnRDIP	BnRDIC	0	0	BnJ2LOL	BnJ2TIM	0	0
05CH 08CH 0BCH 0ECH	BnTCUQ	BnTCAIS	BnTCLM	BnTCLL	BnTCTM	BnTCODI	BnTCRDI	0
044H 074H 0A4H 0D4H	RnFFE	0	1	TAnFE	TBnFE	TnLOS	TnLOC	TnDAIS

Alarms, Interrupt Masks and Interrupt Indications

A Side and B Side Alarms and Interrupts

Latched Alarm Address	Alarm Name	Interrupt Mask or (016H or 021H)	Additional Interrupt Mask (if any)	Interrupt Indication Bit (020H)
022H	ADLOC	ASMSK		ASIDE
	AALOC			
	ADPAR			
	0			
	0			
	A3UAISI			
	A2UAISI			
	A1UAISI			
024H	LEXTC	ECKMSK		EXTCK
	0			
	0			
	0			
	0			
	A3DH4E	ASMSK		ASIDE
	A2DH4E			
	A1DH4E			
026H	BDLOC	BSMSK	-	BSIDE
	BALOC			
	BDPAR			
	0			
	0			
	B3UAISI			
	B2UAISI			
	B1UAISI			
028H	SPTLOC	SPTMSK	-	(Note 1)
	WDTEXP			
	0			
	PERR			
	0			
	B3DH4E	BSMSK	-	BSIDE
	B2DH4E			
	B1DH4E			

Note 1. The SPOT alarm does not have an interrupt indication bit but it can still cause both software interrupt (INT bit) and hardware interrupt (INT/$\overline{IRQ}$ lead).

A Side and B Side Port n Alarms and Interrupts

Latched Alarm Address	Alarm Name	Interrupt Mask (021H)	Additional Interrupt Mask (if any) (017H)	Interrupt Indication Bit (020H)	Latched Alarm Address	Alarm Name	Interrupt Mask (021H)	Additional Interrupt Mask (if any) (017H)	Interrupt Indication Bit (020H)
030 port 1 060 port 2 090 port 3 0C0 port 4	AnAIS	PnMSK	RPTnA	PORTn	03A port 1 06A port 2 09A port 3 0CA port 4	BnAIS	PnMSK	RPTnB	PORTn
	AnLOP					BnLOP			
	AnSIZE					BnSIZE			
	AnNDF					BnNDF			
	AnRDIS					BnRDIS			
	AnRFI		RFIE (Note 1)			BnRFI		RFIE (Note 1)	
	AnUNEQ		RPTnA			BnUNEQ		RPTnB	
	AnSLER					BnSLER			
04E port 1 07E port 2 0AE port 3 0DE port 4	AnRDIP				05E port 1 08E port 2 0BE port 3 0EE port 4	BnRDIP			
	AnRDIC					BnRDIC			
	0					0			
	0					0			
	AnJ2LOL					BnJ2LOL			
	AnJ2TIM					BnJ2TIM			
	0					0			
	0					0			
05A port 1 08A port 2 0BA port 3 0EA port 4	AnTCUQ				05C port 1 08C port 2 0BC port 3 0EC port 4	BnTCUQ			
	AnTCAIS					BnTCAIS			
	AnTCLM					BnTCLM			
	AnTCLL					BnTCLL			
	AnTCTM					BnTCTM			
	AnTCODI					BnTCODI			
	AnTCRDI					BnTCRDI			
	0					0			

Note 1. RFIE (address 012H, bit 3) is a common control bit for all four ports. A 1 enables the RFI indication to cause an interrupt. RPTnA or RPTnB is not required to be set to 1 to enable the interrupt for the RFI indication. A 0 disables an RFI indication from causing an interrupt.

Common Port n Alarms and Interrupts

Latched Alarm Address	Alarm Name	Interrupt Mask (021H)	Additional Interrupt Mask (if any) (018H or 019H)	Interrupt Indication Bit (020H)
044 port 1 074 port 2 0A4 port 3 0D4 port 4	RnFFE	PnMSK	RFIFOn	PORTn
	0			
	1			
	TAnFE		TFIFOnA	
	TBnFE		TFIFOnB	
	TnLOS		TPORTn	
	TnLOC			
	TnDAIS			

Interrupt and Alarm Control Bit Summary

IPOS 012H: 5	INEG 012H: 4	HWDIE 014H: 0	LATEN 011H: 4	Interrupt Mask Bit	Action on an Alarm
0	0	0	1	X	No alarm event indication, or interrupt register indication.
X	X	X	0	0	Alarm event register sets on positive levels of an alarm; no software or hardware interrupt indications.
X	X	0	0	1	Alarm event register sets, and software interrupt indication occurs, on positive levels of the alarm; no hardware interrupt.
X	X	1	0	1	Alarm event register sets, and software and hardware interrupt indications occur, on positive levels of the alarm.
1	0	X	1	0	Alarm event register sets on positive transitions of the alarm; no software or hardware interrupt indications.
1	0	0	1	1	Alarm event register sets, and software interrupt indication occurs, on positive transitions of the alarm; no hardware interrupt.
1	0	1	1	1	Alarm event register sets, and software and hardware interrupt indications occur, on positive transitions of the alarm.
0	1	X	1	0	Alarm event register sets on negative transitions of the alarm; no software or hardware interrupt indications.
0	1	0	1	1	Alarm event register sets, and software interrupt indication occurs, on negative transitions of the alarm; no hardware interrupt.
0	1	1	1	1	Alarm event register sets, and software and hardware interrupt indications occur, on negative transitions of the alarm.
1	1	X	1	0	Alarm event register sets on positive and/or negative transitions of the alarm; no software or hardware interrupt indications.
1	1	0	1	1	Alarm event register sets, and software interrupt indication occurs, on positive and/or negative transitions of the alarm; no hardware interrupt.
1	1	1	1	1	Alarm event register sets, and software and hardware interrupt indications occur, on positive and/or negative transitions of alarm.

SDH/SONET AIS DETECTION

The Quad E1 Mapper can detect an upstream AIS condition using the TOH H1/H2 (pointer) bytes or the TOH E1 (order wire) byte. When control bit SE1AIS (address 014H, bit 3) is 0, the H1/H2 bytes are monitored for an upstream AIS condition. When the MOD control bits (address 010H, bits 7 and 6) select the VC-4/TUG-3 format, the H11 and H21 bytes only are monitored for AIS. The monitoring of AIS in the two other H1n/H2n bytes is disabled. When the MOD control bits select the STS-3 or AU-3 format, each set of the three H1/H2 bytes per A Drop and B Drop buses are monitored for an AIS indication. Each of the three H1/H2 pointer bytes corresponds to the like-numbered AU-3/STS-1 signal (n=1-3). When the MOD control bits select the STS-1 format, the H1/H2 bytes per A Drop and B Drop buses are monitored for an AIS indication.

If all ones are detected in the H1/H2 bytes (whose location is determined by the C1 pulse) for three consecutive frames, the alarm bits AsUAISI in addresses 022H and 023H (A bus detected H1/H2 or E1 byte upstream AIS) or BsUAISI in addresses 026H and 027H (B bus detected H1/H2 or E1 byte upstream AIS) will set. Recovery occurs when a normal NDF (bits 1 through 4) in H1 is detected for three consecutive frames. A normal NDF is defined as a 0110, but 1110, 0010, 0100 and 0111 are also recognized as normal. The H1/H2 byte AIS detection circuits (when selected) for both the A and B Drop buses are disabled by writing a 0 to control bit HEAISE (address 013H, bit 7).

When control bit SE1AIS is 1, the E1n bytes are monitored for an upstream AIS condition. When the MOD control bits select the VC-4/TUG-3 format, the E11 byte in both buses is monitored for AIS. The detection of the upstream AIS indication in the E12 and E13 bytes is disabled. When the MOD control bits select the AU-3/STS-3 format, each of the three E1n bytes in the A and B Drop buses are monitored for AIS. Each of the three E1n bytes corresponds to the like-numbered AU-3/STS-1 signal. For STS-1 operation, the single E1 byte is checked for the upstream AIS indication.

Majority logic is used to determine if an E1n byte is carrying an upstream AIS indication. If 5 or more ones (at least 5 bits equal to 1 out of the 8 bits) are detected once in a A/B Drop bus E1n byte (whose locations are determined by the C1 pulse), the alarm bit AsUAISI (A bus detected H1/H2 or E1 Byte AIS) or BsUAISI (B bus detected H1/H2 or E1 Byte AIS) is set. Recovery occurs when 4 or more zeros (at least 4 bits equal to 0 out of the 8 bits) are detected once. The E1n byte AIS detection circuits (when selected) for both the A and B Drop buses are disabled by writing a 0 to control bit HEAISE.

TU/VT POINTER TRACKING

The starting location of the V1 byte is determined by either the V1 pulses in the A/BC1J1V1 signals or the H4 multiframe detection circuits. The TU/VT pointer bit assignment for the V1 and V2 bytes is shown below. The alignment is necessary to determine the starting locations of the V5 byte and the other bytes that are carrying the 2048 kbit/s format.

	V1 Byte							V2 Byte							
1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
N	N	N	N	SS-bits		I	D	I	D	I	D	I	D	I	D

I = Increment Bit
D = Decrement Bit
N = New Data Flag Bit
(enabled = 1001 or 0001/1101/1011/1000, normal or disabled = 0110 or 1110/0010/0100/0111)
Negative Justification: Inverted 5 D-bits and accept majority rule
Positive Justification: Inverted 5 I-bits and accept majority rule
SS-bits (VT Size) = 10 for 2048 kbit/s

Pointer Bytes Bit Assignment

The pointer value is a binary number with a range of 0 to 139 for the 2048 kbit/s format. The pointer offset indicates the offset from the V2 byte to the first byte in the TU-12/VT2 mapping. The pointer bytes are not counted in the offset calculation. The pointer offset arrangement for this format is shown below.

2048 kbit/s TU-12/VT2

V1
105
106-138
139
V2
0
1-33
34
V3
35
36-68
69
V4
70
71-103
104

TU/VT Pointer Offset Locations

Eight independent pointer-tracking state machines are used in the Quad E1 Mapper, one for each of the A and B buses in each of the four ports 1, 2, 3, and 4. The pointer tracking algorithm is illustrated in 19. The pointer tracking state machine is based on the pointer tracking machine found in the latest ETSI requirements, and is also valid for both Bellcore and ANSI. When control bit PTALTE at address 014H, bit 1 is 0, the transition from AIS to LOP is disabled (shown dotted), which is required in Bellcore recommendations.

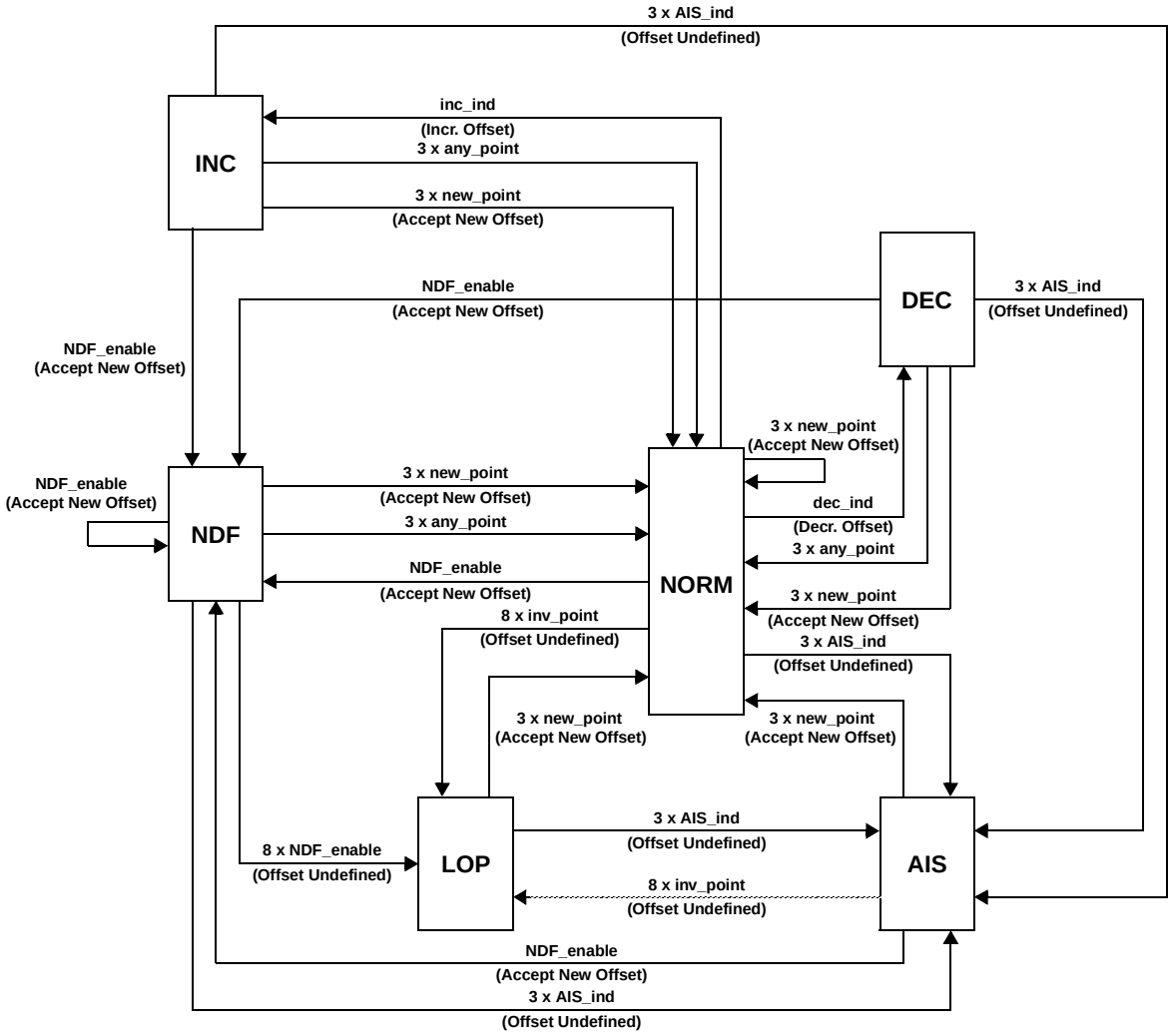


Figure 19. TU/VT Pointer Tracking State Machine

REMOTE DEFECT INDICATIONS

A 1-Bit/3-Bit RDI Selection bit - 1BnRDI (bit 4 in registers 048H, 078H, 0A8H, 0D8H) - has been added to allow the user to select between the Enhanced 3-Bit RDI (1BnRDI = 0) or Single Bit RDI (1BnRDI = 1). The following sections describe the differences.

V5 and K4 (Z7) Byte Coding (for 3-Bit RDI)

Bits 5, 6 and 7 in the K4 (Z7) byte, in conjunction with bit 8 in the V5 byte, provide a detection scheme which is compliant with earlier versions of the RDI standard and also with enhanced TU/VT RDI capability. The enhanced version of RDI allows the user to differentiate between server, connectivity, and payload defects. Bit 8 in V5 is set equal to bit 5 in K4 (Z7). Bit 7 in K4 (Z7) is set to the inverse of bit 6 of K4 (Z7) to distinguish the enhanced version of RDI from the old version of RDI. It should be noted that when bits 6 and 7 in K4 (Z7) are either 01 or 10, the RDI indication is also influenced by Bit 8 of V5, as shown in the table below. When bits 6 and 7 are either 00 or 11, then RDI is determined solely by bit 8 in V5. This allows detection of an RDI originating from older equipment that generates the RDI in the V5 byte. The following table lists the RDI defect indications carried in the V5 and K4 (Z7) bytes.

Bit 8 V5 Bit 5 K4 (Z7)	Bit 6 K4 (Z7)	Bit 7 K4 (Z7)	Definition
0	0	0	No defect indications.
0	0	1	No defect indications.
0	1	0	Remote Payload Defect - Path Label Mismatch - Loss of Multiframe.
0	1	1	No defect indications.
1	0	0	Remote defect (old equipment).
1	0	1	Remote Server Defect - VT Loss of Pointer - VT AIS detected - Upstream AIS detected (E1 or H1/H2 Bytes).
1	1	0	Remote Connectivity Defect - Unequipped Signal Label - J2 Mismatch - J2 Loss of Lock
1	1	1	Remote defect (old equipment).

RDI Bit Assignment for 3-Bit RDI

Receive RDI Detection and Recovery (for 3-Bit RDI)

The RDI alarms are defined in the table below. The number of consecutive events for detection and recovery is controlled by control bit V5AL10 in address 014H, bit 2. The value of five is selected when the V5AL10 control bit is 0, and the value of ten is selected when the V5AL10 control bit is 1.

AnRDIC BnRDIC	AnRDIP BnRDIP	AnRDIS BnRDIS	Action
0	0	1	Remote Server Defect Indication, and old equipment RDI indication (Bit 8 in the V5 byte).
0	1	0	Remote Payload Defect Indication.
1	0	0	Remote Connectivity Indication.

RDI Alarm Definition for 3-Bit RDI

Transmit RDI Generation (for 3-Bit RDI)

An RDI is sent for the following unlatched alarm conditions in the V5 and K4 (Z7) overhead bytes of the VT added to the A or B Add bus, depending on the states of the RnSEL (active bus selected), TnSEL1 and TnSEL0 (bus enabled) control bits. The following examples apply to port 1, but corresponding examples for ports 2 through 4 may be constructed by substituting the port number digit for the 1-digit in the bit symbols (except DV1SEL). The variable s refers to the STS-1 or AU-3/TUG-3 identifier (s = 1 - 3).

- When RDI enable (RDIEN) is 1, a Remote Server Defect Indication is sent for:
    - VT Loss of Pointer (A1LOP, B1LOP)
    - VT AIS (A1AIS, B1AIS)
    - A/B Drop Bus Upstream AIS in H1/H2 or the E1 byte (AsUAISI, BsUAISI), when HEAISE is 1
    - Microprocessor writes a 1 to T1RDIS

- When RDI enable (RDIEN) is 1, a Remote Payload Defect Indication is sent for:
    - A/B Drop H4 Error (AsDH4E, BsDH4E), when DV1SEL is 0
    - Mismatch signal label (A1SLER, B1SLER)
    - Microprocessor writes a 1 to T1RDIP

- When RDI enable (RDIEN) is 1, a Remote Connectivity Defect Indication is sent for:
    - Unequipped signal label (A1UNEQ, B1UNEQ), when UQAE is 1
    - J2 Mismatch (A1J2TIM, B1J2TIM), when J21AISE is 1
    - J2 Loss of Lock (A1J2LOL, B1J2LOL), when J21AISE is a 1
    - Microprocessor writes a 1 to T1RDIC

- When RDI enable (RDIEN) is 0, the microprocessor can control RDI generation:
    - Microprocessor writes a 1 to T1RDIS to generate remote server defect indication.
    - Microprocessor writes a 1 to T1RDIP to generate remote payload defect indication.
    - Microprocessor writes a 1 to T1RDIC to generate remote connectivity defect indication.

Note: The microprocessor may send an RDI by writing to the above control bits at any time, including the add-only mode. To prevent contention between the internal logic and full microprocessor control, the RDIEN control bit should be written with a 0 when microprocessor control is intended. The priority used for sending RDI if more than one of the microprocessor controls are set is: Server, Connectivity, and Payload. When RDIEN = 1 and no defects are generated then K4 bits 5,6,7 = 001.

V5 and K4 (Z7) Byte Coding (for 1-Bit RDI)

In the Receive (Rx) direction bit 8 in the V5 byte is used to detect Remote Defect Indications. Bits 5, 6, and 7 in the Rx K4(Z7) byte are not looked at for detecting RDI and can have any incoming value, 0 or 1.

For transmitting 1-Bit RDI, bit 8 in V5 byte will be set as shown below and bits 5,6,7 in the K4(Z7) byte will be sent as 0. See table below:

Bit 8 V5	Bit 5 K4 (Z7)	Bit 6 K4 (Z7)	Bit 7 K4 (Z7)	Definition
0	0	0	0	No defect indications.
1	0	0	0	Remote Defect Indication.

RDI Bit Assignment for 1-Bit RDI

Receive RDI Detection and Recovery (for 1-Bit RDI)

The RDI alarm is defined in the table below. The number of consecutive events for detection and recovery is controlled by a Common Register - Provisioning Control bit V5AL10 (register 014H, bit 2). When V5AL10 = 0, the value is 5; when V5AL10 = 1, the value is 10. A Remote Defect Indication is indicated by alarm indication bit AnRDIS/BnRDIS. Alarm indication bits AnRDIP/BnRDIP and AnRDIC/BnRDIC are disabled and will always be equal to zero when 1-Bit RDI mode is selected.

AnRDIC BnRDIC	AnRDIP BnRDIP	AnRDIS BnRDIS	Action
0	0	0	No defect indications.
0	0	1	Remote Defect Indication.

RDI Alarm Definition for 1-Bit RDI

Transmit RDI Generation (for 1-Bit RDI)

An RDI is sent for the following unlatched alarm conditions in the V5 overhead byte of the VT added to the A or B Add bus, depending on the states of the RnSEL (active bus selected), TnSEL1 and TnSEL0 (bus enabled) control bits. The following examples apply to port 1, but corresponding examples for ports 2 through 4 may be constructed by substituting the port number digit for the 1-digit in the bit symbols (except DV1SEL). The variable s refers to the STS-1 or AU-3/TUG-3 identifier (s = 1 - 3).

- When RDI enable (RDIEN) is 1, a remote defect indication (bit 8 in V5=1; bits 5,6,7 in K4(Z7)=0) is sent for:
  - VT Loss of Pointer (AnLOP, BnLOP)
  - VT AIS (AnAIS, BnAIS)
  - A/B Drop Bus Upstream AIS in H1/H2 or the E1 byte (AsUAISI, BsUAISI), when HEAISE is 1.
  - Unequipped Signal Label (AnUNEQ, BnUNEQ), when UQAE is 1.
  - J2 Loss of Lock (A1J2LOL, B1J2LOL), when J21AISE is a 1.
  - J2 Mismatch (A1J2TIM, B1J2TIM), when J21AISE is 1
  - Microprocessor writes a 1 to T1RDIS to generate a Remote Defect Indication.

- When RDI enable (RDIEN) is 0, the microprocessor can control RDI generation:
    - Microprocessor writes a 1 to T1RDIS to generate Remote Defect Indication.

Note: For 1-Bit RDI mode the following unlatched alarm conditions will not generate a Remote Defect Indication:

- A drop H4 error (AsDH4E, BsDH4E), when DV1SEL is a 0.
- Mismatch signal label (AnSLER, BnSLER).

Note: For 1-Bit RDI mode the following microprocessor control bits are disabled and will not generate a Remote Defect Indication:

- Microprocessor writes a 1 to TnRDIP.
- Microprocessor writes a 1 to TnRDIC.

OVERHEAD COMMUNICATIONS BIT ACCESS

Microprocessor access is provided for the eight overhead communications bits (O-bits) carried in the two justification control (JC) bytes in the multiframe format, e.g., in a 2048 kbit/s TU/VT, shown partially below. The bits in the justification control byte are numbered 1 through 8, starting with C1 as bit 1.

	Other Bytes							
	J2 Byte							
JC Byte 1	C1	C2	O	O	O	O	R	R
	32 Bytes - Information							
	R	R	R	R	R	R	R	R
	N2 (Z6) Byte							
JC Byte 2	C1	C2	O	O	O	O	R	R
	Other Bytes							

O-bit Placement in a 2048 kbit/s TU/VT

In the receive direction, the eight O-bits are stored in eight 8-bit registers (A and B for each group of 4 ports) and these registers are updated each frame. The two O-bit nibbles that form a byte in the registers for receiving and transmitting are from the same multiframe. Bits 3 through 0 in an O-bit register correspond to bits 3 through 6 (C1C2 OOOO RR) in the first justification control byte, and bits 7 through 4 in an O-bit register correspond to bits 3 through 6 in the second justification control byte, as shown below.

	Second Justification Control Byte				First Justification Control Byte			
Bit	3	4	5	6	3	4	5	6
Register	7	6	5	4	3	2	1	0

O-bit Assignment Memory Map

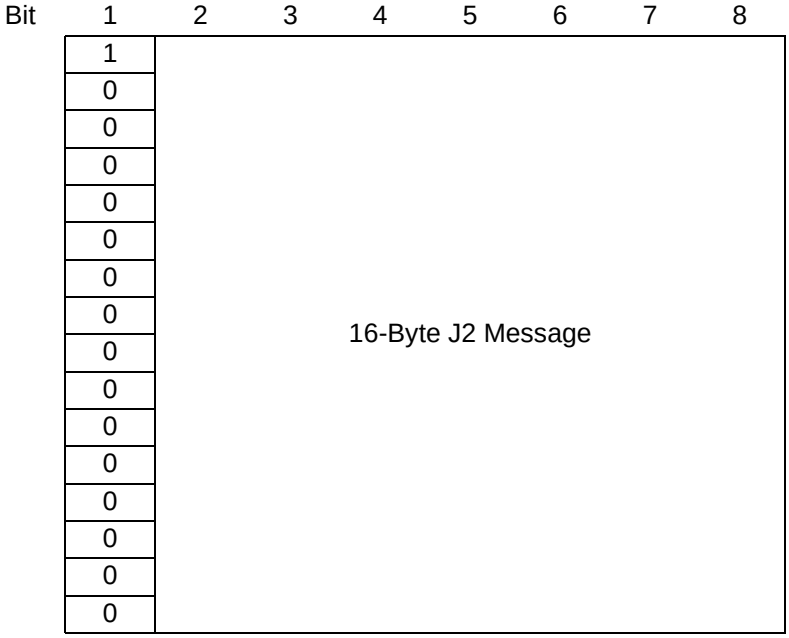
Receive J2 Byte Processing

There are two possible received J2 message sizes, 16 bytes (ITU-T), or 64 bytes (ANSI). The QE1M is capable of dimensioning the transmit (and receive) RAM memory segment to the two sizes (16-Byte or 64-Byte). In addition, two modes of operation are provided for the 16-byte (ITU-T) format: a microprocessor read mode, and a compare read mode. The following table lists the various control states associated with J2 processing.

J2nSIZE	J2nCOM	Action
0	0	Transmit and receive J2 segments are configured for the 16-byte J2 message size. Microprocessor read for the dropped J2 message. J2 alarms are disabled.
0	1	Transmit and receive J2 segments are configured for the 16-byte J2 message size. For receiving, a 16-byte microprocessor message is written into a 16-byte segment for comparison against the received message. The written message must start with the multiframe indicator written into the starting location of the segment.
1	X	Transmit and receive J2 segments are configured for the 64-byte J2 message size. Microprocessor read for the dropped J2 message. J2 alarms are disabled. The tandem connection feature must be disabled by setting TCnEN=0 for the port.

Note: X = Don't Care

The ITU-T defined 16-byte message consists of an alignment signal of (10000000 00000000) in the most significant bit (bit 1) of the message. The remaining 7 bits in each byte carry a data message, as illustrated below.



ITU-T 16-Byte J2 Message Format

The definitions (ITU-T) shown below will be used in the following discussion of the J2 16-byte message comparison function. The memory locations apply to each memory group.

ITU-T Definitions	E1Mx16 Definitions
RxTI - Received TTI (Trail Trace Identifier)	Incoming J2 trace message (Real Time)
ExTI - Expected TTI (Trail Trace Identifier)	Microprocessor-written trace (reference) message. A Side (X50H - X5FH) B Side (XD0H - XDFH)
AcTI - Accepted TTI (Trail Trace Identifier)	Received stable trace message. A Side (X40H - X4FH) B Side (XC0H - XCFH)

The J2 16-byte message comparison works according to the following steps:

1. The microprocessor-written reference message (ExTI) locations should be initialized with the correct J2 16-byte message before enabling the J2 message comparison function.
2. The J2 message comparison function is then enabled (J2nCOM = 1; J2nSIZE = 0) and immediately the J2 Loss of Lock alarm will be active (J2nLOL = 1) and the J2 Trace Identifier Mismatch alarm will be inactive (J2nTIM = 0). This is the first step in the sequence - to initialize these alarms.
3. The incoming trace message (RxTI) is received, and the J2 comparison circuit searches for the J2 alignment pattern (Bit 1: 1000...0 pattern).
4. J2 alignment pattern is found and the Received stable trace message (AcTI) locations are updated with this incoming trace message (RxTI).
5. The incoming trace message (RxTI) is then checked for three consecutive 16-byte message repeats.
6. If an error occurs before step 5 is completed, the sequence repeats, starting at step 3 (searching for the alignment pattern).
7. If the incoming trace message (RxTI) repeats three times in a row (after the alignment pattern is detected) without an error then this is an in-lock condition, and the J2 Loss of Lock alarm is reset (J2nLOL = 0). Note that at this time the J2 mismatch alarm is still inactive (J2nTIM =0).
8. Once the incoming trace message is in-lock, the stable message (AcTI), is compared against the microprocessor-written reference message (ExTI), byte for byte, for 16 bytes (the length of the multiframe message). If they compare (AcTI = ExTI), a match is declared, with no mismatch alarm (J2nTIM = 0). If they do not compare (AcTI ≠ ExTI), a mismatch alarm is declared (J2nTIM = 1). A J2 mismatch alarm results in RDI and receive line AIS being sent continuously, when enabled. There is no Loss of Lock alarm (J2nLOL = 0) because the incoming trace message (RxTI) is stable.
10. If the incoming message (RxTI) changes for three consecutive 16-byte messages, a loss of lock alarm (J2nLOL = 1) occurs and the sequence starts again from the beginning (step 2).

Summary of J2 Alarms:

- J2 Loss of Lock (J2nLOL) is a comparison between the Received stable message (AcTI) and the Receive incoming (real time) message (RxTI).
- Declare Lock (J2nLOL = 0) when AcTI = RxTI for 3 consecutive set of 16 bytes.
- Loss of Lock (J2nLOL = 1) when AcTI ≠ RxTI on at least 1 byte in each of 3 consecutive 16-byte messages
- J2 Trace Identifier Mismatch (J2nTIM) is a comparison between the Received stable message (AcTI) and the microprocessor-written reference message (ExTI).
- Declare Mismatch (J2nTIM = 1) when AcTI ≠ ExTI on any byte once lock is declared.

- Clear Mismatch (J2nTIM = 0) when AcTI = ExTI. See Note below.

Note: A mismatch alarm is declared for the following reasons.

1. A valid mismatch alarm would be declared when the stable message (AcTI) does not match the reference message (ExTI).
2. An invalid mismatch alarm would be declared if the correct start-up procedure was not used and the reference message (ExTI) was not loaded before enabling the J2 comparison function.
3. Another reason for getting an invalid mismatch alarm would be if the reference message was written with the wrong message value.

In any case if the incoming message is stable (or In-Lock - J2nLOL = 0) then the only way to clear the mismatch alarm would be to cause a Loss of Lock condition.

Suggested J2 16-byte Message Comparison Start-up Procedure:

From Start-up:

1) At transmitting device - Send a “valid” message (TxTI).

2) At receive device - a) Load microprocessor-written reference message (ExTI) with a “valid” message.
b) Enable J2 Message Comparison.

Note: 1 and 2 are interchangeable

If Changing Messages:

1) At receive device - Load microprocessor-written reference message (ExTI) with a “new valid” message.

2) At transmitting device - Send a “new valid” message (TxTI).

Note: If 1 is not done before 2 then a mismatch alarm is declared. If this occurs it is not a valid mismatch (assuming that the messages are correct).

Following the start-up procedure above will assure that the Trace Identifier Mismatch alarm only activates when the messages do not match. There is the possibility that a mismatch alarm will activate by not following the correct start-up procedure, upon which the following should be done:

1) At Receive device - verify that microprocessor-written (reference) message (ExTI) is correct

2) At Receive device - verify that the stable message (AcTI) is correct by examining J2nLOL. Since AcTI is written only once at the beginning of the algorithm, when searching for the J2 alignment pattern, if no Loss of Lock alarm is set then the incoming message RxTI is still the same valid message in AcTI. Now force a Loss of Lock condition by using the microprocessor to overwrite any byte of the stable message (AcTI) with a value that corrupts the alignment pattern (i.e., address X40=0x00). The Loss of Lock alarm will set, and then the re-start the algorithm from the beginning, which resets the mismatch alarm, and starts searching again for the alignment pattern.

N2 (Z6) Overhead Byte (Tandem Connection)

The Tandem Connection feature is enabled for a TU/VT by writing a 1 to control bit TCnEN, when control bit J2nSIZE is a 0. When control bit TCnEN is written with a 0, the tandem connection feature is disabled. See address 051H, bit 4, in the Memory Map Descriptions section for more detail on TCnEN. The bit placement in a received N2 (Z6) byte is as shown below:

Bit	1	2	3	4	5	6	7	8
	BIP-2		1	AIS Indication	TC REI	TC OEI (FEBE)	Trace ID TC RDI/ODI	

BIP-2, AIS INDICATION, TC REI AND TC OEI PROCESSING

One or two errors may be detected in the TC BIP-2 comparison, and they are counted individually in an 8-bit counter when control bit BLOCK is written with a 0 (An TC BIP-2 Error Counter, Bn TC BIP-2 Error Counter). When control bit BLOCK is written with a 1, one or two parity errors are counted as a single block error.

A tandem connection AIS alarm (AnTCAIS, BnTCAIS) is declared when bit 4 is equal to 1 for five consecutive frames. Recovery occurs when bit 4 is equal to 0 for five consecutive frames.

An 8-bit counter (An TC REI Counter, Bn TC REI Counter) is provided for counting the number of REI bits received as equal to 1 in bit 5 (TC REI) in the N2 (Z6) byte. A REI indication (a 1) indicates that the distant end has detected one or two errors when the BIP-2 calculated for frame f-1 (all the bytes) is compared against the BIP-2 value carried in the N2 (Z6) byte in frame f.

An 8-bit counter (An TC OEI Counter, Bn TC OEI Counter) is provided for counting the number of OEI bits received as equal to 1 in bit 6 (TC OEI) in the N2 (Z6) byte. An OEI indication (a 1) indicates that the distant end has detected one or two errors when the BIP-2 calculated for frame f-1 is compared against the BIP-2 value carried in the V5 byte in frame f.

Bits 7 and 8

A multiframe alignment pattern, trace identifier message, TC RDI and TC ODI indications are assigned to bits 7 and 8 in the frames of a 76-frame structure, as shown below:

Frame No.	N2 (Z6) Byte Definition
1 - 8	Frame Alignment, 1111 1111 1111 1110
9 - 12	TC Trace ID Byte No. 0 (1 C1 C2 C3 C4 C5 C6 C7)
13 - 16	TC Trace ID Byte No. 1 (0 X X X X X X X)
17 - 20	TC Trace ID Byte No. 2 (0 X X X X X X X)
21 - 24 thru 61 - 64	TC Trace ID Bytes No. 3 thru 13
65 - 68	TC Trace ID Byte No. 14 (0 X X X X X X X)
69 - 72	TC Trace ID Byte No. 15 (0 X X X X X X X)
73	Bit 7 = 0, Bit 8 = TC RDI
74	Bit 7 = TC ODI, Bit 8 = 0
75	Bit 7 = 0, Bit 8 = 0
76	Bit 7 = 0, Bit 8 = 0

Loss of multiframe (status bits AnTCLM, BnTCLM) occurs when four consecutive Frame Alignment Signals (1111 1111 1111 1110) are detected in error (i.e., one or more error in each FAS). Multiframe alignment is recovered when three consecutive non-errored FAS are found.

The TC trace identifier message comparison is based on the same state machine as that used for the 16-byte J2 message. If the message is not locked, an AnTCLL or BnTCLL alarm is declared. After TC lock is established, a comparison is performed between the microprocessor-written TC and the contents of the incoming message. The message consists of TC Trace ID bytes 0 to 15. A TC Trace Identifier Mismatch (AnTCTM, BnTCTM) alarm is declared when any byte does not match. Recovery occurs when there is a match between the microprocessor message and the accepted message.

Bit 8 in frame 73 is defined as a Tandem Connection Remote Defect Indication (TC RDI). A TC RDI alarm occurs when a 1 has been detected in bit 8 in frame 73 for 5 consecutive multiframes (where each multiframe is 38 ms). The TC RDI alarm state is exited when bit 8 is equal to 0 for 5 consecutive multiframes. An alarm indication is reported as AnTCRDI or BnTCRDI.

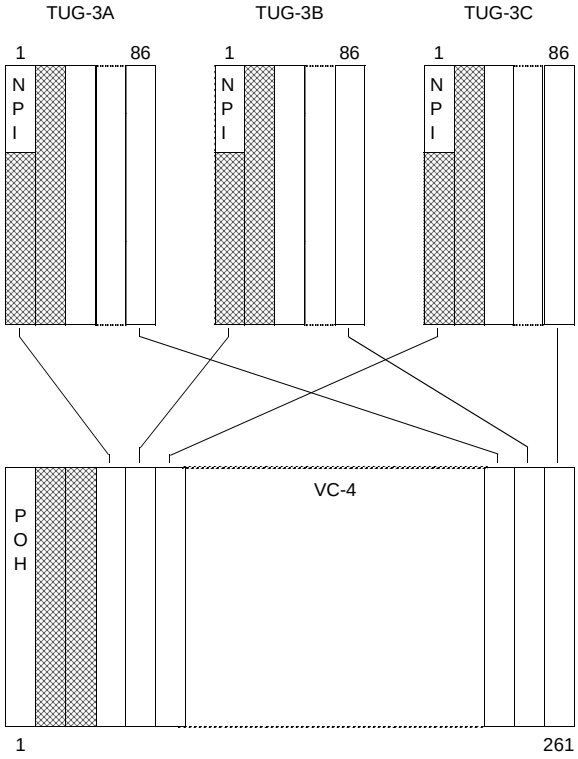
Bit 7 in frame 74 is defined as a Tandem Connection Outgoing Defect Indication (TC ODI). A TC ODI alarm occurs when a 1 has been detected in bit 7 in frame 74 for 5 consecutive multiframes (where each multiframe is 38 ms). The TC ODI alarm state is exited when bit 7 is equal to 0 for 5 consecutive multiframes. An alarm indication is reported as AnTCODI or BnTCODI.

Tandem Connection Unequipped Status

Unequipped Tandem Connection detection is provided. Five or more consecutive received tandem connection N2 (Z6) bytes equal to XX00 0000 result in a TC unequipped indication (AnTCUQ, BnTCUQ). The alarm state is exited when five or more consecutive received tandem connection N2 (Z6) bytes are not equal to XX00 0000. Note that bits 1 and 2 of the N2 (Z6) byte are masked (shown as X) and do not affect the indication.

TUG-3 NULL POINTER INDICATOR

For STM-1 TUG-3 format, the Quad E1 Mapper has the option to generate and transmit a Null Pointer Indicator (NPI) for one or more of the TUG-3s, as shown below.



NPI Structure

Three control bits (NPIA, NPIB and NPIC in address 010H, bits 2-0) are provided for selecting one or more of the TUG-3 NPIs. The three control bits are enabled when the MOD1 and MOD0 control bits are 11 (TUG-3/VC-4 format). The NPI consists of three bytes, starting with row 1. The table below shows the bit assignment for the first two bytes.

Bit	1	2	3	4	5	6	7	8
Row 1	1	0	0	1	0	0	1	1
Row 2	1	1	1	0	0	0	0	0

NPI Bit Assignment

The third NPI byte is designated as fixed stuff and is transmitted as zero. The remaining cross-hatched bytes in the first two columns of the TUG-3 are tristated on the add bus. When a 1 is written to control bit NULLZ in address 013H, bit 3 and the NPI feature is enabled (i.e., NPIA, NPIB or NPIC is a 1) the bytes following the NPI bytes are transmitted as zeros. When the NULLZ bit is a 0, the bytes following the NPI bytes are tristated.

E1 LOOPBACK CAPABILITY

The QE1M provides two types of E1 loopbacks, called facility and line loopbacks (i.e., at the facility side and at the line side, as illustrated in 20). In 20, the E1 Transmit Data and Clock goes into the QE1M, while the E1 Receive Data and Clock comes out of the QE1M. Facility loopback for port n, enabled when a 1 is written to control bit FnLBK, directs the incoming E1 Transmit Data and Clock to the outgoing Receive Data and Clock signal. Line loopback for port n, enabled when a 1 is written to control bit LnLBK, routes the outgoing E1 Receive Data and Clock signal (instead of the incoming E1 Transmit Data and Clock) to the SDH/SONET transmitter.

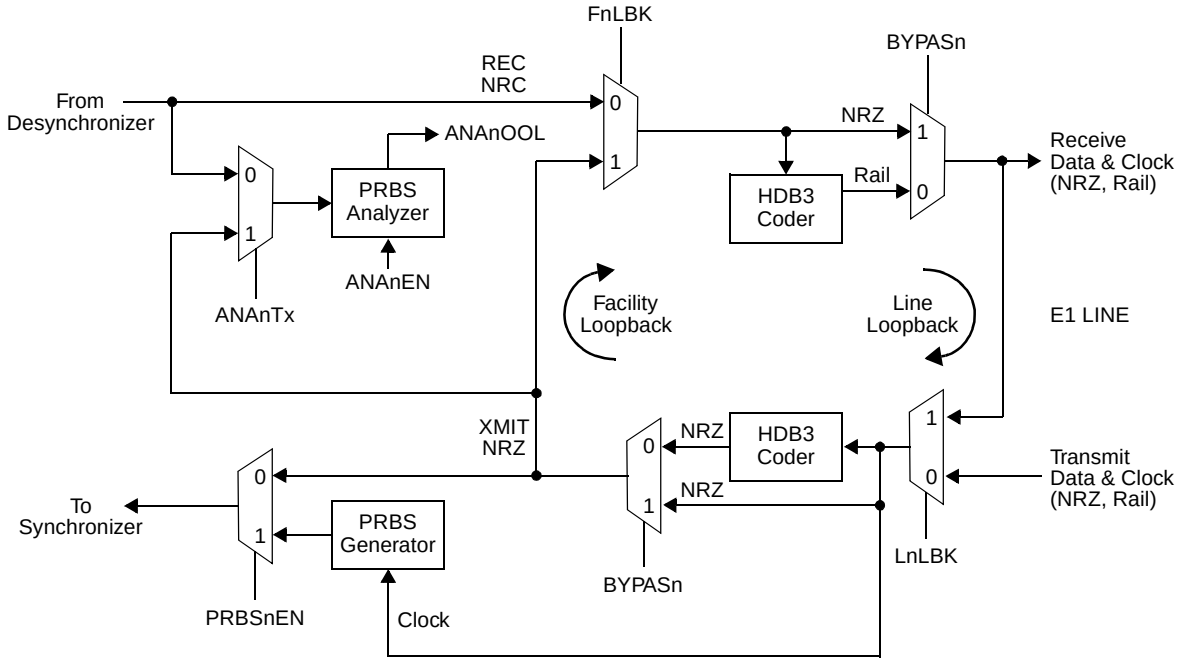


Figure 20. Facility and Line Loopbacks

PRBS PATTERN GENERATOR AND ANALYZER

Each port has a data generator and analyzer for 2^{15}-1 PRBS patterns, as illustrated in 20. The PRBS generator is enabled when a 1 is written to control bit PRBSnEN. The PRBS pattern will be synchronous to the clock driving the HDB3 decoder. When a 1 is written to ANAnEN control bit, the PRBS analyzer is enabled. When control bit ANAnTx is 0, the analyzer will sample the receive NRZ clock and data (REC NRZ) signals. When the control bit ANAnTx is 1, the internal transmit NRZ clock and data signals (XMIT NRZ) will be sampled by the analyzer.

RESETS

The Quad E1 Mapper has several reset options. These include a full hardware and software device reset, partial software resets, and counter software resets. All of the software reset bits are self-clearing (i.e., they do not require 0 to be written to a register location after the reset is applied by setting the bit to 1). Note that the self-clearing function requires the presence of the clock signal provided to the EXTCK lead (lead 138 or D10).

Upon power-up, when the RESET bit (address 015H, bit 7) is written with a 1, or an active low signal is placed on the $\overline{\text{RESET}}$ lead (lead 155 or C5), the add bus data and the port E1 interfaces are forced to a high impedance state until the device is initialized. The control bits AAHZE and BAHZE (address 010H, bits 5 and 4) must be written with zeros to enable the add bus interfaces. The RnEN control bits must be programmed to 1 to activate the line interfaces. In addition, the $\overline{\text{AAIND}}$, $\overline{\text{BAIND}}$, $\overline{\text{AADD}}$ and $\overline{\text{BADD}}$ leads are forced off. All performance counters are reset, and the alarms (except AnLOP and BnLOP) are reset. The control bits (except those shaded in the Memory Map) are also forced to zero, and the various FIFOs are re-initialized. The shaded bits are contained in the Data RAM, and these can be initialized by writing a 1 to INITSP (see Memory Map Descriptions, address 015H, bit 0). A hardware reset can only be applied after the clocks are stable, and must be present for a minimum duration of 150 ns.

Writing a 1 to the RnSETS software reset control bit for any of the ports resets the port n performance counters, re-initializes the FIFO, and clears the alarms, except the AnLOP and BnLOP alarms, which will set for port n. The loss of pointer alarms will recover when a valid pointer is received. The control bits will not be reset.

Writing a 1 to the RnSETC counter reset control bit for any of the ports reset the performance counters for that port. This feature allows the performance measurements to start at the same time for a port.

Writing a 1 to control bit RESTAB (address 015H, bit 6) resets the alarms for the A bus and for LEXTC (i.e., addresses 022H to 025H). Writing a 1 to control bit RESTBB (address 015H, bit 5) resets the alarms for the B bus and the SPOT alarms (i.e., addresses 026H to 028H).

Note that a hardware reset will automatically trigger all the software reset bits. Software reset bit RESET will trigger all RnSETS, all RnSETC, RESTAB and RESTBB automatically. A RnSETS will also automatically trigger a RnSETC.

START-UP PROCEDURE

The following procedure should be followed to start up the QE1M in a known good state from initial power-on, or from a hardware or software reset.

Initial power-on: (start from step 1)

From a hardware reset: (start from step 2)

From a software reset: (start from step 4)

(1) Power up Device

(2) Apply Hardware Reset (lead 155 or C5)

(3) Load SPOT microcode (see flowchart in Figure 26)

(4) Apply Software Reset (RESET=1; register 0x015 = 0x80)

(5) Initialize Data RAM (INITSP=1; register 0x015 = 0x01)

(6) Load all Control Registers for user specific operation

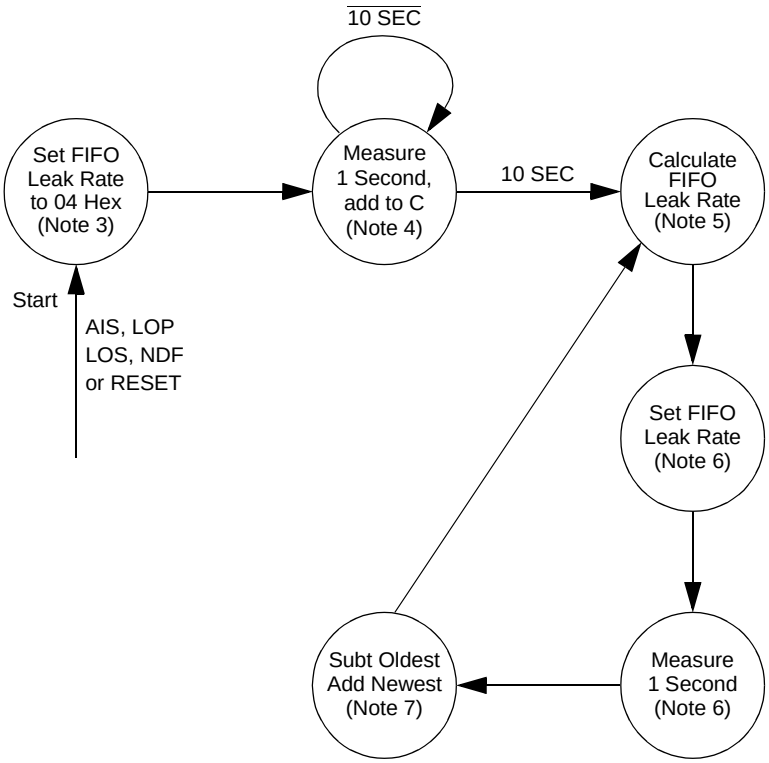
(7) Clear any alarms that may have been latched, by generating the following resets:

- RESTAB and RESTBB (register 0x015 = 0x60)
- R1SETS (register 0x052 = 0x80)
- R2SETS (register 0x082 = 0x80)
- R3SETS (register 0x0B2 = 0x80)
- R4SETS (register 0x0E2 = 0x80)

(8) Clear AnLOP and BnLOP by reading the corresponding Port Status Registers:

- Clear A1LOP (read register 0x030)
- Clear A2LOP (read register 0x060)
- Clear A3LOP (read register 0x090)
- Clear A4LOP (read register 0x0C0)
- Clear B1LOP (read register 0x03A)
- Clear B2LOP (read register 0x06A)
- Clear B3LOP (read register 0x09A)
- Clear B4LOP (read register 0x0CA)

POINTER LEAK RATE CALCULATIONS



Notes:

1. The procedure described in Notes 2 through 8 below must be performed independently for each of the four ports of the QE1M device.
2. The procedure shown in the diagram above uses a ten-second sliding window with a resolution of one second.
3. The initial FIFO Leak Rate Register value (in memory map address 049H, 079H, 0A9H or 0D9H) must first be set to 04 Hex.
4. Measure ten consecutive one-second samples from the Positive and Negative Stuff Counters being used. Store all ten difference values, i.e.,

   S1 = POS STUFF COUNT1 - NEG STUFF COUNT1,
   S2 = POS STUFF COUNT2 - NEG STUFF COUNT2, and so on through
   S10 = POS STUFF COUNT10 - NEG STUFF COUNT10.

   There are eight pairs of stuff counters in the QE1M; care should be taken to use the pair appropriate to the programmed configuration of the device. The counters are located at addresses 032H, 062H, 092H, 0C2H (A side) and 03CH, 06CH, 09CH, 0CCH (B side).
5. Calculate the leak rate (L.R.) using the following equation:

   L.R. = Hex[Int [280 / C]], where
   C = ABS [S1 + S2 + ... + S10].
   Then, if L.R. < 4, let L.R. = 4,
   or if L.R. > 255, let L.R. = 255.
6. Set the FIFO Leak Rate Register (address 049H, 079H, 0A9H or 0D9H) with the value between 4 and 255 calculated above, then take another one-second sample (e.g., S11).
7. Recalculate the value of 'C' by subtracting the oldest sample and adding the newest, and calculate a new leak rate, as described in Note 5 (e.g., using S2 through S11).
8. Continue to repeat the steps described in Notes 5, 6 and 7 until AIS, LOP, LOS or NDF is received or until you reset the QE1M.

JITTER MEASUREMENTS

Equipment used in QE1M jitter measurements:

- Hewlett-Packard Digital Transmission Analyzer:HP-3784A
- Anritsu Digital Transmission Analyzer:ME520B
- Anritsu STM/SONET Analyzer:MP1560A

The following table lists the filter characteristics defined by specification:

Specifications	Filter Characteristics		
G.703 Interface	f1 (High Pass)	f3 (High Pass)	f4 (Low Pass)
2048 kbit/s	20 Hz 20 dB/decade	18 kHz 20 dB/decade	100 kHz -20 dB/decade
Filter Used	HP1	HP2	LP

Jitter Tolerance Test

The jitter tolerance test is performed by inserting various jitter levels at selected frequencies into the 2.048 Mbit/s line input of the QE1M, as shown in the table below and Figure 21. Data is looped back at the SDH/SONET interface and dropped by the same QE1M device. The measured value is the maximum input jitter that the QE1M can tolerate at its input without generating bit errors in the loopback path. Figure 22 is a plot of the measured data listed in the table.

Input Jitter Frequency	Requirement	Maximum Input Jitter Tolerated (UI-PP)
10 Hz	>1.5 UI	10 UI
2.4 kHz	> 1.5 UI	2.3 UI
18 kHz	> 0.2 UI	2.2 UI
100 kHz	> 0.2 UI	1.0 UI

Figure 21. Jitter Tolerance and Jitter Test Arrangements

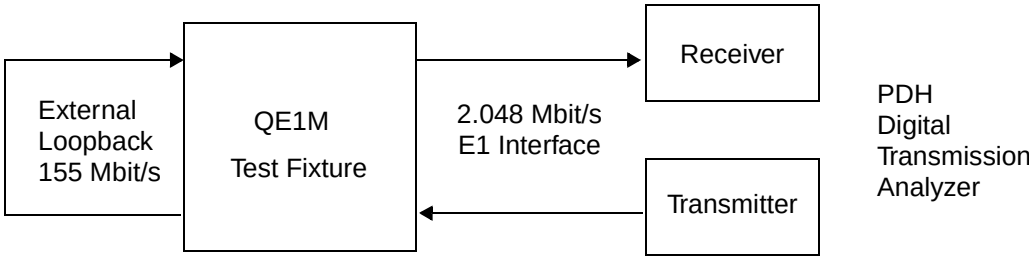
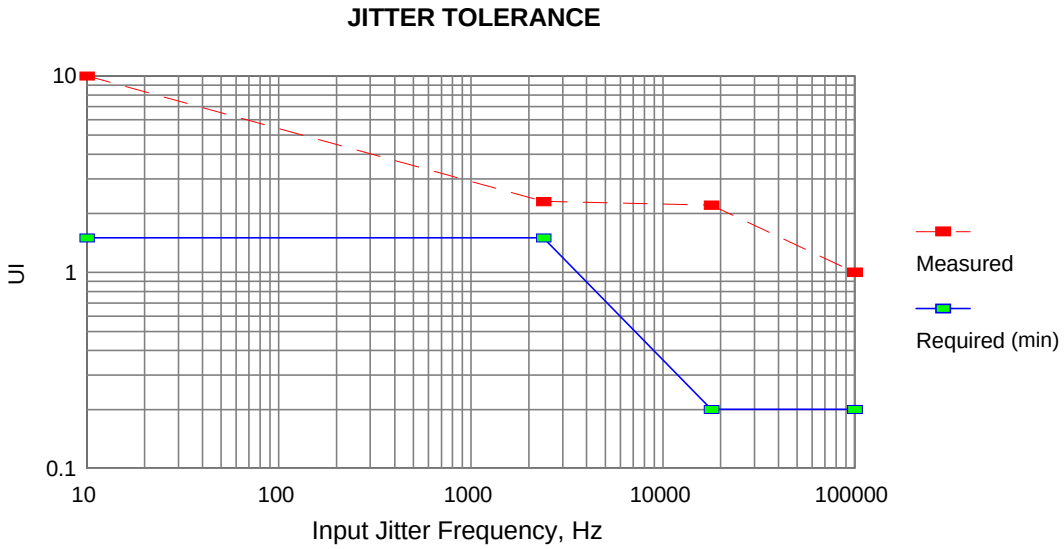


Figure 22. Jitter Tolerance Measurements



Jitter Transfer Test

A fixed jitter level of 0.5 UI is inserted into the transmitted E1 signal. The jitter value measured is achieved using the HP1/LP filter in the PDH receiver. The jitter transfer measurements are provided in the following table and Figure 23.

Input Jitter		Filter Used	Jitter Transfer (UI - PP, max)
Frequency	Unit Interval		
10 Hz	1.0 UI	f1-f4 (HP1/LP)	0.172 UI
50 Hz	1.0 UI		0.127 UI
100 Hz	1.0 UI		0.117 UI
200 Hz	1.0 UI		0.099 UI
600 Hz	1.0 UI		0.076 UI
1000 Hz	1.0 UI		0.075 UI

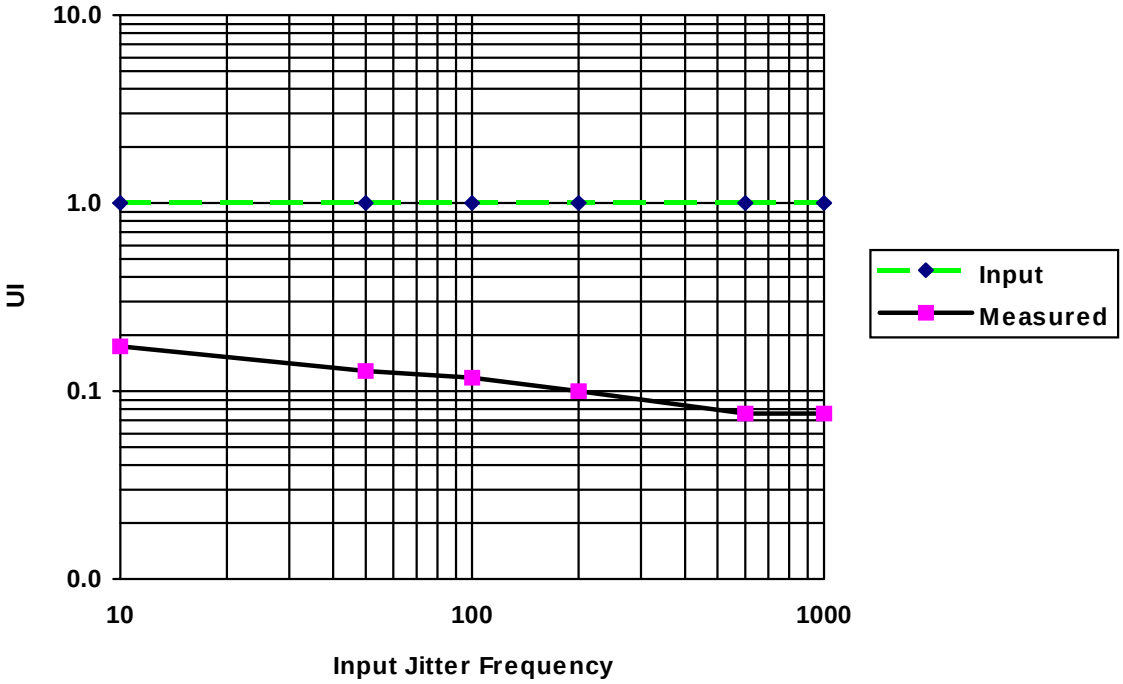


Figure 23. Jitter Transfer Measurements

Mapping Jitter Measurement

The following table lists the mapping jitter measurements, which are made with a SDH/SONET Analyzer replacing the 155 Mbit/s loopback in Figure 21.

G.703 Interface	Filter Characteristics	Maximum Output Jitter (UI-PP)	
		Requirement	Measured Value
2048 kbit/s	f1-f4 (HP1/LP)	(Note 1)	0.032
	f3-f4 (HP2/LP)	≤ 0.075 UI	0.024

Note 1: These values are for further study.

Combined Jitter Measurement

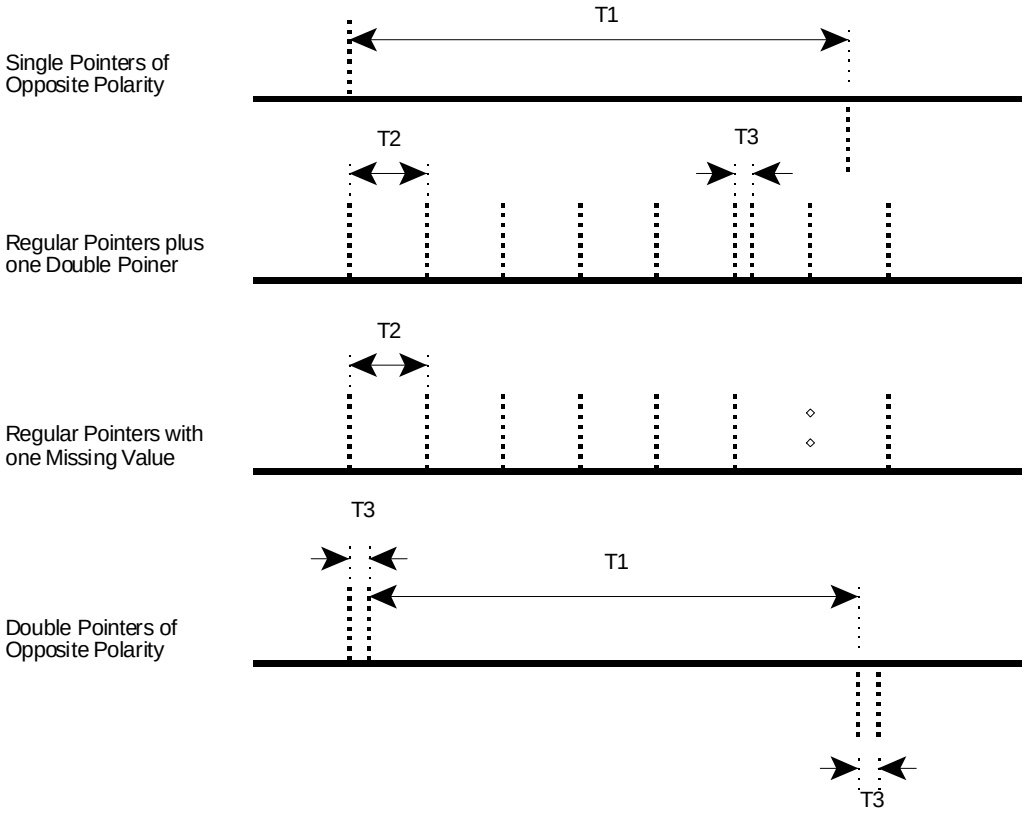
The following table lists the combined jitter measurements.

Pointer Test Sequence		Filter	Leak Rate (Hex) (Note 1)	Maximum Output Jitter (UI - PP)	
				Requirement	Measured
1	Single Pointers of Opposite Polarity	f1-f4 (HP1/LP)	01H	≤ 0.4 (Note 2)	0.019
2	Regular Pointers Plus One Double Pointer		12H		0.169
3	Regular Pointers with One Missing Pointer		12H		0.169
4	Double Pointers of Opposite Polarity		16H		0.164
1	Single Pointers of Opposite Polarity	f3-f4 (HP2/LP)	01H	≤ 0.075 (Note 2)	0.009
2	Regular Pointers Plus One Double Pointer		12H		0.009
3	Regular Pointers with One Missing Pointer		12H		0.009
4	Double Pointers of Opposite Polarity		16H		0.009

Note 1: These values are written into the Desynchronizer Pointer Leak Rate Register for mapper port n (register address 049, 079, 0A9, 0D9 hex, for n = 1 - 4).

Note 2: The limit corresponds to the pointer sequences shown in Figure 24 for Standard Pointer Test Sequences, (T1 ≥ 10 s, T2 > 0.75 s, T3 = 30 ms). The T3 value was constrained by test equipment limitations.

Figure 24. Standard Pointer Test Sequences



(Ref: ITU-T G.783, Fig. 6-2)

INTERNAL SPOT PROCESSOR

The internal SPOT processor of the QE1M device is a SONET Processor for Overhead Termination. The purpose of the SPOT processor is to relieve the device's internal logic of the need to support relatively slow functions like performance monitoring and alarm handling. The utility of this feature will grow as communications standards require tighter control of data flow and network management. In addition, as boards become more densely populated with VLSI components, the availability of the SPOT processor will help by reducing the requirement for external components and the workload of the main processor (and the software engineers who program it).

The SPOT processor is a programmable core which adheres to Reduced Instruction Set Computer (RISC) principles. It executes one instruction per clock cycle. Instructions are simple, performing data movement, basic arithmetic functions (8-bit integer operations, but no multiply/divide) and program control. The executable device microcode required for operation of the SPOT processor and associated descriptive text is available via the QE1M selection option of the Product Finder on the home page of the TranSwitch Internet World Wide Web site at www.transwitch.com, where the files are provided in ZIP format.

The SPOT processor is designed to run at 29.16 MHz. This clock is internally derived from the 58.32 MHz desynchronizer clock input (EXTCK). The Instruction RAM (I-RAM) has 2048 words of 16 bits while the Data RAM (D-RAM) has 2048 words of 8 bits. The SPOT processor has access to the Microprocessor Interface and the Add/Drop Engines of the QE1M via an 8-bit data bus, as shown in Figure 25. The SPOT processor is event-driven, with each client independently and asynchronously requesting service. These maskable requests are surveyed by a task queue and prioritized by function (Add, Drop, Line). When idle, the SPOT processor polls the task queue to identify the next client to be serviced. This results in a call to the appropriate subroutine(s). During each subroutine, the SPOT processor may transfer data to/from the Add/Drop Engines or the Microprocessor Interface. The SPOT processor will make decisions regarding control/status and update any necessary counters and other Data RAM locations. The subroutine is terminated by returning to the idle loop, and the cycle is then repeated.

The E1 data paths (i.e., for the Add/Drop Engines) are implemented in free-running hardware, and are therefore not dependent on the SPOT processor.

The Data RAM contains important information about the status of the E1 channels. Performance counters, J2 messages, etc., are all stored there. The external microprocessor is granted access to the internal Data RAM when addressing the appropriate locations. Since RAM access is arbitrated, the grant will not be immediate, and the RDY/DTACK signal is de-asserted until the requested data becomes available.

Since the SPOT processor is effectively a very large state machine, it could enter an unforeseen state (e.g., due to a software bug or RAM corruption) which prevents it from servicing all requests in a timely manner. Although the data path is not interrupted, the path overhead bytes may not be correctly processed under these conditions. Two status bits have been provided to detect critical errors which are indications of this status:

Parity Error (PERR) in bit 4 of addresses 028H and 029H indicates that a parity error has occurred in reading the Instruction RAM.

Watchdog Timer Expired (WDTEXP) in bit 6 of addresses 028H and 029H indicates that the SPOT processor may be unable to service all requests in a timely manner. Some possible causes for this condition are excessive microprocessor accesses, a SPOT processor clock that is running too slowly, or a software bug.

Upon power-up or hardware reset, the contents of the Instruction RAM are assumed to be invalid and execution of the SPOT program is internally disabled. Before the SPOT processor can begin processing, the microprocessor must reprogram the Instruction RAM, using the instructions described in the following table, by performing the procedure described in the flowchart in Figure 26.

Table 1: Reprogram Functions (valid only when control bit RPSPOT at bit 7 in address 007H is a 1)

Function	Direction	Microprocessor Interface Address	Description
wrPC	write	102H	IRAMptr <== SPOTPCLD(10-0)
rdPC0	read	102H	read IRAMptr[7:0]
rdPC1	read	103H	read IRAMptr[10:8]
IRAMwr	write	100H	*IRAMptr++ <== data
IRAMrd	read	100H	data <== *IRAMptr++

The 11-bit SPOT PC Load register SPOTPCLD at address 007H bits 2-0 and address 006H bits 7-0 is first initialized. This is an offset address into the Instruction RAM. It may not be necessary always to write/read the entire program, but for normal operation this register should be set to 000H.

In order to access the Instruction RAM, set to 1 the Reprogram SPOT control bit RPSPOT at bit 7 in address 007H. At this time the Data RAM is off-line (i.e., it is inaccessible to the microprocessor), but all register-based locations are still available. SPOT program execution is disabled when RPSPOT is a 1.

Function "wrPC" causes the Instruction RAM word pointer to be loaded from the SPOT PC Load register. The SPOT processor automatically increments the Instruction RAM word pointer, which allows the microprocessor to write all instructions to one address (100H). Since the length of the Instruction RAM is 2048 16-bit words, 4096 IRAM 8-bit write functions ("IRAMwr") are required to program the SPOT processor completely. TranSwitch provides the 4096 bytes of code that will implement the features mentioned in this document.

It is recommended, but not required, that the writes to the Instruction RAM should be verified as part of the initialization procedure. As shown in the flowchart, it is necessary only to use the instruction "wrPC" to reload the I-RAM word pointer and then perform 4096 I-RAM read cycles using the same fixed data location (100H) as that used for write (function "IRAMrd").

The programming procedure is completed by setting control bit RPSPOT to 0. At this point, the word pointer is reloaded and execution of the SPOT processor program execution is enabled. It is important to set control bit INITSP at address 015H, bit 0 to 1 at some time after programming the SPOT processor. This will cause the SPOT processor to execute an initialization subroutine from the Instruction RAM that will initialize the Data RAM and reset its general purpose registers to allow other subroutines to begin running from a known state.

Figure 25. Schematic Diagram of QE1M Showing SPOT Processor Interfaces

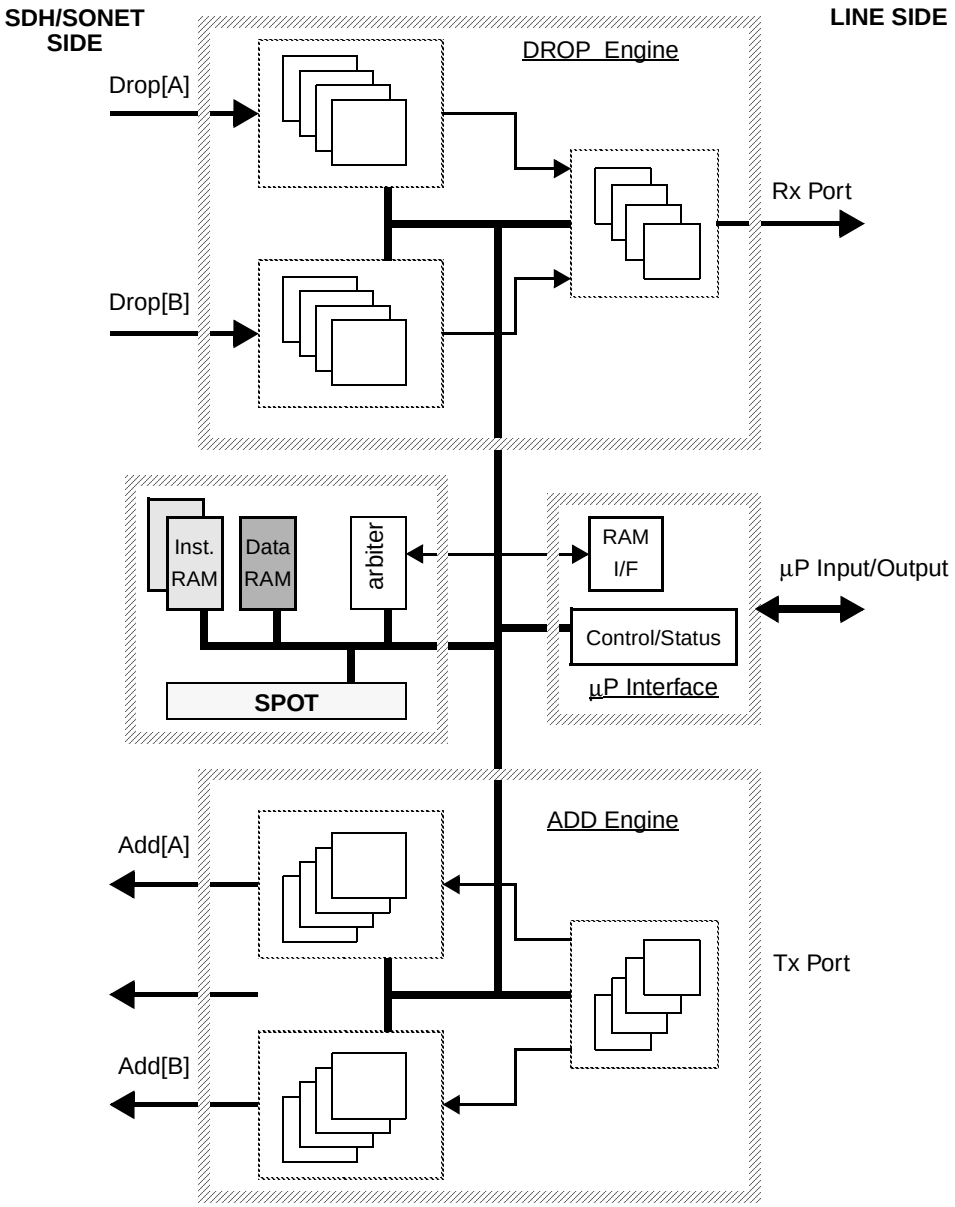
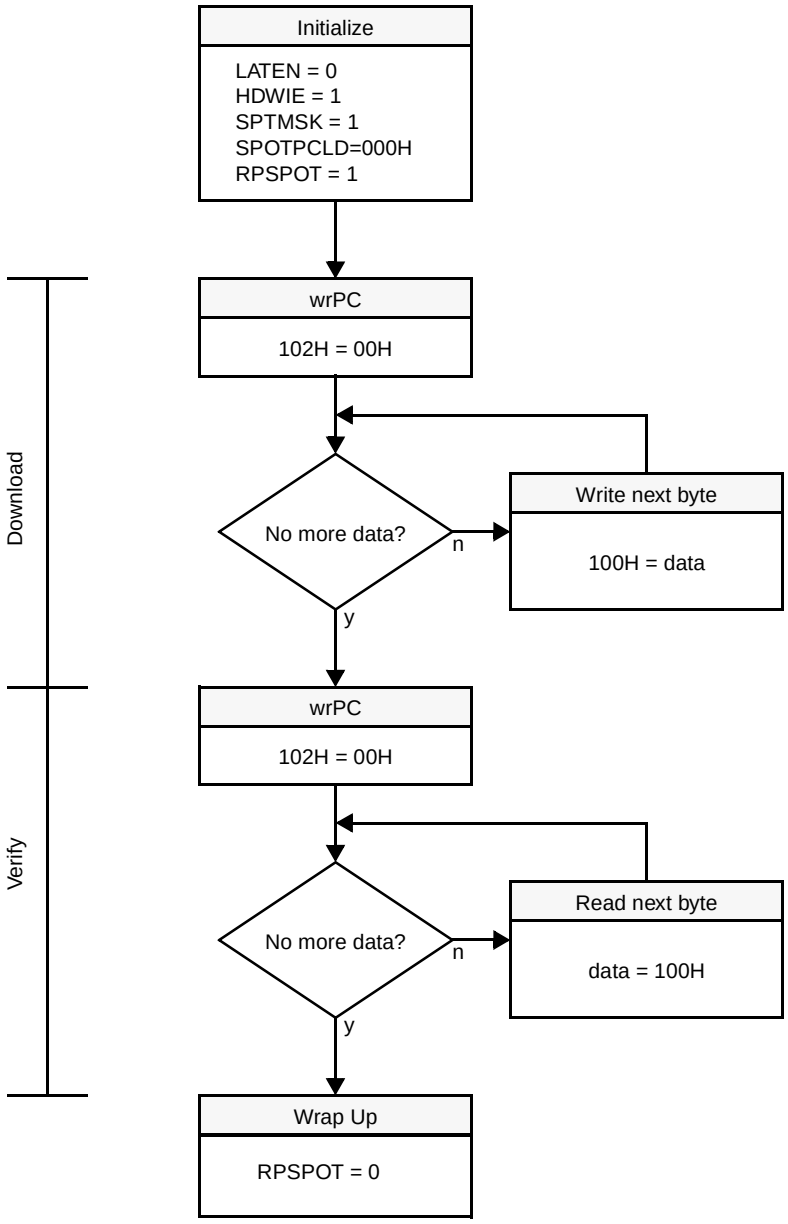


Figure 26. Recommended Implementation Flowchart for Reprogramming the SPOT Processor



Note: RESTSP must be 0 during reprogramming.

BOUNDARY SCAN

Introduction

The Boundary Scan Interface Block provides a five-lead Test Access Port (TAP) that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external Input/Output leads from the TAP for board and component test.

The IEEE 1149.1 standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides observability and controllability for the interface leads of the device. As shown in Figure 27, one cell of a boundary scan register is assigned to each input or output lead to be observed or tested (bidirectional leads may have two cells). The boundary scan capability is based on a Test Access Port (TAP) controller, instruction and bypass registers, and a boundary scan register bordering the input and output leads. The boundary scan test bus interface consists of four input signals (Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$)) and a Test Data Output (TDO) output signal. Boundary scan signal timing is shown in 17.

The TAP controller receives external control information via a Test Clock (TCK) signal and a Test Mode Select (TMS) signal, and sends control signals to the internal scan paths. Detailed information on the operation of this state machine can be found in the IEEE 1149.1 standard. The serial scan path architecture consists of an instruction register, a boundary scan register and a bypass register. These three serial registers are connected in parallel between the Test Data Input (TDI) and Test Data Output (TDO) signals, as shown in Figure 27.

The boundary scan function can be reset and disabled by holding lead $\overline{TRS}$ low. When boundary scan testing is not being performed the boundary scan register is transparent, allowing the input and output signals to pass to and from the QE1M device's internal logic. During boundary scan testing, the boundary scan register may disable the normal flow of input and output signals to allow the device to be controlled and observed via scan operations.

Boundary Scan Operation

The maximum frequency the QE1M device will support for boundary scan is 10 MHz. The timing diagrams for the boundary scan interface leads are shown in 17.

The instruction register contains three bits. The QE1M device performs the following three boundary scan test instructions:

The EXTEST test instruction (000) provides the ability to test the connectivity of the QE1M device to external circuitry.

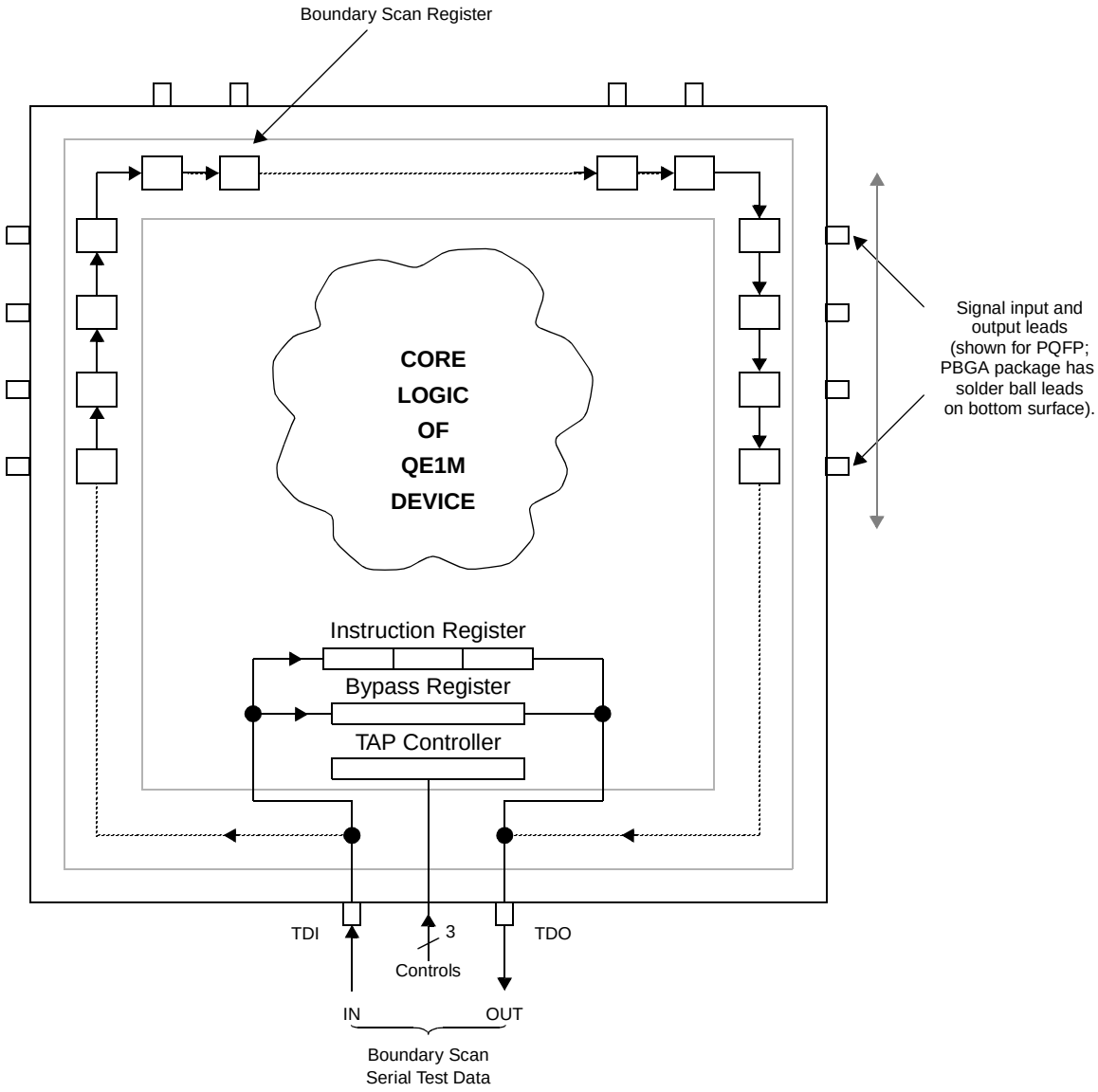
The SAMPLE test instruction (010) provides the ability to examine the boundary scan register contents without interfering with device operation.

The BYPASS test instruction (111) provides the ability to bypass the QE1M boundary scan and instruction registers.

Boundary Scan Reset

Specific control of the $\overline{TRS}$ lead is required in order to ensure that the boundary scan logic does not interfere with normal device operation. This lead must either be held low, asserted low, or asserted low then high (pulsed low), to asynchronously reset the Test Access Port (TAP) controller during power-up of the QE1M. If boundary scan testing is to be performed and the lead is held low, then a pull-down resistor value should be chosen which will allow the tester to drive this lead high, but still meet the V_{IL} requirements listed in the 'Input, Output and Input/Output Parameters' section of this Data Sheet for worst case leakage currents of all devices sharing this pull-down resistor.

Figure 27. Boundary Scan Schematic



Boundary Scan Chain

There are 159 scan cells in the boundary scan chain associated with QE1M core logic functions. Bidirectional signals require two scan cells. Additional scan cells are used for direction control as needed. A boundary scan description language (BSDL) source file is available via the Products page of the TranSwitch Internet World Wide Web site at www.transwitch.com. The following table shows the listed order of the scan cells and their function.

Scan Cell No.	I/O	Lead No.		Symbol	Comments
		PQFP	PBGA		
	Output	37	P1	TDO	SCAN Chain output
0	Input	33	M3	ADSPE	
1	Input	32	L2	ADC1J1V1	
2	Input	31	L1	AASPE	
3	Input	30	L4	AAC1J1V1	
4	Input	28	K2	AACLK	
5	Input	26	K3	ADCLK	
6	Output (2-state)	24	J2	$\overline{\text{ADIND}}$	
7	Output (2-state)	23	J3	$\overline{\text{AAIND}}$	
8	Input	21	H1	TPI1	
9	Input	20	G4	TNI1	
10	Input	19	G1	TCI1	
11	Input	18	G2	QUIET1	
12	Output (3-state)	16	F4	RPO1	
13	Output (3-state)	15	F3	RNO1	
14	---	---		$\overline{RN1\_OE}$	When high, lead 15 or F3 is tristated.
15	Output (3-state)	14	F1	RCO1	
16	---	---		$\overline{RCP1\_OE}$	When high, leads 14 or F1 and 16 or F4 are tristated.
17	Output (3-state)	12	E4	RPO3	
18	Output (3-state)	11	E3	RNO3	
19	---	---		$\overline{RN3\_OE}$	When high, lead 11 or E3 is tristated.
20	Output (3-state)	10	E1	RCO3	
21	---	---		$\overline{RCP3\_OE}$	When high, leads 10 or E1 and 12 or E4 are tristated.
22	Input	8	D4	TPI3	
23	Input	7	D1	TNI3	

Scan Cell No.	I/O	Lead No.		Symbol	Comments
		PQFP	PBGA		
24	Input	6	D3	TCI3	
25	Input	5	D2	QUIET3	
26	Input	3	C1	MUX	
27	Input	2	B1	MOTO	
28	Input	1	C3	UPA10 (A10) (in)	
29	Output (3-state)	1	C3	UPA10 (A10) (out)	Although they are normally inputs, all address leads can be driven internally by the SPOT processor in test mode.
30	Input	160	B2	UPA9 (A9) (in)	
31	Output (3-state)	160	B2	UPA9 (A9) (out)	
32	Input	159	A2	UPA8 (A8) (in)	
33	Output (3-state)	159	A2	UPA8 (A8) (out)	
34	Input	158	A3	A7 (in)	
35	Output (3-state)	158	A3	A7 (out)	
36	Input	157	A4	$\overline{\text{ABUST}}$	
37	---	---		$\overline{\textit{UPA\_OE2}}$	When high, leads 158 or A3, 159 or A2, 160 or B2 and 1 or C3 are tristated.
38	Input	156	B5	A6 (in)	
39	Output (3-state)	156	B5	A6 (out)	
40	Input	155	C5	$\overline{\text{RESET}}$	
41	Input	153	C6	A5 (in)	
42	Output (3-state)	153	C6	A5 (out)	
43	Output (3-state)	152	D6	INT/$\overline{\text{IRQ}}$	
44	---	---		$\overline{\textit{INT\_OE}}$	When high, lead 152 or D6 is tristated.
45	Input	150	B7	INTSH	
46	Input	149	A7	ALE	Used only in MUX mode.
47	Input	148	C7	$\overline{\text{WR}}$ ($\overline{\text{WR}}$/$\overline{\text{LDS}}$)	
48	Input	147	D7	$\overline{\text{RD}}$ ($\overline{\text{RD}}$ / RD/$\overline{\text{WR}}$)	

Scan Cell No.	I/O	Lead No.		Symbol	Comments
		PQFP	PBGA		
49	---	---		*UPA_OE1*	When high, leads 144 or C8, 153 or C6 and 156 or B5 are tristated.
50	Input	146	B8	SEL	
51	---	---		*UPA_OE0*	When high, leads 135 or B10, 140 or B9, 141 or C9 and 143 or D8 are tristated.
52	Input	145	A8	TEST	
53	---	---		*UPD_OE3*	When high, leads 132 or C11 and 133 or D11 are tristated.
54	Input	144	C8	A4 (in)	
55	Output (3-state)	144	C8	A4 (out)	
56	Input	143	D8	A3 (in)	
57	Output (3-state)	143	D8	A3 (out)	
58	Input	141	C9	A2 (in)	
59	Output (3-state)	141	C9	A2 (out)	
60	Input	140	B9	A1 (in)	
61	Output (3-state)	140	B9	A1 (out)	
62	Input	138	D10	EXTCK	
63	---	---		*UPD_OE2*	When high, leads 129 or A12 and 130 or C12 are tristated.
64	Input	136	A10	HIGHZ	
65	---	---		*UPD_OE1*	When high, leads 126 or A13 and 128 or B12 are tristated.
66	Input	135	B10	A0 (in)	
67	Output (3-state)	135	B10	A0 (out)	
68	Input	133	D11	UPAD7 (D7) (in)	
69	Output (3-state)	133	D11	UPAD7 (D7) (out)	
70	Input	132	C11	UPAD6 (D6) (in)	
71	Output (3-state)	132	C11	UPAD6 (D6) (out)	
72	Input	130	C12	UPAD5 (D5) (in)	

Scan Cell No.	I/O	Lead No.		Symbol	Comments
		PQFP	PBGA		
73	Output (3-state)	130	C12	UPAD5 (D5) (out)	
74	Input	129	A12	UPAD4 (D4) (in)	
75	Output (3-state)	129	A12	UPAD4 (D4) (out)	
76	Input	128	B12	UPAD3 (D3) (in)	
77	Output (3-state)	128	B12	UPAD3 (D3) (out)	
78	Input	126	A13	UPAD2 (D2) (in)	
79	Output (3-state)	126	A13	UPAD2 (D2) (out)	
80	Input	125	C13	UPAD1 (D1) (in)	
81	Output (3-state)	125	C13	UPAD1 (D1) (out)	
82	Input	124	B13	UPAD0 (D0) (in)	
83	Output (3-state)	124	B13	UPAD0 (D0) (out)	
84	Output (3-state)	122	A15	RDY/$\overline{\text{DTACK}}$	
85	---	---		$\overline{\textit{RDY\_OE}}$	When high, lead 122 or A15 is tristated.
86	Input	121	C14	SPARE2	
87	---	---		$\overline{\textit{UPD\_OE0}}$	When high, leads 124 or B13 and 125 or C13 are tristated.
88	Input	119	B15	QUIET4	
89	Input	118	A16	TCI4	
90	Input	117	C15	TNI4	
91	Input	116	C16	TPI4	
92	Output (3-state)	114	D14	RCO4	
93	Output (3-state)	113	E15	RNO4	
94	---	---		$\overline{\textit{RN4\_OE}}$	When high, lead 113 or E15 is tristated.
95	Output (3-state)	112	E14	RPO4	

Scan Cell No.	I/O	Lead No.		Symbol	Comments
		PQFP	PBGA		
96	---	---		$\overline{RCP4\_OE}$	When high, leads 112 or E14 and 114 or D14 are tristated.
97	Output (3-state)	111	E13	RCO2	
98	Output (3-state)	110	F16	RNO2	
99	---	---		$\overline{RN2\_OE}$	When high, lead 110 or F16 is tristated.
100	Output (3-state)	109	F14	RPO2	
101	---	---		$\overline{RCP2\_OE}$	When high, leads 109 or F14 and 111 or E13 are tristated.
102	Input	107	G16	QUIET2	
103	Input	106	G14	TCI2	
104	Input	105	G13	TNI2	
105	Input	104	H15	TPI2	
106	Output (2-state)	102	J13	$\overline{BAIND}$	
107	Output (2-state)	101	J14	$\overline{BDIND}$	
108	Input	99	K14	BDCLK	
109	Input	98	K16	BACLK	
110	Input	96	L13	BAC1J1V1	
111	Input	95	L14	BASPE	
112	Input	94	L16	BDC1J1V1	
113	Input	93	L15	BDSPE	
114	Input	91	M14	BDPAR	
115	Input	90	M16	BD7	
116	Input	89	M15	BD6	
117	Input	88	N13	BD5	
118	Input	87	N16	BD4	
119	Input	85	P16	BD3	
120	Input	84	P15	BD2	
121	Input	83	R16	BD1	
122	Input	82	P14	BD0	
123	Input	80	R15	SPARE1	
124	Output (2-state)	78	R14	$\overline{BADD}$	
125	Output (3-state)	77	T14	BAPAR	

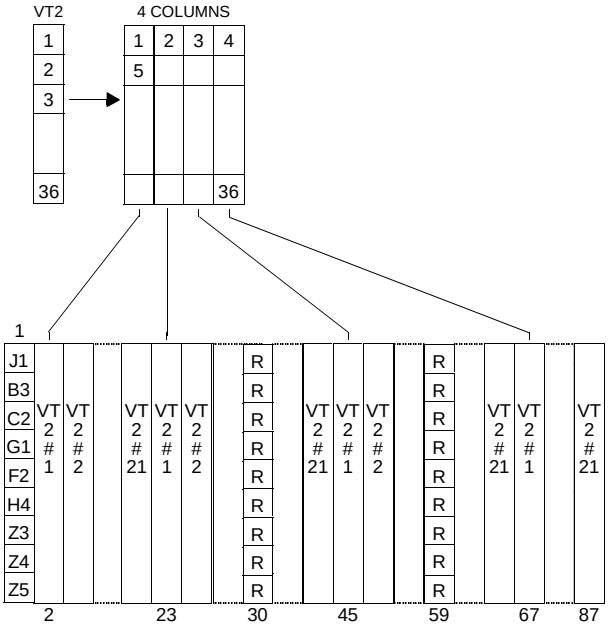
Scan Cell No.	I/O	Lead No.		Symbol	Comments
		PQFP	PBGA		
126	Output (3-state)	76	T13	BA7	
127	---	---		$\overline{BA\_OE2}$	When high, leads 75 or R13, 76 or T13 and 77 or T14 are tristated.
128	Output (3-state)	75	R13	BA6	
129	Output (3-state)	73	R12	BA5	
130	Output (3-state)	72	T12	BA4	
131	---	---		$\overline{BA\_OE1}$	When high, leads 71 or P12, 72 or T12 and 73 or R12 are tristated.
132	Output (3-state)	71	P12	BA3	
133	Output (3-state)	69	T11	BA2	
134	Output (3-state)	68	P11	BA1	
135	---	---		$\overline{BA\_OE0}$	When high, leads 67 or N11, 68 or P11 and 69 or T11 are tristated.
136	Output (3-state)	67	N11	BA0	
137	Output (3-state)	65	T10	AA0	
138	Output (3-state)	64	P10	AA1	
139	---	---		$\overline{AA\_OE0}$	When high, leads 63 or N10, 64 or P10 and 65 or T10 are tristated.
140	Output (3-state)	63	N10	AA2	
141	Output (3-state)	62	R9	AA3	
142	Output (3-state)	60	N9	AA4	
143	---	---		$\overline{AA\_OE1}$	When high, leads 59 or N8, 60 or N9 and 62 or R9 are tristated.
144	Output (3-state)	59	N8	AA5	
145	Output (3-state)	58	P8	AA6	
146	Output (3-state)	56	P7	AA7	
147	Output (3-state)	55	T7	AAPAR	
148	---	---		$\overline{AA\_OE2}$	When high, leads 55 or T7, 56 or P7 and 58 or P8 tristated.
149	Output (2-state)	54	R7	$\overline{AADD}$	
150	Input	52	N6	AD0	
151	Input	51	P6	AD1	
152	Input	50	T6	AD2	

Scan Cell No.	I/O	Lead No.		Symbol	Comments
		PQFP	PBGA		
153	Input	48	N5	AD3	
154	Input	47	P5	AD4	
155	Input	46	T5	AD5	
156	Input	44	P4	AD6	
157	Input	43	R4	AD7	
158	Input	42	T3	ADPAR	
	Input	38	R1	TDI	SCAN chain input

MULTIPLEX FORMAT AND MAPPING INFORMATION

STS-1 VT2 (2.048 Mbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the 21 VT2s into an STS-1 SPE. Column 1 is assigned to carry the path overhead bytes.



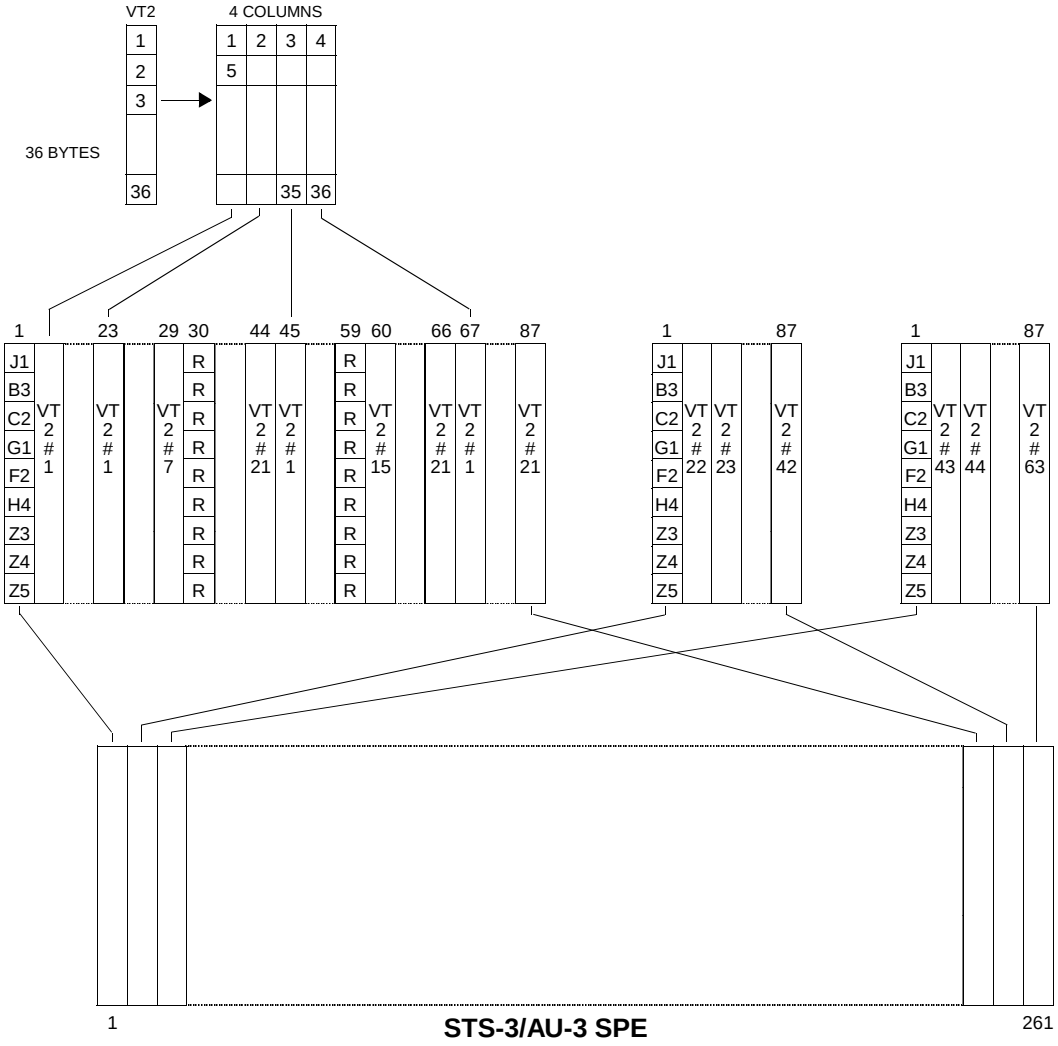
STS-1 Mapping (2.048 Mbit/s)

VT#	RTUNn, TTUNn Locations 04CH, 04DH Port 1 0ACH, 0ADH Port 3 07CH, 07DH Port 2 0DCH, 0DDH Port 4							VT2 Column Numbers*
	6	5	4	3	2	1	0	
	0	0	0	0	0	0	0	No VT Selected
1	0	0	0	0	1	0	1	2, 23, 45, 67
2	0	0	0	1	0	0	1	3, 24, 46, 68
3	0	0	0	1	1	0	1	4, 25, 47, 69
4	0	0	1	0	0	0	1	5, 26, 48, 70
5	0	0	1	0	1	0	1	6, 27, 49, 71
6	0	0	1	1	0	0	1	7, 28, 50, 72
7	0	0	1	1	1	0	1	8, 29, 51, 73
8	0	0	0	0	1	1	0	9, 31, 52, 74
9	0	0	0	1	0	1	0	10, 32, 53, 75
10	0	0	0	1	1	1	0	11, 33, 54, 76
11	0	0	1	0	0	1	0	12, 34, 55, 77
12	0	0	1	0	1	1	0	13, 35, 56, 78
13	0	0	1	1	0	1	0	14, 36, 57, 79
14	0	0	1	1	1	1	0	15, 37, 58, 80
15	0	0	0	0	1	1	1	16, 38, 60, 81
16	0	0	0	1	0	1	1	17, 39, 61, 82
17	0	0	0	1	1	1	1	18, 40, 62, 83
18	0	0	1	0	0	1	1	19, 41, 63, 84
19	0	0	1	0	1	1	1	20, 42, 64, 85
20	0	0	1	1	0	1	1	21, 43, 65, 86
21	0	0	1	1	1	1	1	22, 44, 66, 87

* Note: Columns 30 and 59 carry fixed stuff bytes. Column 1 is assigned for the POH bytes.

STS-3/AU-3 VT2/TU-12 (2.048 Mbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the 63 VT2/TU-12s into an STS-3/AU-3 SPE. Each STS-3 carries three STS-1s. Column 1 in each STS-1/AU-3 is assigned to carry the path overhead bytes.



Note: Columns 88, 89, 90, 175, 176 and 177 are fixed stuff.

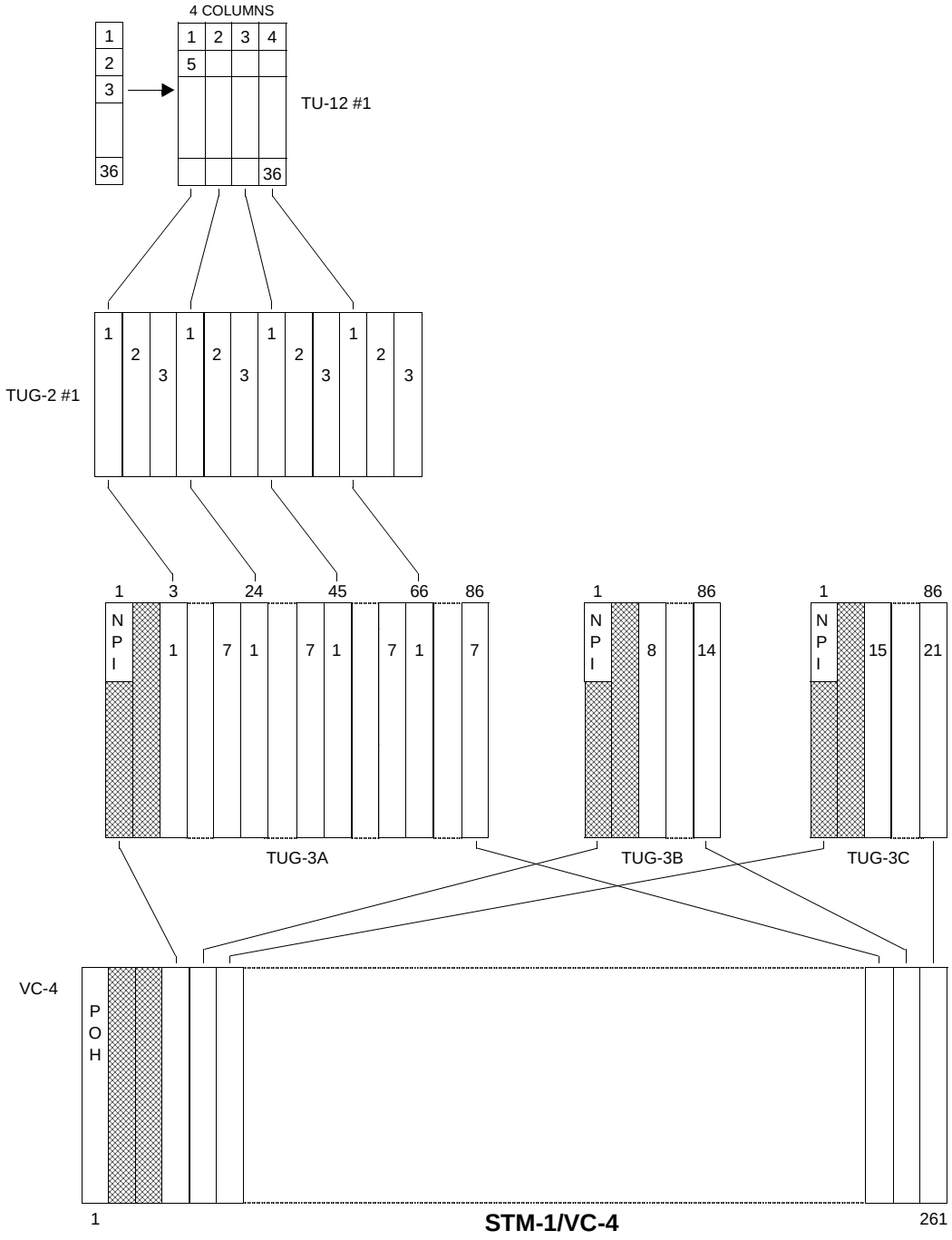
STS-3/AU-3 Mapping (2.048 Mbit/s)

TU/ VT #	RTUNn, TTUNn 04CH, 04DH Port 1 07CH, 07DH Port 2 0ACH, 0ADH Port 3 0DCH, 0DDH Port 4 Registers 6 5 4 3 2 1 0	STS-3/AU-3 Column Numbers*	TU/ VT #	RTUNn, TTUNn 04CH, 04DH Port 1 07CH, 07DH Port 2 0ACH, 0ADH Port 3 0DCH, 0DDH Port 4 Registers 6 5 4 3 2 1 0	STS-3/AU-3 Column Numbers*	TU/ VT #	RTUNn, TTUNn 04CH, 04DH Port 1 07CH, 07DH Port 2 0ACH, 0ADH Port 3 0DCH, 0DDH Port 4 Registers 6 5 4 3 2 1 0	STS-3/AU-3 Column Numbers*
	0 0 0 0 0 0 0	No TU/VT Selected						
1	0 1 0 0 1 0 1	4, 67, 133, 199	22	1 0 0 0 1 0 1	5, 68, 134, 200	43	1 1 0 0 1 0 1	6, 69, 135, 201
2	0 1 0 1 0 0 1	7, 70, 136, 202	23	1 0 0 1 0 0 1	8, 71, 137, 203	44	1 1 0 1 0 0 1	9, 72, 138, 204
3	0 1 0 1 1 0 1	10, 73, 139, 205	24	1 0 0 1 1 0 1	11, 74, 140, 206	45	1 1 0 1 1 0 1	12, 75, 141, 207
4	0 1 1 0 0 0 1	13, 76, 142, 208	25	1 0 1 0 0 0 1	14, 77, 143, 209	46	1 1 1 0 0 0 1	15, 78, 144, 210
5	0 1 1 0 1 0 1	16, 79, 145, 211	26	1 0 1 0 1 0 1	17, 80, 146, 212	47	1 1 1 0 1 0 1	18, 81, 147, 213
6	0 1 1 1 0 0 1	19, 82, 148, 214	27	1 0 1 1 0 0 1	20, 83, 149, 215	48	1 1 1 1 0 0 1	21, 84, 150, 216
7	0 1 1 1 1 0 1	22, 85, 151, 217	28	1 0 1 1 1 0 1	23, 86, 152, 218	49	1 1 1 1 1 0 1	24, 87, 153, 219
8	0 1 0 0 1 1 0	25, 91, 154, 220	29	1 0 0 0 1 1 0	26, 92, 155, 221	50	1 1 0 0 1 1 0	27, 93, 156, 222
9	0 1 0 1 0 1 0	28, 94, 157, 223	30	1 0 0 1 0 1 0	29, 95, 158, 224	51	1 1 0 1 0 1 0	30, 96, 159, 225
10	0 1 0 1 1 1 0	31, 97, 160, 226	31	1 0 0 1 1 1 0	32, 98, 161, 227	52	1 1 0 1 1 1 0	33, 99, 162, 228
11	0 1 1 0 0 1 0	34, 100, 163, 229	32	1 0 1 0 0 1 0	35, 101, 164, 230	53	1 1 1 0 0 1 0	36, 102, 165, 231
12	0 1 1 0 1 1 0	37, 103, 166, 232	33	1 0 1 0 1 1 0	38, 104, 167, 233	54	1 1 1 0 1 1 0	39, 105, 168, 234
13	0 1 1 1 0 1 0	40, 106, 169, 235	34	1 0 1 1 0 1 0	41, 107, 170, 236	55	1 1 1 1 0 1 0	42, 108, 171, 237
14	0 1 1 1 1 1 0	43, 109, 172, 238	35	1 0 1 1 1 1 0	44, 110, 173, 239	56	1 1 1 1 1 1 0	45, 111, 174, 240
15	0 1 0 0 1 1 1	46, 112, 178, 241	36	1 0 0 0 1 1 1	47, 113, 179, 242	57	1 1 0 0 1 1 1	48, 114, 180, 243
16	0 1 0 1 0 1 1	49, 115, 181, 244	37	1 0 0 1 0 1 1	50, 116, 182, 245	58	1 1 0 1 0 1 1	51, 117, 183, 246
17	0 1 0 1 1 1 1	52, 118, 184, 247	38	1 0 0 1 1 1 1	53, 119, 185, 248	59	1 1 0 1 1 1 1	54, 120, 186, 249
18	0 1 1 0 0 1 1	55, 121, 187, 250	39	1 0 1 0 0 1 1	56, 122, 188, 251	60	1 1 1 0 0 1 1	57, 123, 189, 252
19	0 1 1 0 1 1 1	58, 124, 190, 253	40	1 0 1 0 1 1 1	59, 125, 191, 254	61	1 1 1 0 1 1 1	60, 126, 192, 255
20	0 1 1 1 0 1 1	61, 127, 193, 256	41	1 0 1 1 0 1 1	62, 128, 194, 257	62	1 1 1 1 0 1 1	63, 129, 195, 258
21	0 1 1 1 1 1 1	64, 130, 196, 259	42	1 0 1 1 1 1 1	65, 131, 197, 260	63	1 1 1 1 1 1 1	66, 132, 198, 261
	STS-1 #1, AU-3 A			STS-1 #2, AU-3 B			STS-1 #3, AU-3 C	

* Note: Columns 88, 89, 90, 175, 176 and 177 are fixed stuff.

STM-1/VC-4 TU-12 (2048 kbit/s) Multiplex Format Mapping

The following diagram and table illustrate the mapping of the 63 TU-12s into an STM-1/VC-4. The QE1M provides control bits for enabling the Null Pointer Indicators (NPIs) for the columns indicated.



STM-1 VC-4 Mode (2048 kbit/s)

TU #	RTUNn, TTUNn 04CH, 04DH Port 1 07CH, 07DH Port 2 0ACH, 0ADH Port 3 0DCH, 0DDH Port 4 Registers 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	RTUNn, TTUNn 04CH, 04DH Port 1 07CH, 07DH Port 2 0ACH, 0ADH Port 3 0DCH, 0DDH Port 4 Registers 6 5 4 3 2 1 0	VC-4 Column Numbers	TU #	RTUNn, TTUNn 04CH, 04DH Port 1 07CH, 07DH Port 2 0ACH, 0ADH Port 3 0DCH, 0DDH Port 4 Registers 6 5 4 3 2 1 0	VC-4 Column Numbers
	0 0 0 0 0 0 0	No TU Selected						
1	0 1 0 0 1 0 1	10, 73, 136, 199	22	1 0 0 0 1 0 1	11, 74, 137, 200	43	1 1 0 0 1 0 1	12, 75, 138, 201
2	0 1 0 1 0 0 1	13, 76, 139, 202	23	1 0 0 1 0 0 1	14, 77, 140, 203	44	1 1 0 1 0 0 1	15, 78, 141, 204
3	0 1 0 1 1 0 1	16, 79, 142, 205	24	1 0 0 1 1 0 1	17, 80, 143, 206	45	1 1 0 1 1 0 1	18, 81, 144, 207
4	0 1 1 0 0 0 1	19, 82, 145, 208	25	1 0 1 0 0 0 1	20, 83, 146, 209	46	1 1 1 0 0 0 1	21, 84, 147, 210
5	0 1 1 0 1 0 1	22, 85, 148, 211	26	1 0 1 0 1 0 1	23, 86, 149, 212	47	1 1 1 0 1 0 1	24, 87, 150, 213
6	0 1 1 1 0 0 1	25, 88, 151, 214	27	1 0 1 1 0 0 1	26, 89, 152, 215	48	1 1 1 1 0 0 1	27, 90, 153, 216
7	0 1 1 1 1 0 1	28, 91, 154, 217	28	1 0 1 1 1 0 1	29, 92, 155, 218	49	1 1 1 1 1 0 1	30, 93, 156, 219
8	0 1 0 0 1 1 0	31, 94, 157, 220	29	1 0 0 0 1 1 0	32, 95, 158, 221	50	1 1 0 0 1 1 0	33, 96, 159, 222
9	0 1 0 1 0 1 0	34, 97, 160, 223	30	1 0 0 1 0 1 0	35, 98, 161, 224	51	1 1 0 1 0 1 0	36, 99, 162, 225
10	0 1 0 1 1 1 0	37, 100, 163, 226	31	1 0 0 1 1 1 0	38, 101, 164, 227	52	1 1 0 1 1 1 0	39, 102, 165, 228
11	0 1 1 0 0 1 0	40, 103, 166, 229	32	1 0 1 0 0 1 0	41, 104, 167, 230	53	1 1 1 0 0 1 0	42, 105, 168, 231
12	0 1 1 0 1 1 0	43, 106, 169, 232	33	1 0 1 0 1 1 0	44, 107, 170, 233	54	1 1 1 0 1 1 0	45, 108, 171, 234
13	0 1 1 1 0 1 0	46, 109, 172, 235	34	1 0 1 1 0 1 0	47, 110, 173, 236	55	1 1 1 1 0 1 0	48, 111, 174, 237
14	0 1 1 1 1 1 0	49, 112, 175, 238	35	1 0 1 1 1 1 0	50, 113, 176, 239	56	1 1 1 1 1 1 0	51, 114, 177, 240
15	0 1 0 0 1 1 1	52, 115, 178, 241	36	1 0 0 0 1 1 1	53, 116, 179, 242	57	1 1 0 0 1 1 1	54, 117, 180, 243
16	0 1 0 1 0 1 1	55, 118, 181, 244	37	1 0 0 1 0 1 1	56, 119, 182, 245	58	1 1 0 1 0 1 1	57, 120, 183, 246
17	0 1 0 1 1 1 1	58, 121, 184, 247	38	1 0 0 1 1 1 1	59, 122, 185, 248	59	1 1 0 1 1 1 1	60, 123, 186, 249
18	0 1 1 0 0 1 1	61, 124, 187, 250	39	1 0 1 0 0 1 1	62, 125, 188, 251	60	1 1 1 0 0 1 1	63, 126, 189, 252
19	0 1 1 0 1 1 1	64, 127, 190, 253	40	1 0 1 0 1 1 1	65, 128, 191, 254	61	1 1 1 0 1 1 1	66, 129, 192, 255
20	0 1 1 1 0 1 1	67, 130, 193, 256	41	1 0 1 1 0 1 1	68, 131, 194, 257	62	1 1 1 1 0 1 1	69, 132, 195, 258
21	0 1 1 1 1 1 1	70, 133, 196, 259	42	1 0 1 1 1 1 1	71, 134, 197, 260	63	1 1 1 1 1 1 1	72, 135, 198, 261

MEMORY MAP

The QE1M memory map consists of counters and register bit positions which may be accessed by the microprocessor. The memory map segment consists of 7FF (hex) address locations. Address locations in the range 000H - 7FFH that are shown as unused, or are unlisted, must not be accessed by the microprocessor. Unused bit positions within register locations will contain unspecified values when read, unless a 0 or 1 value is indicated in the tables below, or the address can be written by the microprocessor, in which case unused bit positions must always be set to 0. All counters saturate at full count and are cleared when they are read.

The common memory map segment consists of the Device ID, Program ID, Internal Processor, Control, Provisioning, Interrupt Indication, and Interrupt Status registers. The A bus segment consists of the A Drop and Add status registers. The B bus segment consists of the B Drop and Add status registers. Each Port n memory map segment (where n = 1-4) consists of the Desynchronizer, Provisioning, Status and Operations registers, and various counters. There are also Port n registers for J2 and N2 (Z6) message segments.

Some memory locations, at addresses 032H and above, are shown shaded in the memory map. These locations reside in the 2k x 8 Data RAM of the internal SPOT processor and are not reset by the software or hardware resets but only by INITSP. They are subject to arbitrated access by both the internal SPOT processor and the external microprocessor. An attempt to access any of these locations will toggle the RDY/$\overline{\text{DTACK}}$ output lead to pause the external microprocessor until the location is available for external access. While control bit RPSPOT is set to 1, these locations are assigned to use by the SPOT processor and must not be accessed by the external microprocessor unless they are addresses designated for microprocessor access while the SPOT processor is being reprogrammed (i.e., addresses 100H, 102H and 103H).

DEVICE ID

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
000	R	1	1	0	1	0	1	1	1
001	R	1	1	0	0	0	0	0	0
002	R	0	0	0	0	1	0	0	1
003	R	Revision (Version) Level				0	0	0	1
004	R	Mask Level (reads as 0000)				Growth (reads as 0000)			

PROGRAM ID

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
6BD	R/W	Program Revision Checksum/execution flag (PID-CHK)							
6BE	R/W	Part 1 of two-part program release number (PGMRV1)							
6BF	R/W	Part 2 of two-part program release number (PGMRV2)							

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

INTERNAL PROCESSOR (SPOT)

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
005	R/W	TranSwitch Test Register (set to 00H)							
006	R/W	SPOTPCLD (7 - 0)							
007	R/W	RPSPOT	TranSwitch Test Bits (set to 0000)				SPOTPCLD (10 - 8)		
008	R/W	TranSwitch Test Register (set to 00H)							

COMMON REGISTERS - CONTROLS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
010	R/W	MOD1	MOD0	AAHZE	BAHZE	BLOCK	NPIA	NPIB	NPIC
011	R/W	SBTEN	DRPBT	ABD	LATEN	TAISE	TCLKI	RAISE	RCLKI
012	R/W	ADDI	APE	IPOS	INEG	RFIE	THRSBY	DPE	PDDO
013	R/W	HEAISE	DV1SEL	DV1REF	RDIEN	NULLZ	DDIND	UQAE	TOBWZ

COMMON REGISTERS - PROVISIONING (CONTROL)

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
014	R/W	Unused (set to 000)			UEAME	SE1AIS	V5AL10	PTALTE	HDWIE
015	W	RESET	RESTAB	RESTBB	RESTSP	Unused (set to 000)			INITSP
0F1	R/W	0	0	0	0	V4EN	0	0	0
0F5	R/W	TxB2DIS	0	0	0	0	0	0	0

COMMON REGISTERS - INTERRUPT INDICATION

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
020	R	INT	EXTCK	ASIDE	BSIDE	PORT4	PORT3	PORT2	PORT1

COMMON REGISTERS - INTERRUPT MASK

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
016	R/W	0	0	0	0	0	0	0	SPTMSK
017	R/W	RPT4A	RPT4B	RPT3A	RPT3B	RPT2A	RPT2B	RPT1A	RPT1B
018	R/W	TFIFO4A	TFIFO4B	TFIFO3A	TFIFO3B	TFIFO2A	TFIFO2B	TFIFO1A	TFIFO1B
019	R/W	TPORT4	TPORT3	TPORT2	TPORT1	RFIFO4	RFIFO3	RFIFO2	RFIFO1
021	R/W	0	ECKMSK	ASMSK	BSMSK	P4MSK	P3MSK	P2MSK	P1MSK

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

A/B DROP AND ADD BUS REGISTERS - DESYNCHRONIZER AND INTERNAL PROCESSOR (SPOT) STATUS

Address (Hex)	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
022	R(L)	ADLOC	AALOC	ADPAR	0	0	A3UAISI	A2UAISI	A1UAISI
023	R	ADLOC	AALOC	ADPAR	0	0	A3UAISI	A2UAISI	A1UAISI
024	R(L)	LEXTC	0	0	0	0	A3DH4E	A2DH4E	A1DH4E
025	R	LEXTC	0	0	0	0	A3DH4E	A2DH4E	A1DH4E
026	R(L)	BDLOC	BALOC	BDPAR	0	0	B3UAISI	B2UAISI	B1UAISI
027	R	BDLOC	BALOC	BDPAR	0	0	B3UAISI	B2UAISI	B1UAISI
028	R(L)	SPTLOC	WDTEXP	0	PERR	0	B3DH4E	B2DH4E	B1DH4E
029	R	SPTLOC	WDTEXP	0	PERR	0	B3DH4E	B2DH4E	B1DH4E

DESYNCHRONIZER CONTROL - PORT n

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
049 079 0A9 0D9	R/W	Desynchronizer Pointer Leak Rate Register							

PROVISIONING (CONTROL) - PORT n

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04A 07A 0AA 0DA	R/W	TnSEL1	TnSEL0	RnSEL	UCHnE	USCHnE	BYPASn	RnEN	0
04B 07B 0AB 0DB	R/W	ADnEN	BDnEN	AAnEN	BAnEN	ANAnTx	ANAnEN	PRBSnEN	FRDISn
04C 07C 0AC 0DC	R/W	0	Receive TU/VT Select (RTUNn)						
04D 07D 0AD 0DD	R/W	0	Transmit TU/VT Select (TTUNn)						

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

STATUS REGISTERS AND COUNTERS - PORT n (A SIDE)

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
030 060 090 0C0	R(L)	AnAIS	AnLOP	AnSIZE	AnNDF	AnRDIS	AnRFI	AnUNEQ	AnSLER
031 061 091 0C1	R	AnAIS	AnLOP	AnSIZE	AnNDF	AnRDIS	AnRFI	AnUNEQ	AnSLER
032 062 092 0C2	R	AnPJ Counter				AnNJ Counter			
033 063 093 0C3	R	AnBIP2 Error Counter							
034 064 094 0C4	R	AnFEBE Counter							
035 065 095 0C5	R	Unused					An Rx Label		
04E 07E 0AE 0DE	R(L)	AnRDIP	AnRDIC	Unused (00)		AnJ2LOL	AnJ2TIM	Unused (00)	
04F 07F 0AF 0DF	R	AnRDIP	AnRDIC	Unused (00)		AnJ2LOL	AnJ2TIM	Unused (00)	
036 066 096 0C6	R	Unused							
037 067 097 0C7	R	Unused							
038 068 098 0C8	R	An Receive K4 (Z7) Byte							
039 069 099 0C9	R	An Receive O-Bits							
05A 08A 0BA 0EA	R(L)	AnTCUQ	AnTCAIS	AnTCLM	AnTCLL	AnTCTM	AnTCODI	AnTCRDI	0
05B 08B 0BB 0EB	R	AnTCUQ	AnTCAIS	AnTCLM	AnTCLL	AnTCTM	AnTCODI	AnTCRDI	0
100 200 300 400	R	An TC BIP-2 Error Counter							
101 201 301 401	R	An TC REI Counter							
102 202 302 402	R	An TC OEI Counter							
116 216 316 416	R	An Receive V4 Byte							

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

STATUS REGISTERS - PORT n (B SIDE)

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03A 06A 09A 0CA	R(L)	BnAIS	BnLOP	BnSIZE	BnNDF	BnRDIS	BnRFI	BnUNEQ	BnSLER
03B 06B 09B 0CB	R	BnAIS	BnLOP	BnSIZE	BnNDF	BnRDIS	BnRFI	BnUNEQ	BnSLER
03C 06C 09C 0CC	R	BnPJ Counter				BnNJ Counter			
03D 06D 09D 0CD	R	BnBIP2 Error Counter							
03E 06E 09E 0CE	R	BnFEBE Counter							
03F 06F 09F 0CF	R	Unused					Bn Rx Label		
05E 08E 0BE 0EE	R(L)	BnRDIP	BnRDIC	Unused (00)		BnJ2LOL	BnJ2TIM	Unused (00)	
05F 08F 0BF 0EF	R	BnRDIP	BnRDIC	Unused (00)		BnJ2LOL	BnJ2TIM	Unused (00)	
040 070 0A0 0D0	R	Unused							
041 071 0A1 0D1	R	Unused							
042 072 0A2 0D2	R	Bn Receive K4 (Z7) Byte							
043 073 0A3 0D3	R	Bn Receive O-Bits							
05C 08C 0BC 0EC	R(L)	BnTCUQ	BnTCAIS	BnTCLM	BnTCLL	BnTCTM	BnTCODI	BnTCRDI	0
05D 08D 0BD 0ED	R	BnTCUQ	BnTCAIS	BnTCLM	BnTCLL	BnTCTM	BnTCODI	BnTCRDI	0
180 280 380 480	R	Bn TC BIP-2 Error Counter							
181 281 381 481	R	Bn TC REI Counter							
182 282 382 482	R	Bn TC OEI Counter							
196 296 396 496	R	Bn Receive V4 Byte							

STATUS REGISTERS - PORT n (A AND B SIDES)

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
044 074 0A4 0D4	R(L)	RnFFE	0	ANAnOOL	TAnFE	TBnFE	TnLOS	TnLOC	TnDAIS
045 075 0A5 0D5	R	RnFFE	0	ANAnOOL	TAnFE	TBnFE	TnLOS	TnLOC	TnDAIS
046 076 0A6 0D6	R	Port n HDB3 Coding Errors (Low Byte)							
047 077 0A7 0D7	R	Port n HDB3 Coding Errors (High Byte)							

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

OPERATIONS (CONTROL) REGISTERS - PORT n

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
048 078 0A8 0D8	R/W	Unused (set to 000)			1BnRDI	J2nTEN	J2nSIZE	J2nCOM	J2nAISE
050 080 0B0 0E0	R/W	FnLBK	LnLBK	RnAIS	TnAIS	TnVTAIS	TnRFI	TnRDIS	TnRDIP
051 081 0B1 0E1	R/W	TCnRDI	TCnODI	TCnAIS	TCnEN	TCnRE	TCnOE	TCnAEN	TnRDIC
052 082 0B2 0E2	W	RnSETS	RnSETC	Unused (set to 0000)				TnFB2	TnFFB
053 083 0B3 0E3	R/W	Unused (set to 00000)					An µP Mismatch Label		
054 084 0B4 0E4	R/W	Unused (set to 00000)					Bn µP Mismatch Label		
055 085 0B5 0E5	R/W	Unused (set to 00000)					Tn TX Label		
056 086 0B6 0E6	R/W	Unused							
057 087 0B7 0E7	R/W	Unused							
058 088 0B8 0E8	R/W	Transmit K4 (Z7) Byte Value (4-7)				Unused (set to 000)			TZ7BV(0)
059 089 0B9 0E9	R/W	Transmit O-Bits - Port n							
511 591 611 691	R/W	Transmit V4 Bytes - Port n							

J2 AND N2 (Z6) MESSAGE SEGMENTS - PORT n

Address Port 1, 2, 3, 4	Status*	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
140 240 340 440 to 17F 27F 37F 47F	R/W	Port n A side J2 64-byte trace message received (X40 - X7F) or A side J2 16-byte trace message received (X40 - X4F) A side J2 16-byte microprocessor-written trace message (X50 - X5F) A side TC (N2 (Z6)) 16-byte trace message received (X60 - X6F) A side TC (N2 (Z6)) 16-byte microprocessor-written trace message (X70 - X7F)							
1C0 2C0 3C0 4C0 to 1FF 2FF 3FF 4FF	R/W	Port n B side J2 64-byte trace message received (XC0 - XFF) or B side J2 16-byte trace message received (XC0 - XCF) B side J2 16-byte microprocessor-written trace message (XD0 - XDF) B side TC (N2 (Z6)) 16-byte trace message received (XE0 - XEF) B side TC (N2 (Z6)) 16-byte microprocessor-written trace message (XF0 - XFF)							
540 5C0 640 6C0 to 57F 5FF 67F 6FF	R/W	Port n J2 64-byte trace message transmitted (540 - 57F Port 1, 5C0 - 5FF Port 2, 640 - 67F Port 3, 6C0 - 6FF Port 4) or J2 16-byte trace message transmitted (540-54F Port 1, 5C0-5CF Port 2, 640-64F Port 3, 6C0-6CF Port 4) TC (N2 (Z6)) 16-byte trace message transmitted (560-56F Port 1, 5E0-5EF Port 2, 660-66F Port 3, 6E0-6EF Port 4)							

Where X = 1 for Port 1, 2 for Port 2, 3 for Port 3, 4 for Port 4.

* R=Read Only; R(L)=Read Only (Latched); R/W=Read/Write; W=Write Only.

MEMORY MAP DESCRIPTIONS

COMMON REGISTERS - PROGRAM ID

Address	Bit	Symbol	Description
6BD	7-0	PID-CHK	This value (register 6BEH + register 6BFH + 0x55) is written by SPOT during initialization, and at the start of each maintenance cycle (2 kHz rate). The external microprocessor can read this checksum to validate the revision numbers in registers 6BEH and 6BFH. By writing this location with a different value, waiting at least 1 ms, and then reading this location, the external microprocessor can determine whether the SPOT program is running.
6BE	7-0	PGMRV1*	Part 1 of two-part program release number.
6BF	7-0	PGMRV2*	Part 2 of two-part program release number.

* Registers 6BEH and 6BFH contain the two-part SPOT program release number. In documentation, this number is written as “PGMRV1, PGMRV2”.

COMMON REGISTERS - INTERNAL PROCESSOR (SPOT)

Address	Bit	Symbol	Description
005	7-0		**TranSwitch Test Register:** These bits must be written to 0.
006	7-0	SPOTPCLD	**Internal SPOT Processor Load Register:** These bits are the lower 8 bits of the 11-bit register which is used as the offset address access for the SPOT Instruction RAM. During normal operation these bits must be written to 0.
007	7	RPSPOT	**Reprogram Internal SPOT Processor Control Bit:** This bit is written to 1 for accessing the SPOT Instruction RAM. During normal operation this bit must be written to 0.
	6-3		**TranSwitch Test Bits:** These bits must be written to 0.
	2-0	SPOT PC Load	**Internal SPOT Processor Load Register:** These bits are the upper 3 bits of the 11-bit register which is used as the offset address access for the SPOT Instruction RAM. During normal operation these bits must be written to 0.
008	7-0		**TranSwitch Test Register**: These bits must be written to 0.

COMMON REGISTERS - CONTROL DESCRIPTIONS

Address	Bit	Symbol	Description
010	7 6	MOD1 MOD0	**Format Selection:** The format selection is made according to the table given below. MOD1 MOD0 Format Selected 0 0 STS-1 Format 0 1 STS-3 Format 1 0 STM-1/AU-3 Format 1 1 STM-1/TUG-3/VC-4 Format
	5	AAHZE	**A Add Bus High Impedance Enable:** A 1 forces the A-side add bus data output to a high impedance state. Upon power-up, or on a hardware or software reset, this bit is set to a 1. Note: For normal bus operation this bit position must be written with a 0. See Note 1.
	4	BAHZE	**B Add Bus High Impedance Enable:** A 1 forces the B-side add bus data output to a high impedance state. Upon power-up, or on a hardware or software reset, this bit is set to a 1. Note: For normal bus operation this bit position must be written with a 0. See Note 1
	3	BLOCK	**Block Count:** A 1 enables two BIP-2 errors to be counted as a single error (block) for the BIP-2 performance counters (V5 and K4 (Z7) bytes). A 0 enables two BIP-2 errors to be counted as two errors.
	2 1 0	NPIA NPIB NPIC	**Null Pointer Indicator Selection:** A 1 enables a null pointer indicator to be generated for the corresponding TUG-3 when control bits MOD1 and MOD0 are a 1 (STM-1/TUG-3/VC-4 format). A null pointer indicator is carried in the first three bytes of column 1 in a TUG-3. The null pointer indicator byte values are 93H, E0H and 00H. A 0 forces the NPI byte position to a high impedance state on the A/B buses.

Note 1: The add bus will be forced to a high impedance state automatically when loss of clock is detected on the transmit clock signal selected by control bit DBPBT.

Address	Bit	Symbol	Description
011	7	SBTEN	**Software Bus Timing Enable**: This bit works in conjunction with control bit DRPBT in bit 6 and the $\overline{\text{ABUST}}$ lead according to the following table (where X = Don't Care): SBTEN / DRPBT / $\overline{\text{ABUST}}$ / Action 0 / X / Low / Add bus timing selected. Add bus data derived from add bus timing signals. Software control of bus timing disabled. 0 / X / High / Drop bus timing selected. Add bus data derived from like-named drop bus. Software control of bus timing disabled. 1 / 0 / X / Add bus timing selected. Add bus data derived from add bus timing signals. Hardware control of bus timing disabled. 1 / 1 / X / Drop bus timing selected. Add bus data derived from like-named drop bus. Hardware control of bus timing disabled. This SBTEN bit is reset to 0 upon power-up and by a device reset.
	6	DRPBT	**Drop Bus Timing:** Enabled when a 1 is written to control bit SBTEN. A 1 selects the drop bus timing mode, while a 0 selects the add bus timing mode. See table above.
	5	ABD	**Add Bus Delay:** A 0 delays the add bus data with respect to the drop bus by one clock cycle, when the drop bus or add bus timing modes are selected. A 1 delays the add bus data with respect to the drop bus or add bus by one additional clock cycle, for a total of two clock cycles.
	4	LATEN	**Latch On Transitions Enable Bit:** A 0 disables the states of the IPOS and INEG control bits, and causes the event alarm bits (latched alarm bits in the registers) to latch on the positive (1) level of an alarm. A 1 enables the states of the IPOS and INEG control bits in register 012H.
	3	TAISE	**Transmit E1 Line AIS Enable:** A common control for all four ports. A 1 enables an E1 AIS (unframed all ones) to be generated and sent from port n to the SDH/SONET side when an E1 line input loss of signal, or loss of clock, occurs for port n.
	2	TCLKI	**Transmit E1 Line Clock Inversion:** A common control for the four ports. A 0 enables transmit data to be clocked in on the negative (falling) clock edges. A 1 enables transmit data to be clocked in on the positive (rising) clock edges.

Address	Bit	Symbol	Description

011 (cont.)	1	RAISE	**Receive E1 Line AIS Enable:** A common control for the four ports. A 1 enables a receive E1 AIS to be sent from port n when internal defined alarms occur for a port n. An E1 AIS is an unframed all ones signal. For example, receive AIS for port 1 will be generated:
			- When R1SEL is 0 and any of:
			  - Loss of pointer detected (A1LOP)
			  - VT AIS detected (A1AIS)
			  - A Drop Bus Loss Of Clock (ADLOC)
			  - A Drop Bus Upstream AIS detected (AsUAISI) when HEAISE is 1.
			- or when R1SEL is 0 and RAISE is 1 (drop VT from A side) and any of:
			  - A Drop H4 Error (AsDH4E) when DV1SEL is 0
			  - Unequipped signal label (A1UNEQ) and UQAE is 1
			  - Mismatch signal label (A1SLER)
			  - J2 Loss Of Lock Alarm (A1J2LOL) when J21COM and J21AISE are 1, and J21SIZE=0
			  - J2 Mismatch Alarm (A1J2TIM) when J21COM and J21AISE are 1, and J21SIZE=0
			  - TC Unequipped Alarm (A1TCUQ) when TC1EN and TC1AEN are 1
			  - TC Loss Of Lock Alarm (A1TCLL) when TC1EN and TC1AEN are 1
			  - TC Mismatch Alarm (A1TCTM) when TC1EN and TC1AEN are 1
			  - TC Loss Of Multiframe Alarm (A1TCLM) when TC1EN and TC1AEN are 1
			  - TC AIS Detected (A1TCAIS) when TC1EN and TC1AEN are 1.
			- or when R1SEL is a 1 and any of:
			  - Loss of pointer detected (B1LOP)
			  - VT AIS detected (B1AIS)
			  - B Drop Bus Loss Of Clock (BDLOC)
			  - B Drop Bus Upstream AIS detected (BsUAISI) and HEAISE is 1.
			- or when R1SEL is 1 and RAISE is 1 (drop VT from B side) and any of:
			  - B Drop H4 Error (BsDH4E) when DV1SEL is 0
			  - Unequipped signal label (B1UNEQ) and UQAE is 1
			  - Mismatch signal label (B1SLER)
			  - J2 Loss Of Lock Alarm (B1J2LOL) when J21COM and J21AISE are 1, and J21SIZE=0.
			  - J2 Mismatch Alarm (B1J2TIM) when J21COM and J21AISE are 1, and J21SIZE=0
			  - TC Unequipped Alarm (B1TCUQ) when TC1EN and TC1AEN are 1
			  - TC Loss Of Lock Alarm (B1TCLL) when TC1EN and TC1AEN are 1
			  - TC Mismatch Alarm (B1TCTM) when TC1EN and TC1AEN are 1
			  - TC Loss Of Multiframe Alarm (B1TCLM) when TC1EN and TC1AEN are 1
			  - TC AIS Detected (B1TCAIS) when TC1EN and TC1AEN are 1.
			- or when Receive FIFO Error (R1FFE) and RAISE are 1.
			- or when a 1 is written to send receive AIS (R1AIS).
			- or when RTUN1 is invalid.
			The AIS will be sent for one multiframe when a receive FIFO error occurs. The s in AsUAISI, BsUAISI, AsDH4E and BsDH4E represents the STS-1 or TUG in which the TU/VT has been selected, where s = 1-3.

	0	RCLKI	**Receive E1 Line Clock Inversion:** A common control for the four ports. A 0 enables the E1 receive data signal to be clocked out on positive (rising) RCOn clock edges. A 1 causes E1 data to be clocked out on negative (falling) RCOn clock edges.

Address	Bit	Symbol	Description
012	7	ADDI	**Add Indicator Inversion:** A 1 causes the A and B Add bus output indicator signals ($\overline{\text{AADD}}$ and $\overline{\text{BADD}}$) to be active high instead of active low when a time slot is added to the bus.
	6	APE	**A/B Add Bus Even Parity Generated:** A 1 enables even parity to be generated, while a 0 enables odd parity to be generated. Parity is calculated over the data byte only.
	5 4	IPOS INEG	**Interrupt/Event Positive/Negative Alarm Transition Selection:** An event register bit will latch, and a software interrupt indication will occur, according to the transitions given in the table below. The appropriate interrupt mask bit(s) must be set if an interrupt is required. A hardware interrupt occurs when the hardware interrupt bit is also enabled (control bit HDWIE is 1). These bits are disabled when a 0 is written to control bit LATEN. IPOS INEG Action 0 0 No event or interrupt indication 1 0 Event and interrupt on positive alarm transition 0 1 Event and interrupt on negative alarm transition 1 1 Event and interrupt on both positive and negative alarm transitions
	3	RFIE	**RFI Enable:** A common control bit for all four ports. A 1 enables an RFI indication to cause an interrupt. A 0 disables an RFI indication (bit 4 in V5 of the TU/VT) from causing an interrupt.
	2	THRSBY	**Threshold Modulation Disabled:** A 1 disables the threshold modulation capability in each of the four modulation circuits. A 0 enables threshold modulation capability in each of the four modulation circuits.
	1	DPE	**A/B Drop Bus Even Parity Detected:** This bit works in conjunction with the PDDO control bit to determine the parity calculation in the drop direction. DPE PDDO Action (for both A and B buses) 0 0 Odd parity check over drop data, SPE, and C1J1V1. 0 1 Odd parity check over drop data only. 1 0 Even parity check over drop data, SPE, and C1J1V1. 1 1 Even parity check over drop data only. Other than reporting the event, no action is taken upon parity error indication.
	0	PDDO	**A/B Drop Bus Parity Detected on Data Only:** Common control bit for both buses. A 1 causes parity to be calculated over the data byte only. A 0 causes parity to be calculated over the data byte, SPE and C1J1V1 signals. Please refer to the table provided for DPE.

Address	Bit	Symbol	Description
013	7	HEAISE	**A/B H1/H2 or E1 Byte AIS Enable:** Common control for both the A and B Drop buses. A 1 enables an AIS detected in either the SDH/SONET H1/H2 bytes, or in the E1 bytes, to generate a receive E1 line AIS and transmit an RDI (when enabled).
	6	DV1SEL	**Drop Bus V1 Reference Enable:** Common control bit for both buses. In the Drop Bus Timing Mode this bit must be set to zero. In the Add Bus Timing Mode this control bit works in conjunction with the DV1REF control bit according to the following table.
	5	DV1REF	**Drop Bus V1 Reference Enable:** Common control bit for both buses. Enabled when add bus timing is selected. This control bit works in conjunction with the DV1SEL control bit according to the following table: DV1SEL / DV1REF / Action 0 / 0 / Drop side uses H4 multiframe detector to determine V1 pulse Add side uses V1 pulse from add bus C1J1V1 signal 0 / 1 / Drop side uses H4 multiframe detector to determine V1 pulse Add side uses V1 pulse from drop side H4 multiframe detector 1 / 0 / Drop side uses V1 pulse from drop bus C1J1V1 signal Add side uses V1 pulse from add side C1J1V1 signal 1 / 1 / Drop side uses V1 pulse from drop side C1J1V1 signal Add side uses V1 pulse from drop side C1J1V1 signal
	4	RDIEN	**Transmit Remote Defect Indication Enable:** Common control for both buses. This control bit enables incoming receive side (Drop) alarms to generate a Remote Defect Indication in the transmit (Add) direction. This bit also works in conjunction with the control bit 1BnRDI found in the Operations (Control) Registers (048H, 078H, 0A8H, 0D8H). More details of how these control bits function can be found in the Operation Section on Remote Defect Indications.
	3	NULLZ	**Force the NPI Column Unused Bytes to Zero:** A 1 forces to 00H the unused bytes in the column following the NPI bytes when the NPI feature is enabled for the same TUG-3 (NPIA, NPIB or NPIC is a 1). A 0 forces the unused bytes following the NPI to a high impedance state on the A/B buses.
	2	DDIND	**Delay Drop Bus Indication Signal:** A 1 increases the delay of the drop bus indication signals ($\overline{\text{ADIND}}$ and $\overline{\text{BDIND}}$) by one clock cycle.
	1	UQAE	**Unequipped Alarm AIS/RDI/TC Alarm Enable:** A common control for both the A and B Drop buses. A 1 enables a receive E1 line AIS, an RDI and both of the TC alarms (TCnODI, TCnRDI) to be transmitted when an unequipped alarm is detected in either the A or B Drop bus signals.
	0	TOBWZ	**Transmit O-Bit Channel With Zeros:** A common control for all four ports. A 0 enables the microprocessor-written values for the O-bit channel and the unused bits in the K4 (Z7) byte to be transmitted. A 1 forces the O-bit channel and the unused bits in the K4 (Z7) byte to be transmitted as zero for all four ports.

COMMON REGISTERS - PROVISIONING DESCRIPTIONS

Address	Bit	Symbol	Description
014	7-5	Unused	**Unused:** These bits must be written to 0.
	4	UEAME	**Unequipped All Modes Enable:** A 0 enables an unequipped channel or an unequipped supervisory channel to be generated in the Multiplexer Mode only, according to the table given below: Drop / Add / Action A / B / Unequipped or unequipped supervisory channel can be transmitted for the TU/VT selected on the A Bus. B / A / Unequipped or unequipped supervisory channel can be transmitted for the TU/VT selected on the B Bus. A 1 enables an unequipped channel or unequipped supervisory channel to be transmitted only on the active bus for the TU/VT selected. See control bits UCHnE and USCHnE below (Addresses 04A, 07A, 0AA, 0DA) for associated control functions.
	3	SE1AIS	**Select E1AIS:** A 1 disables the TOH H1/H2n AIS detection circuit and enables the AIS detection circuit for the TOH E1n bytes. A 0 enables the AIS detection circuit for the H1/H2n bytes. Here the value of n is 1 for an STM-1 format and 1, 2 or 3 for an AU-3/STS-1 signal.
	2	V5AL10	**V5 Alarm Detection Select 10:** A 1 selects 10 consecutive RDI assertions for detection and recovery. A 0 selects 5 consecutive RDI assertions for detection and recovery.
	1	PTALTE	**Pointer Tracking AIS to LOP Transition Enabled:** A 1 enables the AIS to LOP transition in the pointer tracking state machine, as required by ETSI standards. A 0 will disable the transition, as required by Bellcore and ANSI standards.
	0	HDWIE	**Hardware Interrupt Enable:** A 1 enables the interrupt lead to be activated when an interrupt occurs.
015	7	RESET	**Reset:** A 1 clears to zero all controls, alarms, internal counters and performance counters, sets control bits AAHZE and BAHZE to 1, and re-initializes the receive and transmit FIFOs. This bit is self-clearing, and will reset to 0 after the reset cycle is completed. See Note 1.
	6	RESTAB	**Reset A Side Bus Alarms:** A 1 clears the alarms associated with the A side bus and the LEXTC alarm. This bit is self-clearing, and will reset to 0 after the reset cycle is completed. See Note 2.
	5	RESTBB	**Reset B Side Bus Alarms:** A 1 clears the alarms associated with the B side bus and SPOT alarms. This bit is self-clearing, and will reset to 0 after the reset cycle is completed. See Note 2.
	4	RESTSP	**Reset Internal Processor (SPOT):** A 1 resets the SPOT processor, without affecting its RAM. This bit will reset itself to 0 after the reset cycle is completed. See Note 1.
	3-1	Unused	**Unused:** These bits must be written to 0.
	0	INITSP	**Initialize Internal Processor (SPOT) Data RAM:** A 1 initializes the Data RAM associated with the SPOT processor and resets the general purpose registers of this processor. This bit should only be set to 1 after a hardware reset (lead 155 or C5) or a software reset (control bit RESET above) has been activated. This bit is self-clearing and will reset to 0 after the Data RAM initialization is complete. See Note 1.

Note 1: The control bits RESET, RESTSP and INITSP in address 015H should not be applied simultaneously, but only serially (e.g., 80H followed by 01H, rather than 81H).

Note 2: Control bits RESTAB and RESTBB may be applied at the same time (60H).

COMMON REGISTERS - INTERRUPT INDICATION REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
020	7	INT	**Software Interrupt Indication:** A 1 indicates that a latched alarm has occurred for which the corresponding interrupt mask bit(s) is/are set to 1.
	6	EXTCK	**External Clock Interrupt Indication:** Enabled when a 1 is written into the ECKMSK bit. A 1 indicates that the external clock at input lead EXTCK has failed (i.e., LEXTC=1).
	5	ASIDE	**A Side Interrupt Indication:** Enabled when a 1 is written into the ASMSK bit. A 1 indicates that an alarm has occurred in one of the A-side alarm registers (i.e., 022H and 024H, bits 2, 1 and 0).
	4	BSIDE	**B Side Interrupt Indication:** Enabled when a 1 is written into the BSMSK bit. A 1 indicates that an alarm has occurred in one of the B-side alarm registers (i.e., 026H and 028H, bits 2, 1 and 0).
	3	PORT4	**Port 4 Interrupt Indication:** Enabled when a 1 is written into the P4MSK bit. A 1 indicates that an alarm has occurred in one of the port 4 alarm registers for which the corresponding additional interrupt mask bit is also set to 1 (addresses 017H, 018H and 019H).
	2	PORT3	**Port 3 Interrupt Indication:** Enabled when a 1 is written into the P3MSK bit. A 1 indicates that an alarm has occurred in one of the port 3 alarm registers for which the corresponding additional interrupt mask bit is also set to 1 (addresses 017H, 018H and 019H).
	1	PORT2	**Port 2 Interrupt Indication:** Enabled when a 1 is written into the P2MSK bit. A 1 indicates that an alarm has occurred in one of the port 2 alarm registers for which the corresponding additional interrupt mask bit is also set to 1 (addresses 017H, 018H and 019H).
	0	PORT1	**Port 1 Interrupt Indication:** Enabled when a 1 is written into the P1MSK bit. A 1 indicates that an alarm has occurred in one of the port 1 alarm registers for which the corresponding additional interrupt mask bit is also set to 1 (addresses 017H, 018H and 019H).

COMMON REGISTERS - INTERRUPT MASK DESCRIPTIONS

Address	Bit	Symbol	Description
016	7-1	Unused	**Unused**: These bits must be written to 0.
	0	SPTMSK	**SPOT Status Interrupt Mask:** A 1 enables a hardware interrupt (lead INT/$\overline{IRQ}$) and a software interrupt indication (INT) when a SPOT alarm has occurred in any of the SPOT alarm register bits (address 028H, bits 7, 6 and 4). A 0 disables the SPOT alarms from causing an interrupt. See Note 1.
017	7, 5, 3, 1	RPTnA (n=4-1)	**Receive A Side Status Interrupt Mask Bit:** A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred in an A-side port n alarm register while PnMSK is set for port n. A 0 disables the A side receive alarms for port n from causing an interrupt. See Note 1.
	6, 4, 2, 0	RPTnB (n=4-1)	**Receive B Side Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred in a B-side port n alarm register while PnMSK is set for port n. A 0 disables the B side receive alarms for port n from causing an interrupt**.** See Note 1.
018	7, 5, 3, 1	TFIFOnA (n=4-1)	**Transmit FIFO Error A Side Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for an A-side port n transmit FIFO while PnMSK is set for port n. A 0 disables a transmit FIFO error A side alarm for port n from causing an interrupt. See Note 1.
	6, 4, 2, 0	TFIFOnB (n=4-1)	**Transmit FIFO Error B Side Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for a B-side port n transmit FIFO while PnMSK is set for port n. A 0 disables a transmit FIFO error B side alarm for port n from causing an interrupt. See Note 1.
019	7, 6, 5, 4	TPORTn (n=4-1)	**Transmit Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for one of the port n transmit alarms while PnMSK is set for port n. A 0 disables a transmit alarm from causing an interrupt. See Note 1.
	3, 2, 1, 0	RFIFOn (n=4-1)	**Receive FIFO Error Status Interrupt Mask Bit**: A 1 enables a hardware interrupt and software interrupt indication (INT) when an alarm has occurred for a port n receive FIFO while PnMSK is set for port n. A 0 disables a receive FIFO error alarm for port n from causing an interrupt. See Note 1.

Note 1: Please refer to the tables in the Operation - Interrupt Structure section for the specific alarms and register locations to which these interrupt masks apply. RPTnA or RPTnB is not required to be set to 1 to enable an interrupt for AnRFI or BnRFI alarms. Control bit HDWIE must be set to 1 if a hardware interrupt is required.

Address	Bit	Symbol	Description
021	7	Unused	**Unused:** This bit must be written to 0.
	6	ECKMSK	**External Clock Interrupt Mask Bit:** A 1 enables a hardware interrupt and software interrupt indications (INT and ETXCK) when an external clock failure alarm has occurred. See Note 1.
	5	ASMSK	**A Side Interrupt Mask Bit**: A 1 enables the A Side Interrupt Indication (ASIDE). See Note 1.
	4	BSMSK	**B Side Interrupt Mask Bit:** A 1 enables the B Side Interrupt Indication (BSIDE). See Note 1.
	3	P4MSK	**Port 4 Interrupt Mask Bit**: A 1 enables the Port 4 Interrupt Indication (PORT4). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 4, when the corresponding RPT4A, RPT4B, TFIFO4A, TFIFO4B, RFIFO4 or TPORT4 mask bit is set to 1. See Note 1.
	2	P3MSK	**Port 3 Interrupt Mask Bit**: A 1 enables the Port 3 Interrupt Indication (PORT3). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 3, when the corresponding RPT3A, RPT3B, TFIFO3A, TFIFO3B, RFIFO3 or TPORT3 mask bit is set to 1. See Note 1.
	1	P2MSK	**Port 2 Interrupt Mask Bit**: A 1 enables the Port 2 Interrupt Indication (PORT2). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 2, when the corresponding RPT2A, RPT2B, TFIFO2A, TFIFO2B, RFIFO2 or TPORT2 mask bit is set to 1. See Note 1.
	0	P1MSK	**Port 1 Interrupt Mask Bit**: A 1 enables the Port 1 Interrupt Indication (PORT1). It permits a hardware interrupt and a software interrupt indication (INT) when an alarm has occurred in one of the alarm registers for port 1, when the corresponding RPT1A, RPT1B, TFIFO1A, TFIFO1B, RFIFO1 or TPORT1 mask bit is set to 1. See Note 1.

Note 1: Please refer to the tables in the Operation - Interrupt Structure section for the specific alarms and register locations to which these interrupt masks apply. RPTnA or RPTnB is not required to be set to 1 to enable an interrupt for AnRFI or BnRFI alarms. Control bit HDWIE must be set to 1 if a hardware interrupt is required.

A/B DROP AND ADD BUS - STATUS REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
022	7-0		Same bit definitions as in register 023 hex, except the bits are latched.
023	7	ADLOC	**A Drop Bus Loss Of Clock:** A 1 indicates that the A Drop bus has detected a loss of clock. An alarm occurs when the input drop clock is stuck high or low for 1000 ns +/- 500 ns. Recovery to 0 occurs on the first clock transition. Please note that an alarm will force the add bus data and parity bits to a high impedance state, and will set the add indicator off for the duration of the alarm, when the drop bus timing mode is selected.
	6	AALOC	**A Add Bus Loss Of Clock:** A 1 indicates that the A Add bus has detected a loss of clock, when add bus timing is selected. A loss of clock alarm forces the add bus data and parity bit to a high impedance state, and sets the add indicator off for the duration of the alarm. An alarm occurs when the input add clock is stuck high or low for 1000 ns +/- 500 ns. Recovery to 0 occurs on the first clock transition.
	5	ADPAR	**A Drop Bus Parity Error Detected:** A 1 indicates that an even or odd parity error has been detected in the A Drop bus signals. Other than an alarm indication, no action is taken. Parity is monitored for each drop bus clock cycle.
	4-3	Unused	**Unused:** These bits read out as 0.
	2	A3UAISI	**A Side Received Upstream AIS Indication - AU-3 C/STS-1 No. 3:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 C/STS-1 No. 3. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E13 byte for AU-3 C/STS-1 No. 3. Disabled when the format is an AU-4 VC-4, or STS-1.
	1	A2UAISI	**A Side Received Upstream AIS Indication - AU-3 B/STS-1 No. 2:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 B/STS-1 No. 2. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E12 byte for AU-3 B/STS-1 No. 2. Disabled when the format is an AU-4 VC-4, or STS-1.
	0	A1UAISI	**A Side Received Upstream AIS Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 A/STS-1 No. 1, or in the AU-4 VC-4 signal. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E11 byte for AU-3 A/STS-1 No. 1, AU-4 VC-4, or the STS-1 signal.
024	7-0		Same bit definitions as in register 025 hex, except the bits are latched.

Address	Bit	Symbol	Description
025	7	LEXTC	**Loss Of External Clock:** A 1 indicates an external loss of clock alarm when the external clock (present on lead 138) is stuck high or low for 1000 ns +/- 500 ns. Recovery to 0 occurs on the first clock transition.
	6-3	Unused	**Unused:** These bits read out as 0.
	2	A3DH4E	**A Drop Bus Loss of H4 Indication - AU-3 C/STS-1 No. 3:** Loss of multiframe for AU-3 C/STS-1 No. 3 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.
	1	A2DH4E	**A Drop Bus Loss of H4 Indication - AU-3 B/STS-1 No. 2:** Loss of multiframe for AU-3 B/STS-1 No. 2 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.
	0	A1DH4E	**A Drop Bus Loss of H4 Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** Loss of multiframe for AU-3 A/STS-1 No. 1, AU-4 VC-4 or STS-1 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This bit is forced to 1 at power-up.
026	7-0		Same bit definitions as in register 027 hex, except the bits are latched.

Address	Bit	Symbol	Description
027	7	BDLOC	**B Drop Bus Loss Of Clock:** A 1 indicates that the B Drop bus has detected a loss of clock. An alarm occurs when the input drop clock is stuck high or low for 1000 ns +/- 500 ns. Recovery to 0 occurs on the first clock transition. Please note that an alarm will force the add bus data and parity bits to a high impedance state, and will set the add indicator off for the duration of the alarm, when the drop bus timing mode is selected.
	6	BALOC	**B Add Bus Loss Of Clock:** A 1 indicates that the B Add bus has detected a loss of clock, when add bus timing is selected. A loss of clock alarm forces the add bus data and parity bit to a high impedance state, and sets the add indicator off for the duration of the alarm. An alarm occurs when the input drop clock is stuck high or low for 1000 ns +/- 500 ns. Recovery to 0 occurs on the first clock transition.
	5	BDPAR	**B Drop Bus Parity Error Detected:** A 1 indicates that an even or odd parity error has been detected in the B Drop bus signals. Other than an alarm indication, no action is taken. Parity is monitored for each drop bus clock cycle.
	4-3	Unused	**Unused:** These bits read out as 0.
	2	B3UAISI	**B Side Received Upstream AIS Indication - AU-3 C/STS-1 No. 3:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 C/STS-1 No. 3. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E13 byte for AU-3 C/STS-1 No. 3. Disabled when the format is a AU-4 VC-4, or STS-1.
	1	B2UAISI	**B Side Received Upstream AIS Indication - AU-3 B/STS-1 No. 2:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 B/STS-1 No. 2. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E12 byte for AU-3 B/STS-1 No. 2. Disabled when the format is a AU-4 VC-4, or STS-1
	0	B1UAISI	**B Side Received Upstream AIS Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** When control bit SE1AIS is 0, a 1 indicates that AIS has been detected in the H1/H2 bytes for AU-3 A/STS-1 No. 1, or in the AU-4 VC-4 signal. When control bit SE1AIS is 1, a 1 indicates that AIS has been detected in the E11 byte for AU-3 A/STS-1 No. 1, AU-4 VC-4, or the STS-1 signal.
028	7-0		Same bit definitions as in register 029 hex, except the bits are latched.

Address	Bit	Symbol	Description
029	7	SPTLOC	**Internal Processor (SPOT) Loss of Clock:** The 29.16 MHz clock internally derived from the 58.32 MHz desynchronizer clock input (EXTCK) is monitored for loss of clock. Loss of clock is declared if this clock is stuck high or low for 1000 +/- 500 ns. Recovery to 0 occurs on the first clock transition.
	6	WDTEXP	**Watch Dog Timer Expired:** This bit is set to 1 when the SPOT is unable to service all requests in a timely manner.
	5	Unused	**Unused:** This bits reads out as 0.
	4	PERR	**Parity Error:** This bit is set to 1 when a parity error is detected while reading the Instruction RAM of the SPOT.
	3	Unused	**Unused:** This bits reads out as 0.
	2	B3DH4E	**B Drop Bus Loss of H4 Indication - AU-3 C/STS-1 No. 3:** Loss of multiframe for AU-3 C/STS-1 No. 3 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.
	1	B2DH4E	**B Drop Bus Loss of H4 Indication - AU-3 B/STS-1 No. 2:** Loss of multiframe for AU-3 B/STS-1 No. 2 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This H4 detector is disabled when the format is an AU-4 VC-4, or STS-1. This bit is forced to 1 at power-up.
	0	B1DH4E	**B Drop Bus Loss of H4 Indication - AU-3 A/STS-1 No. 1, AU-4 VC-4, or STS-1:** Loss of multiframe for AU-3 A/STS-1 No. 1, AU-4 VC-4 or STS-1 is declared if one or more H4 values differ from those of a two-bit counter once per multiframe for two consecutive multiframes, when control bit DV1SEL is 0. The received H4 multiframe sequence is 00, 01, 10, and 11. The multiframe detector will continue to operate in a free running mode, but will lock to a new H4 sequence after one multiframe sequence has been received correctly. This bit is forced to 1 at power-up.

PORT n - DESYNCHRONIZER CONTROL REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
049 Port 1 079 Port 2 0A9 Port 3 0D9 Port 4	7-0	Pointer Leak Rate Value	**Desynchronizer Pointer Leak Rate Register - Port n:** The count written into this location is used for the internal leak rate buffer, and represents the average leak rate. A count of one represents 8 frames, or 2 multiframes, in the rate of occurrence of pointer movements from the number of counts read from the positive and negative stuff counters.

PORT n - PROVISIONING REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
04A Port 1 07A Port 2 0AA Port 3 0DA Port 4	7 6 5	TnSEL1 TnSEL0 RnSEL	**Transmit Port n A/B Drop/Add Bus Selection:** The table below lists the selection criteria for the eight available modes of operation of port n: 7 6 5 Operating Mode 0 0 0 A Drop only (Drop) 0 0 1 B Drop only (Drop) 0 1 0 A Drop A Add (Single Unidirectional Ring) 0 1 1 B Drop B Add (Single Unidirectional Ring) 1 0 0 A Drop B Add (Multiplexer) 1 0 1 B Drop A Add (Multiplexer) 1 1 0 A Drop A and B Add (Dual Unidirectional Ring) 1 1 1 B Drop B and A Add (Dual Unidirectional Ring)
	4	UCHnE	**Unequipped Channel for Port n Enabled:** The UCHnE control bit works in conjunction with the USCHnE control bit (in bit position 3) according to the following table: UCHnE USCHnE Action 0 X Normal Operation. 1 0 Unequipped TU/VT generated. An unequipped TU/VT consists of a normal NDF, size bits equal to 10, a fixed pointer equal to 105, and all other bytes equal to 00H. 1 1 Unequipped supervisory TU/VT generated. An unequipped supervisory TU/VT consists of a normal NDF, size bits equal to 10, a fixed pointer equal to 105, and a valid J2 byte. The V5 byte will consist of a valid BIP-2, with the signal label sent as zeros by setting control bit TnTx Label to 0. The N2 (Z6) byte can be sent as zero by setting TCnEN=0 and TxB2DIS=1. The K4 (Z7) byte, bits 1, 2, 3, 4 and 8 can be sent as zeros by setting control bit TOBWZ=1. The RDI bits, V5 bit 8 and K4 (Z7) bits 5, 6 and 7 can be disabled and sent as zeros by setting control bit RDIEN=0. Note: X = don't care (0 or 1).
	3	USCHnE	**Unequipped Supervisory Channel for Port n Enabled:** Works in conjunction with the UCHnE bit according to the table given above.
	2	BYPASn	**Bypass Codec of Port n:** A 1 disables the HDB3 Codec (coder and decoder) of port n for NRZ operation. A 0 enables the HDB3 Codec.
	1	RnEN	**Receive Port n Enable:** A 1 enables the receive data (NRZ or rail) output and clock output for port n when lead QUIETn is low. A 0 forces the data and clock output leads to a high impedance state. The four bits power up as 0 and are reset to 0. A 1 must be written to these control bits to enable the port E1 outputs.
	0	Unused	**Unused:** This bit must be written to 0.

Address	Bit	Symbol	Description
04B Port 1 07B Port 2 0AB Port 3 0DB Port 4	7	ADnEN	**A Side Drop Bus Port n TU/VT Selection Output Enable:** A 1 enables the drop bus $\overline{\text{ADIND}}$ signal output. This signal will be active low for the time slots corresponding to the TU/VT selected for port n.
	6	BDnEN	**B Side Drop Bus Port n TU/VT Selection Output Enable**: A 1 enables the drop bus $\overline{\text{BDIND}}$ signal output. This signal will be active low for the time slots corresponding to the TU/VT selected for port n.
	5	AAnEN	**A Side Add Bus Port n TU/VT Selection Output Enable:** A 1 enables the add bus $\overline{\text{AAIND}}$ signal output. This signal will be active low for the time slots corresponding to the TU/VT selected for port n.
	4	BAnEN	**B Side Add Bus Port n TU/VT Selection Output Enable:** A 1 enables the add bus $\overline{\text{BAIND}}$ signal output. This signal will be active low for the time slots corresponding to the TU/VT selected for port n.
	3	ANAnTx	**PRBS Analyzer Sampling Tx E1 Signal:** A 1 enables the internal PRBS analyzer to sample the Tx E1 signal to be sent to the synchronizer. A 0 enables the internal PRBS analyzer to sample the E1 signal to be sent to the Rx E1 ports.
	2	ANAnEN	**PRBS Analyzer Enable:** A1 enables the internal 2^{15}-1 PRBS analyzer. A 0 disables the analyzer.
	1	PRBSnEN	**PRBS Generator Enable:** A 1 enables the internal 2^{15}-1 PRBS generator. A 0 disables the generator.
	0	FRDISn	**FEBE and RDI Disabled For Port n:** Enabled when the single unidirectional mode (control bits TnSEL1, TnSEL0 are equal to 01) is selected. A 1 disables receive side alarms or an out of range condition from generating an RDI. In addition, the REI (FEBE) value is transmitted as a zero.
04C Port 1 07C Port 2 0AC Port 3 0DC Port 4	7	Unused	**Unused:** This bit must be written to 0.
	6-0	RTUNn	**Receive TU/VT Selection for Port n:** The seven-bit binary code written into this location selects the TU/VT that is to be dropped from the A and/or B-side drop bus. Control bits TSEL1, TSEL0 and RSEL determine the drop bus(es) that the data is dropped from. If no TU/VT is selected, the microprocessor should either write a 1 to control bit RnAIS, thereby forcing an E1 AIS, or should write a 0 to RnEN, which will tristate the port n data and clock output leads. Also, the FEBE and RDI values are transmitted as zero.
04D Port 1 07D Port 2 0AD Port 3 0DD Port 4	7	Unused	**Unused:** This bit must be written to 0.
	6-0	TTUNn	**Transmit TU/VT Selection for Port n:** The seven-bit binary code written into this location selects the TU/VT that is to be added to the A and/or B-side add bus. Control bits TSEL1, TSEL0 and RSEL determine the add bus(es) that the data is added to. If no TU/VT is selected, the A or B add bus will tristate.
0F1	7-4	Unused	**Unused:** These bits must be written to 0.
	3	V4EN	**V4EN:** A 1 enables the V4 access function in both receive and transmit directions.
	2-0	Unused	**Unused:** These bits must be written to 0.

Address	Bit	Symbol	Description
0F5	7	TxB2DIS	**Transmit BIP-2 Disable (Test Bit):** A 0 is used for normal operation and will allow the calculated N2 (Z6) BIP-2 and V5 BIP-2 values to be transmitted. A 1 will disable N2 (Z6) BIP-2 calculation as well as V5 BIP-2 calculation for all 4 ports and output zeros in its place.
	6-0	Unused	**Unused:** These bits must be written to 0.

PORT n - RECEIVE STATUS REGISTER AND COUNTER DESCRIPTIONS

The following descriptions pertain to the status registers and counters assigned to Port n. The status registers provide two readable bit positions per alarm. One bit (in an odd-numbered address) indicates the detected alarm as unlatched. The second bit (in the preceding even-numbered address) provides the alarm status as an latched alarm indication. A latched bit position is set on positive, negative, or both positive and negative transitions of the alarm, or on a positive level of the alarm. A latched alarm is cleared on a microprocessor read cycle of its address. During a read cycle for a counter, internal logic holds any increment to the counter until the read cycle is complete, and then updates the counter afterwards.

Address	Bit	Symbol	Description
030 Port 1 060 Port 2 090 Port 3 0C0 Port 4	7-0	Latched An Alarms	Same alarms as the unlatched indications in the following address locations (7-0), except that these alarm states are latched.
031 Port 1 061 Port 2 091 Port 3 0C1 Port 4	7	AnAIS	**A Drop Bus Port n TU/VT AIS Alarm:** A 1 indicates that an AIS has been detected in the V1/V2 pointer bytes for the TU/VT selected.
	6	AnLOP	**A Drop Bus Port n Loss Of TU/VT Pointer Alarm:** A 1 indicates that a loss of pointer has been detected in the V1/V2 pointer bytes for the TU/VT selected.
	5	AnSIZE	**A Drop Bus Port n TU/VT Pointer Size Error Indication:** A 1 indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) is not 10 for the TU/VT selected. The detection and recovery time is immediate.
	4	AnNDF	**A Drop Bus Port n New Data Flag Indication:** A 1 indicates that a New Data Flag (1001 or 0001/1101/1011/1000) has been detected in the V1 pointer byte for the TU/VT selected (i.e., bits 1-4 in the V1 byte are the inverse of the normal 0110 pattern or differ in only one bit, with a correct size indicator and a valid pointer value).
	3	AnRDIS	**A Drop Bus Port n Remote Server Defect Indication:** A 1 indicates that either a remote server defect alarm has been detected (bits 5, 6 and 7 in K4 (Z7) byte are equal to 101), or an RDI has been detected coming from older equipment (bit 8 in V5 byte equals 1 when bits 6 and 7 in K4 (Z7) byte are equal to 00 or 11). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	2	AnRFI	**A Drop Bus Port n Remote Failure Indication:** A 1 indicates that bit 4 in the V5 byte is equal to 1 for the TU/VT selected. The detection and recovery time is immediate.

Address	Bit	Symbol	Description
031 Port 1 061 Port 2 091 Port 3 0C1 Port 4 (cont.)	1	AnUNEQ	**A Drop Bus Port n Unequipped Indication:** A 1 indicates that an Unequipped status has been detected in the V5 signal label (Bits 5-7 in V5 byte = 0) for the TU/VT selected in the A side drop bus. An unequipped signal label is equal to 000. Five or more consecutive received unequipped signal labels will cause this alarm. Recovery occurs when five or more consecutive signal labels are received not equal to 000.
	0	AnSLER	**A Drop Bus Port n Signal Label Mismatch Indication:** A 1 indicates that the receive signal label (Bits 5-7 in V5 byte) does not match the microprocessor-written signal label in the TU/VT selected for the A side drop bus. Five or more consecutive signal label mismatches (against the microprocessor-written value), or received labels not equal to 001, results in an alarm. Recovery occurs upon receipt of five or more consecutive correct signal labels, or 001 values.
032 Port 1 062 Port 2 092 Port 3 0C2 Port 4	7-4	AnPJ Counter	**A Drop Bus Port n Positive Pointer Justification Counter:** A four-bit counter that increments on a positive pointer movement for the TU/VT selected. The counter saturates at full count and is cleared when it is read.
	3-0	AnNJ Counter	**A Drop Bus Port n Negative Pointer Justification Counter:** A four-bit counter that increments on a negative pointer movement for the TU/VT selected. The counter saturates at full count and is cleared when it is read.
033 Port 1 063 Port 2 093 Port 3 0C3 Port 4	7-0	AnBIP2 Counter	**A Drop Bus Port n BIP-2 Counter:** An 8-bit counter which counts the number of BIP-2 errors detected for the TU/VT selected. A maximum of two errors can occur each frame. These two errors cause a single count if the BLOCK control bit is set to 1. The counter saturates at full count and is cleared when it is read.
034 Port 1 064 Port 2 094 Port 3 0C4 Port 4	7-0	AnFEBE Counter	**A Drop Bus Port n FEBE Counter:** An 8-bit counter which counts the number of FEBE errors received (Bit 3 in V5 byte = 1) for the TU/VT selected. The counter saturates at full count and is cleared when it is read.
035 Port 1 065 Port 2 095 Port 3 0C5 Port 4	7-3	Unused	**Unused:** These bits read out as indeterminate.
	2-0	An Rx Label	**A Drop Bus Port n Received Signal Label**: These three bit positions correspond to the three signal label bits in bits 5 through 7 of the V5 byte in the TU/VT selected. This location is updated every 500 microseconds. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor-written mismatch signal label bits for an unequipped and mismatch indication. Code 1 (001) has been implemented in hardware and does not have to be written into this location.
04E Port 1 07E Port 2 0AE Port 3 0DE Port 4	7-6	Latched An Alarms	Same alarms as the corresponding address 04F, 07F, 0AF, 0DF bit positions, except that these alarms are latched.
	5-4	Unused	**Unused:** These bits read out as zero.
	3-2	Latched An Alarms	Same alarms as the corresponding address 04F, 07F, 0AF, 0DF bit positions, except that these alarms are latched.
	1-0	Unused	**Unused:** These bits read out as zero.

Address	Bit	Symbol	Description
04F Port 1 07F Port 2 0AF Port 3 0DF Port 4	7	AnRDIP	**A Drop Bus Port n Remote Payload Defect Indication:** A 1 indicates that a remote payload defect alarm has been detected (bits 5, 6 and 7 in K4 (Z7) byte are equal to 010). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	6	AnRDIC	**A Drop Bus Port n Remote Connectivity Defect Indication:** A 1 indicates that a remote connectivity defect alarm has been detected (bits 5, 6 and 7 in K4 (Z7) byte are equal to 110). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	5-4	Unused	**Unused:** These bits read out as zero.
	3	AnJ2LOL	**A Drop Bus Port n J2 Loss Of Lock Alarm:** Enabled when control bit J2nSIZE is a 0, and control bit J2nCOM is a 1. A 1 indication occurs when the alignment of the 16-byte J2 trace identifier label (message) has not been established.
	2	AnJ2TIM	**A Drop Bus Port n J2 Trail Trace Mismatch Alarm:** Enabled when control bit J2nSIZE is a 0, and control bit J2nCOM is a 1. A 1 indicates that the stable 16-byte message did not match for one message time. Recovery occurs when the J2 state machine loses lock and then acquires lock with a 16-byte stable J2 message that matches the J2 comparison message written by the microprocessor.
	1-0	Unused	**Unused:** These bits read out as zero.
038 Port 1 068 Port 2 098 Port 3 0C8 Port 4	7-0	An Receive K4 (Z7) Byte	**A Drop Bus Port n Receive K4 (Z7) Byte**: The eight bits in this register position correspond to the K4 (Z7) byte received in the TU/VT selected. Bit 7 corresponds to bit 1 in the K4 (Z7) byte.
039 Port 1 069 Port 2 099 Port 3 0C9 Port 4	7-0	An Receive O-Bits	**A Drop Bus Port n Receive O-bits**: The two nibbles (bits 7-4 and 3-0) in this register correspond to the two sets of four overhead communication bits received in the TU/VT selected. Bit 7 corresponds to bit 3 in the second justification control byte, while bit 0 corresponds to bit 6 in the first justification control byte. The two nibbles written into this register location will be from the same frame.
05A Port 1 08A Port 2 0BA Port 3 0EA Port 4	7-1	Latched An Alarms	Same alarms as the following address locations (7-1), except that these alarm states are latched.
	0	Unused	**Unused:** This bit reads out as indeterminate.

Address	Bit	Symbol	Description
05B Port 1 08B Port 2 0BB Port 3 0EB Port 4	7	AnTCUQ	**A Drop Bus Port n Tandem Connection Unequipped Alarm:** A TC unequipped alarm indication (a 1) occurs when bits 3 through 8 in the N2 (Z6) byte are all equal to 0 for 5 or more consecutive frames. Recovery to 0 occurs when bits 3 through 8 are not all equal to 0 for 5 or more consecutive frames.
	6	AnTCAIS	**A Drop Bus Port n Tandem Connection AIS Alarm:** A TC AIS alarm indication (a 1) occurs when bit 4 in the N2 (Z6) byte is equal to 1 for five or more consecutive frames. Recovery to 0 occurs when bit 4 is a 0 for five or more consecutive frames.
	5	AnTCLM	**A Drop Bus Port n Tandem Connection Loss Of Multiframe Alarm:** A TC loss of multiframe alarm indication (a 1) occurs when four or more consecutive errored multiframes are detected in bits 7 and 8 in the N2 (Z6) byte. Recovery to 0 occurs when three consecutive non-errored multiframes (1111 1111 1111 1110) are detected.
	4	AnTCLL	**A Drop Bus Port n Bus Tandem Connection Trail Trace Message Loss Of Lock Alarm:** An alarm indication (a 1) occurs when the alignment of the 16-byte N2 (Z6) Tandem Connection Trace identifier label (message) has not been established.
	3	AnTCTM	**A Drop Bus Port n Bus Tandem Connection Trail Trace Message Mismatch Alarm:** An alarm indication (a 1) indicates that the stable Tandem Connection 16-byte message did not match for one message time. Recovery to 0 occurs when the N2 (Z6) byte TC message state machine loses lock and then acquires lock with a 16-byte stable N2 (Z6) byte message that matches the N2 (Z6) byte comparison message written by the microprocessor.
	2	AnTCODI	**A Drop Bus Port n Tandem Connection ODI Alarm:** A TC ODI alarm indication (a 1) occurs when N2 (Z6) byte bit 7 in frame 74 is equal to 1 for five or more consecutive frames. Recovery to 0 occurs when bit 7 is a 0 for five or more consecutive frames.
	1	AnTCRDI	**A Drop Bus Port n Tandem Connection RDI Alarm:** A TC RDI alarm indication (a 1) occurs when N2 (Z6) byte bit 8 in frame 73 is equal to 1 for five or more consecutive frames. Recovery to 0 occurs when bit 8 is a 0 for five or more consecutive frames.
	0	Unused	**Unused:** This bit reads out as indeterminate.
100 Port 1 200 Port 2 300 Port 3 400 Port 4	7-0	An TC BIP-2 Error Counter	**A Drop Bus Port n Tandem Connection BIP-2 Counter:** An 8-bit counter which counts the number of BIP-2 errors detected in the N2 (Z6) byte for the TU/VT selected when the tandem connection feature is enabled. A maximum of two errors can be counted each frame. These two errors cause a single count if the BLOCK control bit is set to 1. The counter saturates at full count and is cleared when it is read.
101 Port 1 201 Port 2 301 Port 3 401 Port 4	7-0	An TC REI Error Counter	**A Drop Bus Port n Tandem Connection REI Counter:** An 8-bit counter which counts the number of REI errors detected in bit 5 in the N2 (Z6) byte for the TU/VT selected when the tandem connection feature is enabled. The counter saturates at full count and is cleared when it is read.

Address	Bit	Symbol	Description
102 Port 1 202 Port 2 302 Port 3 402 Port 4	7-0	An TC OEI Error Counter	**A Drop Bus Port n Tandem Connection OEI Counter:** An 8-bit counter which counts the number of OEI errors detected in bit 6 in the N2 (Z6) byte for the TU/VT selected when the tandem connection feature is enabled. The counter saturates at full count and is cleared when it is read.
116 Port 1 216 Port 2 316 Port 3 416 Port 4	7-0	An Receive V4 Byte	**A Drop Bus Port n Receive V4 Byte:** When control bit V4EN is 1, the eight bits in this register position correspond to the V4 byte received in the TU/VT selected. Bit 7 corresponds to bit 1 in the V4 byte.
03A Port 1 06A Port 2 09A Port 3 0CA Port 4	7-0	Latched Bn Alarms	Same alarms as the following address locations (7-0), except that these alarm states are latched.
03B Port 1 06B Port 2 09B Port 3 0CB Port 4	7	BnAIS	**B Drop Bus Port n TU/VT AIS Alarm:** A 1 indicates that an AIS has been detected in the V1/V2 pointer bytes for the TU/VT selected.
	6	BnLOP	**B Drop Bus Port n Loss Of TU/VT Pointer Alarm:** A 1 indicates that a loss of pointer has been detected in the V1/V2 pointer bytes for the TU/VT selected.
	5	BnSIZE	**B Drop Bus Port n TU/VT Pointer Size Error Indication:** A 1 indicates that the receive size indicator in the pointer (Bits 5 and 6 in the V1 pointer byte) is not 10 for the TU/VT selected. The detection and recovery time is immediate.
	4	BnNDF	**B Drop Bus Port n New Data Flag Indication:** A 1 indicates that a New Data Flag (1001 or 0001/1101/1011/1000) has been detected in the V1 pointer byte for the TU/VT selected (i.e., bits 1-4 in the V1 byte are the inverse of the normal 0110 pattern or differ in only one bit, with a correct size indicator and a valid pointer value).
	3	BnRDIS	**B Drop Bus Port n Remote Server Defect Indication:** A 1 indicates that either a remote server defect alarm has been detected (bits 5, 6 and 7 in K4 (Z7) byte are equal to 101), or an RDI has been detected coming from older equipment (bit 8 in V5 byte equals 1 when bits 6 and 7 in K4 (Z7) byte are equal to 00 or 11). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	2	BnRFI	**B Drop Bus Port n Remote Failure Indication:** A 1 indicates that bit 4 in the V5 byte is equal to 1 for the TU/VT selected. The detection and recovery time is immediate.

Address	Bit	Symbol	Description
03B Port 1 06B Port 2 09B Port 3 0CB Port 4 (cont.)	1	BnUNEQ	**B Drop Bus Port n Unequipped Indication:** A 1 indicates that an Unequipped status has been detected in the V5 signal label (Bits 5-7 in V5 byte = 0) for the TU/VT selected in the B side drop bus. An unequipped signal label is equal to 000. Five or more consecutive received unequipped signal labels will cause this alarm. Recovery occurs when five or more consecutive signal labels are received not equal to 000.
	0	BnSLER	**B Drop Bus Port n Signal Label Mismatch Indication:** A 1 indicates that the receive signal label (Bits 5-7 in V5 byte) does not match the microprocessor-written signal label in the TU/VT selected for the B side drop bus. Five or more consecutive signal label mismatches (against the microprocessor-written value), or received labels not equal to 001, results in an alarm. Recovery occurs upon receipt of five or more consecutive correct signal labels, or 001 values.
03C Port 1 06C Port 2 09C Port 3 0CC Port 4	7-4	BnPJ Counter	**B Drop Bus Port n Positive Pointer Justification Counter:** A four-bit counter that increments on a positive pointer movement for the TU/VT selected. The counter saturates at full count and is cleared when it is read.
	3-0	BnNJ Counter	**B Drop Bus Port n Negative Pointer Justification Counter:** A four-bit counter that increments on a negative pointer movement for the TU/VT selected. The counter saturates at full count and is cleared when it is read.
03D Port 1 06D Port 2 09D Port 3 0CD Port 4	7-0	BnBIP2 Counter	**B Drop Bus Port n BIP-2 Counter:** An 8-bit counter which counts the number of BIP-2 errors detected for the TU/VT selected. A maximum of two errors can occur each frame. These two errors cause a single count if the BLOCK control bit is set to 1. The counter saturates at full count and is cleared when it is read.
03E Port 1 06E Port 2 09E Port 3 0CE Port 4	7-0	BnFEBE Counter	**B Drop Bus Port n FEBE Counter:** An 8-bit counter which counts the number of FEBE errors received (Bit 3 in V5 byte = 1) for the TU/VT selected. The counter saturates at full count and is cleared when it is read.
03F Port 1 06F Port 2 09F Port 3 0CF Port 4	7-3	Unused	**Unused:** These bits read out as indeterminate.
	2-0	Bn RX Label	**B Drop Bus Port n Received Signal Label:** These three bit positions correspond to the three signal label bits located in bits 5 through 7 of the V5 byte for the TU/VT selected. This location is updated every 500 microseconds. Bit 2 corresponds to bit 7 in the V5 byte. These bits are also compared against the microprocessor-written mismatch signal label bits for an unequipped and mismatch indication. Code 1 (001) has been implemented in hardware and does not have to be written into this location.
05E Port 1 08E Port 2 0BE Port 3 0EE Port 4	7-6	Latched Bn Alarms	Same alarms as the corresponding address 05F, 08F, 0BF, 0EF bit positions except that these alarms are latched.
	5-4	Unused	**Unused:** These bits read out as zero.
	3-2	Latched Bn Alarms	Same alarms as the corresponding address 05F, 08F, 0BF, 0EF bit positions except that these alarms are latched.
	1-0	Unused	**Unused:** These bits read out as zero.

Address	Bit	Symbol	Description
05F Port 1 08F Port 2 0BF Port 3 0EF Port 4	7	BnRDIP	**B Drop Bus Port n Remote Payload Defect Indication:** A 1 indicates that a remote payload defect alarm has been detected (bits 5, 6 and 7 in K4 (Z7) byte are equal to 010). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	6	BnRDIC	**B Drop Bus Port n Remote Connectivity Defect Indication:** A 1 indicates that a remote connectivity defect alarm has been detected (bits 5, 6 and 7 in K4 (Z7) byte are equal to 110). The number of consecutive events used for detection and recovery is determined by control bit V5AL10.
	5-4	Unused	**Unused:** These bits read out as zero.
	3	BnJ2LOL	**B Drop Bus Port n J2 Loss Of Lock Alarm:** Enabled when control bit J2nSIZE is a 0, and control bit J2nCOM is a 1. A 1 indication occurs when the alignment of the 16-byte J2 trace identifier label (message) has not been established.
	2	BnJ2TIM	**B Drop Bus Port n J2 Trail Trace Mismatch Alarm:** Enabled when control bit J2nSIZE is a 0, and control bit J2nCOM is a 1. A 1 indicates that the stable 16-byte message did not match for one message time. Recovery occurs when the J2 state machine loses lock and then acquires lock with a 16-byte stable J2 message that matches the J2 comparison message written by the microprocessor.
	1-0	Unused	**Unused:** These bits read out as zero.
042 Port 1 072 Port 2 0A2 Port 3 0D2 Port 4	7-0	Bn Receive K4 (Z7) Byte	**B Drop Bus Port n Receive K4 (Z7) Byte:** The eight bits in this register position correspond to the K4 (Z7) byte received for the TU/VT selected. Bit 7 corresponds to bit 1 in the K4 (Z7) byte.
043 Port 1 073 Port 2 0A3 Port 3 0D3 Port 4	7-0	Bn Receive O-Bits	**B Drop Bus Port n Receive O-bits:** The two nibbles (bits 7-4 and 3-0) in this register correspond to the two sets of four overhead communication bits received in the TU/VT selected. Bit 7 corresponds to bit 3 in the second justification control byte, while bit 0 corresponds to bit 6 in the first justification control byte. The two nibbles written into this register location will be from the same frame.
05C Port 1 08C Port 2 0BC Port 3 0EC Port 4	7-1	Latched Bn Alarms	Same alarms as the following address locations (7-1), except that these alarm states are latched.
	0	Unused	**Unused:** This bit reads out as indeterminate.

Address	Bit	Symbol	Description
05D Port 1 08D Port 2 0BD Port 3 0ED Port 4	7	BnTCUQ	**B Drop Bus Port n Tandem Connection Unequipped Alarm:** A TC unequipped alarm indication (a 1) occurs when bits 3 through 8 in the N2 (Z6) byte are all equal to 0 for 5 or more consecutive frames. Recovery to 0 occurs when bits 3 through 8 are not all equal to 0 for 5 or more consecutive frames.
	6	BnTCAIS	**B Drop Bus Port n Tandem Connection AIS Alarm:** A TC AIS alarm indication (a 1) occurs when bit 4 in the N2 (Z6) byte is equal to 1 for five or more consecutive frames. Recovery to 0 occurs when bit 4 is a 0 for five or more consecutive frames.
	5	BnTCLM	**B Drop Bus Port n Tandem Connection Loss Of Multiframe Alarm:** A TC loss of multiframe alarm indication (a 1) occurs when four or more consecutive errored multiframes are detected in bits 7 and 8 in the N2 (Z6) byte. Recovery to 0 occurs when three consecutive non-errored multiframes (1111 1111 1111 1110) are detected.
	4	BnTCLL	**B Drop Bus Port n Bus Tandem Connection Trail Trace Message Loss Of Lock Alarm:** An alarm indication (a 1) occurs when the alignment of the 16-byte N2 (Z6) Tandem Connection Trace identifier label (message) has not been established.
	3	BnTCTM	**B Drop Bus Port n Bus Tandem Connection Trail Trace Message Mismatch Alarm:** An alarm indication (a 1) indicates that the stable Tandem Connection 16-byte message did not match for one message time. Recovery to 0 occurs when the N2 (Z6) byte TC message state machine loses lock and then acquires lock with a 16-byte stable N2 (Z6) byte message that matches the N2 (Z6) byte comparison message written by the microprocessor.
	2	BnTCODI	**B Drop Bus Port n Tandem Connection ODI Alarm:** A TC ODI alarm indication (a 1) occurs when N2 (Z6) byte bit 7 in frame 74 is equal to 1 for five or more consecutive frames. Recovery to 0 occurs when bit 7 is a 0 for five or more consecutive frames.
	1	BnTCRDI	**B Drop Bus Port n Tandem Connection RDI Alarm:** A TC RDI alarm indication (a 1) occurs when N2 (Z6) byte bit 8 in frame 73 is equal to 1 for five or more consecutive frames. Recovery to 0 occurs when bit 8 is a 0 for five or more consecutive frames.
	0	Unused	**Unused:** This bit reads out as indeterminate.
180 Port 1 280 Port 2 380 Port 3 480 Port 4	7-0	Bn TC BIP-2 Error Counter	**B Drop Bus Port n Tandem Connection BIP-2 Counter:** An 8-bit counter which counts the number of BIP-2 errors detected in the N2 (Z6) byte for the TU/VT selected when the tandem connection feature is enabled. A maximum of two errors can be counted each frame. These two errors cause a single count if the BLOCK control bit is set to 1. The counter saturates at full count and is cleared when it is read.
181 Port 1 281 Port 2 381 Port 3 481 Port 4	7-0	Bn TC REI Error Counter	**B Drop Bus Port n Tandem Connection REI Counter:** An 8-bit counter which counts the number of REI errors detected in bit 5 in the N2 (Z6) byte for the TU/VT selected when the tandem connection feature is enabled. The counter saturates at full count and is cleared when it is read.

Address	Bit	Symbol	Description
182 Port 1 282 Port 2 382 Port 3 482 Port 4	7-0	Bn TC OEI Error Counter	**B Drop Bus Port n Tandem Connection OEI Counter:** An 8-bit counter which counts the number of OEI errors detected in bit 6 in the N2 (Z6) byte for the TU/VT selected when the tandem connection feature is enabled. The counter saturates at full count and is cleared when it is read.
196 Port 1 296 Port 2 396 Port 3 496 Port 4	7-0	Bn Receive V4 Byte	**B Drop Bus Port n Receive V4 Byte:** When control bit V4EN is 1, the eight bits in this register position correspond to the V4 byte received in the TU/VT selected. Bit 7 corresponds to bit 1 in the V4 byte.
044 Port 1 074 Port 2 0A4 Port 3 0D4 Port 4	7	RnFFE	Same alarms as the corresponding address 045, 075, 0A5 and 0D5 bits, except that these alarm states are latched.
	6	Unused	**Unused:** This bit reads out as 0.
	5-0	Latched Tx Alarms	Same alarms as the corresponding address 045, 075, 0A5 and 0D5 bits, except that these alarm states are latched.
045 Port 1 075 Port 2 0A5 Port 3 0D5 Port 4	7	RnFFE	**Receive Port n FIFO Error:** A 1 indicates that the receive FIFO for port 1 has overflowed or underflowed. The FIFO is reset automatically. Other than an alarm indication, no action is taken.
	6	Unused	**Unused:** This bit reads out as 0.
	5	ANAnOOL	**PRBS Analyzer Out of Lock:** A 1 indicates that the internal PRBS Analyzer is out of lock.
	4	TAnFE	**Transmit A Add Bus Port n FIFO Error:** A 1 indicates that the A Add bus FIFO has overflowed or underflowed. The FIFO is recentered and is held reset for up to two multiframes automatically. The VT AIS payload will be transmitted via the add bus when the FIFO error occurs.
	3	TBnFE	**Transmit B Add Bus Port n FIFO Error:** A 1 indicates that the B Add bus FIFO has overflowed or underflowed. The FIFO is recentered and is held reset for up to two multiframes automatically. The VT AIS payload will be transmitted via the add bus when the FIFO error occurs.
	2	TnLOS	**Transmit Port n Loss Of Signal:** An alarm occurs when there are no signal transitions detected on the positive rail or negative rail for a period of 256 consecutive pulse positions. Recovery occurs when there are at least 32 transitions counted for 256 consecutive pulse positions. For an NRZ signal, this alarm is active when a low occurs on the external transmit loss of signal indication lead $\overline{\text{TLOSn}}$, which is shared with the TNIn lead.
	1	TnLOC	**Transmit Port n Loss Of Clock:** A 1 indicates that the transmit clock (TCIn) for port n has stuck high or low for 6 or more clock cycles. Recovery occurs on the first clock transition.
	0	TnDAIS	**Transmit Port n AIS Detected:** A 1 indicates that line AIS (one or less zero in 256 bits) has been detected in the bit stream for port n. Recovery occurs when there are 3 or more zeros in 256 bits. Other than reporting the alarm, no action is taken.

Address	Bit	Symbol	Description
046 Port 1 076 Port 2 0A6 Port 3 0D6 Port 4	7-0	Coding Violation Counter Low Order Byte	**Transmit Port n Coding Violation Counter:** Low order byte of a 16-bit saturating counter which counts the number of coding errors that have occurred in the HDB3 line code. During a read cycle, internal logic holds any new count until the read cycle is complete, and then the counter is updated. This counter is cleared on a reset pulse, any RESET, RnSETS or RnSETC control bit = 1, or when its low order byte is read. This low order byte must be read before the high order byte for the same port, which is located in the following address.
047 Port 1 077 Port 2 0A7 Port 3 0D7 Port 4	7-0	Coding Violation Counter High Order Byte	**Transmit Port n Coding Violation Counter:** High order byte of an 16-bit saturating counter which counts the number of coding errors that have occurred in the HDB3 line codes. During a read cycle, internal logic holds any new count until the read cycle is complete, and then the counter is updated. This counter is cleared on a reset pulse, any RESET, RnSETS or RnSETC control bit = 1, or when its low order byte is read. This high order byte must be read after the low order byte for the same port, which is located in the preceding address, but before the next read of the low order byte for any port. (Reading the low order byte for any port causes a simultaneous transfer of the contents of the high order byte for the same port into a high order byte memory location that is common to all four ports. When any high order byte is read, the data output from the high order byte address is the content of this common memory location, not the current content of the addressed high order byte.)

PORT n - OPERATION REGISTER DESCRIPTIONS

Address	Bit	Symbol	Description
048 Port 1 078 Port 2 0A8 Port 3 0D8 Port 4	7-5	Unused	**Unused:** These bits must be written to 0.
	4	1BnRDI	**1-Bit/3-Bit RDI Selection for Port n:** When set to 0, the selected port will function as a 3-Bit enhanced RDI. When set to a 1, the selected port will function as 1-Bit RDI.
	3	J2nTEN	**J2 Transmit Message Enable for Port n:** A 1 enables a microprocessor-written message to be transmitted. A 0 disables the transmission of the J2 message from RAM. Instead, the J2 byte is transmitted as 00H.
	2	J2nSIZE	**J2 Message Size Segment for Port n:** Works in conjunction with the J2nCOM bit according to the following table: J2nSIZE / J2nCOM / Action 0 / 0 / Transmit and receive J2 message segments are configured for a 16-byte message size. Microprocessor reads 16-byte segment. J2 comparison circuit and alarms are disabled. 0 / 1 / Transmit and receive J2 message segments are configured for a 16-byte message size. Trail Trace message comparison circuit enabled. 1 / X / Transmit and receive J2 message segments are configured for a 64-byte message size. Microprocessor reads 64-byte segment. J2 comparison circuit and alarms are disabled. The Tandem Connection feature must be disabled by setting TCnEN=0.
	1	J2nCOM	**J2 Message Comparison Enable Bit for Port n:** Works in conjunction with the J2nSIZE control bit according to the table given above.
	0	J2nAISE	**J2 AIS/RDI/TC Alarm Enable for Port n:** A 1 enables Receive E1 AIS, a Remote Connectivity Defect Indication, and both of the TC alarms (TCnODI, TCnRDI) to be transmitted when either an AnJ2TIM/BnJ2TIM or an AnJ2LOL/BnJ2LOL occurs. The AIS, RDI and TC alarm generated depend on the bus side selected.

Address	Bit	Symbol	Description
050 Port 1 080 Port 2 0B0 Port 3 0E0 Port 4	7	FnLBK	**Facility Loopback:** A 1 enables an E1 facility (side) loopback for port n. The E1 transmit clock and data output signals are looped back internally as the E1 receive clock and data input signals. The external E1 receive input signals are disabled. The E1 transmit clock and data output signals are provided at the interface.
	6	LnLBK	**Line Loopback:** A 1 enables an E1 line (side) loopback for port n. The receive E1 clock and data output signals are looped back internally as the E1 transmit input signals. The external E1 transmit clock and data input signals are disabled. The E1 receive clock and data output signals are provided at the interface.
	5	RnAIS	**Send Receive E1 Line AIS for Port n:** A 1 enables an E1 AIS (unframed all ones signal) to be inserted into the receive data stream for port n independent of the status of the internal alarms.
	4	TnAIS	**Transmit E1 Line AIS for Port n:** A 1 enables an E1 AIS (unframed all ones signal) to be inserted into the transmit data stream for port n independent of the status of the internal alarms.
	3	TnVTAIS	**Transmit VT AIS for the TU/VT Selected for Port n:** A 1 enables a TU/VT AIS to be transmitted for the TU/VT selected. A TU/VT AIS consists of all ones in the entire TU/VT, including bytes V1 through V4.
	2	TnRFI	**Transmit Port n RFI (Remote Failure Indication):** A 1 enables an RFI alarm to be transmitted (bit 4 in the V5 byte is set to 1).
	1	TnRDIS	**Transmit Port n RDIS (Remote Server Defect Indication):** A 1 enables an RDIS to be transmitted (bit 8 in the V5 byte is set to 1, and bits 5, 6 and 7 in the K4 (Z7) byte are set to 101).
	0	TnRDIP	**Transmit Port n RDIP (Remote Payload Defect Indication):** A 1 enables an RDIP to be transmitted (bit 8 in the V5 byte is set to 0, and bits 5, 6 and 7 in the K4 (Z7) byte are set to 010).

Address	Bit	Symbol	Description
051 Port 1 081 Port 2 0B1 Port 3 0E1 Port 4	7	TCnRDI	**Tandem Connection RDI Generation for Port n:** A 1 enables a TC RDI to be generated (bit 8 in frame 73 is a 1).
	6	TCnODI	**Tandem Connection ODI Generation for Port n:** A 1 enables a TC ODI to be generated (bit 7 in frame 74 is a 1).
	5	TCnAIS	**Tandem Connection AIS Indication Transmitted for Port n:** A 1 enables a TC AIS indication to be generated (bit 4 in the N2 (Z6) byte is a 1).
	4	TCnEN	**Tandem Connection Feature Enable for Port n:** A 1 enables the TU Tandem Connection Feature (J2nSIZE must be 0). A 0 disables the tandem connection feature. In the receive direction all TC alarms are disabled. In the transmit direction, bits 3 through 8 in the N2(Z6) byte are transmitted as 0 while bits 1 and 2 still contain the calculated BIP-2.

	3	TCnRE	**Tandem Connection Remote Defect Indication Enable for Port n:** As explained in Note1, a 1 enables internal defined tandem connection alarms to send a TC RDI (bit 8 in frame 73). For example, a TC RDI for port 1 is generated:
			
			- When TC enable (TC1EN) and TC RDI enable (TC1RE) are 1 and any of:
			  - Loss Of Pointer Alarm (A1LOP, B1LOP)
			  - TU AIS Alarm (A1AIS, B1AIS)
			  - Drop Bus AIS Alarm (AsUASI, BsUASI) when HEAISE is 1
			  - Drop Bus H4 Alarm (AsDH4E, BsDH4E) when DV1SEL is 1
			  - Unequipped signal label (A1UNEQ, B1UNEQ) when UQAE is 1
			  - Mismatch signal label (A1SLER, B1SLER)
			  - J2 Loss Of Lock Alarm (A1J2LOL, B1J2LOL) when J2AISEN is 1
			  - J2 Mismatch Alarm (A1J2TIM, B1J2TIM) when J2AISEN is 1
			  - TC Unequipped Alarm (A1TCUQ, B1TCUQ)
			  - TC Loss Of Lock Alarm (A1TCLL, B1TCLL)
			  - TC Mismatch Alarm (A1TCTM, B1TCTM)
			  - TC Loss Of Multiframe Alarm (A1TCLM, B1TCLM)
			  - A 1 written to TC1RDI
			
			- When TC enable (TC1EN) is a 1 and TC RDI enable (TC1RE) is 0 and:
			  - A 1 written to TC1RDI.

Note 1: In determining whether to send TC ODI or TC RDI, it is necessary to sample certain alarm conditions. Since TC ODI or TC RDI are sent only once for every 38 ms multiframe, it is conceivable that these alarms may toggle more than one time in this interval. Therefore, all the alarms needed to generate TC ODI or TC RDI are sampled during every 500 µs multiframe, setting the TC ODI or TC RDI alarm.

Address	Bit	Symbol	Description

051 Port 1
081 Port 2
0B1 Port 3
0E1 Port 4
(cont.)
	2	TCnOE	**Tandem Connection Outgoing Defect Indication Enable for Port n:** As explained in Note 1, a 1 enables internal defined tandem connection alarms to send a TC ODI (bit 7 in frame 74). For example, a TC ODI for port 1 is generated:
			
			- When TC enable (TC1EN) and TC ODI enable (TC1OE) are 1 and any of:
			  - Loss Of Pointer Alarm (A1LOP, B1LOP)
			  - TU AIS Alarm (A1AIS, B1AIS)
			  - Drop Bus AIS Alarm (AsUASI, BsUASI) when HEAISE is 1
			  - Drop Bus H4 Alarm (AsDH4E, BsDH4E) when DV1SEL is 1
			  - Unequipped signal label (A1UNEQ, B1UNEQ) when UQAE is 1
			  - Mismatch signal label (A1SLER, B1SLER)
			  - J2 Loss Of Lock Alarm (A1J2LOL, B1J2LOL) when J2AISEN is 1
			  - J2 Mismatch Alarm (A1J2TIM, B1J2TIM) when J2AISEN is 1
			  - TC Unequipped Alarm (A1TCUQ, B1TCUQ)
			  - TC AIS alarm (A1TCAIS, B1TCAIS)
			  - TC Loss Of Lock Alarm (A1TCLL, B1TCLL)
			  - TC Mismatch Alarm (A1TCTM, B1TCTM)
			  - TC Loss Of Multiframe Alarm (A1TCLM, B1TCLM)
			  - A 1 written to TC1ODI.
			  (where S is the STS-1 or AU-3 identifier, 1-3)
			
			- When TC enable (TC1EN) is a 1 and TC ODI enable (TC1OE) is 0 and:
			  - A 1 written to TC1ODI.

	1	TCnAEN	**Tandem Connection Line AIS Enable for Port n:** A 1 enables internal receive TC alarms to generate receive E1 line AIS.
	0	TnRDIC	**Transmit Port n RDIC (Remote Connectivity Defect Indication):** A 1 enables an RDIC to be transmitted (bit 8 in the V5 byte is set to 1, and bits 5, 6 and 7 in the K4 (Z7) byte are set to 110).
052 Port 1 082 Port 2 0B2 Port 3 0E2 Port 4	7	RnSETS	**Reset Port n Selected Functions:** A 1 will clear the alarms, reset the performance counters to 0, and re-initialize the FIFOs associated with port n. The control bits for port n are not reset. This bit is self-clearing, and will reset to 0 after the reset cycle is completed.
	6	RnSETC	**Reset Port n Performance Counters:** A 1 resets the performance counters to 0 for port n. This bit is self-clearing, and will reset to 0 after the reset cycle is completed.
	5-2	Unused	**Unused:** These bits must be written to 0.
	1	TnFB2	**Transmit Port n BIP-2 Error Mask (Force BIP-2 Error):** A 1 causes bits 1 and 2 (the BIP-2 value) in the V5 byte to be inverted from the calculated value and transmitted for one frame. This bit is self-clearing, and will reset to 0 after the single error is transmitted.

Note 1: In determining whether to send TC ODI or TC RDI, it is necessary to sample certain alarm conditions. Since TC ODI or TC RDI are sent only once for every 38 ms multiframe, it is conceivable that these alarms may toggle more than one time in this interval. Therefore, all the alarms needed to generate TC ODI or TC RDI are sampled during every 500 μs multiframe, setting the TC ODI or TC RDI alarm.

Address	Bit	Symbol	Description
052 Port 1 082 Port 2 0B2 Port 3 0E2 Port 4 (cont.)	0	TnFFB	**Transmit Port n FEBE Error Mask (Force FEBE Error):** A 1 causes bit 3 (the FEBE value) of the V5 byte to be transmitted as a 1. This control bit is self-clearing, and will reset to 0 after the V5 byte has been transmitted. Please note that if a FEBE is being sent as a result of a receive BIP-2 error, the FEBE error set by this bit is transmitted afterwards.
053 Port 1 083 Port 2 0B3 Port 3 0E3 Port 4	7-3	Unused	**Unused:** These bits must be written to 0.
	2-0	AnUPSL	**A Drop Bus Port n Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the TU/VT selected. Bit 2 in this register corresponds to bit 7 in the V5 byte. The bits written into this register are compared against the received signal for a mismatch signal label alarm.
054 Port 1 084 Port 2 0B4 Port 3 0E4 Port 4	7-3	Unused	**Unused:** These bits must be written to 0.
	2-0	BnUPSL	**B Drop Bus Port n Microprocessor-Written Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the TU/VT selected. Bit 2 in this register corresponds to bit 7 in the V5 byte. The bits written into this register are compared against the received signal for a mismatch signal label alarm.
055 Port 1 085 Port 2 0B5 Port 3 0E5 Port 4	7-3	Unused	**Unused:** These bits must be written to 0.
	2-0	Tn TX Label	**Transmit Port n Signal Label:** The three bit positions correspond to the three signal label bits found in bits 5 through 7 in the V5 byte for the TU/VT selected for transmission. Bit 2 in this register corresponds to bit 7 in the V5 byte.
058 Port 1 088 Port 2 0B8 Port 3 0E8 Port 4	7-4	Transmit K4 (Z7) Byte Value	**Transmit K4 (Z7) Value Port n:** The value written into bits 7, 6, 5, 4 and 0 in this register is transmitted when control bit TOBWZ is 0. Bits 3, 2, and 1 are assigned for the RDI indicators and cannot be written to in this register. Bit 7 corresponds to bit 1 in the K4 (Z7) byte.
	3-1	Unused	**Unused:** These bits must be written to 0.
	0	Transmit K4 (Z7) Byte Value	**Transmit K4 (Z7) Value Port n:** The value written into bits 7, 6, 5, 4 and 0 in this register is transmitted when control bit TOBWZ is 0. Bits 3, 2, and 1 are assigned for the RDI indicators and cannot be written to in this register. Bit 0 corresponds to bit 8 in the K4 (Z7) byte.
059 Port 1 089 Port 2 0B9 Port 3 0E9 Port 4	7-0	Transmit O-bits	**Transmit O Bits Port n:** The value written into this register is transmitted when control bit TOBWZ is 0. Bits 7 through 4 correspond to bits 3 through 6 in the second justification control byte. Bits 3 through 0 correspond to bits 3 through 6 in the first justification control byte.
511 Port 1 591 Port 2 611 Port 3 691 Port 4	7-0	Transmit V4 Byte	**Transmit V4 Byte Port n:** The value written into this register will be transmitted as the V4 byte. Bits 7-0 of the register correspond to bits 1-8 of the V4 byte.

PORT n - A AND B DROP J2 AND N2 (Z6) MESSAGE SEGMENTS

Address	Bit	Symbol	Description
140 Port 1 240 Port 2 340 Port 3 440 Port 4 to 17F Port 1 27F Port 2 37F Port 3 47F Port 4	7-0	A Side Receive J2 and N2 (Z6) Message Segments	**A Side Drop J2 and N2 (Z6) Message Segments:** The following locations store the received 64-byte J2 message when control bit J2nSIZE is a 1, and the received 16-byte J2 message, and microprocessor-written 16-byte J2 message when J2nSIZE is a 0, and the received 16-byte N2 (Z6) trail trace message and microprocessor-written 16-byte N2 (Z6) message used for message mismatch. Location — Message Segment X40-X7F — J2 Message size configured for 64 bytes. The 64-byte message is written into memory with no specific starting address location. The N2 (Z6) tandem connection feature is disabled. X40-X4F — Received 16-byte J2 message segment. X50-X5F — Microprocessor-written 16-byte J2 message segment. The starting address of the message must be written to location X50 (multiframe value of 1). X60-X6F — Received 16-byte N2 (Z6) message segment. X70-X7F — Microprocessor-written 16-byte N2 (Z6) message segment. The starting address of the message must be written to location X70 (multiframe value of 1).
1C0 Port 1 2C0 Port 2 3C0 Port 3 4C0 Port 4 to 1FF Port 1 2FF Port 2 3FF Port 3 4FF port 4	7-0	B Side Receive J2 and N2 (Z6) Message Segments	**B Side Drop J2 and N2 (Z6) Message Segments:** The following locations store the received 64-byte J2 message when control bit J2nSIZE is a 1, and the received 16-byte J2 message, and microprocessor-written 16-byte J2 message when J2nSIZE is a 0, and the received 16-byte N2 (Z6) trail trace message and microprocessor-written 16-byte N2 (Z6) message used for message mismatch. Location — Message Segment XC0-XFF — J2 Message size configured for 64 bytes. The 64-byte message is written into memory with no specific starting address location. The N2 (Z6) tandem connection feature is disabled. XC0-XCF — Received 16-byte J2 message segment. XD0-XDF — Microprocessor-written 16-byte J2 message segment. The starting address of the message must be written to location XD0 (multiframe value of 1). XE0-XEF — Received 16-byte N2 (Z6) message segment. XF0-XFF — Microprocessor-written 16-byte N2 (Z6) message segment. The starting address of the message must be written to location XF0 (multiframe value of 1).

Address	Bit	Symbol	Description
540 Port 1 5C0 Port 2 640 Port 3 6C0 Port 4 to 57F Port 1 5FF Port 2 67F Port 3 6FF Port 4	7-0	Transmit J2 and N2 (Z6) Message Segments	**Transmit J2 and N2 (Z6) Message Segments:** The following locations store the transmitted 64-byte J2 message when control bit J2nSIZE is a 1, and the transmitted 16-byte J2 and N2 (Z6) messages when J2nSIZE is a 0. Location — Message Segment 540-57F (Port 1), 5C0-5FF (Port 2), 640-67F (Port 3), 6C0-6FF (Port 4) — J2 Message size configured for 64 bytes. The 64-byte message is transmitted from no specific starting address. The tandem connection feature is disabled. 540-54F (Port 1), 5C0-5CF (Port 2), 640-64F (Port 3), 6C0-6CF (Port 4) — J2 Message size configured for 16 bytes. The 16-byte message is transmitted with no specific starting address. 560-56F (Port 1), 5E0-5EF (Port 2), 660-66F (Port 3), 6E0-6EF (Port 4) — N2 (Z6) Message size configured for 16 bytes. The 16-byte message is transmitted with no specific starting address.

PACKAGE INFORMATION

The QE1M device is packaged in two formats. One is a 160-lead plastic quad flat package (PQFP) suitable for surface mounting, as illustrated in Figure 28.

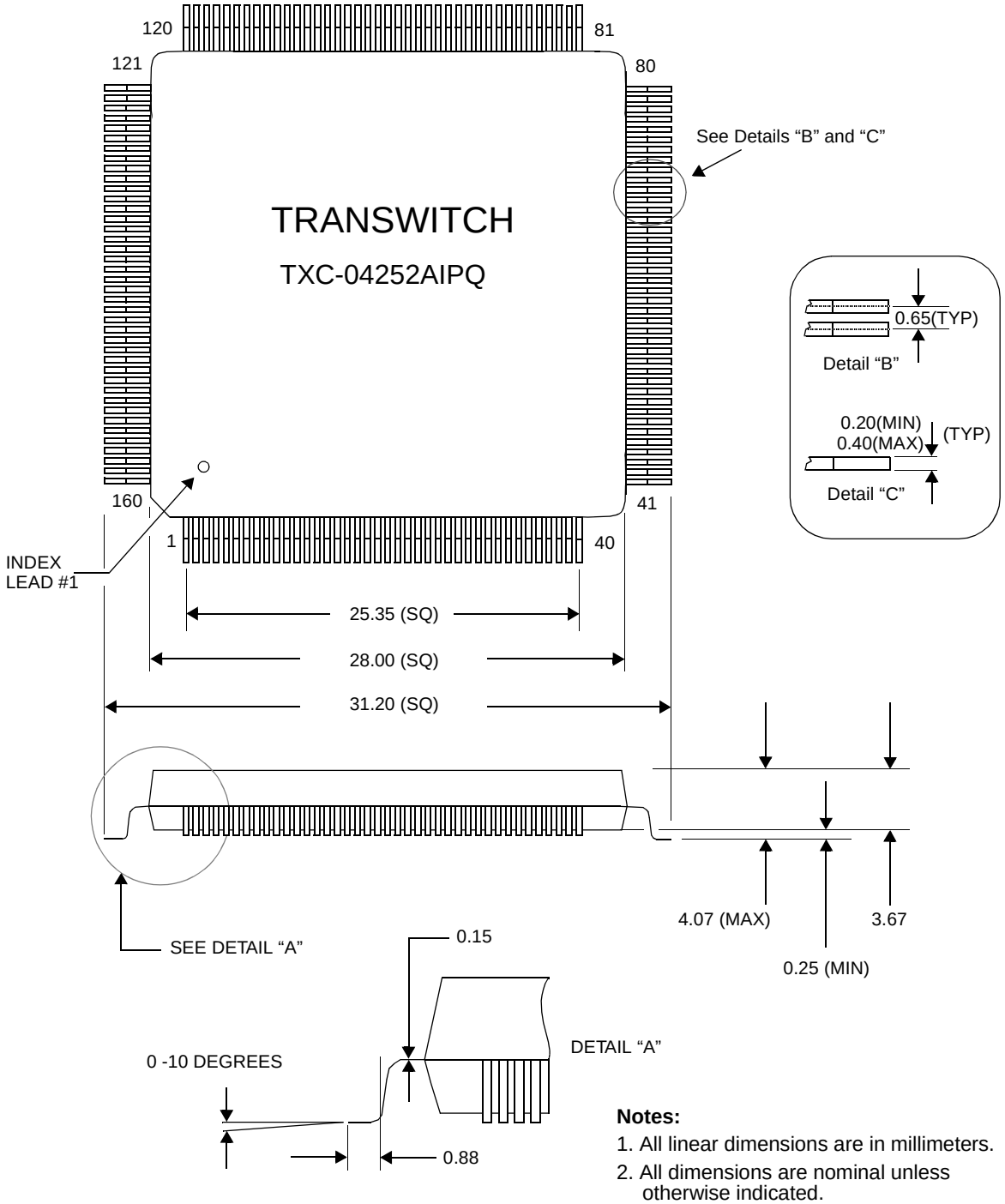
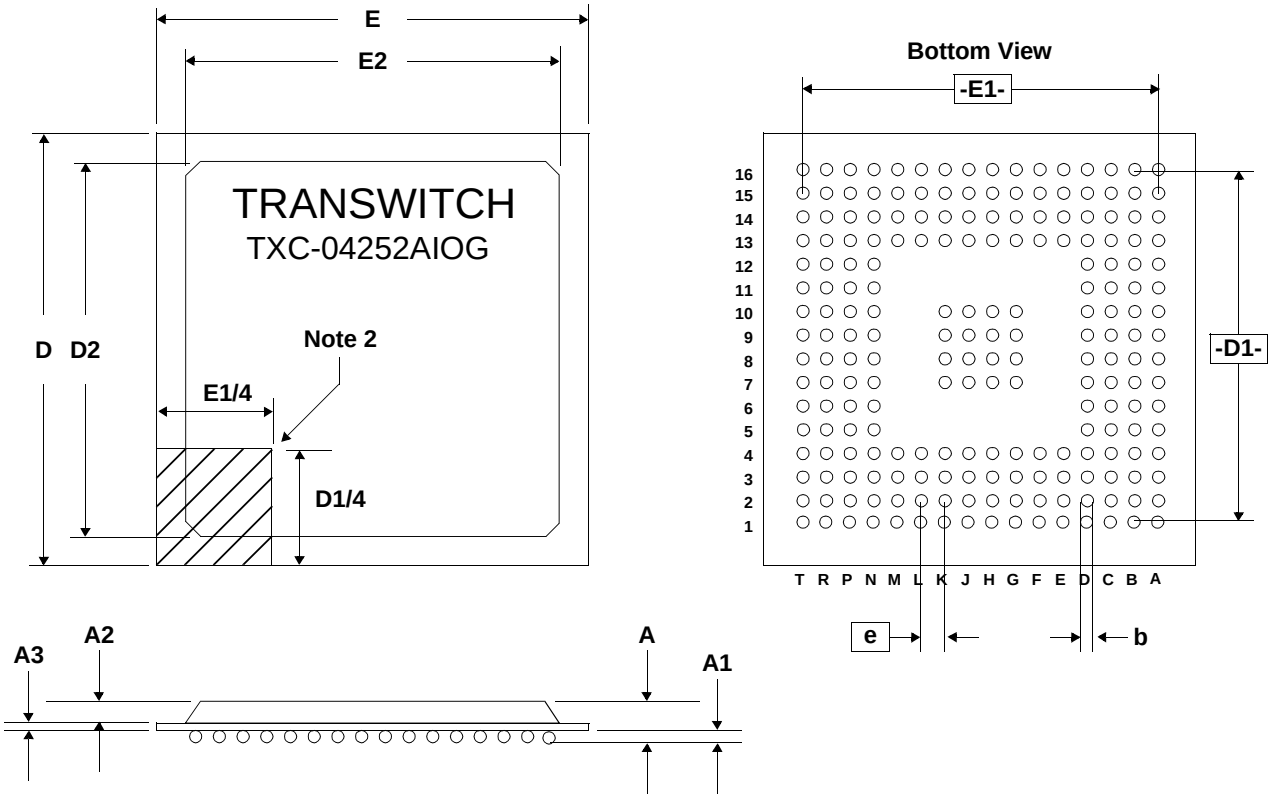


Figure 28. QE1M TXC-04252 160-Lead Plastic Quad Flat Package

The other is a 208-lead plastic ball grid array package (PBGA) suitable for surface mounting, as illustrated in Figure 29.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. This package corner may be a 90° angle, or chamfered for A1 identification.
3. Size of array: 16 x 16, JEDEC code MO-151-AAF-1

Dimension (Note 1)	Min	Max
A	1.35	1.75
A1	0.30	0.50
A2	0.75	0.85
A3 (Ref.)	0.36	
b	0.40	0.60
D	17.00	
D1 (BSC)	15.00	
D2	15.00	15.70
E	17.00	
E1 (BSC)	15.00	
E2	15.00	15.70
e (BSC)	1.00	

Figure 29. QE1M TXC-04252 208-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number:	TXC-04252AIPQ	160-lead plastic quad flat package (PQFP)
	TXC-04252AIOG	208-lead plastic ball grid array package (PBGA)

RELATED PRODUCTS

TXC-02302B, SYN155C VLSI Device (155-Mbit/s Synchronizer, Clock and Data Output). Provides complete STS-3/STM-1 frame synchronization on incoming 155 Mbit/s signals in a single low power CMOS unit. It has both clock and data outputs on the line side.

TXC-03001B, SOT-1 VLSI Device (SONET STS-1 Overhead Terminator). In a single device, it provides the SONET interface to any payload. Provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal.

TXC-03003B, SOT-3 VLSI Device (STM-1/STS-3/STS-3c Overhead Terminator). This device performs section, line, and path overhead processing for a STS-3/STS-3c/STM-1 signal. Compliant with ANSI and ITU-TSS standards.

TXC-03011, SOT-1E VLSI Device (SONET STS-1 Overhead Terminator). In a single device, it provides the SONET interface to any payload. It provides access to all of the transport and path overhead defined for an STS-1/STS-N SONET signal. This device has extended features relative to the TXC-03001B that use more input/output pins. It has a larger package.

TXC-04002B, ADMA-E1 Device (2 Mbit/s to TU-12 Async Mapper-Desync). Interconnects two E1 signals with any two asynchronous mode TU-12 tributaries carried in an SDH VC-4 formatted bus at the STM-1 byte rate. This is a functionally enhanced version of the TXC-04002 device, and it is also a two-channel predecessor of the QE1M four-channel device.

TXC-04216, E1Mx16 VLSI Device (Sixteen channel E1 to AU-4/VT2 or TU-12 Async Mapper-Desync) - E1Mx16 is a module containing four QE1M chips. It interconnects sixteen E1 signals with any sixteen asynchronous mode VT2 or TU-12 tributaries carried in SDH AU-4/AU-3 rate payload interface.

TXC-06101, PHAST-1 VLSI Device (SONET STS-1 Overhead Terminator). This device provides features similar to those of the TXC-03011 SOT-1E device, but it operates from a power supply of 3.3 volts rather than 5 volts.

TXC-06103, PHAST-3N VLSI Device (SONET STM-1, STS-3 or STS-3c Overhead Terminator). This PHAST-3N VLSI device provides a Telecom Bus interface for downstream devices. It operates from a power supply of 3.3 volts.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
11 West 42nd Street
New York, New York 10036

Tel: (212) 642-4900
Fax: (212) 302-1286
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

2570 West El Camino Real
Suite 304
Mountain View, CA 94040

Tel: (650) 949-6700
Fax: (650) 949-6705
Web: www.atmforum.com

ATM Forum Europe Office

Av. De Tervueren 402
1150 Brussels
Belgium

Tel: 2 761 66 77
Fax: 2 761 66 79

ATM Forum Asia-Pacific Office

Hamamatsu-cho Suzuki Building 3F
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
7730 Carondelet Avenue, Suite 407
Clayton, MO 63105-3329

Tel: (800) 854-7179 (within U.S.A.)
Tel: (314) 726-0444 (outside U.S.A.)
Fax: (314) 726-6418
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia Antipolis Cedex
France

Tel: 4 92 94 42 22
Fax: 4 92 94 43 33
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (508) 650-1375
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5111
Fax: 22 733 7256
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
2575 NE Kathryn Street #17
Hillsboro, OR 97124

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 693-6232 (outside U.S.A.)
Fax: (503) 693-8344
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: (800) 521-CORE (within U.S.A.)
Tel: (908) 699-5800 (outside U.S.A.)
Fax: (908) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunications Technology Committee
2nd Floor, Hamamatsu-cho Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within this updated QE1M Data Sheet that have significant differences relative to the previous and now superseded QE1M Data Sheet.

Updated QE1M Data Sheet: Edition 3, December 2000

Previous QE1M Data Sheet: Edition 2, October 1997

The page numbers indicated below of this updated Data Sheet include significant changes relative to the previous data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Added TranSwitch document proprietary markings. Changed edition number and date.
All	Changed 'Pin' to 'Lead' throughout entire document.
1	Added PBGA package option to last bullet item of Features list. Added to list of Patents.
2-3	Updated Table of Contents and List of Figures.
9	Modified Note and title of Figure 3.
10	Added Figure 4.
11-20	Added new column '208-Lead PBGA Lead No.' and changed column heading 'Lead No.' to '160-Lead PQFP Lead No.' in all tables.
12	Changed 'I/O' to 'Input/Output' in table footnote.
16	Changed last sentence of Name/Function column for Symbol MUX.
20	Added second sentence to Name/Function column for Symbol $\overline{TRS}$.
21	Modified first and second tables. Moved first row from last table to first table and added Note 3. Modified Note 2.
26-30	Modified table in Figure 6. Added DPAR and APAR to Figures 7 and 8. Added APAR to Figures 9 and 10.
35-40	Added address and data signal labels to tables in Figures 13, 14, 15 and 16.
38-41	Modified waveforms, tables and Notes 3 and 4 in Figures 15 and 16.
42	Modified waveform and table in Figure 17.
47-48	Added 'Unequipped Operation' section.
50	Changed 'X' to '0' in first and second rows for DV1REF column.
51	Changed 'SLER' to 'SLER[5]' in first column of table and added Note 5.
61	Added new paragraph under 'Remote Defect Indications' heading. Modified second heading title and title of table. Switched the position of the words connectivity and payload in the third line of the second paragraph.
62-67	Made changes in text.

Page Number of Updated Data Sheet	Summary of the Change
78	Changed first column of second table.
80	Modified last sentence in second paragraph.
84	Added 'Boundary Scan Reset' section.
86-92	Added column for PBGA and its Lead No. Changed related Comments to include PBGA lead numbers.
104	Added '1BnRDI' for Bit 4 column in first row of first table.
107	Modified Description column for Symbol ABD.
110	Modified Description column for Bits 6 and 4 of Address 013.
121	Modified Description column for Address 0F5, Bit 7.
131	Added the new row for Symbol 1BnRDI and changed '7-4' to '7-5' for Bit column in first row of table.
133	Modified Description column for Symbol TCnEN.
138, 140	Removed second hyphen from device part number (now TXC-04252AIPQ).
139	Added Figure 29.
140	Added Part Number for PBGA under Ordering Information section.
141-142	Updated Standard Documentation Sources section.
143-144	Updated List of Data Sheet Changes section.
147	Updated Documentation Update Registration Form.

- NOTES -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