

FEATURES

- **25MHz Gain-Bandwidth**
- **600V/ μ s Slew Rate**
- **2.5mA Maximum Supply Current**
- Unity Gain Stable
- C-Load™ Op Amp Drives All Capacitive Loads
- 8nV/ $\sqrt{\text{Hz}}$ Input Noise Voltage
- 600 μ V Maximum Input Offset Voltage
- 500nA Maximum Input Bias Current
- 120nA Maximum Input Offset Current
- 20V/mV Minimum DC Gain, $R_L=1k$
- 115ns Settling Time to 0.1%, 10V Step
- 220ns Settling Time to 0.01%, 10V Step
- $\pm 12.5\text{V}$ Minimum Output Swing into 500 Ω
- $\pm 3\text{V}$ Minimum Output Swing into 150 Ω
- Specified at $\pm 2.5\text{V}$, $\pm 5\text{V}$, and $\pm 15\text{V}$

APPLICATIONS

- Wideband Amplifiers
- Buffers
- Active Filters
- Data Acquisition Systems
- Photodiode Amplifiers

DESCRIPTION

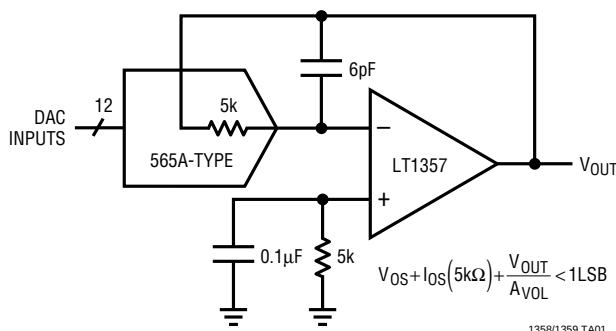
The LT1357 is a high speed, very high slew rate operational amplifier with outstanding AC and DC performance. The LT1357 has much lower supply current, lower input offset voltage, lower input bias current, and higher DC gain than devices with comparable bandwidth. The circuit topology is a voltage feedback amplifier with the slewing characteristics of a current feedback amplifier. The amplifier is a single gain stage with outstanding settling characteristics which makes the circuit an ideal choice for data acquisition systems. The output drives a 500 Ω load to $\pm 12.5\text{V}$ with $\pm 15\text{V}$ supplies and a 150 Ω load to $\pm 3\text{V}$ on $\pm 5\text{V}$ supplies. The amplifier is also stable with any capacitive load which makes it useful in buffer or cable driver applications.

The LT1357 is a member of a family of fast, high performance amplifiers using this unique topology and employing Linear Technology Corporation's advanced bipolar complementary processing. For dual and quad amplifier versions of the LT1357 see the LT1358/LT1359 data sheet. For higher bandwidth devices with higher supply current see the LT1360 through LT1365 data sheets. For lower supply current amplifiers see the LT1354 and LT1355/LT1356 data sheets. Singles, duals, and quads of each amplifier are available.

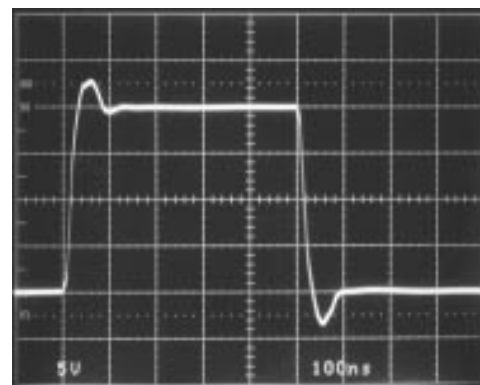
C-Load is a trademark of Linear Technology Corporation

TYPICAL APPLICATION

DAC I-to-V Converter



$A_V = -1$ Large-Signal Response



1357 TA02

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V^+ to V^-) 36V
 Differential Input Voltage $\pm 10V$
 Input Voltage $\pm V_S$
 Output Short-Circuit Duration (Note 1) Indefinite
 Operating Temperature Range -40°C to 85°C

Specified Temperature Range -40°C to 85°C
 Maximum Junction Temperature (See Below)
 Plastic Package 150°C
 Storage Temperature Range -65°C to 150°C
 Lead Temperature (Soldering, 10 sec) 300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE, 8-LEAD PLASTIC DIP $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 130^\circ\text{C/W}$	ORDER PART NUMBER LT1357CN8	TOP VIEW S8 PACKAGE, 8-LEAD PLASTIC SOIC $T_{JMAX} = 150^\circ\text{C}$, $\theta_{JA} = 190^\circ\text{C/W}$	ORDER PART NUMBER LT1357CS8 S8 PART MARKING 1357
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Consult factory for Industrial and Military grade parts.

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15V$		0.2	0.6	mV
			$\pm 5V$		0.2	0.6	mV
			$\pm 2.5V$		0.3	0.8	mV
I_{OS}	Input Offset Current		$\pm 2.5V$ to $\pm 15V$		40	120	nA
I_B	Input Bias Current		$\pm 2.5V$ to $\pm 15V$		120	500	nA
e_n	Input Noise Voltage	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		8		nV/ $\sqrt{\text{Hz}}$
i_n	Input Noise Current	$f = 10\text{kHz}$	$\pm 2.5V$ to $\pm 15V$		0.8		pA/ $\sqrt{\text{Hz}}$
R_{IN}	Input Resistance	$V_{CM} = \pm 12V$ Differential	$\pm 15V$	35	80		M Ω
			$\pm 15V$		6		M Ω
C_{IN}	Input Capacitance		$\pm 15V$		3		pF
	Input Voltage Range $^+$		$\pm 15V$	12.0	13.4		V
			$\pm 5V$	2.5	3.5		V
			$\pm 2.5V$	0.5	1.1		V
	Input Voltage Range $^-$		$\pm 15V$	-13.2	-12.0		V
			$\pm 5V$	-3.3	-2.5		V
			$\pm 2.5V$	-0.9	-0.5		V
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12V$	$\pm 15V$	83	97		dB
		$V_{CM} = \pm 2.5V$	$\pm 5V$	78	84		dB
		$V_{CM} = \pm 0.5V$	$\pm 2.5V$	68	75		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5V$ to $\pm 15V$		92	106		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12V$, $R_L = 1k$	$\pm 15V$	20.0	65		V/mV
		$V_{OUT} = \pm 10V$, $R_L = 500\Omega$	$\pm 15V$	7.0	25		V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 1k$	$\pm 5V$	20.0	45		V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 500\Omega$	$\pm 5V$	7.0	25		V/mV
		$V_{OUT} = \pm 2.5V$, $R_L = 150\Omega$	$\pm 5V$	1.5	6		V/mV
		$V_{OUT} = \pm 1V$, $R_L = 500\Omega$	$\pm 2.5V$	7.0	30		V/mV
V_{OUT}	Output Swing	$R_L = 1k$, $V_{IN} = \pm 40mV$	$\pm 15V$	13.3	13.8		$\pm V$
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	$\pm 15V$	12.5	13.0		$\pm V$
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	$\pm 5V$	3.5	4.0		$\pm V$
		$R_L = 150\Omega$, $V_{IN} = \pm 40mV$	$\pm 5V$	3.0	3.3		$\pm V$
		$R_L = 500\Omega$, $V_{IN} = \pm 40mV$	$\pm 2.5V$	1.3	1.7		$\pm V$

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
I_{OUT}	Output Current	$V_{OUT} = \pm 12.5\text{V}$ $V_{OUT} = \pm 3\text{V}$	$\pm 15\text{V}$	25	30		mA
			$\pm 5\text{V}$	20	25		mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}$, $V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	30	42		mA
SR	Slew Rate	$A_V = -2$, (Note 2)	$\pm 15\text{V}$	300	600		$\text{V}/\mu\text{s}$
			$\pm 5\text{V}$	150	220		$\text{V}/\mu\text{s}$
	Full Power Bandwidth	10V Peak, (Note 3) 3V Peak, (Note 3)	$\pm 15\text{V}$		9.6		MHz
			$\pm 5\text{V}$		11.7		MHz
GBW	Gain-Bandwidth	$f = 200\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$	18	25		MHz
			$\pm 5\text{V}$	15	22		MHz
			$\pm 2.5\text{V}$		20		MHz
t_r , t_f	Rise Time, Fall Time	$A_V = 1$, 10%-90%, 0.1V	$\pm 15\text{V}$		8		ns
			$\pm 5\text{V}$		9		ns
	Overshoot	$A_V = 1$, 0.1V	$\pm 15\text{V}$		27		$\%$
			$\pm 5\text{V}$		27		$\%$
	Propagation Delay	50% V_{IN} to 50% V_{OUT} , 0.1V	$\pm 15\text{V}$		9		ns
			$\pm 5\text{V}$		11		ns
t_s	Settling Time	10V Step, 0.1%, $A_V = -1$	$\pm 15\text{V}$		115		ns
		10V Step, 0.01%, $A_V = -1$	$\pm 15\text{V}$		220		ns
		5V Step, 0.1%, $A_V = -1$	$\pm 5\text{V}$		110		ns
		5V Step, 0.01%, $A_V = -1$	$\pm 5\text{V}$		380		ns
	Differential Gain	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.1		$\%$
			$\pm 5\text{V}$		0.1		$\%$
	Differential Phase	$f = 3.58\text{MHz}$, $A_V = 2$, $R_L = 1\text{k}$	$\pm 15\text{V}$		0.50		Deg
			$\pm 5\text{V}$		0.35		Deg
R_O	Output Resistance	$A_V = 1$, $f = 100\text{kHz}$	$\pm 15\text{V}$		0.3		Ω
I_S	Supply Current		$\pm 15\text{V}$		2.0	2.5	mA
			$\pm 5\text{V}$		1.9	2.4	mA

ELECTRICAL CHARACTERISTICS $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15\text{V}$	●		0.8	mV
			$\pm 5\text{V}$	●		0.8	mV
			$\pm 2.5\text{V}$	●		1.0	mV
	Input V_{OS} Drift	(Note 4)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●	5	8	$\mu\text{V}/^\circ\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		180	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		750	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	●	81		dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	77		dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	●	67		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	90		dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}$, $R_L = 1\text{k}$	$\pm 15\text{V}$	●	15		V/mV
		$V_{OUT} = \pm 10\text{V}$, $R_L = 500\Omega$	$\pm 15\text{V}$	●	5		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 1\text{k}$	$\pm 5\text{V}$	●	15		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 500\Omega$	$\pm 5\text{V}$	●	5		V/mV
		$V_{OUT} = \pm 2.5\text{V}$, $R_L = 150\Omega$	$\pm 5\text{V}$	●	1		V/mV
		$V_{OUT} = \pm 1\text{V}$, $R_L = 500\Omega$	$\pm 2.5\text{V}$	●	5		V/mV

ELECTRICAL CHARACTERISTICS $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OUT}	Output Swing	$R_L = 1\text{k}, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	13.2			$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	12.2			$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.4			$\pm\text{V}$
		$R_L = 150\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	2.8			$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	●	1.2			$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 12.2\text{V}$	$\pm 15\text{V}$	●	24.4			mA
		$V_{OUT} = \pm 2.8\text{V}$	$\pm 5\text{V}$	●	18.7			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}, V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	●	25			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	$\pm 15\text{V}$	●	225			V/ μs
			$\pm 5\text{V}$	●	125			V/ μs
GBW	Gain-Bandwidth	$f = 200\text{kHz}, R_L = 2\text{k}$	$\pm 15\text{V}$	●	15			MHz
			$\pm 5\text{V}$	●	12			MHz
I_S	Supply Current		$\pm 15\text{V}$	●			2.9	mA
			$\pm 5\text{V}$	●			2.8	mA

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{CM} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage		$\pm 15\text{V}$	●			1.3	mV
			$\pm 5\text{V}$	●			1.3	mV
			$\pm 2.5\text{V}$	●			1.5	mV
	Input V_{OS} Drift	(Note 4)	$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●		5	8	$\mu\text{V}/^{\circ}\text{C}$
I_{OS}	Input Offset Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●			300	nA
I_B	Input Bias Current		$\pm 2.5\text{V}$ to $\pm 15\text{V}$	●			900	nA
CMRR	Common-Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	$\pm 15\text{V}$	●	80			dB
		$V_{CM} = \pm 2.5\text{V}$	$\pm 5\text{V}$	●	76			dB
		$V_{CM} = \pm 0.5\text{V}$	$\pm 2.5\text{V}$	●	66			dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 2.5\text{V}$ to $\pm 15\text{V}$		●	90			dB
A_{VOL}	Large-Signal Voltage Gain	$V_{OUT} = \pm 12\text{V}, R_L = 1\text{k}$	$\pm 15\text{V}$	●	10.0			V/mV
		$V_{OUT} = \pm 10\text{V}, R_L = 500\Omega$	$\pm 15\text{V}$	●	2.5			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 1\text{k}$	$\pm 5\text{V}$	●	10.0			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 500\Omega$	$\pm 5\text{V}$	●	2.5			V/mV
		$V_{OUT} = \pm 2.5\text{V}, R_L = 150\Omega$	$\pm 5\text{V}$	●	0.6			V/mV
		$V_{OUT} = \pm 1\text{V}, R_L = 500\Omega$	$\pm 2.5\text{V}$	●	2.5			V/mV
V_{OUT}	Output Swing	$R_L = 1\text{k}, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	13.0			$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 15\text{V}$	●	12.0			$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	3.4			$\pm\text{V}$
		$R_L = 150\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 5\text{V}$	●	2.6			$\pm\text{V}$
		$R_L = 500\Omega, V_{IN} = \pm 40\text{mV}$	$\pm 2.5\text{V}$	●	1.2			$\pm\text{V}$
I_{OUT}	Output Current	$V_{OUT} = \pm 12\text{V}$	$\pm 15\text{V}$	●	24.0			mA
		$V_{OUT} = \pm 2.6\text{V}$	$\pm 5\text{V}$	●	17.3			mA
I_{SC}	Short-Circuit Current	$V_{OUT} = 0\text{V}, V_{IN} = \pm 3\text{V}$	$\pm 15\text{V}$	●	24			mA
SR	Slew Rate	$A_V = -2$, (Note 2)	$\pm 15\text{V}$	●	180			V/ μs
			$\pm 5\text{V}$	●	100			V/ μs

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $V_{\text{CM}} = 0\text{V}$ unless otherwise noted. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	V_{SUPPLY}	MIN	TYP	MAX	UNITS
GBW	Gain-Bandwidth	$f = 200\text{kHz}$, $R_L = 2\text{k}$	$\pm 15\text{V}$ $\pm 5\text{V}$	● ●	14 11		MHz MHz
I_S	Supply Current		$\pm 15\text{V}$ $\pm 5\text{V}$	● ●		3.0 2.9	mA mA

The ● denotes specifications that apply over the full operating temperature range.

Note 1: A heat sink may be required to keep the junction temperature below absolute maximum when the output is shorted indefinitely.

Note 2: Slew rate is measured between $\pm 10\text{V}$ on the output with $\pm 6\text{V}$ input for $\pm 15\text{V}$ supplies and $\pm 1\text{V}$ on the output with $\pm 1.75\text{V}$ input for $\pm 5\text{V}$ supplies.

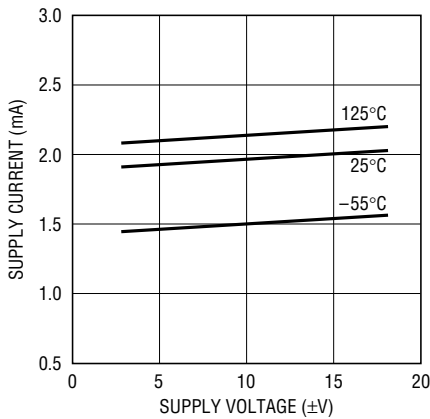
Note 3: Full power bandwidth is calculated from the slew rate measurement: $\text{FPBW} = \text{SR}/2\pi V_p$.

Note 4: This parameter is not 100% tested.

Note 5: The LT1357 is not tested and is not quality-assurance sampled at -40°C and at 85°C . These specifications are guaranteed by design, correlation, and/or inference from 0°C , 25°C , and/or 70°C tests.

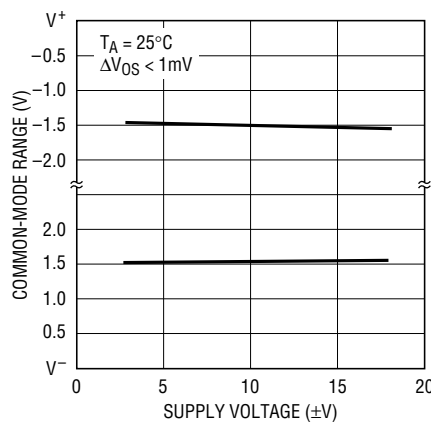
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage and Temperature



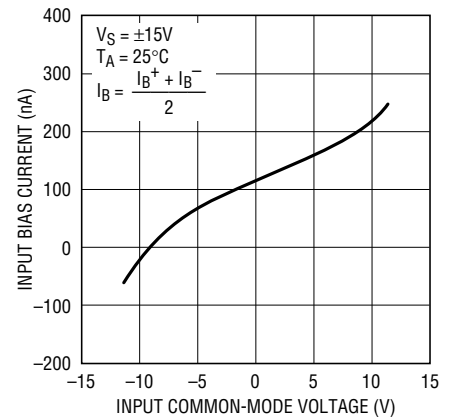
1357 G01

Input Common-Mode Range vs Supply Voltage



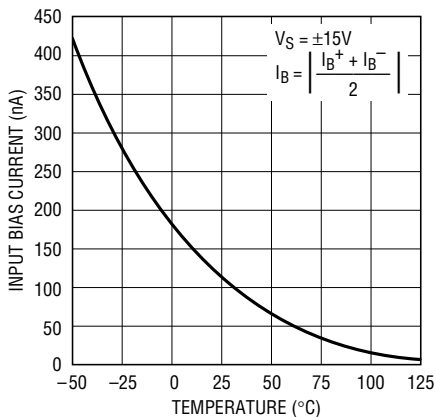
1357 G02

Input Bias Current vs Input Common-Mode Voltage



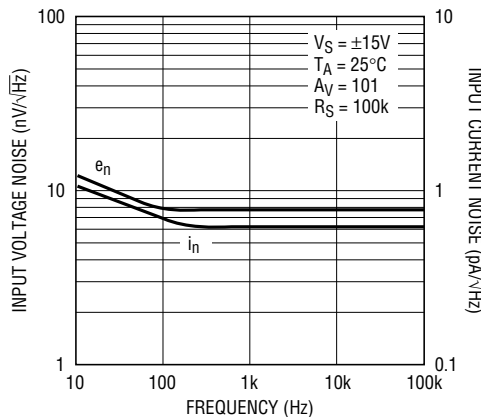
1357 G03

Input Bias Current vs Temperature



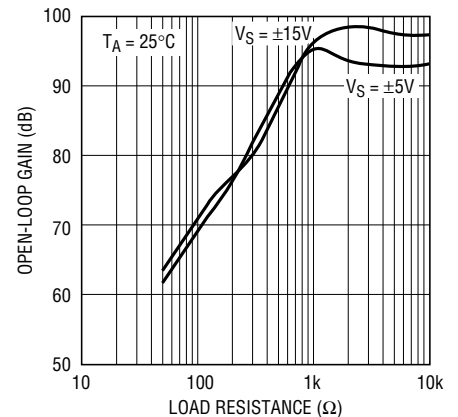
1358/1359 G04

Input Noise Spectral Density



1357 G05

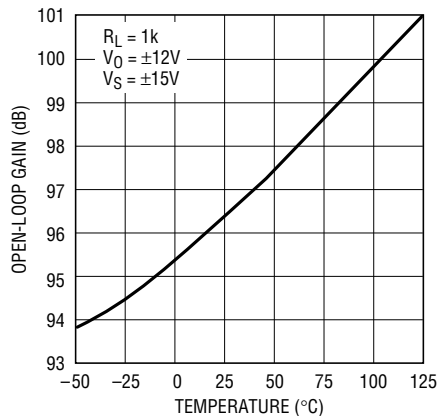
Open-Loop Gain vs Resistive Load



1357 G06

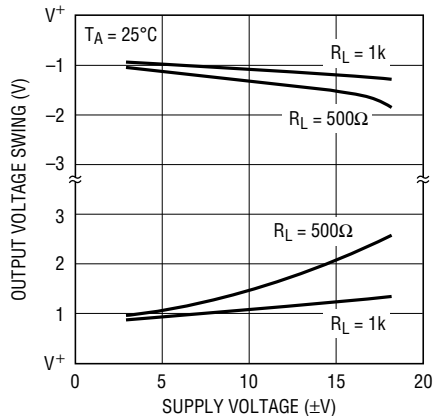
TYPICAL PERFORMANCE CHARACTERISTICS

Open-Loop Gain vs Temperature



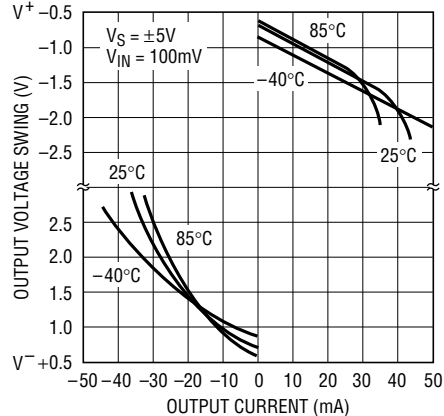
1357 G07

Output Voltage Swing vs Supply Voltage



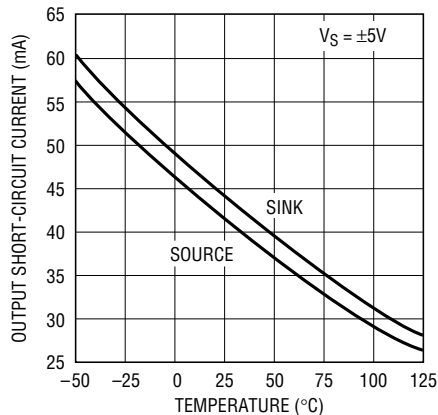
1357 G08

Output Voltage Swing vs Load Current



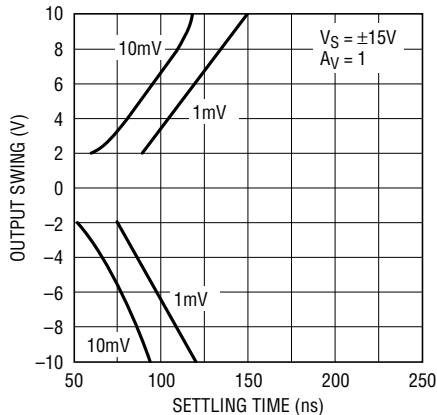
1357 G09

Output Short-Circuit Current vs Temperature



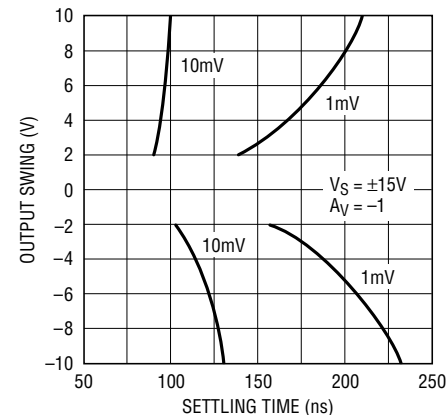
1357 G10

Settling Time vs Output Step (Noninverting)



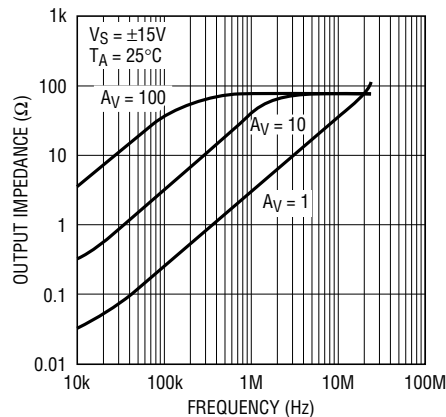
1357 G11

Settling Time vs Output Step (Inverting)



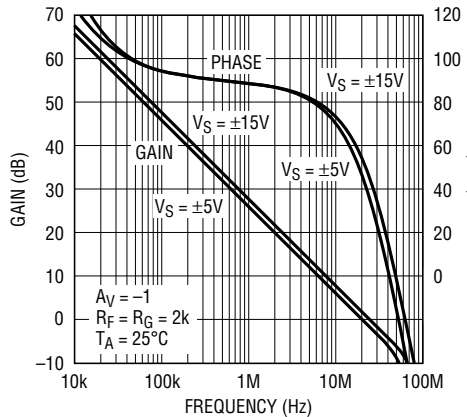
1357 G12

Output Impedance vs Frequency



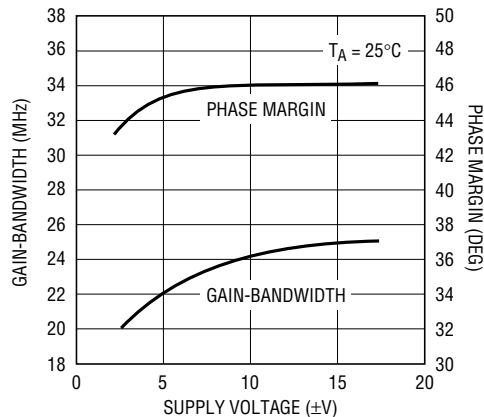
1357 G13

Gain and Phase vs Frequency



1357 G14

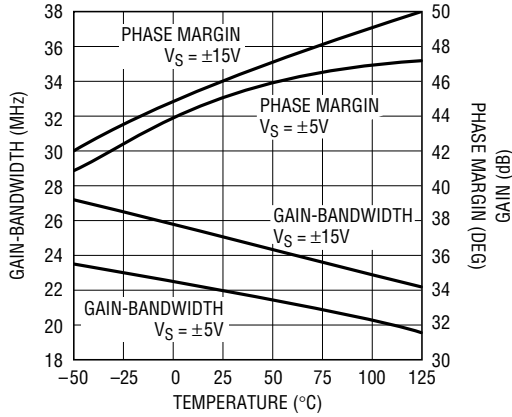
Gain-Bandwidth and Phase Margin vs Supply Voltage



1357 G15

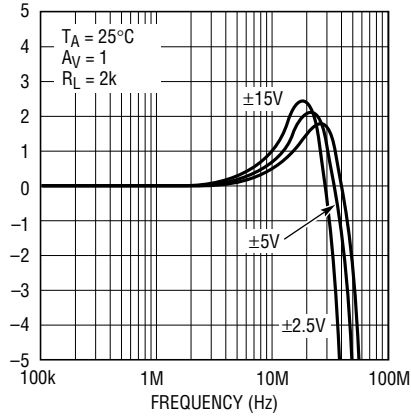
TYPICAL PERFORMANCE CHARACTERISTICS

Gain-Bandwidth and Phase Margin vs Temperature



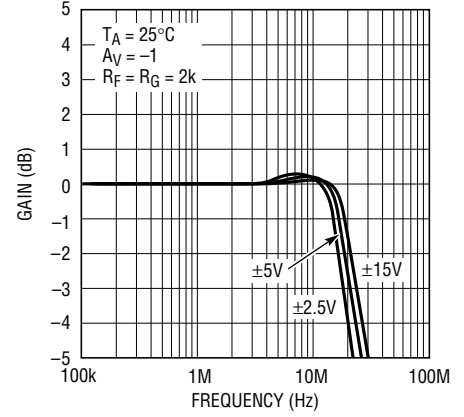
1357 G16

Frequency Response vs Supply Voltage ($A_V = 1$)



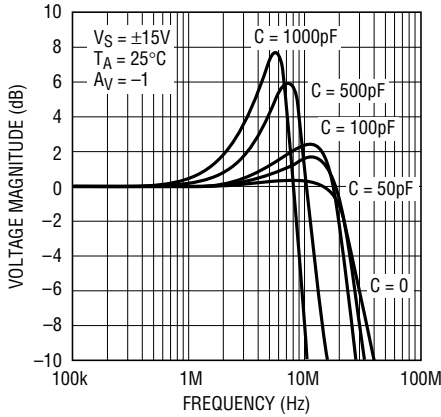
1357 G17

Frequency Response vs Supply Voltage ($A_V = -1$)



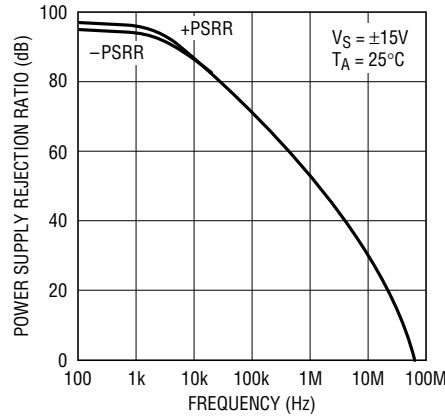
1357 G18

Frequency Response vs Capacitive Load



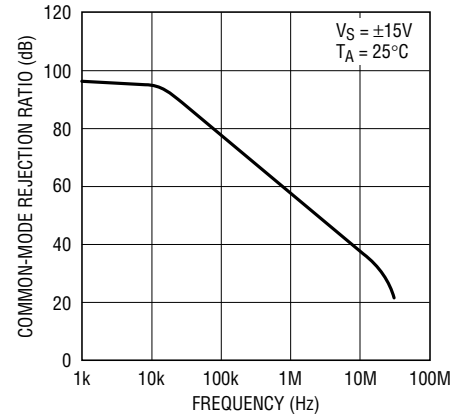
1358/1359 G19

Power Supply Rejection Ratio vs Frequency



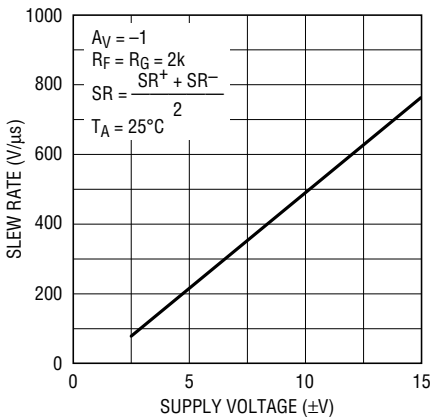
1357 G20

Common-Mode Rejection Ratio vs Frequency



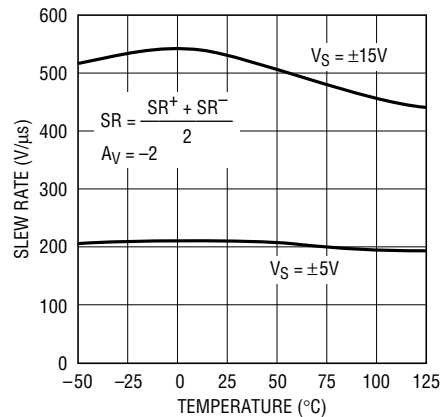
1357 G21

Slew Rate vs Supply Voltage



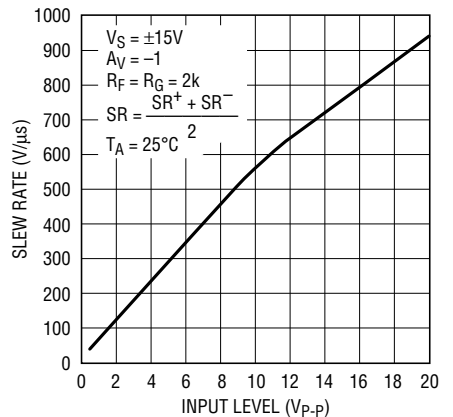
1357 G22

Slew Rate vs Temperature



1357 G23

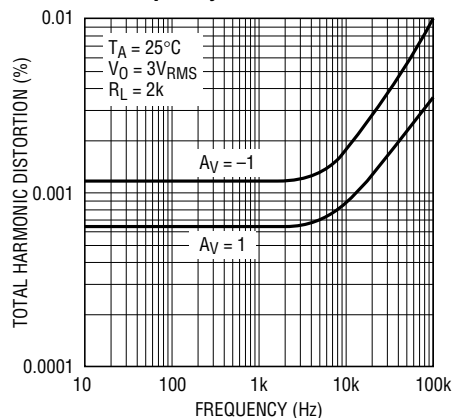
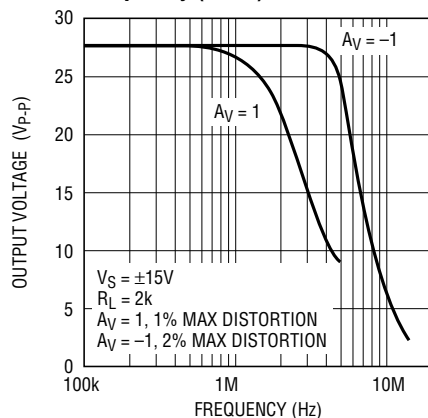
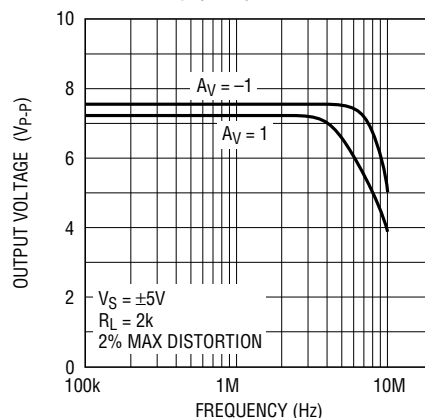
Slew Rate vs Input Level



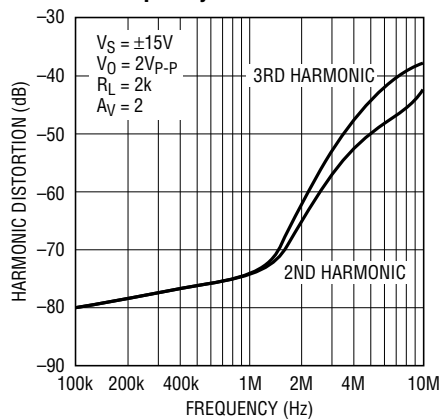
1357 G24

TYPICAL PERFORMANCE CHARACTERISTICS

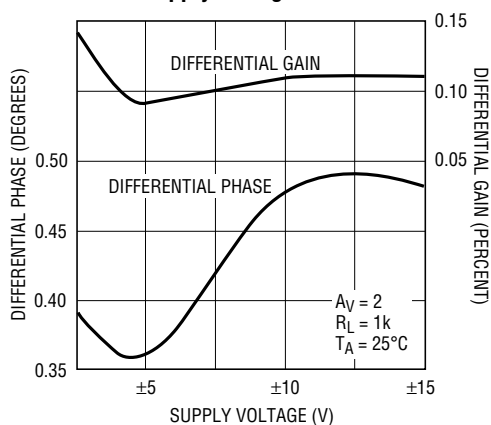
Total Harmonic Distortion vs Frequency

Undistorted Output Swing vs Frequency ($\pm 15V$)Undistorted Output Swing vs Frequency ($\pm 5V$)

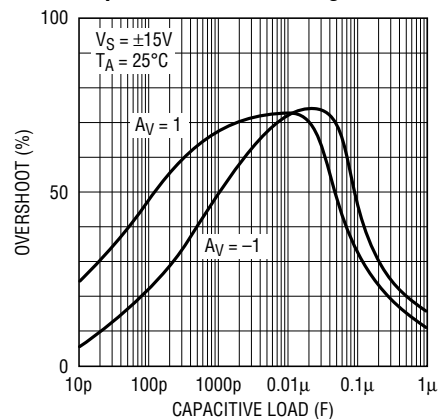
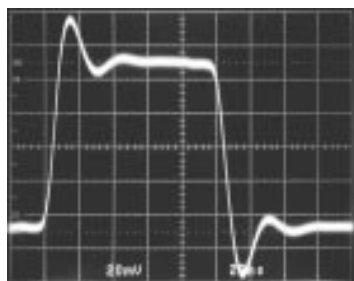
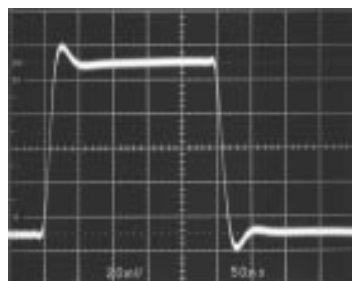
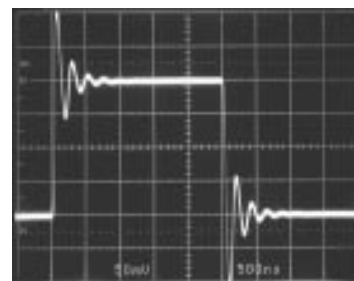
2nd and 3rd Harmonic Distortion vs Frequency



Differential Gain and Phase vs Supply Voltage

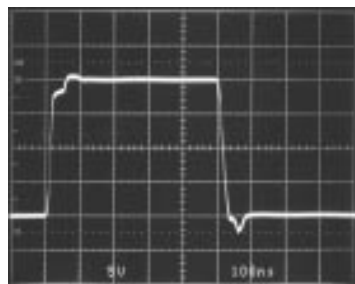


Capacitive Load Handling

Small-Signal Transient ($A_V = 1$)Small-Signal Transient ($A_V = -1$)Small-Signal Transient ($A_V = -1, C_L = 1000pF$)

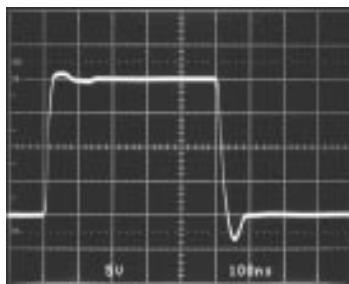
TYPICAL PERFORMANCE CHARACTERISTICS

Large-Signal Transient
($A_V = 1$)



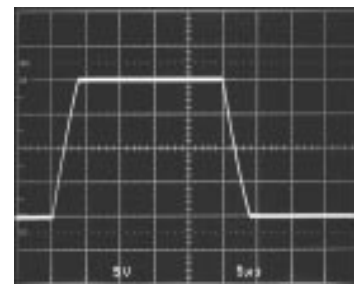
1357 TA34

Large-Signal Transient
($A_V = -1$)



1357 TA35

Large-Signal Transient
($A_V = 1$, $C_L = 10,000\text{pF}$)

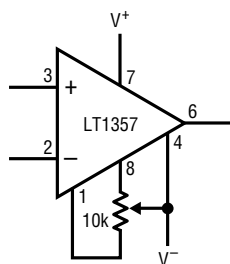


1357 TA36

APPLICATIONS INFORMATION

The LT1357 may be inserted directly into many high speed amplifier applications improving both DC and AC performance, provided that the nulling circuitry is removed. The suggested nulling circuit for the LT1357 is shown below.

Offset Nulling



1357 AI01

Layout and Passive Components

The LT1357 amplifier is easy to apply and tolerant of less than ideal layouts. For maximum performance (for example fast settling time) use a ground plane, short lead lengths, and RF-quality bypass capacitors ($0.01\mu\text{F}$ to $0.1\mu\text{F}$). For high drive current applications use low ESR bypass capacitors ($1\mu\text{F}$ to $10\mu\text{F}$ tantalum). Sockets should be avoided when maximum frequency performance is required, although low profile sockets can provide reasonable performance up to 50MHz. For more details see Design Note 50.

The parallel combination of the feedback resistor and gain setting resistor on the inverting input can combine with the input capacitance to form a pole which can cause peaking or oscillations. For feedback resistors greater than $5\text{k}\Omega$, a parallel capacitor of value

$$C_F > R_G \times C_{IN}/R_F$$

should be used to cancel the input pole and optimize dynamic performance. For unity-gain applications where a large feedback resistor is used, C_F should be greater than or equal to C_{IN} .

Capacitive Loading

The LT1357 is stable with any capacitive load. This is accomplished by sensing the load induced output pole and adding compensation at the amplifier gain node. As the capacitive load increases, both the bandwidth and phase margin decrease so there will be peaking in the frequency domain and in the transient response as shown in the typical performance curves. The photo of the small-signal response with 1000pF load shows 50% peaking. The large signal response with a $10,000\text{pF}$ load shows the output slew rate being limited to $5\text{V}/\mu\text{s}$ by the short-circuit current. Coaxial cable can be driven directly, but for best pulse fidelity a resistor of value equal to the characteristic impedance of the cable (i.e., 75Ω) should be placed in series with the output. The other end of the cable should be terminated with the same value resistor to ground.

APPLICATIONS INFORMATION

Input Considerations

Each of the LT1357 inputs is the base of an NPN and a PNP transistor whose base currents are of opposite polarity and provide first-order bias current cancellation. Because of variation in the matching of NPN and PNP beta, the polarity of the input bias current can be positive or negative. The offset current does not depend on beta matching and is well controlled. The use of balanced source resistance at each input is recommended for applications where DC accuracy must be maximized. The inputs can withstand differential input voltages of up to 10V without damage and need no clamping or source resistance for protection.

Power Dissipation

The LT1357 combines high speed and large output drive in a small package. Because of the wide supply voltage range, it is possible to exceed the maximum junction temperature under certain conditions. Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) as follows:

$$\text{LT1357CN8: } T_J = T_A + (P_D \times 130^\circ\text{C/W})$$

$$\text{LT1357CS8: } T_J = T_A + (P_D \times 190^\circ\text{C/W})$$

Worst case power dissipation occurs at the maximum supply current and when the output voltage is at 1/2 of either supply voltage (or the maximum swing if less than 1/2 supply voltage). Therefore $P_{D\text{MAX}}$ is:

$$P_{D\text{MAX}} = (V^+ - V^-)(I_{S\text{MAX}}) + (V^+/2)^2/R_L$$

Example: LT1357CS8 at 70°C , $V_S = \pm 15\text{V}$, $R_L = 120\Omega$
(Note: the minimum short-circuit current at 70°C is 25mA, so the output swing is guaranteed only to 3V with 120Ω .)

$$P_{D\text{MAX}} = (30\text{V})(2.9\text{mA}) + (15\text{V}-3\text{V})(25\text{mA}) = 387\text{mW}$$

$$T_{J\text{MAX}} = 70^\circ\text{C} + (387\text{mW})(190^\circ\text{C/W}) = 144^\circ\text{C}$$

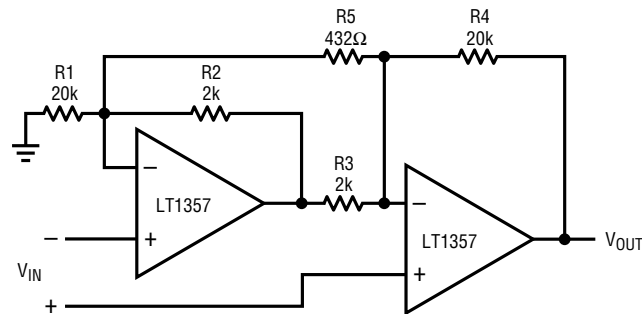
Circuit Operation

The LT1357 circuit topology is a true voltage feedback amplifier that has the slewing behavior of a current feedback amplifier. The operation of the circuit can be understood by referring to the simplified schematic. The inputs are buffered by complementary NPN and PNP emitter followers which drive a 500Ω resistor. The input voltage appears across the resistor generating currents which are mirrored into the high impedance node. Complementary followers form an output stage which buffers the gain node from the load. The bandwidth is set by the input resistor and the capacitance on the high impedance node. The slew rate is determined by the current available to charge the gain node capacitance. This current is the differential input voltage divided by R_1 , so the slew rate is proportional to the input. Highest slew rates are therefore seen in the lowest gain configurations. For example, a 10V output step in a gain of 10 has only a 1V input step, whereas the same output step in unity gain has a 10 times greater input step. The curve of Slew Rate vs Input Level illustrates this relationship. The LT1357 is tested for slew rate in a gain of -2 so higher slew rates can be expected in gains of 1 and -1 , and lower slew rates in higher gain configurations.

The RC network across the output stage is bootstrapped when the amplifier is driving a light or moderate load and has no effect under normal operation. When driving a capacitive load (or a low value resistive load) the network is incompletely bootstrapped and adds to the compensation at the high impedance node. The added capacitance slows down the amplifier which improves the phase margin by moving the unity gain frequency away from the pole formed by the output impedance and the capacitive load. The zero created by the RC combination adds phase to ensure that even for very large load capacitances, the total phase lag can never exceed 180 degrees (zero phase margin) and the amplifier remains stable.

TYPICAL APPLICATIONS

Instrumentation Amplifier

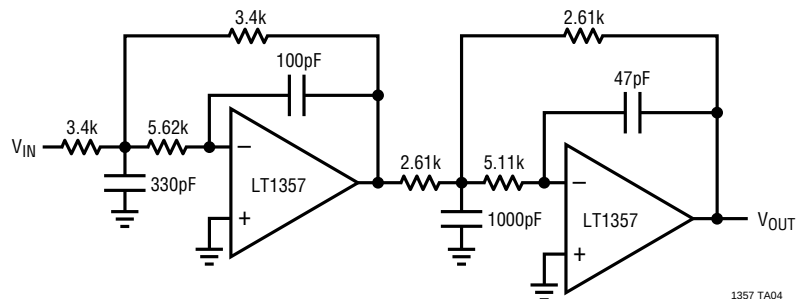


$$A_V = \frac{R_4}{R_3} \left[1 + \frac{1}{2} \left(\frac{R_2}{R_1} + \frac{R_3}{R_4} \right) + \frac{R_2 + R_3}{R_5} \right] = 104$$

TRIM R5 FOR GAIN
TRIM R1 FOR COMMON-MODE REJECTION
BW = 250kHz

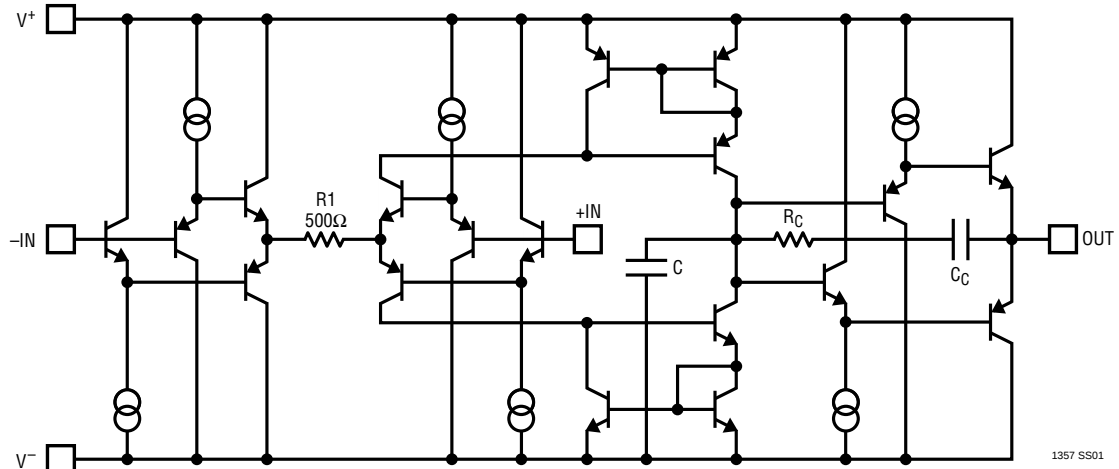
1357 TA03

200kHz, 4th Order Butterworth Filter



1357 TA04

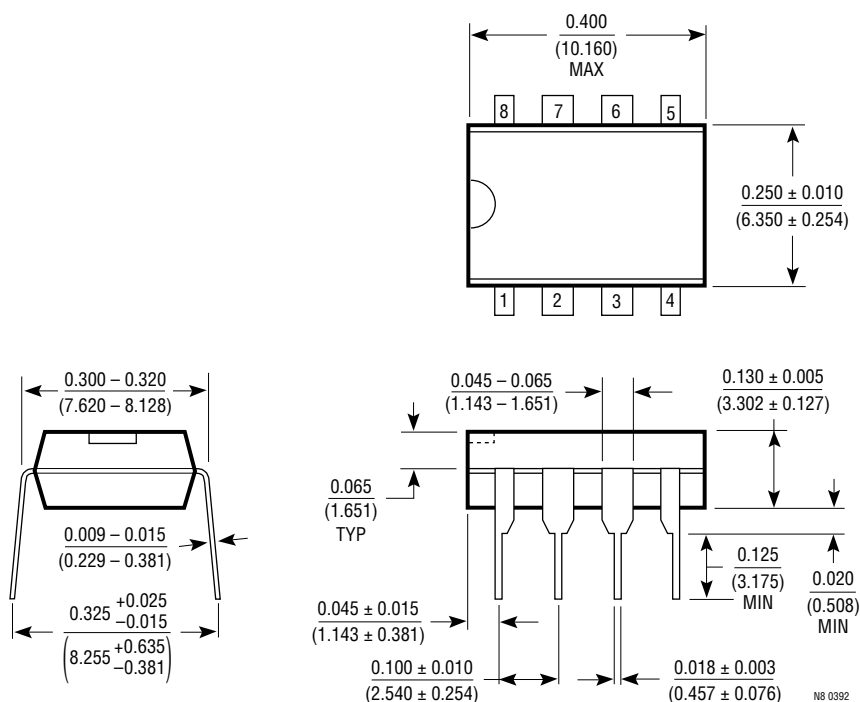
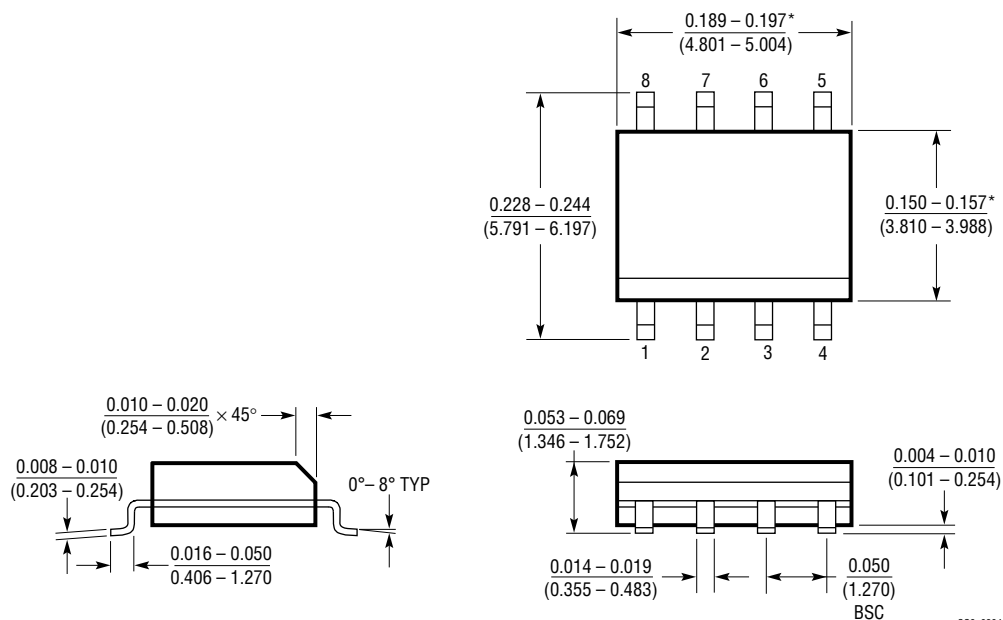
SIMPLIFIED SCHEMATIC



1357 SS01

PACKAGE DESCRIPTION

Dimension in inches (millimeters) unless otherwise noted.

**N8 Package
8-Lead Plastic DIP****S8 Package
8-Lead Plastic SOIC**

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCH (0.15mm).