NCN6004A

Dual SAM/SIM Interface Integrated Circuit

The NCN6004A is an interface IC dedicated for Secured Access Module reader/writer applications. It allows the management of two external ISO/EMV cards thanks to a simple and flexible microcontroller interface. Several NCN6004A interfaces can share a single data bus, assuming the external MPU provides the right Chip Select signals to identify each IC connected on the bus. A built in accurate protection system guarantees timely and controlled shutdown in the case of external error conditions.

On top of that, the NCN6004A can independently handle the power supply, in the range 2.7 V to 5.0 V input voltage, provided to each external Smart Card. The interface monitors the current flowing into each Smart Card, a flag being set in the case of overload.

Features

- Separated, Built-in DC/DC Converters Supply V_{CC} Power to External Cards
- 100% Compatible with ISO 7816-3, EMV and GIE-CB Standards
- Fully GSM Compliant
- Individually Programmable ISO/EMV Clock Generator
- Built-in Programmable CRD_CLK Stop Function Handles Run or High/Low State
- Programmable CRD_CLK Slopes to Cope with Wide Operating Frequency Range
- Programmable Independent V_{CC} Supply for Each Smart Card
- Support up to 65 mA V_{CC} Supply to Each ISO/EMV Card
- Multiple NCN6004A Parallel Operation on a Shared Bus
- 8 kV/Human Model ESD Protection on Each Interface Pin
- Provides C4/C8 Channels
- Provides 1.80 V, 3.0 V or 5.0 V Card Supply Voltages

Typical Applications

- Set Top Box Decoder
- ATM Multi Systems, POS, Handheld Terminals
- Internet E-commerce PC Interface
- Multiple Self Serve Automatic Machines
- Wireless Phone Payment Interface
- Automotive Operating Time Controller

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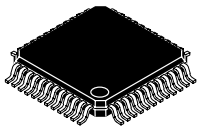
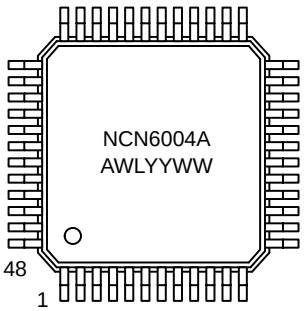


TQFP48
CASE 932F
PLASTIC

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
NCN6004AFTBR2	TQFP48	2000 Tape & Reel

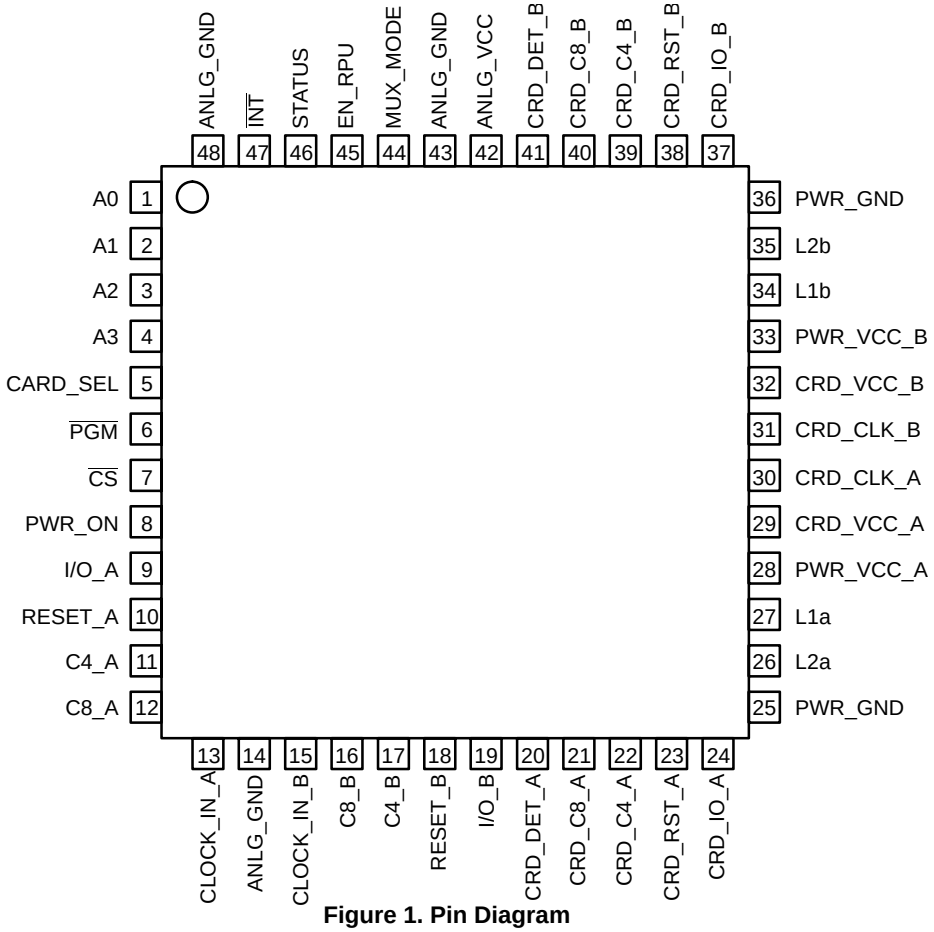


Figure 1. Pin Diagram

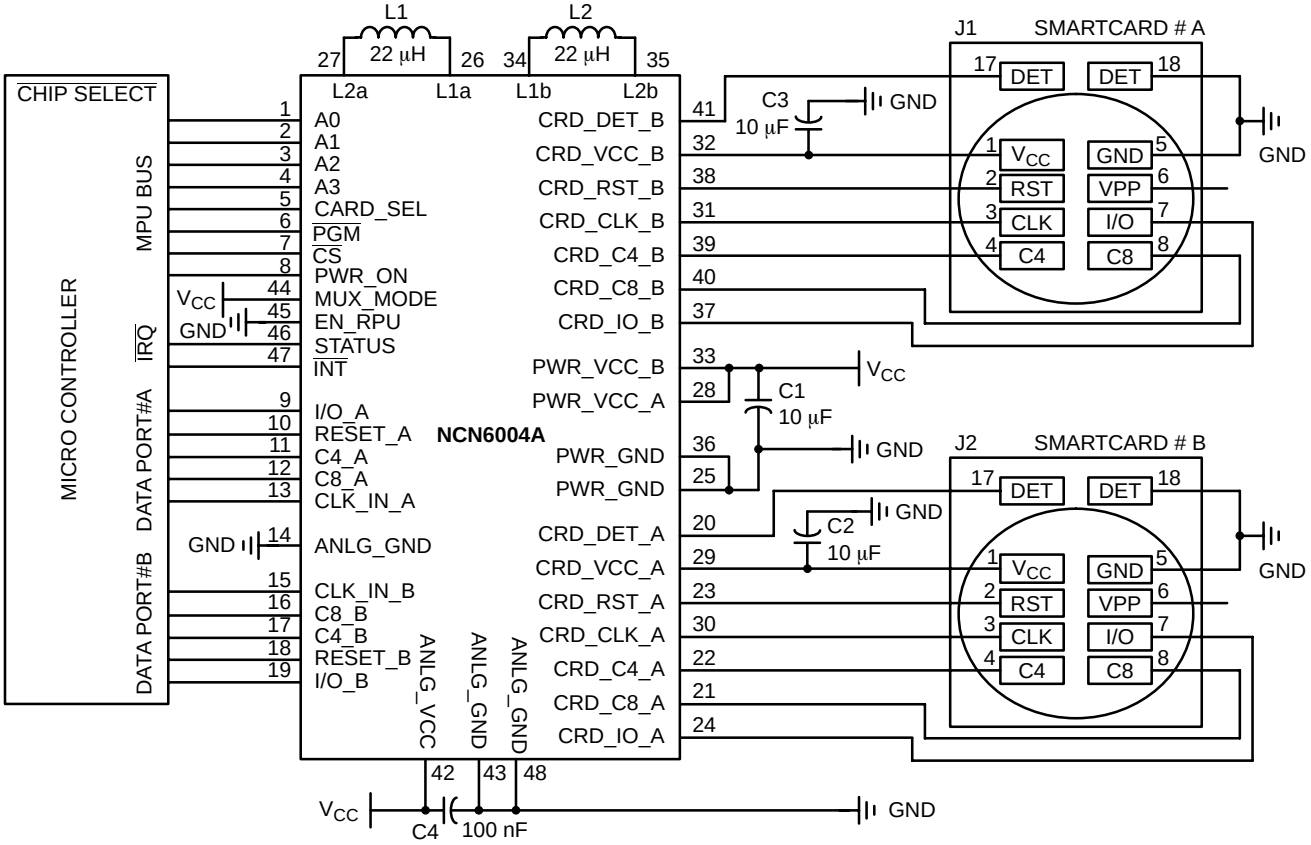


Figure 2. Typical Application

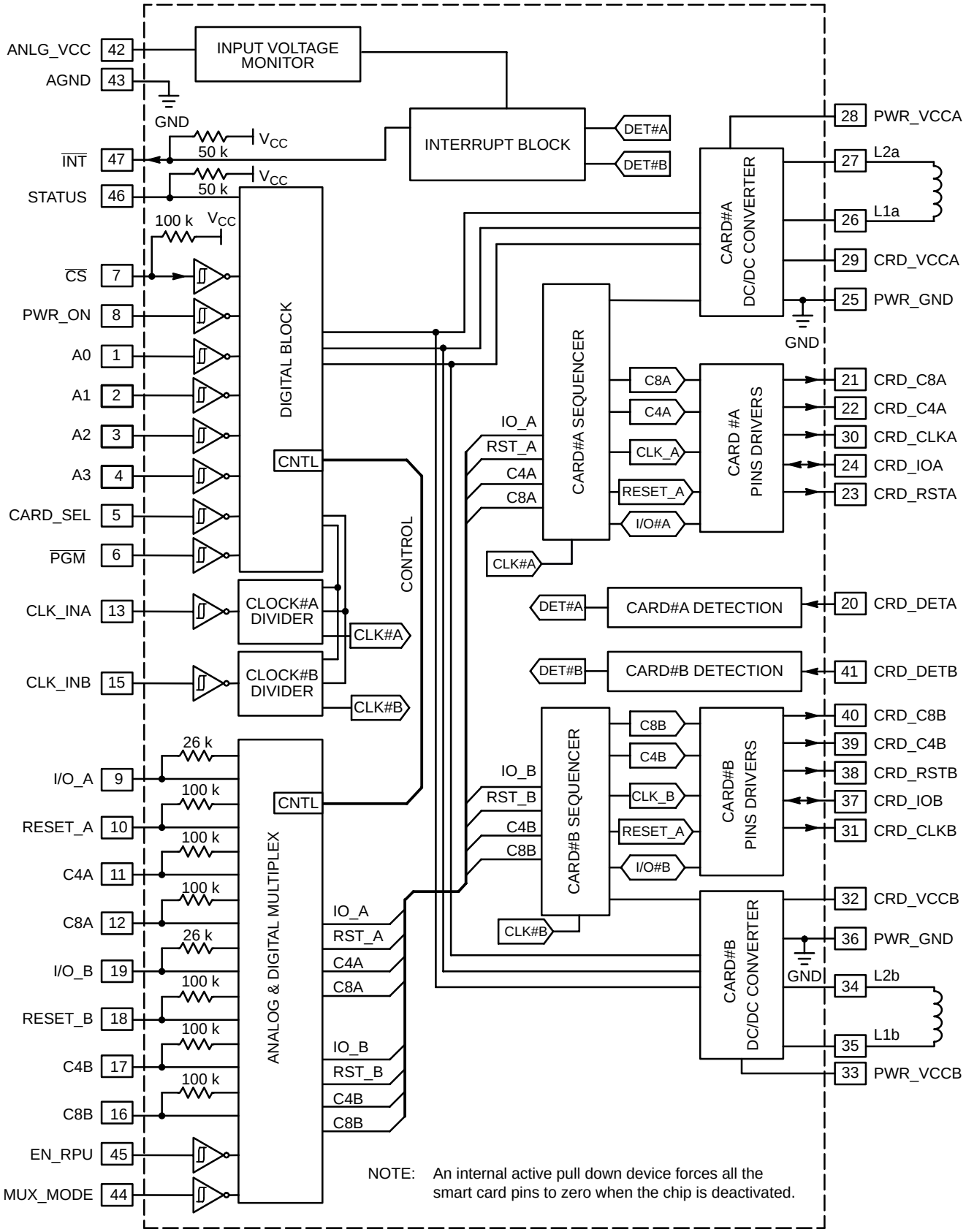


Figure 3. Block Diagram

PIN DESCRIPTION

Pin	Symbol	Type	Description
1	A0	INPUT	This pin is combined with $\overline{CS}$, A1, A2, A3, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).
2	A1	INPUT	This pin is combined with $\overline{CS}$, A0, A2, A3, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).
3	A2	INPUT	This pin is combined with $\overline{CS}$, A0, A1, A3, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).
4	A3	INPUT	This pin is combined with $\overline{CS}$, A0, A1, A2, CARD_SEL and $\overline{PGM}$ to program the chip mode of operation, the CRD_VCC voltage value, and to read the data provided by the internal STATUS register (Table 1).

5	CARD_SEL	INPUT	This pin provides logic identification of the Card #A/Card #B external smart card. The logic signal is set up by the external microcontroller.
			CARD_SEL = High → selection of the Smart Card A connected to pins 20, 21, 22, 23, 24, 29 and 30 (respectively CRD_DET_A, CRD_C8_A, CRD_C4_A, CRD_RST_A, CRD_IO_A, CRD_VCC_A and CRD_CLK_A).
			CARD_SEL = Low → selection of the Smart Card B connected to pins 41, 39, 40, 31, 38, 37, and 32 (respectively CRD_DET_B, CRD_C4_B, CRD_C8_B, CRD_CLK_B, CRD_RST_B, CRD_IO_B, and CRD_VCC_B).

6	$\overline{PGM}$	DIGITAL INPUT	This pin is combined with $\overline{CS}$, A0, A1, A2, A3, and CARD_SEL to program the chip mode of operation and to read the data provided by the internal STATUS register (Figure 4 and Table 1). $\overline{PGM}$ = H→ the NCN6004A is under normal operation and all the data with the external card can be exchanged using any of the Smart Card A or Smart Card B Lines $\overline{PGM}$ = Low → the NCN6004A runs the programming mode and related parameters can be re programmed according to a given need. In this case, the related card side logic signals are latched in their previous states and no transaction can occurs. The programmed states are latched upon the $\overline{PGM}$ rising slope (Figure 4).
7	$\overline{CS}$	DIGITAL INPUT	This pin provides the Chip Select Function for the NCN6004A device. $\overline{CS}$ = High → Pins A0, A1, A2, A3, CARD_SEL, $\overline{PGM}$, PWR_ON, RESET_A, RESET_B, C4_A, C4_B, C8_A, C8_B, I/O_A and I/O_B are disabled, the pre activated CRD_VCC maintains it's currently programmed value. $\overline{CS}$ = Low → Pins A0, A1, A2, A3, CARD_SEL, $\overline{PGM}$, PWR_ON, RESET_A, RESET_B, C4_A, C4_B, C8_A, C8_B, I/O_A and I/O_B are activated, all the functions being available.An internal pull up resistor, connected to V_{CC}, provides a logic bias when the external μP is in the high impedance state.
8	PWR_ON	DIGITAL INPUT	This pin activates or deactivates the DC/DC converter selected by CARD_SEL upon positive/negative going transient. PWR_ON = Positive going High → DC/DC Activated PWR_ON = Negative going L → DC/DC switched Off, no power is applied to the associated output CRD_VCC pin. Since uncontrolled action could take place during the rise voltage of the related CRD_VCC_x output, care must be observed to avoid a PWR_ON negative going transient during this period of time. To avoid any logical latch up, using a minimum 1.0 ms delay is recommended prior to power down the related DC/DC converter following a power up command (Figure 12).
9	I/O_A	INPUT/OUTPUT	This pin carries the data transmission between an external microcontroller and the external smart card #A. A built-in bi-directional level translator adapts the signal flowing between the card and the MCU. The level translator is enabled when $\overline{CS}$ = Low. Since a dedicated line is used to communicate the data between the MPU and the smart card, the user can activate the two channels simultaneously, assuming the μP provides a pair of I/O lines. When MUX_MODE = High, this pin provides an access to either card A or B I/O by means of CARD_SEL selection bit. On the other hand, the internal pull up resistor is automatically disconnected when MUX_MODE = High, avoiding a current overload on the I/O line, regardless of the EN_RPU logic level. This pull up resistor is under the EN_RPU control when MUX_MODE = Low.

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
10	RESET_A	INPUT	The signal present on this pin is translated to the RST pin of the external smart card #A. The $\overline{CS}$ signal must be Low to validate the RESET function, regardless of the selected card. Assuming the μP provides two independent lines to control the RESET pins, the NCN6004A can control two cards simultaneously. When MUX_MODE = High, this pin provides an access to either card A or B Reset by means of CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
11	C4_A	INPUT	This pin controls the card #A C4 contact The signal can be either de-multiplexed, at MPU level, or is multiplexed with C4_B, depending upon the MUX_MODE logic state. When MUX_MODE = High, this pin provides an access to either card A or B C4 channel by means of CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
12	C8_A	INPUT	This pin controls the card #A C8 contact. The signal can be either de-multiplexed, at MPU level, or is multiplexed with C8_B, depending upon the MUX_MODE logic state. When MUX_MODE = High, this pin provides an access to either card A or B C8 channel by means of CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
13	CLOCK_IN_A	Clock Input, High Impedance	The signal present on this pin comes from either the MCU master clock, or from any signal fulfilling the logic level and frequency specifications. This signal is fed to the internal clock selection circuit prior to be connected to the external smart card #A. Each of the external card can have different division ratio, depending upon the state of the CRD_SEL pin and associated programming bits. The built-in circuit can be programmed to 1/1, 1/2, 1/4 or 1/8 frequency division ratio. This input is valid and routed to either CRD_CLK_A _DIVIDER or CRD_CLK_B_DIVIDER regardless of the MUX_MODE state, depending upon the CLK_D_A/ CRD_D_B and CARD_SEL programmed states (Table 1). Although this input supports the signal coming from a crystal oscillator, care must be observed to avoid digital levels outside the specified V_{IH}/V_{IL} range. Similarly, the input clock signal shall have rise and fall times compatible with the operating frequency.
14	ANLG_GND	POWER	This pin is the ground reference for both analog and digital signals and must be connected to the system Ground. Care must be observed to provide a copper PCB layout designed to avoid small signals and power transients sharing the same track. Good high frequency techniques are strongly recommended.
15	CLOCK_IN_B	Clock Input, High Impedance	The signal present on this pin comes from either the MCU master clock, or from any signal fulfilling the logic level and frequency specifications. This signal is fed to the internal clock selection circuit prior to be connected to the external smart card #B. Each of the external card can have different division ratio, depending upon the state of the CRD_SEL pin and associated programming bits. The built-in circuit can be programmed to 1/1, 1/2, 1/4, or 1/8 frequency division ratio. This input is valid and routed to either CRD_CLK_B_DIVIDER or CRD_CLK_A_DIVIDER regardless of the MUX_MODE state, depending upon the CRD_D_B/CRD_D_A and CARD_SEL programmed states (Table 1). Although this input supports the signal coming from a crystal oscillator, care must be observed to avoid digital levels outside the specified V_{IH}/V_{IL} range. Similarly, the input clock signal shall have rise and fall times compatible with the operating frequency.
16	C8_B	INPUT	This pin controls the card #B C8 contact. The signal can be either de -multiplexed, at MPU level, or is multiplexed with C8_A, depending upon the MUX_MODE logic state. When MUX_MODE = High, this pin is internally disable, a pull up resistor is connected to V_{CC} (regardless of the logic state of EN_RPU is), and the access to card B takes place by C8_A associated with CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
17	C4_B	INPUT	This pin controls the card #B C4 contact. The signal can be either de -multiplexed, at MPU level, or is multiplexed with C8_A, depending upon the MUX_MODE logic state. When MUX_MODE = High, this pin is internally disable, a pull up resistor is connected to V_{CC}, (regardless of the logic state of EN_RPU), and the access to card B takes place by C4_A associated with CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
18	RESET_B	INPUT	The signal present on this pin is translated to the RST pin of the external smart card #B. The $\overline{CS}$ signal must be Low to valid the RESET function, regardless of the selected card. Assuming the μP provides two independent lines to control the RESET pins, and MUX_MODE = Low, the NCN6004A can control two cards simultaneously. When MUX_MODE = High, this pin is internally disable, a pull up resistor is connected to V_{CC}, (regardless of the logic state of EN_RPU), and the access to card B takes place by RESET_A associated with CARD_SEL selection bit. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
19	I/O_B	INPUT/OUTPUT	This pin carries the data transmission between an external microcontroller and the external smart card #B. A built-in bi-directional level translator adapts the signal flowing between the card and the MCU. The level translator is enabled when $\overline{CS}$ = Low. The signal present on this pin is latched when $\overline{CS}$ = High. Since a dedicated line is used to communicate the data between the μP and the smart card, (assuming MUX_MODE = Low) the user can activate the two channels simultaneously, assuming the μP provides a pair of I/O lines. When MUX_MODE = High, this pin is internally disable, the pull up resistor is connected to V_{CC}, (regardless of the logic state of EN_RPU), and the access to card B takes place by I/O_A associated with CARD_SEL selection bit.
20	CRD_DET_A	INPUT	This pin senses the signal coming from the external smart card connector to detect the presence of card #A. The polarity of the signal is programmable as Normally Open or Normally Close switch. The logic signal will be activated when the level is either Low or High, with respect to the polarity defined previously. By default, the input is Normally Open. A built-in circuit prevents uncontrolled short pulses to generate an INT signal. The digital filter eliminates pulse width below 50μs (see spec).
21	CRD_C8_A	OUTPUT	This pin controls the card #A C8 contact, according to the ISO7816 specifications. A built-in level shifter is used to adapt the card and the μC, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL =L, or $\overline{CS}$ = H or $\overline{PGM}$ = L, and resume to a transparent mode when card #A is selected and operates in the transfer mode.The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_A start-up time.
22	CRD_C4_A	OUTPUT	This pin controls the card #A C4 contact, according to the ISO7816 specifications. A built-in level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL = L, or $\overline{CS}$ = H, or $\overline{PGM}$ = L, and resume to a transparent mode when card #A is selected and operates in the transfer mode. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_A start-up time.
23	CRD_RST_A	OUTPUT	This pin is connected to the external smart card #A to support the RESET signal. A built-in level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL = Low, or when $\overline{CS}$ or $\overline{PGM}$ returns to a High, and resume to a transparent mode when card #A is selected. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_A start-up time.

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
24	CRD_IO_A	INPUT/OUTPUT	This pin carries the data serial connection between the external smart card #A and the microcontroller. A built-in bidirectional level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. This pin is biased by a pull up resistor connected to CRD_VCC_A. When $\overline{CS}$ = High, the CRD_IO_A holds the previous I/O logic state and resume to a normal operation when this pin is reactivated. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_A start-up time.
25	PWR_GND	POWER	This pin carries the power current flow coming from the built in DC/DC converters. It is associated with the external card # A. It must be connected to the system Ground and care must be observed at PCB layout level to avoid the risk of spike voltages on the logic lines.
26	L2_A	POWER	Connects one side of the external DC/DC converter inductor #A (Note 1)
27	L1_A	POWER	Connects one side of the external DC/DC converter inductor #A (Note 1).
28	PWR_VCC_A	POWER	This pin is connected to the positive external power supply. The device sustains any voltage from +2.7 V to +5.5 V. This voltage supplies the NCN6004A internal circuits and is regulated by the internal DC/DC converter to provide the DC voltage to the external card. A high quality capacitor must be connected across pin 28 and PWR_GND, 10 μF/6.0 V ceramic X7R or X5R type is recommended. Note: The voltage present at pin 28 and 33 must be equal to the voltage present at pin 42.
29	CRD_VCC_A	POWER	This pin provides the power supply to the external smart card #A. The V_{CC} voltage is defined by programming the NCN6004A accordingly. Since the cards have independent DC/DC converter, the output voltage can have any value independently from CARD_B. A high quality, low ESR capacitor is mandatory to achieve the V_{CC} specifications. Using two 4.7 μF/6.0 V ceramic X7R or X5R capacitors in parallel is recommended.
30	CRD_CLK_A	OUTPUT	This pin is connected to the CLK external smart card #A pin. The signal comes from the built- in frequency divider dedicated to the #A card. The clock is selected and controlled by setting the logic inputs according to Table 1. The slope of the output clock can be selected between one of the two programmable mode: SLOW or FAST (Table 8). The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_A start- up time.
31	CRD_CLK_B	OUTPUT	This pin is connected to the CLK external smart card #B pin. The signal comes from the built- in frequency divider dedicated to the #B card. The clock is selected and controlled by setting the logic inputs according to Table 1. The slope of the output clock can be selected between one of the two programmable mode: SLOW or FAST (Table 8). The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_B start- up time.
32	CRD_VCC_B	POWER	This pin provides the power supply to the external smart card #B. The V_{CC} voltage is defined by programming the NCN6004A accordingly. Since the cards have independent DC/DC converter, the output voltage can have any value independently from CARD_A. A high quality, low ESR capacitor is mandatory to achieve the V_{CC} specifications. Using two 4.7 μF/6.0 V ceramic X7R or X5R capacitors in parallel is recommended.
33	PWR_VCC_B	POWER	This pin is connected to the positive external power supply. The device sustains any voltage from +2.7 V to +6.0 V. This voltage supplies the NCN6004A internal circuits and is regulated by the internal DC/DC converter to provide the DC voltage to the external card. A high quality capacitor must be connected across pin 33 and PWR_GND, 10 μF/6.0 V ceramic X7R type is recommended. Note: The voltage present on pin 28 and 33 must be equal to the voltage present on pin 42
34	L2b	POWER	Connects one side of the external DC/DC converter inductor #B (Note 1).
35	L1b	POWER	Connects one side of the external DC/DC converter inductor #B (Note 1).
36	PWR_GND	POWER	This pin carries the power current flow coming from the built in DC/DC converters. It is associated with the external card # B. It must be connected to the system Ground and care must be observed at PCB layout level to avoid the risk of spike voltages on the logic lines.

1. The external inductors shall preferably have the same values. Depending upon the power absorbed by the load, the inductor can range from 10 μH to 47 μH. To achieve the highest yield, the inductor shall have an ESR < 1.0 Ω.

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
37	CRD_IO_B	INPUT/OUTPUT	This pin carries the data serial connection between the external smart card #B and the microcontroller. A built-in bi-directional level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. This pin is biased by a pull up resistor connected to CRD_VCC_A. When $\overline{CS}$ = High, the CRD_IO_A holds the previous I/O logic state and resume to a normal operation when this pin is reactivated. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_B start-up time.
38	CRD_RST_B	OUTPUT	This pin is connected to the external smart card #B to support the RESET signal. A built-in level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL or $\overline{CS}$ or $\overline{PGM}$ positive going transient and resume to a transparent mode when card #B is selected. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_B start-up time.
39	CRD_C4_B	OUTPUT	This pin controls the card #B C4 contact, according to the ISO specification. A built-in level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL or $\overline{CS}$ or $\overline{PGM}$ positive going transient and resume to a transparent mode when card #B is selected. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_B start-up time.
40	CRD_C8_B	OUTPUT	This pin controls the card #B C8 contact, according to the ISO specification. A built-in level shifter is used to adapt the card and the MCU, regardless of the power supply voltage of each signals. The signal present at this pin is latched upon either CARD_SEL or $\overline{CS}$ or $\overline{PGM}$ positive going transient and resume to a transparent mode when card #B is selected. The pin is hardwired to zero, the bias being provided by the V_{CC} supply, when either the V_{CC} voltage drops below 2.7 V, or during the CRD_VCC_B start-up time.
41	CRD_DET_B	INPUT	This pin senses the signal coming from the external smart card connector to detect the presence of card #B. The polarity of the signal is programmable as Normally Open or Normally Close switch. The logic signal will be activated when the level is either Low or High, with respect to the polarity defined previously. By default, the input is Normally Open. A built-in circuit prevents uncontrolled short pulses to generate an INT signal. The digital filter eliminates pulse width below 50 μs.
42	ANLG_VCC	POWER	This pin is connected to the positive external power supply. The device sustains any voltage from +2.7 V to +5.5 V. This voltage supplies the NCN6004A internal Analog and Logic circuits. A high quality capacitor must be connected across this pin and ANLG_GND, 10 μF/6 V is recommended. A set of extra pins (28 and 33) are provided to connect the power supply to the internal DC/DC converter. Note: The voltage present at pin 28 and 33 must be equal to the voltage present at pin 42
43	ANLG_GND	GROUND	This pin is the ground reference for both analog and digital signals and must be connected to the system Ground. Care must be observed to provide a copper PCB layout designed to avoid small signals and power transients sharing the same track. Good high frequency techniques are strongly recommended.
44	MUX_MODE	INPUT	This pin selects the mode of operation of the card signals from the MPU side. When MUX_MODE = Low, all the card signals are fully de-multiplexed and data transfers can take place with both cards simultaneously. On top of that, both cards can be accessed during the programming sequence, assuming the external microcontroller is capable to run multi tasks software. When MUX_MODE = High, all the card signals are multiplexed and the communications with the cards shall take place in a sequential mode. The card is selected by setting CARD_SEL high or Low. The internal logic will disable the CARD_B inputs and use CARD_SEL inputs as a single channel to controls both output smart cards sequentially when MUX_MODE = H. Moreover, when MUX_MODE = High, all the B channel μP dedicated pins, except CLOCK_IN_B, pin 15, are forced to a high level by means of internal pull up resistors. It is not necessary to connect these pins (16, 17, 18 and 19) to an external bias voltage, but it is mandatory to avoid any connections to ground. On the other hand, in this case the internal pull up resistor connected across I/O_A, pin 9 and V_{CC} is automatically disconnected to avoid a current overload on the I/O line.

PIN DESCRIPTION (continued)

Pin	Symbol	Type	Description
45	EN_RPU	INPUT	This pin provides a logic input to valid or not the internal pull up resistors connected across each I/O, RESET, C4 and C8 lines and ANLG_VCC. When EN_RPU = High, the pull up resistors are connected When EN_RPU = Low, the pull up resistors are disconnected and it is up to the designer to set up the external resistor to cope with the ISO/EMV specifications. The logic signal must be set up prior to apply the ANLG_VCC supply. Once the logic mode has been acknowledged by the internal Power On reset, it cannot be changed until a new start-up sequence is launched.
46	STATUS	OUTPUT	This pin provides a logic state related to the card [A or B] insertion, the VCC_OK, the CRD_VCC value and the current overflow powered to either card [A or B]. The internal register can be read when $\overline{PGM}$ = High. The logic level is forced to High when the input voltage drops below the V_{bat} min (2.0 V), thus reducing the stand by current, assuming the STATUS pin is not pulled down externally. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
47	$\overline{INT}$	OUTPUT	This pin is activated LOW when a card has been inserted and detected in either of the external ports. The signal is reset by either a positive going transition on pin $\overline{CS}$, or by a High level on pin PWR_ON combined with $\overline{CS}$ = Low. Similarly, an interrupt is generated when either one of the CRD_VCC output is overloaded. On the other hand, the pin is forced to a logic High when the input voltage V_{CC} drops below 2.0 V min. The associated pull up resistor is either connected to V_{CC} (EN_RPU = H) or disconnected when EN_RPU = Low.
48	ANLG_GND	GROUND	This pin is the ground reference for both analog and digital signals and must be connected to the system Ground. Care must be observed to provide a copper PCB layout designed to avoid small signals and power transients sharing the same track. Good high frequency techniques are strongly recommended.

MAXIMUM RATINGS (Note 2)

Rating	Symbol	Value	Unit
Power Supply Input Supply Voltage	V_{CC}	6	V
V_{in}	Digital Input Pins	-0.5 V < V_{in}< V_{CC} +0.5 V, but < 6.0 V	V
Power Supply Input Current	IV_{CC}	500	mA
Digital Input Pins	V_{in} In	-0.5 < V_{CC} or V_{CC} < 5.5 ± 5	V mA
Digital Output Pins	V_{out} I_{out}	-0.5 < V_{CC} or V_{CC} < 5.5 ±10	V mA
Card Interface Pins	V_{card} I_{card}	-0.5V < V_{card} < CRD_VCC +0.5V 15 mA (internally limited)	V mA
ESD Capability, Human Body Model (Note 3) Standard Pins Card Interface Pins (Card A or B)	V_{ESD}	 2 8	 kV kV
TQFP48 Power Dissipation @ Tab = +85°C Thermal Resistance Junction-to-Air	 P_D $R_{J\theta A}$	 800 50	 mW °C/W
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Maximum Junction Temperature (Note 4)	T_{Jmax}	+150	°C
Storage Temperature Range	Tag	-65 to +150	°C

2. Maximum Electrical Ratings are defined as those values beyond which damage(s) to the device may occur at T_A = +25°C.
3. Human Body Model, R = 1500 Ω, C = 100 pF.
4. Absolute Maximum Rating beyond which damage(s) to the device may occur.

POWER SUPPLY SECTION General test conditions, unless otherwise specified: Operating temperature: -25°C < T_A < +85°C, V_{CC} = +3.0 V, CRD_VCC_A = CRD_VCC_B = +5.0 V.

Rating	Symbol	Pin	Min	Typ	Max	Unit
I_{out} = 2 x 65 mA (both external cards running simultaneously) @ 3.0 V < V_{CC} < 5.5 V	CRD_VCC	29, 32	4.6	-	5.4	V
I_{out} = 2 x 55 mA per pin (both external cards running) V_{out} defined @ CRD_VCC = 3.0 V @ 3.0 V < V_{CC} < 5.5 V	CRD_VCC	29, 32	2.7	-	3.3	V
I_{out} = 2 x 35 mA per pin (both external cards running) V_{out} defined @ CRD_VCC = 1.80 V @ 3.0 V < V_{CC} < 5.5 V	CRD_VCC	29, 32	1.65	-	1.95	V
Output Card Supply Voltage Ripple (per CRD_VCC outputs) @ : L_{out} = 22 μH, L_{ESR} < 2.0 Ω, C_{out} = 10 μF per CRD_VCC (Note 5) I_{out} = 35 mA, V_{out} = 1.80 V I_{out} = 55 mA, V_{out} = 3.0 V I_{out} = 65 mA, V_{out} = 5.0 V	 V_{ORA} V_{ORB}	 29 32	 - - -	 - - -	 50 50 50	mV
DC/DC Dynamic Inductor Peak Current @ V_{bat} = 5.0 V, L_{out} = 22 μH, C_{out} = 10 μF CRD_VCC = 1.8 V CRD_VCC = 3.0 V CRD_VCC = 5.0 V	I_{ccov}	29, 32	 - - -	 200 280 430	 - - -	mA
Standby Supply Current Conditions (Note 5): ANLG_VCC = PWR_VCC = 3.0 V PWR_ON = H, STATUS = H, $\overline{CS}$ = H Card A and Card B CLOCK_IN = H, I/O = H, RESET = H All Logic Inputs = H, Temperature range = 0°C to +50°C ANLG_VCC = PWR_VCC = 5.0 V Temperature range –25°C to +85°C All other test conditions identical ANLG_VCC = PWR_VCC = 1.8 V Temperature range –25°C to +50°C All other test conditions identical Note: This parameter is guaranteed by design, not production tested.	I_{DD}	42, 28, 33	 - - - - - - -	 	 20 - - 50 - - 5.0 -	μA
Operating Supply Current ANLG_VCC = PWR_VCC = 5.5 V @ CRD_VCC_A/B = 5.0 V @ CRD_VCC_ A/B = 3.0 V @ CRD_VCC_ A/B = 1.85 V ANLG_VCC = PWR_VCC = 3.3 V @ CRD_VCC_A/B = 5.0 V @ CRD_VCC_ A/B = 3.0 V @ CRD_VCC_ A/B = 1.85 V PWR_ON = H, $\overline{CS}$ = H, CLK_A = CLK_B = Low, all card pins unloaded	I_{DDop}	42, 28, 33	 	 0.7 0.7 0.7 0.2 0.2 0.2	 	mA
V_{bat} Under Voltage Detection Positive Going Slope V_{bat} Under Voltage Detection Negative Going Slope V_{bat} Under Voltage Detection Hysteresis Note: The voltage present in pins 28 and 33 must be equal to or lower than the voltage present in pin 42.	V_{batLH} V_{batLL} V_{batHY}	42	2.1 2.0 -	- - 100	2.7 2.6 -	V V mV
Output Continuous Current Card A or Card B (both cards can be operating simultaneously) @ 3.0 < V_{CC} < 5.5 V Output Voltage = 1.85 V Output Voltage = 3.0 V Output Voltage = 5.0 V	I_{ccp}	31, 42	 35 55 65			mA
Output Over Current Limit (A or B) V_{bat} = 3.3 V, CRD_VCC = 1.8 V, 3.0 V or 5.0 V V_{bat} = 5.0 V, CRD_VCC = 1.8 V, 3.0 V or 5.0 V	I_{ccov}	31, 42		 100 150		mA
Output Over Current Time Out Per Card	I_{tdoff}	31, 42		4.0		ms
Output Card Supply Turn On Time @ L_{out} = 22 μF, C_{out} = 10 μF Ceramic. V_{CC} = 2.7 V, CRD_VCC = 5.0 V (A or B)	V_{CCTON}	31, 42			 500	μs

5. Assuming ANLG_VCC and PWR_VCC pins are connected to the same power supply.

POWER SUPPLY SECTION General test conditions, unless otherwise specified: Operating temperature: -25°C < T_A < +85°C, V_{CC} = +3.0 V, CRD_VCC_A = CRD_VCC_B = +5.0 V. (continued)

Rating	Symbol	Pin	Min	Typ	Max	Unit
Output Card Supply Shut Off Time @ C_{out} = 10 μF, ceramic. V_{CC} = 2.7 V, CRD_VCC = 5.0 V, V_{CCOFF} < 0.4 V (A or B)	V_{CCTOFF}	31, 42		100	250	μs
DC/DC Converter Operating Frequency (A or B)	F_{SW}	31, 42		600		kHz

5. Assuming ANLG_VCC and PWR_VCC pins are connected to the same power supply.

DIGITAL INPUT/OUTPUT SECTION

2.70 < V_{CC} < 5.50 V, Normal Operating Mode (-25°C to +85°C ambient temperature, unless otherwise noted)

Rating	Symbol	Pin	Min	Typ	Max	Unit
A0, A1, A2, A3, CARD_SEL, PWR_ON, $\overline{PGM}$, $\overline{CS}$, MUX_MODE, EN_RPU, RESET_A, RESET_B, C4_A, C8_A, C4_B, C8_B High Level Input Voltage Low Level Input Voltage Input Capacitance	 V_{IH} V_{IL} C_{in}	1, 2, 3, 4, 5, 6, 7, 8, 44, 45, 10, 18, 11, 12, 16, 17	 0.7 * V_{bat}		 V_{bat} 0.3 * V_{bat} 10	 V V pF
STATUS, $\overline{INT}$ Output High Voltage @ I_{OH} = -10 μA Output Low Voltage @ I_{OH} = 200 μA	 V_{OH} V_{OL}	46, 47	 V_{bat} –1.0 V		 0.40	V
STATUS, $\overline{INT}$ Output Rise Time @ C_{out} = 30 pF Output Fall Time @ C_{out} = 30 pF	 trsta, trint tfsta, tfint				 5 100	 μs ns
CLOCK_A Asynchronous Input Clock @ DC = 50% ±1%	F_{CLKINA}	13			40	MHz
CLOCK_B Asynchronous Input Clock @ DC = 50% ±1%	F_{CLKINB}	15			40	MHz
I/O_A, I/O_B, both directions @ C_{out} = 30 pF I/O Rise Time I/O Fall Time	 t_{rioA}, t_{rioB} t_{fioA}, t_{fioB}	9, 19			 0.8 0.8	μs
STATUS Pull Up Resistance	R_{STA}	46	35	50		kΩ
INT Pull Up Resistance	R_{INT}	47	35	50		kΩ
I/O_A Pull Up Resistance	R_{IOA}	9	14	20	35	kΩ
I/O_B Pull Up Resistance	R_{IOB}	19	14	20	35	kΩ
RESET_A Pull Up Resistance	R_{RSTA}	10	60	100		kΩ
RESET_B Pull Up Resistance	R_{RSTB}	18	60	100		kΩ
C4_A Pull Up Resistance	R_{C4A}	11	60	100		kΩ
C8_A Pull Up Resistance	R_{C8A}	12	60	100		kΩ
C4_B Pull Up Resistance	R_{C4B}	17	60	100		kΩ
C8_B Pull Up Resistance	R_{C8B}	16	60	100		kΩ
CS Pull Up Resistance	R_{CS}	7	60	100		kΩ
CRD_DET_A and CRD_DET_B Pull Up Resistance	R_{DETA} R_{DETB}	20 41		500 500		kΩ kΩ

CARD INTERFACE SECTION @ 2.70 < V_{CC} < 5.50 V, Normal Operating Mode (-25°C to +85°C ambient temperature, unless otherwise noted) CRD_VCC_A = CRD_VCC_B = 1.8 V or 3.0 V or 5.0 V

Rating	Symbol	Pin	Min	Typ	Max	Unit
CRD_RST_A, CRD_RST_B Output Voltage						
Output RST High Level @ Irst = -200 μA	V_{OH}	23, 38	CRD_VCC-0.5		CRD_VCC	V
Output RST Low Level @ Irst = 200 μA	V_{OL}	23, 38	0		0.4	V
CRD_RST_A, CRD_RST_B Rise and Fall time						
RST Rise Time @ C_{out} = 30 pF	trrst	23, 38			100	ns
RST Fall Time @ C_{out} = 30 pF	tfrst	23, 38			100	ns
CRD_CLK_A, CRD_CLK_B Output Clock		30, 31				
Output Operating Clock Card A and Card B	F_{clkA}, F_{clkB}				20	MHz
Output Operating Clock DC, Card A and Card B (Input DC = 50%, ±1%)			45		55	%
Note: This parameter is guaranteed by design, functionality 100% tested at production.						
Output Operating Clock Rise Time SLOW Mode Card A and Card B	trclka, trclkb				16	ns
Output Operating Clock Fall Time SLOW Mode Card A and Card B	tfclka, tfclkb				16	ns
Output Operating Clock Rise Time FAST Mode Card A and Card B	trclka, trclkb				4	ns
Output Operating Clock Fall Time FAST Mode Card A and Card B	tfclka, tfclkb				4	ns
Output Clock High Level, Card A and Card B, @ Iclk = -200 μA	V_{OH}		CRD_VCC-0.5		CRD_VCC	V
Output Clock Low Level, Card A and Card B, @ Iclkc = 200 μA	V_{OL}		0		0.4	V
CRD_IO_A, CRD_IO_B Data Transfer		24, 37				
Data Transfer Frequency, Card A and Card B	F_{IOA}, F_{IOB}			400		kHz
Data Rise Time, Card A and Card B, @ C_{out} = 30 pF	t_{rioa}, t_{riob}				0.8	μs
Data Fall Time, Card A and Card B, @ C_{out} = 30 pF	t_{fioa}, t_{fiob}				0.8	μs
Data Output High Level, Card A and Card B @ Icrd_io = -20 μA	V_{OH}		CRD_VCC-0.5		CRD_VCC	V
Data Output Low Level, Card A and Card B @ Icrd_io = 20 μA	V_{OL}		0		0.4	V
CRD_IO_A and CRD_IO_B Output Voltages		24, 37				V
I/O_A = I/O_B = 0, I_{OL} = 500 μA	V_{OL}				0.40	
CRD_C4_A, CRD_C4_B Output Voltages		22, 39				
Output C4 High Level @ Irst = -200 μA	V_{OH}		CRD_VCC-0.5		CRD_VCC	V
Output C4 Low Level @ Irst = 200 μA	V_{OL}		0		0.4	V
CRD_C4_A, CRD_C4_B Rise and Fall time						
C4 Rise Time @ C_{out} = 30 pF	trc_4				100	ns
C4 Fall Time @ C_{out} = 30 pF	tfc_4				100	ns
CRD_C8_A, CRD_C8_B Output Voltages		21, 40				
Output C4 High Level @ Irst = -200 μA	V_{OH}		CRD_VCC-0.5		CRD_VCC	V
Output C4 Low Level @ Irst = 200 μA	V_{OL}		0		0.4	V
CRD_C8_A, CRD_C8_B Rise and Fall Time						
C8 Rise Time @ C_{out} = 30 pF	trc_8				100	ns
C8 RST Fall Time @ C_{out} = 30 pF	tfc_8				100	
Pull Up resistance, $\overline{CS}$ = Low, PWR_ON = High						kΩ
CRD_IO_A	R_{OLA}	24	14	20	35	
CRD_IO_B	R_{OLB}	37	14	20	35	
Card Detection Bias Pull Up Current, Card A or Card B	I_{DETA}	20		15		μA
CRD_DET_A, CRD_DET_B	I_{DETB}	41		15		
Card Insertion/Extraction Negative Going Input Low Voltage	V_{ILDETA}	20	0		0.30 * V_{bat}	V
	V_{ILDETB}	41	0		0.30 * V_{bat}	
Card Detection Insertion/Extraction Digital Filtering Delay						μs
CRD_DET_A	t_{dcina}	20		50		
CRD_DET_B	t_{dcinb}	41		50		
CARD_A or CARD_B short circuit current:						mA
CRD_IO, CRD_RST, CRD_C4, CRD_C8	Ishort				15	
CRD_CLK	Ishortclk				70	
(According to ISO and EMV specifications)						

DIGITAL DYNAMIC SECTION NORMAL OPERATING MODE

Rating	Symbol	Pin	Min	Typ	Max	Unit
Card Signal Sequence Interval, CRD_VCC_A and CRD_VCC_B: CRD_IO_A, CRD_RST_A, CRD_CLK_A, CRD_C4_A, CRD_C8_A CRD_IO_B, CRD_RST_B, CRD_CLK_B, CRD_C4_B, CRD_C8_B	td_{seq}	24, 23, 30, 37, 38, 31		 0.5 0.5	 2 2	μs
Internal RESET Delay	td_{reset}			1.0		μs
Internal STATUS Delay Time	td_{ready}	46		1.0		μs
PWR_ON Low State Pulse Width (Figure 11), Assuming CRD_VCC reservoir capacitor = 10 μF.	t_{pwrlow}	8	 5			μs
PWR_ON High State Pulse Width (Figure 11)	t_{pwrset}	8	200			ns
PWR_ON Preset Delay (Figure 11)	t_{pwrpre}	5, 7, 8	300			ns
PWR_ON Programming Hold Time (Figure 11)	$t_{pwrhold}$	5, 7, 8	100			ns
PWR_ON to CARD_SEL Change Delay Time (Figure 12)	$t_{cseldly}$	5, 6, 8	100			ns
$\overline{PGM}$ to PWR_ON Delay Time (Figure 12)	tpgmdly	5, 6, 8	300			ns
PWR_ON internal Set/Reset Pulses Width (Figure 12)	tpwrp	8		20		ns

DIGITAL DYNAMIC SECTION PROGRAMMING MODE

Rating	Symbol	Pin	Min	Typ	Max	Unit
Data Set-up Time, Time Reference = $\overline{PGM}$, A0, A1, A2, A3, CARD_SEL, and $\overline{CS}$. Data Signal Rise and Fall Time	t_{smod} t_{smodtr}	8, 46, 1, 2, 3, 4, 5, 6	100		 50	ns ns
Data Hold Time, Time Reference = $\overline{PGM}$, A0, A1, A2, A3, CARD_SEL, and $\overline{CS}$.	t_{smod} t_{smodtr}	8, 46, 1, 2, 3, 4, 5, 6	100		 50	ns ns
Chip Select $\overline{CS}$ Low State Pulse Width $\overline{CS}$ Signal Rise and Fall Time	t_{wcs} t_{rfcs}	7	300		 50	ns ns

PROGRAMMING AND STATUS FUNCTIONS

The NCN6004A includes a programming interface and a status interface. Figure 4 illustrates the sequence one must follow to enter and exit the programming mode. Table 1 and Table 2 provide the logical functions associated with the input and output signals. The parameters are latched upon the rising edge of the $\overline{PGM}$ signal, the $\overline{CS}$ pin being held low. Any number of programming sequences can be performed while the $\overline{CS}$ pin is Low, but the minimum timings must be observed.

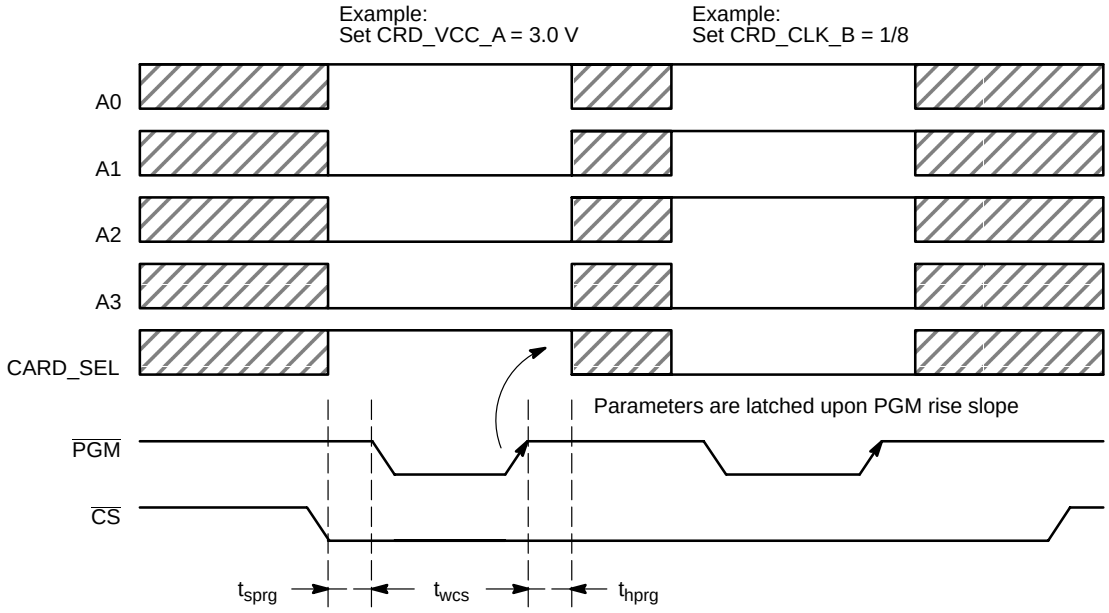


Figure 4. Programming Sequence

On the other hand, since the programming data are latched upon the rising edge of the $\overline{PGM}$ signal, the most up to date selected card (using CARD_SEL = H or L) is used to activate the associated card. Consequently, when both cards must be updated with the same programmed content, a dual $\overline{PGM}$ sequence must be carried out, changing the CARD_SEL signal during the High level state of the $\overline{PGM}$ pin.

Although selecting a card in possible during the same Chip Select sequence (as depicted here above), the user must make sure that no data will be present to a card not ready for such a function. As a matter of fact, all the card signals are routed to the selected card immediately after a CARD_SEL change, the NCN6004A taking no further logic control prior to activate the swap. To avoid any risk, one can run a sequence with the selected card, return $\overline{CS}$ to High, change the CARD_SEL according to the expected card selection, and pull $\overline{CS}$ to Low to activate the selected card.

Table 1. Programming and Reading Basic Functions

Pin	Name	Select #A #B	Select V_{CC} ON/OFF	Program CLOCK_IN	Poll Card Status #A or #B	Poll I_{CC} Overload #A or #B	ANLG_VCC Input Voltage OK
7	$\overline{CS}$	0	0	0	0	0	0
46	STATUS	-	-	-	READ	READ	READ
1	A0	0/1	0/1	0/1	1	0	0
2	A1	0/1	0/1	0/1	1	1	0
3	A2	0/1	0/1	0/1	X	X	X
4	A3	0/1	0/1	0/1	X	X	X
5	CARD_SEL	0/1	0/1	0/1	0/1	0/1	0/1
6	$\overline{PGM}$	0/1	0/1	0/1	1	1	1

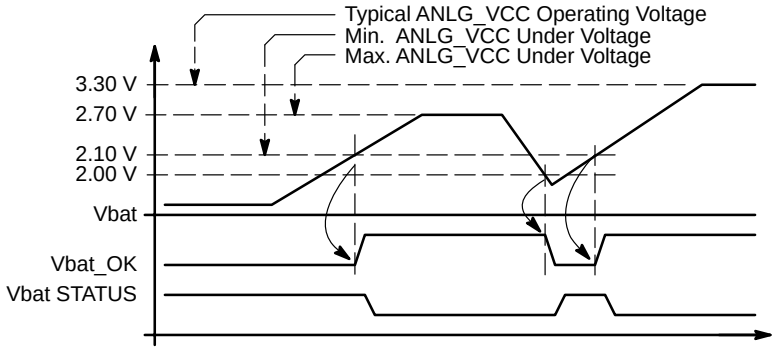
Table 2. Programming Functions (Conditions at start-up are in **Bold**)

(HEX)	$\overline{PGM}$	A3	A2	A1	A0	CARD_SEL	CRD_V_{CC} #A	CRD_VCC #B	CRD_CLK #A	CRD_CLK #B	CRD_DET #A	CRD_DET #B	CLOCK SLOPE
00	0	0	0	0	0	1	1.80 V	-	-	-	-	-	-
01	**0**	**0**	**0**	**0**	**1**	**1**	**3.0 V**	**-**	**-**	**-**	**-**	**-**	**-**
02	0	0	0	1	0	1	5.0 V	-	-	-	-	-	-
03	**0**	**0**	**0**	**1**	**1**	**1**	**-**	**-**	**-**	**-**	**-**		**SLOW**
00	0	0	0	0	0	0	-	1.80 V	-	-	-	-	-
01	**0**	**0**	**0**	**0**	**1**	**0**	**-**	**3.0 V**	**-**	**-**	**-**	**-**	**-**
02	0	0	0	1	0	0	-	5.0 V	-		-	-	-
03	**0**	**0**	**0**	**1**	**1**	**0**	**-**	**-**	**-**	**-**	**-**	**-**	**SLOW**
04	**0**	**0**	**1**	**0**	**0**	**1**	**-**	**-**	**1/1**		**-**	**-**	**-**
05	0	0	1	0	1	1	-	-	1/2	-	-	-	-
06	0	0	1	1	0	1	-	-	1/4	-	-	-	-
07	0	0	1	1	1	1	-	-	1/8	-	-	-	
04	**0**	**0**	**1**	**0**	**0**	**0**	**-**	**-**	**-**	**1/1**	**-**	**-**	**-**
05	0	0	1	0	1	0	-	-	-	1/2	-	-	-
06	0	0	1	1	0	0	-	-	-	1/4	-	-	-
07	0	0	1	1	1	0	-	-	-	1/8	-	-	-
08	**0**	**1**	**0**	**0**	**0**	**1**	**-**	**-**	**START**	**-**	**-**	**-**	**-**
09	0	1	0	0	1	1	-	-	STOPL	-	-	-	-
0A	0	1	0	1	0	1	-	-	STOPH	-	-	-	-
0B	0	1	0	1	1	1	-	-	-	**-**	-	-	FAST
08	**0**	**1**	**0**	**0**	**0**	**0**	**-**	**-**	**-**	**START**	**-**	**-**	**-**
09	0	1	0	0	1	0	-	-	-	STOPL	-	-	-
0A	0	1	0	1	0	0	-	-	-	STOPH	-	-	-
0B	0	1	0	1	1	0	-	-	-	-	**-**	-	FAST
0C	**0**	**1**	**1**	**0**	**0**	**1**	**-**	**-**	**-**	**-**	**NO**	**-**	**-**
OD	0	1	1	0	1	1	-	-	-	-	NC		-
0C	**0**	**1**	**1**	**0**	**0**	**0**	**-**	**-**	**-**	**-**	**-**	**NO**	**-**
0D	0	1	1	0	1	0						NC	-
0E	**0**	**1**	**1**	**1**	**0**	**1**	**-**	**-**	**CLK_D_A**	**-**	**-**	**-**	**-**
0F	0	1	1	1	1	1	-	-	CLK_D_B	-	-	-	-
0E	**0**	**1**	**1**	**1**	**0**	**0**	**-**	**-**	**-**	**CLK_D_B**	**-**	**-**	**-**
0F	0	1	1	1	1	0	-	-	-	CLK_D_A	-	-	-

Table 3. Status Pins Data

STATE (HEX)	$\overline{PGM}$	A3	A2	A1	A0	CARD_SEL	STATUS #A	STATUS #B
00	1	X	X	0	0	X	Vcc_V_{bat}_OK Pass = Low VCC_OK Fail = High	
01	1	X	X	0	1	1	CRD_VCC_A In Range Pass = High Fail =Low	
02	1	X	X	1	0	1	CRD_VCCA Overloaded Pass = High Fail = Low	
03	1	X	X	1	1	1	CRD_DET_A Card Present = High	
00	1	X	X	0	0	X		VCC_OK Pass = Low VCC_OK Fail = High
01	1	X	X	0	1	0		CRD_VCC_B In Range Pass = High Fail =Low
02	1	X	X	1	0	0		CRD_VCC_B Overloaded Pass = High Fail = Low
03	1	X	X	1	1	0		CRD_DET_A Card Present = High

*The STATUS register is not affected when the NCN6004A operates in any of the programming mode. Initialized conditions upon start-up are depicted by bold characters in Table 2 and Table 4.



The input power supply voltage monitoring applies to the card selected.

Figure 5. Reading ANLG_VCC Status (monitoring ANLG_VCC input voltage)

SYSTEM STATES UPON UPON START-UP

Table 4. Operating Conditions Upon Start-up

CRD_VCC_A	3.0 V
CRD_VCC_B	3.0 V
CRD_CLK_A	1/1 Ratio
CRD_CLK_B	1/1 Ratio
CRD_CLK_A	START (clock is valid)
CRD_CLK_B	START (clock is valid)
CRD_CLK_A	Low Speed Slope
CRD_CLK_B	Low Speed Slope
CLOCK Route	Direct (CLK_A $\rightarrow$ A, CLK_B $\rightarrow$ B)

Depending upon the logic state at turn on present on pin 44, the system will run into a parallel mode (MUX_MODE = L) or a multiplexed mode (MUX_MODE = H). It is not possible to change the logic state once the system is running.

Similarly, depending upon the logic state present pin 45, the internal pull up resistors (I/O_A and I/O_B line) will be either connected to ANLG_VCC voltage (EN_RPU = H) or disconnected (EN_RPU = L). It is not possible to change this operating condition once the system is running.

PARALLEL/MULITPLEXED OPERATION MODES

The logic input MUX_MODE, pin 44, provides a way to select the operation mode of the NCN6004A. Depending upon the logic level, the device operates either in a parallel mode (all the card pins, on the μP side, are fully independent) or in multiplexed mode (all the logic card pins, on the μP side, share a common bus). Figure 6 shows a simplified schematic of the multiplex circuit built in the NCN6004A chip.

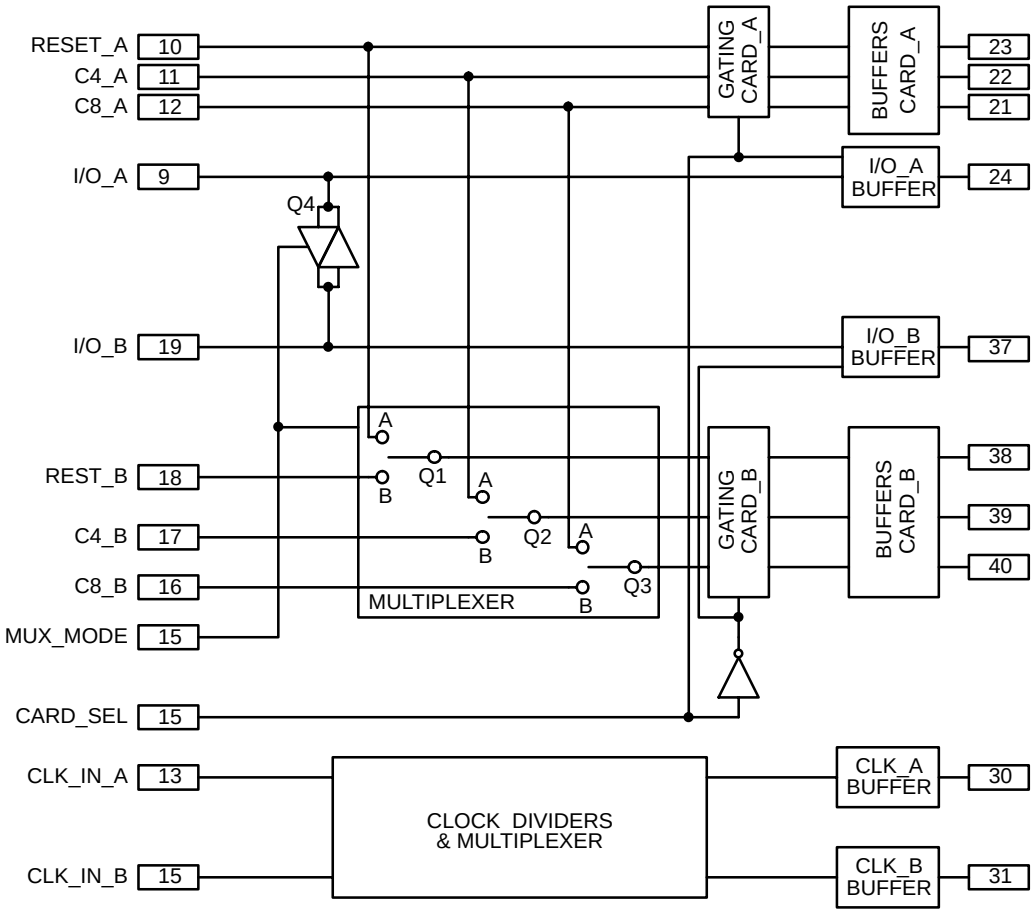


Figure 6. Simplified MUX_MODE Logic and Multiplex Circuit

In both case, the device is programmed by means of the common logic controls pins (A0, A1, A2, A3, $\overline{PGM}$, PWR_ON, CARD_SEL and $\overline{CS}$). On the other hand, the logic status returned by the interface (STATUS pin 46) is shared by the two channels and can be read independently by setting CARD_SEL accordingly.

The card related signals connected on the μC side are multiplexed or independent, depending upon the MUX_MODE state as described here below.

MUX_MODE = Low → PARALLEL MODE

When pin 44 is low, the device operates in the parallel mode. The transfer gate Q4 and the multiplexer circuit are disconnected and all the data will be carried out through their respective paths. The switches Q1, Q2 and Q3 are flipped to the B position, thus providing a direct connection from port B control signals to CARD_B

All the CARD_A and CARD_B signals are independent and both cards can operate simultaneously, the data transaction can take place at the same time and processed independently. Of course, the microcontroller must have the right data bus available to handle this process.

However, it is not possible to change the operating mode once the system has been started. If such a function is needed, one must pull down the related NCN6004A power supply, change the MUX_MODE logic level, and re-start the interface.

MUX_MODE = High → MULTIPLEXED MODE

When pin 44 is High, the device operates in a multiplexed mode and all the card signals are shared between CARD_A and CARD_B, except the input clocks which are independent at any time. The RST_B, C4_B and C8_B pins are preferably left open at PCB level. The I/O_B pin must be left open and cannot be connected to any external signal or bias voltages.

The transfer gate Q4 is switched ON and, depending upon the CARD_SEL logic level, the I/O data will be transferred

to either CARD_A or CARD_B. It is neither possible to connect directly I/O_A to I/O_B nor to connect the I/O_B pin to ground or voltage supply.

The multiplexer is activated and the CARD_SEL signal is used to select the card in use for a given transaction. The switches Q1, Q2 and Q3 and swapped to the A position, thus providing a path for the control signals applied to the CARD_A side.

When the CARD_SEL signal flips from one card to the other, the previous logic states of the on going card are latched in the chip and the related output card pin are maintained at the appropriate levels. When the system resumes to the previous card, the latches return to the transparent operation and the signals presented by the μP take priority over the previously latched states.

On the other hand, the input clocks (CLK_IN_A and CLK_IN_B) are maintained independent and can be routed to either CARD_A or CARD_B according to the programming functions given in Table 2.

CARD POWER SUPPLY TIMING

When the PWR_ON signal is high, the associated CRD_VCC_A or CRD_VCC_B power supply rise time depends upon the current capability of the DC/DC converter together with the external inductors L1/L2 and the reservoir capacitor connected across each card power supply pin and GROUND.

On the other hand, at turn off, the CRD_VCC_A and CRD_VCC_B fall times depend upon the external reservoir capacitor and the peak current absorbed by the internal NMOS device built across each CRD_VCC_A/ CRD_VCC_B and GROUND. These behaviors are depicted by Figure 7, assuming a 10 μF output capacitor.

Since none of these parameters can have infinite values, the designer must take care of these limits if the t_{ON} or the t_{OFF} provided by the data sheets does not meet his requirement.

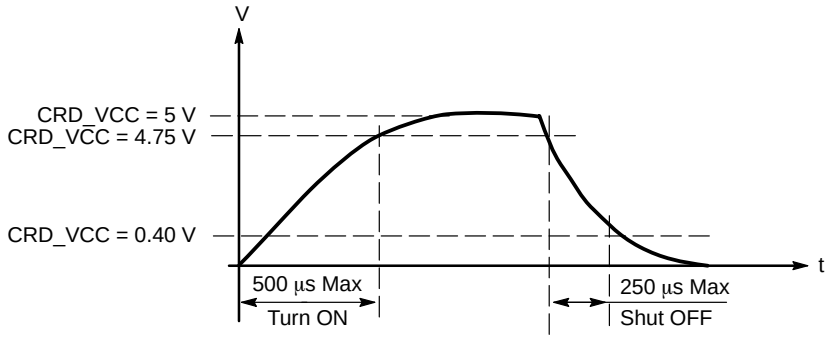


Figure 7. Card Power Supply Turn ON and Shut OFF Typical Timings

POWER DOWN OPERATION

The power down mode can be initiated by either the external MPU or by the internal error condition. The communication session is terminated immediately, according to the ISO7816-3 sequence. On the other hand, the MPU can run the Stand By mode by forcing $\overline{CS}$ = H, leaving the chip in the previous operating mode.

When the card is extracted, the interface will detect the operation and will automatically run the Power Down Sequence of the related card as described by the ISO/CEI 7816-3 sequence depicted in Figure 8 and illustrated by the oscillogram in Figure 9.

Force RST to Low
Force CLK to Low, unless it is already in this state
Force C4 and C8 to Low
Force CRD_IO to Low
Shut Off the CRD_VCC Supply

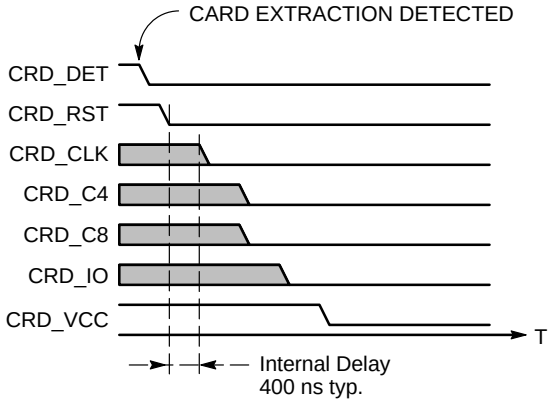


Figure 8. Card Power Down Sequence

On the other hand, the Power Down sequence is automatically activated when the V_{bat} voltage drops below the VCC_OK level, regardless of the logic conditions present on the control pins, or when the related CRD_VCC_x output voltage reaches the overload condition.

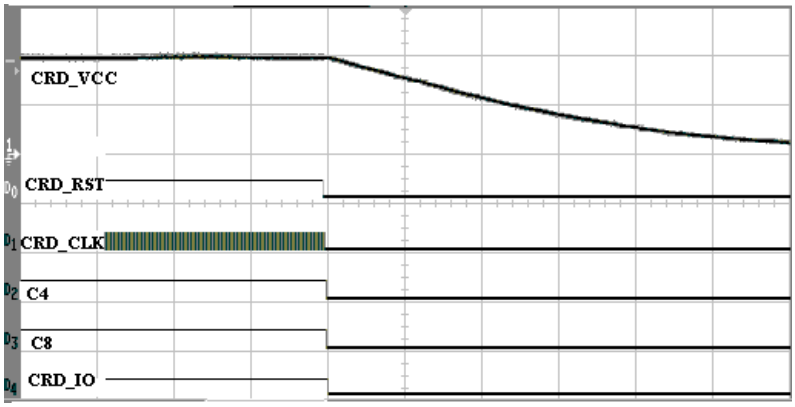


Figure 9. Power Down Sequence

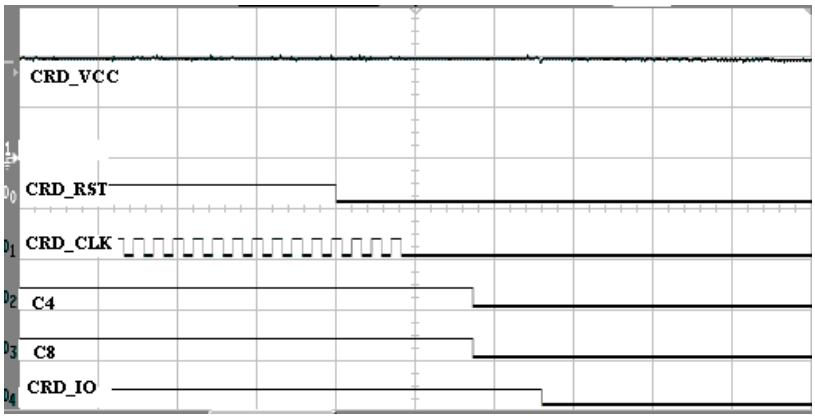


Figure 10. Power Down Sequence: Timing Details

CARD DETECTION

The card detector circuit provides a constant low current to bias the CRD_DET_A and CRD_DET_B pins, yielding a logic High when no card is present and the external switch is Normally Open type. The internal logic associated with pins 20 and 41 provides a programmable selection of the slope card detection. The transition is filtered out by the internal digital filter circuit, avoiding false interrupt. In addition to the typical 50 μs delay, the MPU shall provide an additional delay to cope with the mechanical stabilization of the card interface (typically 1 ms), prior to valid the CRD_VCC_A or CRD_VCC_B supply.

When a card is inserted, the detector circuit asserts $\overline{INT}$ = Low as depicted before, the external μP being responsible to clear the interrupt signal, taking the necessaries actions. When the NCN6004A detects a card extraction, the power down sequence is automatically activated for the related interface section, regardless of the PWR_ON state, and the $\overline{INT}$ pin is asserted Low. It is up to the external MPU to clear this interrupt by pulsing the $\overline{CS}$ pin.

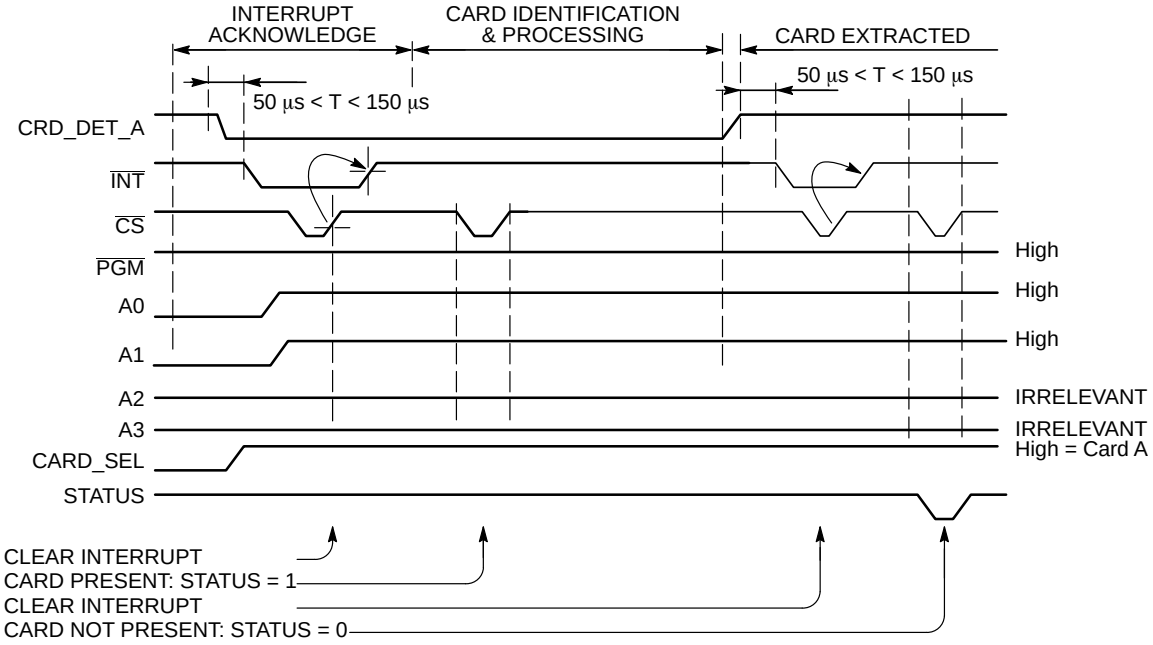


Figure 11. Typical Interrupt Sequence

The interrupt signal can be cleared either by a positive going slope on the Chip Select pin as depicted in Figure 11, or by forcing the PWR_ON signal High (keeping $\overline{CS}$ = Low) for the related card.

The polarity of the card detection switch can be either Normally Open or Normally Close and is software controlled as defined here below and in Table 2.

Table 5. Card Detection Polarity

$\overline{CS}$	$\overline{PGM}$	A3	A2	A1	A0	CARD_SEL	CRD_DET_A	CRD_DET_B
1	X	X	X	X	X	X	Qn -1	Qn -1
0	1	X	X	X	X	X	Qn -1	Qn -1
0	0	1	1	0	0	1	Normally Open	Qn -1
0	0	1	1	0	1	1	Normally Close	Qn -1
0	0	1	1	0	0	0	Qn -1	Normally Open
0	0	1	1	0	1	0	Bn -1	Normally Close

*The polarity change is validated upon the next positive $\overline{PGM}$ transient.

POWER MANAGEMENT

The main purpose of the power management is to provides the necessary output voltages to drive the 1.80 V, 3.0 V or 5.0 V smart card types. On top of that, the DC/DC converter efficiency must absorb a minimum current on the V_{bat} supply.

Beside the power conversion, in the Stand by mode (PWR_ON = L), the power management provides energy to the card detection circuit only. All the card interface pins are forced to ground potential, saving as much current as possible out of the battery supply.

In the event of a power up request coming from the external MPU (CARD_SEL =H/L, PWR_ON = H, $\overline{CS}$ = L), the power manager starts the DC/DC converter related to the selected interface section.

When the selected section (either CRD_VCC_A or CRD_VCC_B) voltage reaches the programmed value (1.8 V, 3.0 V or 5.0 V), the circuit activates the card signals according to the following sequence:

CRD_VCC_x → CRD_IO_x → CRD_C4_x → CRD_C8_x → CRD_CLK_x → CRD_RST_x

The logic level of the data lines are asserted High or Low, depending upon the state forced by the external MPU, when the start-up sequence is completed. Under no situation the NCN6004A shall automatically launch a smart card ATR sequence.

At the end of the transaction, asserted by the MPU (CARD_SEL = H/L, PWR_ON = L, $\overline{CS}$ = L), or under a card extraction, the ISO7816-3 power down sequence takes place:

CRD_RST_x → CRD_CLK_x → CRD_C4_x → CRD_C8_x → CRD_IO_x → CRD_VCC_x

When $\overline{CS}$ = H, the bi-directional I/O lines (pins 9 and 19) are forced into the High impedance mode to avoid signal collision with any data coming from the external MPU.

OUTPUT VOLTAGE PROGRAMMING

The internal logic provides a reliable circuit to activate any of the DC/DC converters safely. In particular, the Turn On/Turn Off of these converters is edge sensitive and controlled by the rising/falling edges of the PWR_ON signal applied with Chip Select pin Low. The CARD_SEL signal is used to select either CRD_VCC_A or CRD_VCC_B as defined by the functions programming in Table 2.

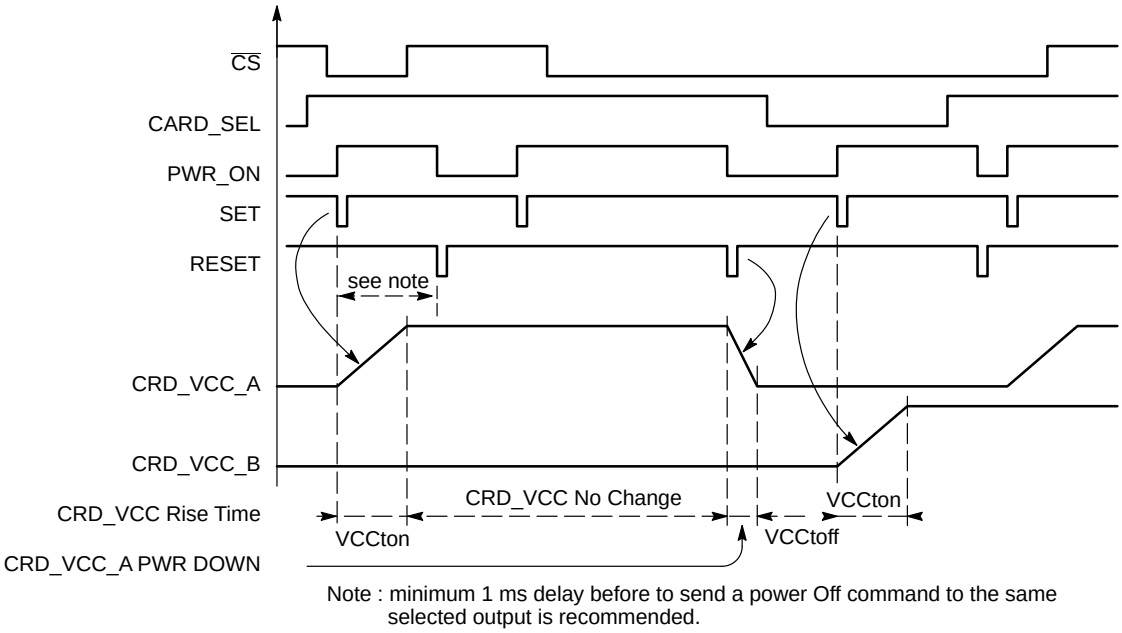
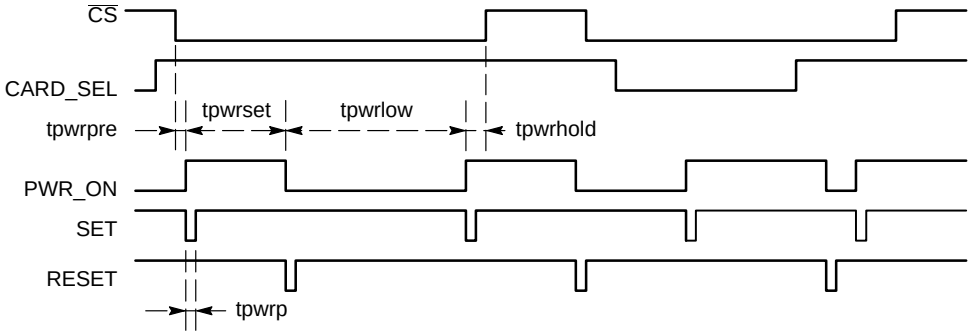


Figure 12. Card Power Supply Controls

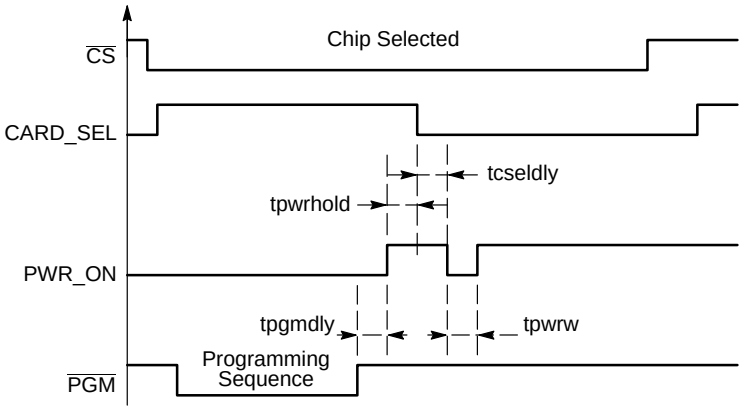
Although it is possible to change the output voltage straightly from 5.0 V to 1.80 V, care must be observed as the stabilization time will be relatively long if no current is absorbed from the related output pin.

According to the typical sequence depicted, it is not possible to program simultaneously the two DC/DC converters, but two separate sequences must take place. On top of that, since the circuit is edge sensitive, the PWR_ON signal must present such a transient when a given state is expected for the converter. The PWR_ON and $\overline{CS}$ timings definitions are given in Figure 13.



NOTE: tpwrset: This delay is necessary to latch–up the PWR_ON condition and does not represent the CRD_VCC output voltage rise time.
tpwrlow: This delay includes the internal ISO7816-3 power down sequence to make sure the DC/DC converter is fully deactivated.

Figure 13. Power On Sequence Timings



NOTE: tpwrw: This delay represents the minimum pulse width needed to write the PWR_ON status into the associated DC/DC latch

Figure 14. Power On and CARD_SEL Sequence Timings

DC/DC CONVERTER

The power conversion is carried out either in step up or step down mode. The operation is fully automatic and, beside the output voltage programming, does not need any further adjustments.

The simplified DC/DC converter, given in Figure 15, is based on a full bridge structure capable to handle either step up or step down power supply using an external inductor. This structure brings the capability to operate from a wide range of input voltage, while providing the accurate 1.80 V, 3.0 V or 5.0 V requested by the smart cards. Beside the accuracy, the major aim of this structure is the high efficiency necessary to save energy taken from the battery. On the other hand, using two independent converters provides a high flexibility and prevent a total system crash in the event of a failure on one of the card connected to the interface.

OPERATION

NOTE: Described operation makes reference to CARD_A and can be applied to CARD_B.

The system operates with a two cycles concept:

1. Cycle 1: Q15 and Q4 are switched ON and the inductor L1 is charged by the energy supplied by the external battery. During this phase, the pairs Q1/Q16 and Q2/Q3 are switched OFF.
   The current flowing into the two MOSFET Q1 and Q4 is internally monitored and will be switched OFF when the Ipeak value (depending upon the programmed output voltage value) is reached. At this point, Cycle 1 is completed and Cycle 2 takes place. The ON time is a function of the battery voltage and the value of the inductor network (L and Zr) connected across pins 26/27 and 34/35.
   A 4 μs time out structure makes sure the system does run in a continuous Cycle 1 loop.
2. Cycle 2: Q1 and Q16 are switched ON and the energy stored into the inductor L1 is dumped into the external load through Q16. During this phase, the pair Q15/Q4 and the pair Q2/Q3 are switched OFF.
   The current flow period is constant (900 ns typical) and Cycle 1 repeats after this time if the CRD_VCC voltage is below the specified value.

When the output voltage reaches the specified value (1.80 V or 3.0 V or 5.0 V), Q1 and Q16 are switched OFF immediately to avoid over voltage on the output load. In the mean time, the two extra NMOS Q2 and Q3 are switched ON to fully discharge any current stored into the inductor, avoiding ringing and voltage spikes over the system. Figure 16 illustrates the theoretical basic waveforms present in the DC/DC converter.

The control block gives the logic states according to the bits provided by the external μP. These controls bits are applied to the selected DC/DC converter to generate the programmed output voltage. The MOS drive block includes the biases necessaries to drive the NMOS and PMOS devices as depicted in the block diagram given Figure 15.

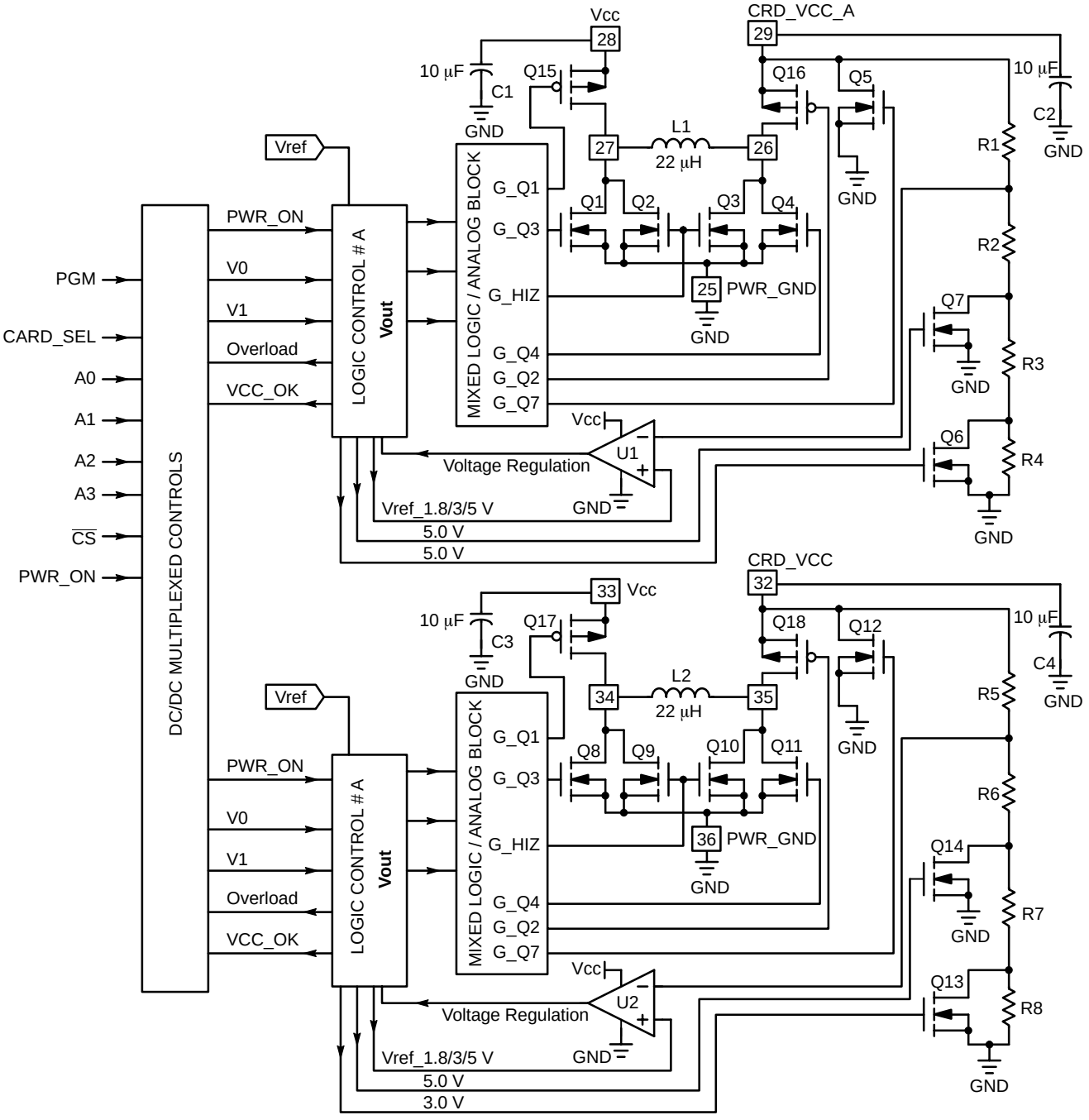


Figure 15. Basic DC/DC Converter Diagram

Since the output inductor L1 and the reservoir capacitor C1 carry relative high peak current, low ESR devices must be used to prevent the system from poor output voltage ripple and low efficiency. Using ceramic capacitors, X5R or X7R type, are recommended, splitting the 10 μF in two separate parts when there is a relative long distance between the CRD_VCC_x output pin and the card VCC input. On the other hand, the inductor shall have an ESR below 1.0 Ω to achieve the high efficiency over the full temperature range. However, inductor with 2.0 Ω ESR can be used when a slight decrease of the efficiency is acceptable at system level.

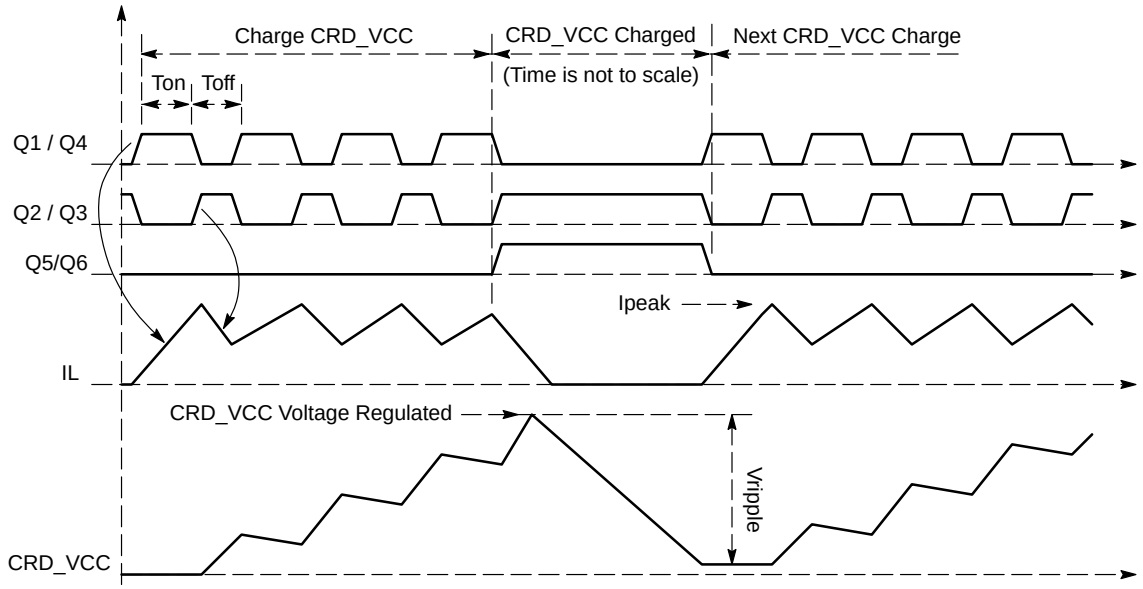


Figure 16. Theoretical DC/DC Operating

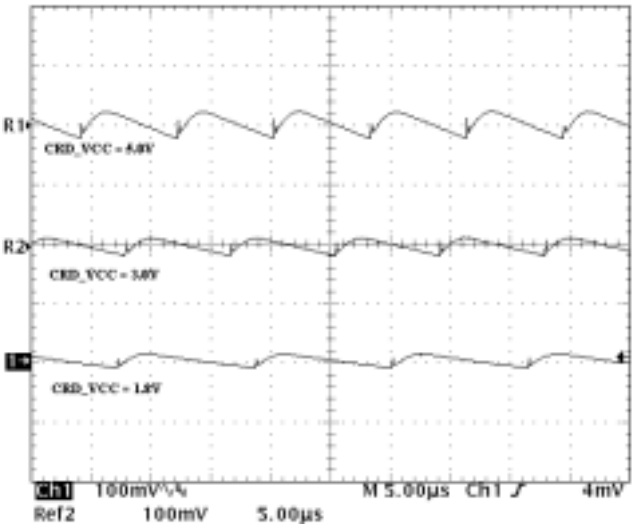
When the CRD_VCC is programmed to zero volt, or when the card is extracted from the socket, the active pull down Q5 rapidly discharges the output reservoir capacitor, making sure the output voltage is below 0.40 V when the card slides across the contacts.

Based on the experiments carried out during the NCN6004A characterization, the best comprise, at time of printing this document, is to use two 4.7 μF/10 V/ceramic/X7R capacitor in parallel to achieve the CRD_VCC filtering. The ESR will not extend 50 mΩ over the temperature range and the combination of standard parts provide an acceptable –20% to +20% tolerance, together with a low cost. Table 6 shows a quick comparison between the most common type of capacitors. Obviously, the capacitor must be SMD type to achieve the extremely low ESR and ESL necessary for this application.

Figure 17 illustrates the CRD_VCC ripple observed in the NCN6004A demo board running with X7R ceramic capacitors.

Table 6. Ceramic/Electrolytic Capacitors Comparison

Manufacturer	Type/Series	Format	Max Value	Tolerance	Typ. Z @ 500 kHz
MURATA	CERAMIC/GRM225	0805	10 μF/6.3 V	-20% /+20%	30 mΩ
MURATA	CERAMIC/GRM225	0805	4.7 μF/6.3 V	-20% /+20%	30 mΩ
VISHAY	Tantalum/594C/593C	1206	10 μF/16 V		450 mΩ
VISHAY	Electrolytic/94SV	1812	10 μF/10 V	-20%/+20%	400 mΩ
Miscellaneous	Electrolytic Low Cost	1812	10 μF/10 V	-35%/+50%	2.0 Ω



NOTE: Operating conditions under full output load.

Figure 17. Typical CRD_VCC Ripple Voltage

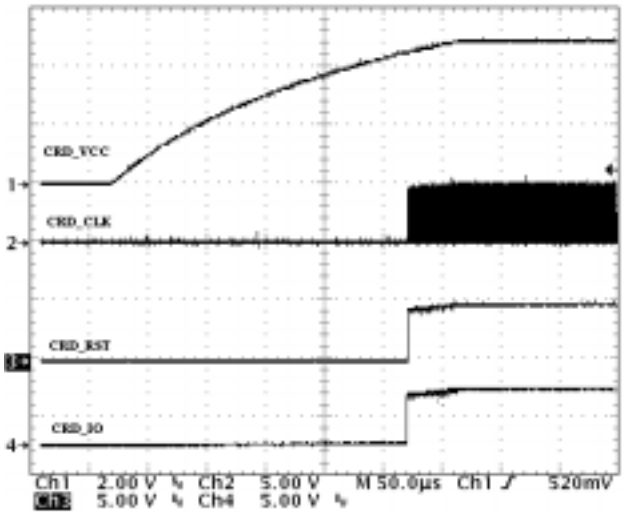


Figure 18. Typical Card Voltage Turn ON and Start-up Sequence

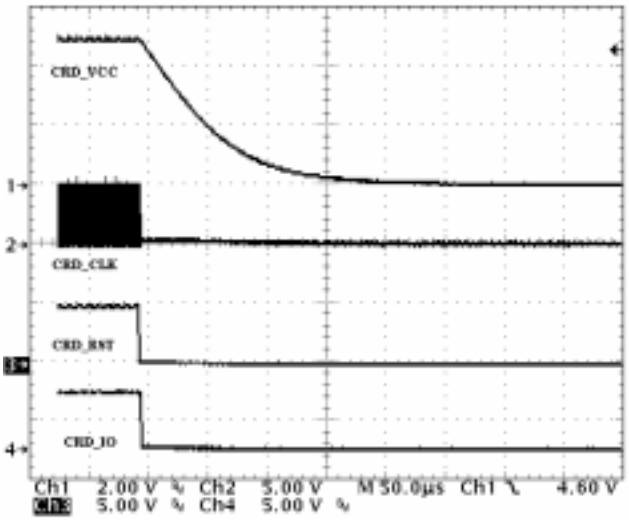


Figure 19. Typical Card Supply Turn OFF

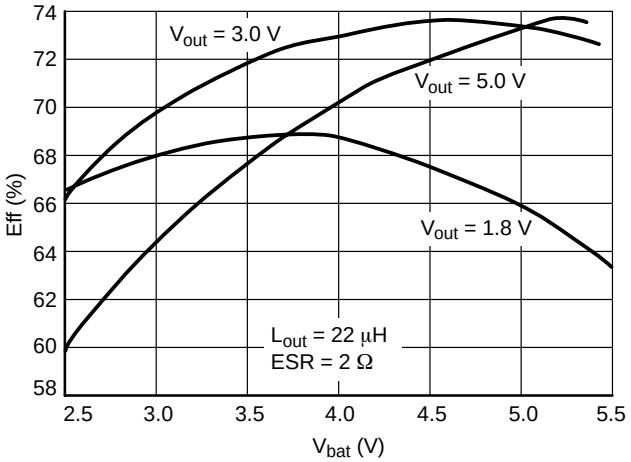
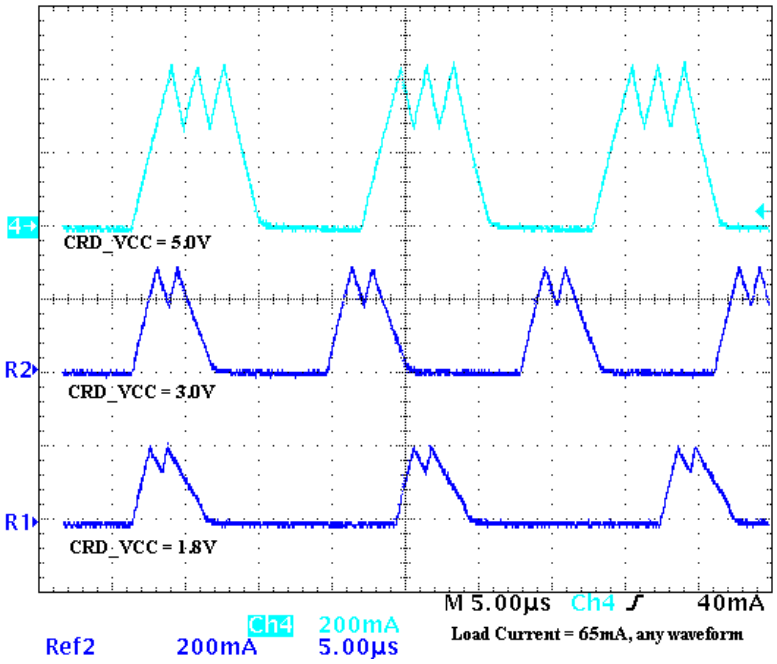


Figure 20. CRD_VCC Efficiency as a Function of the Input Supply Voltage

The curves in Figure 20, illustrate the typical behavior under full output current load (35 mA, 60 mA and 65 mA), according to EMV specifications.

During the operation, the inductor is subject to high peak current as depicted in Figure 21 and the magnetic core must sustain this level of current without damage. In particular, the ferrite material shall not be saturated to avoid uncontrolled current spike during the charge up cycle. Moreover, since the DC/DC efficiency depends upon the losses developed into the active and passive components, selecting a low ESR inductor is preferred to reduce these losses to a minimum.



Test conditions: Input V_{CC} voltage = 5.0 V, Current = 200 mA /div, T_{amb} = +20°C

Figure 21. Typical Output Voltage Ripple

According to the ISO7816-3 and EMV specifications, the interface shall limits the CRD_VCC output current to 200 mA maximum, under short circuit conditions. The NCN6004A supports such a parameter, the limit being depending upon the input and output voltages as depicted in Figure 22.

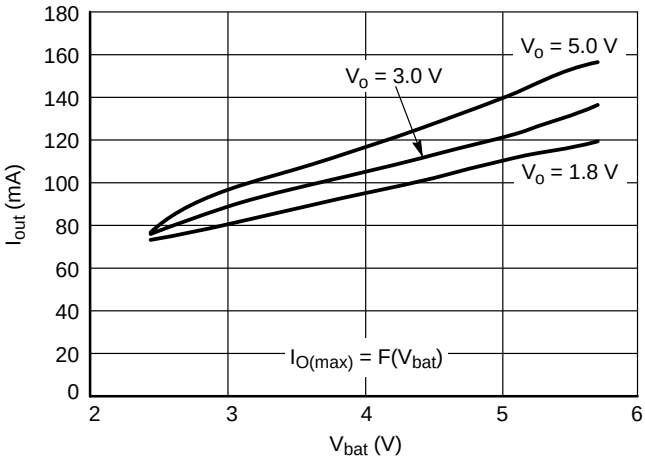


Figure 22. Output Current Limit

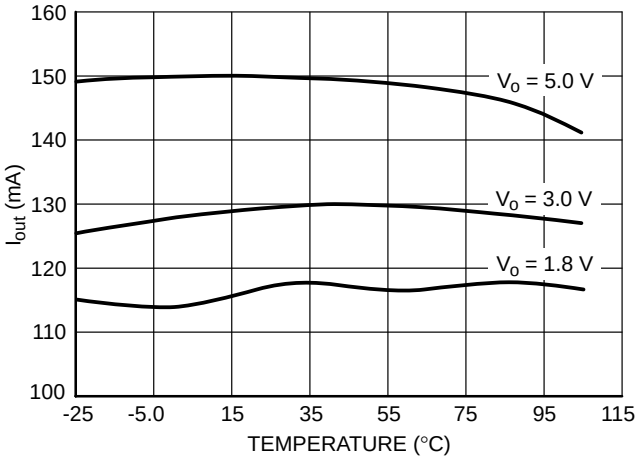


Figure 23. Output Current Limit as a Function of the Temperature

Beside the continuous current capability, the smart card power supply must be capable of providing a 100 mA pulsed current during the data transaction. The ISO7816-3, paragraph 4.3.2, defines this 400 ns pulse as a function of the environment. As a matter of fact, this pulse does not come solely from the NCN6004A DC/DC converter, but the reservoir capacitor and the associated PCB tracks shall be considered as well.

CLOCK DIVIDER

The main purpose of the built in clock generator is four folds:

1. Adapts the voltage level shifter to cope with the different voltages that might exist between the MPU and the Smart Card
2. Provides a frequency division to adapt the Smart Card operating frequency from the external clock source.
3. Control the clock state according to the smart card specification.
4. Provides an input clock re-routing to route the CLOCK_IN_A and CLOCK_IN_B signals to either CRD_CLK_A or CRD_CLK_B output pins.

In addition, the NCN6004A adjusts the signal coming from the microprocessor to get the Duty Cycle window as defined by the ISO7816-3 specification.

The logic input pins CARD_SEL, A0, A1, $\overline{\text{PGM}}$, I/O and RESET fulfill the programming functions when both $\overline{\text{PGM}}$ and $\overline{\text{CS}}$ are Low. The clock input stage (CLOCK_IN) can handle a 40 MHz frequency maximum, the divider being capable to provide an 1:8 ratio. Of course, the ratio must be defined by the engineer to cope with the Smart Card considered in a given application and, in any case, the output clock (CRD_CLK_A and CRD_CLK_B) shall be limited to 20 MHz maximum when the system is considered to operate over the full temperature range.

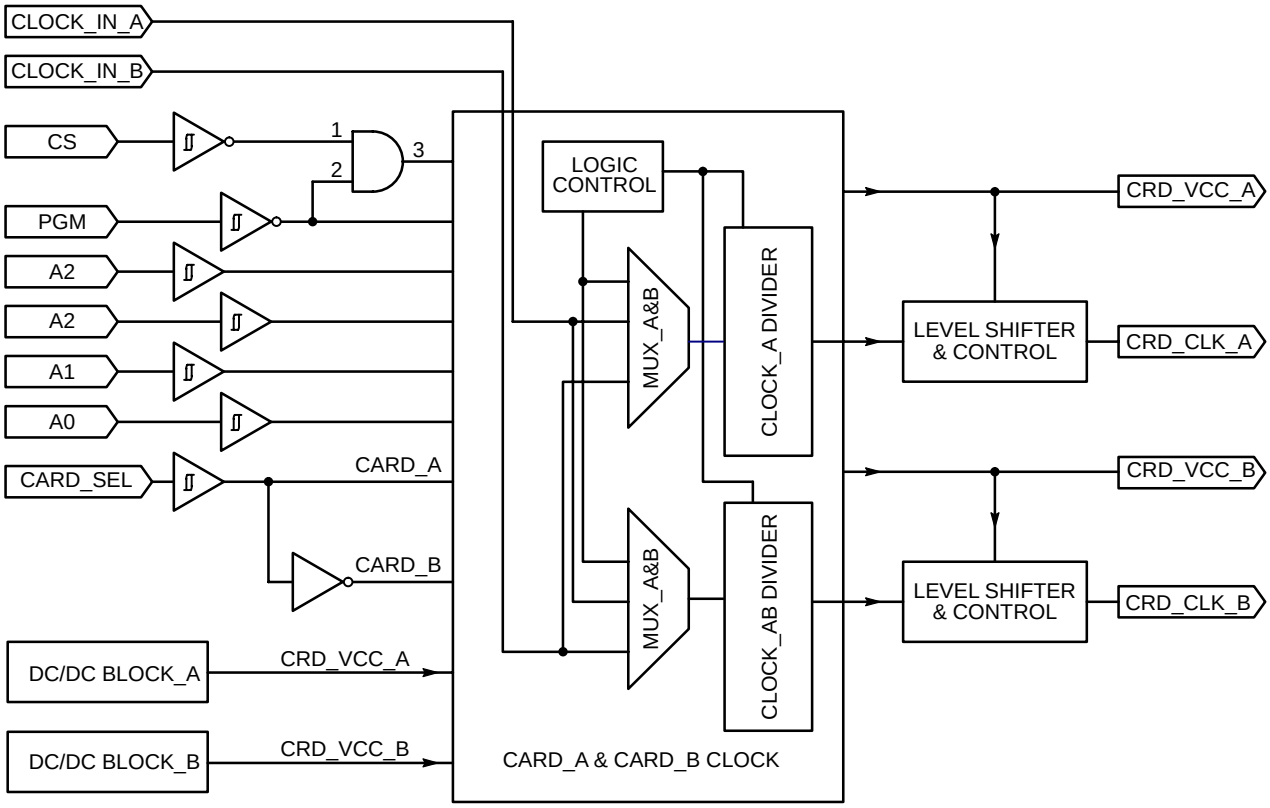


Figure 24. Simplified Frequency Divider and Programming Functions

In order to avoid any duty cycle out of the frequency smart card ISO7816-3 and EMV specifications, the clock divider is synchronized by the last flip flop, thus yielding a constant 50% duty cycle, regardless of the divider ratio. Consequently, the output CRD_CLK_A or CRD_CLK_B frequency division can be delayed by eight CLOCK_IN pulses and the microcontroller software must take this delay into account prior to launch a new data transaction.

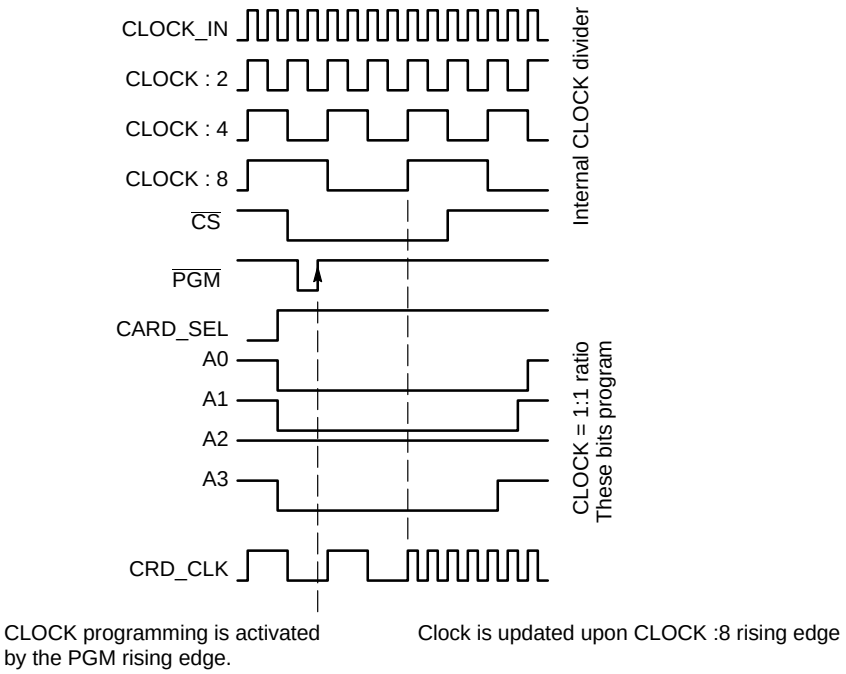


Figure 25. Clock Programming Timings

The example given in Figure 25 highlights the delay coming from the internal clock duty cycle re-synchronization. Since the clock signal is asynchronous, it is up to the programmer to make sure the next card transaction is not activated before, respectively, either the CRD_CLK_A or CRD_CLK_B signal has been updated. Generally speaking, such a delay can be derived from the maximum clock frequency provided to the interface.

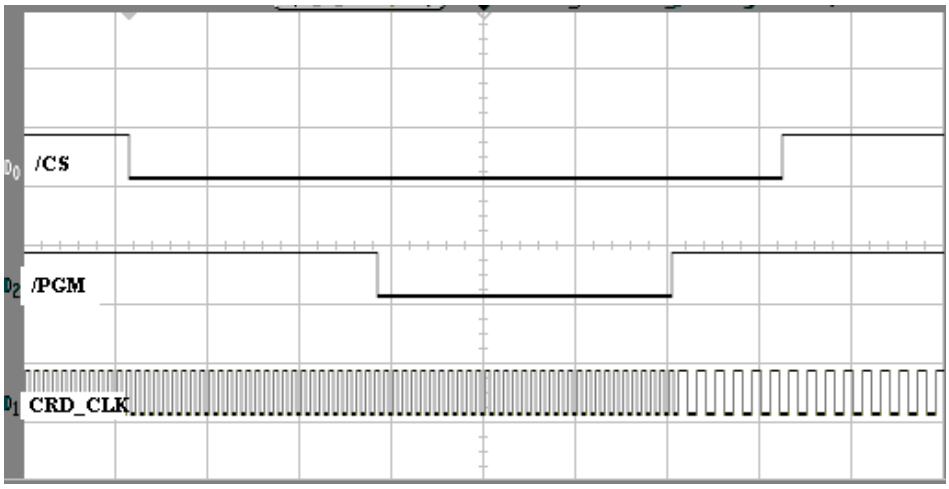


Figure 26. Card Clock 1/2 Divider Operation

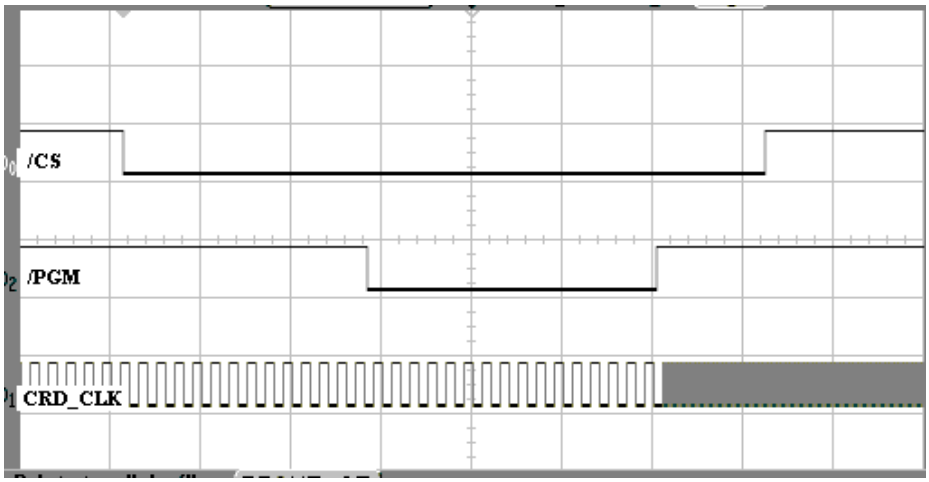


Figure 27. Clock Divider: 8 to 1 Operation

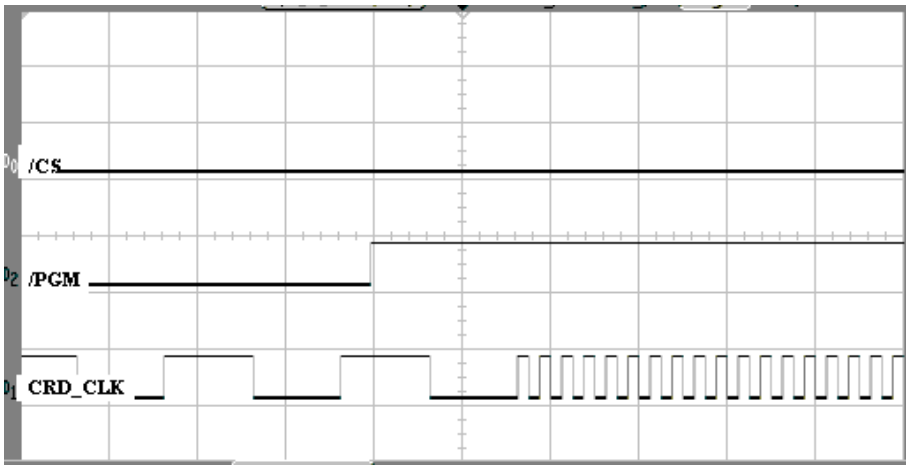


Figure 28. Clock Divider Timing Details

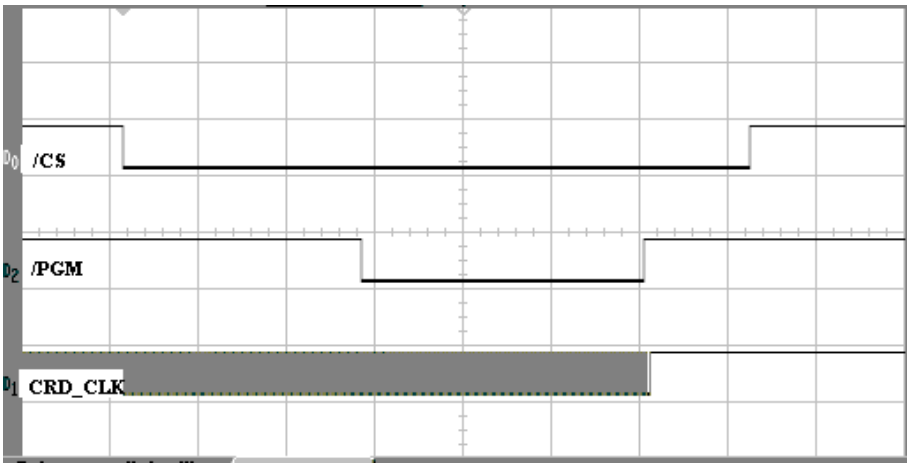


Figure 29. Clock Divider: Run to Stop High Operation

The input clock A and B can be re routed to either CRD_CLK_A or CRD_CLK_B output pins by using the programming function as defined in Table 2 and Table 7. The clock signals can have any frequency value necessary to handle a given type of card (asynchronous or synchronous). These clock signals can be multiplexed at any time, but the system must be locked in a safe state prior to make such a change. In particular, the designer must make sure that A and B cards can support such a hot change prior to change the related clocks.

Table 7. Programming Clock Routing

STATE	$\overline{CS}$	$\overline{PGM}$	A3	A2	A1	A0	CARD_SEL	CRD_CLK_A	CRD_CLK_B	
0E	**0**	**0**	**1**	**1**	**1**	**0**	**1**	**CLK_D_A**	**-**	**Default**
0F	0	0	1	1	1	1	1	CLK_D_B	-	-
0E	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**-**	**CLK_D_B**	**Default**
0F	0	0	1	1	1	1	0	-	CLK_D_A	-

On the other hand, the slope of the CRD_CLK_x signal can be set to either FAST or SLOW, depending upon the frequency of the output clock. This selection is achieved by programming the chip according to Table 8.

Table 8. Output Clock Slope Selection

STATE	$\overline{CS}$	$\overline{PGM}$	A3	A2	A1	A0	CARD_SEL	CLOCK SLOPE	
$03	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**SLOW**	**Default**
$0B	0	0	1	0	1	1	1	FAST	-
$03	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**SLOW**	**Default**
$0B	0	0	1	0	1	1	0	FAST	-

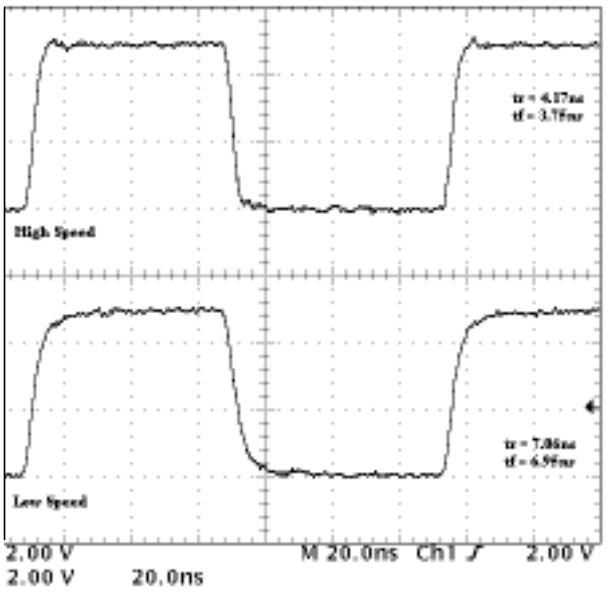


Figure 30. Typical Rise and Fall Time in Fast and Slow Operating Mode

PARALLEL OPERATION

When two or more NCN6004A parts operate in parallel on a common digital bus, the Chip Select pin allows the selection of one chip from the bank of the paralleled devices. Of course, the external MPU shall provide one unique $\overline{CS}$ line for each of the NCN6004A considered interface. When a given interface is selected by $\overline{CS}$ = L, all the logic inputs becomes active, the chip can be programmed or/and the external card can be accessed. When $\overline{CS}$ = H, all the input logic pins are in the high impedance state, thus leaving the bus available for other purpose.

The pull up resistors connected on each logic input lines on the MPU side (see block diagram in Figure 30), can be either activated (connected to V_{CC}) or disconnected, depending upon the logic state present at EN_RPU, pin 45. When these resistors are disconnected, it is the system responsibility to set up the external pull up resistors according to the application's requirements.

When the device operates in the multiplexed mode (MUX_MODE = High), the internal card #B pull up resistors are connected to V_{CC}, regardless of the EN_RPU logic state.

On the other hand, when $\overline{CS}$ = H, the CRD_IO and CRD_RST hold the previous I/O and RESET logic state, the CRD_CLK being either active or stopped and the CRD_VCC output voltage will maintain is previous value, according to the programmed state forced by the MPU.

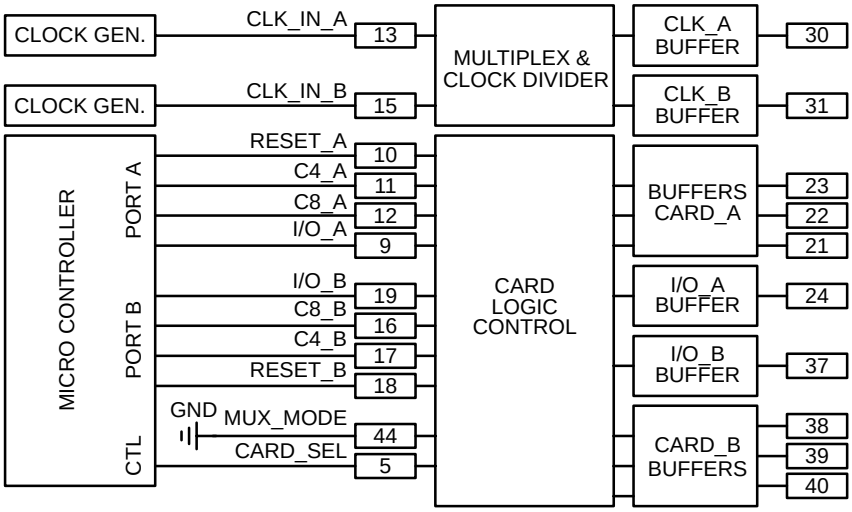


Figure 31. Parallel Operation Wiring → MUX_MODE = Low

When the chip operates in the parallel mode, all the logic signals must be independently controlled by the microcontroller as depicted in Figure 31. The MUX_MODE pin must be hardwired to VCC and it cannot be changed during an operation of the chip. Beside this parameter, the user must select to force or not the internal pull up resistors as defined by the EN_RPU logic state.

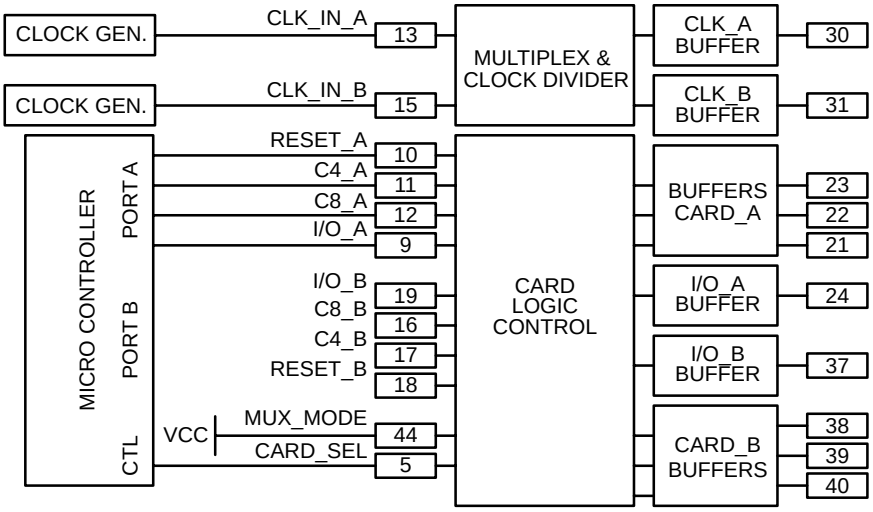


Figure 32. Multiplexed Operation Wiring → MUX_MODE = High

In the multiplexed mode, the microprocessor CARD_B side pins are not connected, the logic signals and the I/O line being shared with CARD_A associated with the CRD_SEL control bit: Figure 32. A key point is to make sure there is no connection associated with the I/O_B pin since this pin is internally shared with the I/O line transaction. The CLK_IN_A and CLK_IN_B signals are independent and can be routed to any of the card thanks to the built-in clock multiplexer.

DATA I/O LEVEL SHIFTER

The built in structure provides a level shifter on each card output signals, the I/O line being driven differently as depicted in Figure 33. Since the NCN6004A can operate in either a multiplexed or parallel mode, provisions have been made to route the I/O_A input pin to either CARD_A or CARD_B.

In both case, the I/O pins are driven by an open drain structure with a 20 kΩ pull up resistor as shown Figure 33. To achieve the 0.80 μs maximum rise time requested by the EMV specifications, an accelerator circuit is added on both side of each I/O line. These pulsed circuits yield boost current to charge the stray capacitance, thus accelerating the positive going slope of the I/O signal. On the other hand, the active pull down NMOS device Q5 provides a low impedance to ground during the battery up and DC/DC start-up phase, avoiding any uncontrolled voltage spikes on the I/O lines.

MUX_MODE = Low → PARALLEL OPERATION

The bi-directional switch Q9 is OFF and the I/O signals are routed straightforward to their appropriate outputs. The two I/O lines can operate simultaneously, depending upon the μP capabilities, regardless of the CARD_SEL signal logic level.

The pull up resistors, on the μP side of each I/O line, can be connected or not as defined by the EN_RPU signal.

MUX_MODE = High → MULTIPLEXED OPERATION

The bi-directional switch Q9 is ON and the I/O_A pin is used to handle data for CARD_A and CARD_B. The signal is routed to the appropriate card by means of the CARD_SEL logic signal. In this mode, the I/O_B pin 19 must be left open since the internal data signal will be present on this pin.

Moreover, since R1 and R3 are in parallel, the pull up resistor R1 is automatically disconnected to maintain the I/O line impedance to 20 kΩ (typical), what ever be the EN_RPU logic level. This feature makes sure the current flowing trough the external card is limited to 500 μA during a low level state.

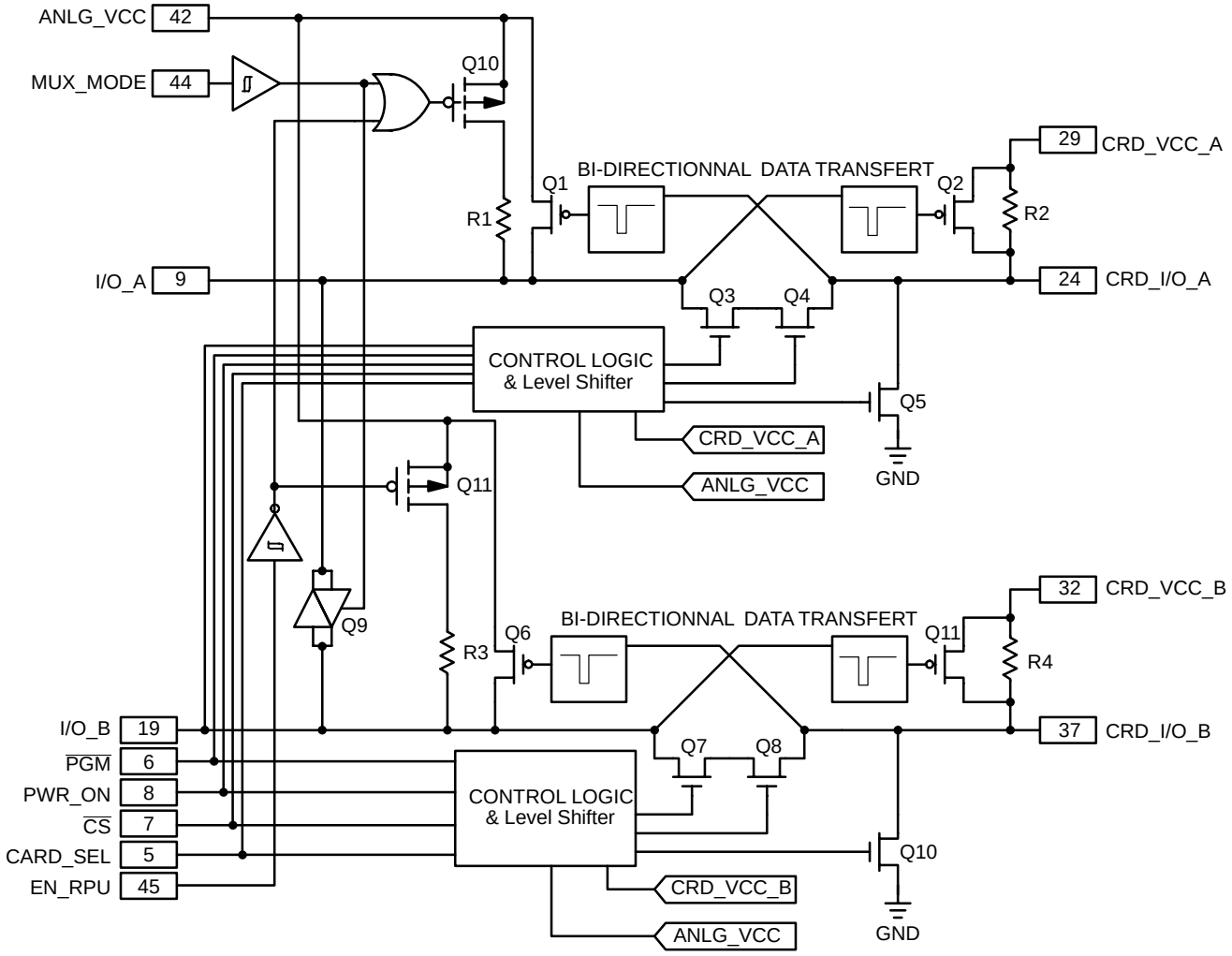
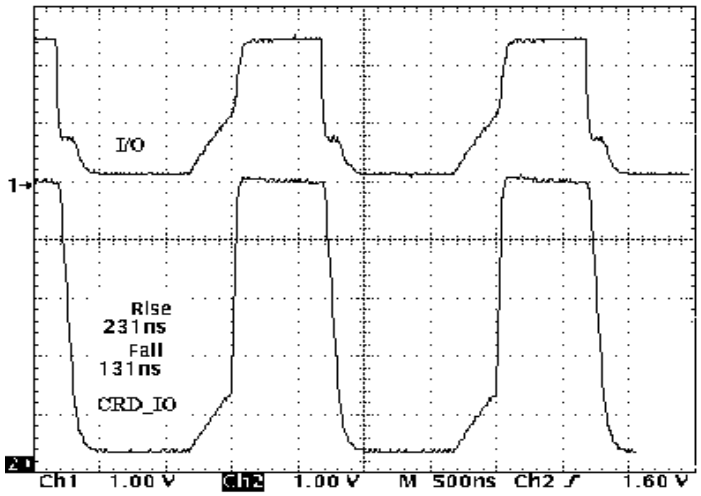


Figure 33. Dual Bi-directional I/O Line Level Shifter and Multiplex



NOTE: Both sides of the interface run with open drain load (worst case condition)

Figure 34. Typical I/O Rise and Fall Time

ESD Protection

The NCN6004A includes silicon devices to protect the pins against the ESD spikes voltages. To cope with the different ESD voltages developed across these pins, the built in structures have been designed to handle either 2 kV, when related to the microcontroller side, or 8 kV when connected with the external contacts. Practically, the CRD_RST, CRD_CLK, CRD_IO, CRD_C4 and CRD_C8 (both A and B sections) pins can sustain 8 kV, the maximum short circuit current being limited to 15 mA. The CRD_VCC_A and CRD_VCC_B pins have the same ESD protection, but can source up to 65 mA continuously each, the absolute maximum current being 150 mA per section.

Security Features

In order to protect both the interface and the external smart card, the NCN6004A provides security features to prevent catastrophic failures as depicted here after.

Pin Current Limitation: in case of a short circuit to ground, the current forced by the device is limited to 10 mA for any pins, except CRD_CLK_A and CRD_CLK_B pins which are both limited to 70 mA. No feedback is provided to the external MPU.

DC/DC Operation: The internal circuit continuously senses the CRD_VCC_A and CRD_VCC_B voltages and, in the case of either over or under voltage situation, update the STATUS register accordingly. This register can be read out by the MPU but no interrupts are activated.

DC/DC Overload: When an overload is sensed across the CRD_VCC_A or CRD_VCC_B output, during either the power on sequence or when the system was previously running, the NCN6004A generates an interrupt by pulling down the $\overline{\text{INT}}$ pin. It is up to the microcontroller to identify the origin of the overload by reading the STATUS pin accordingly.

Battery Voltage: Both the Positive going and the Negative going voltage are detected by the NCN6004A, a POWER_DOWN sequence and the STATUS register being updated accordingly. The external MPU can read the STATUS pin to take whatever is appropriate to cope with the situation. The NCN6004A does not provide any further internal voltage regulation.

TEST BOARD SCHEMATIC DIAGRAM

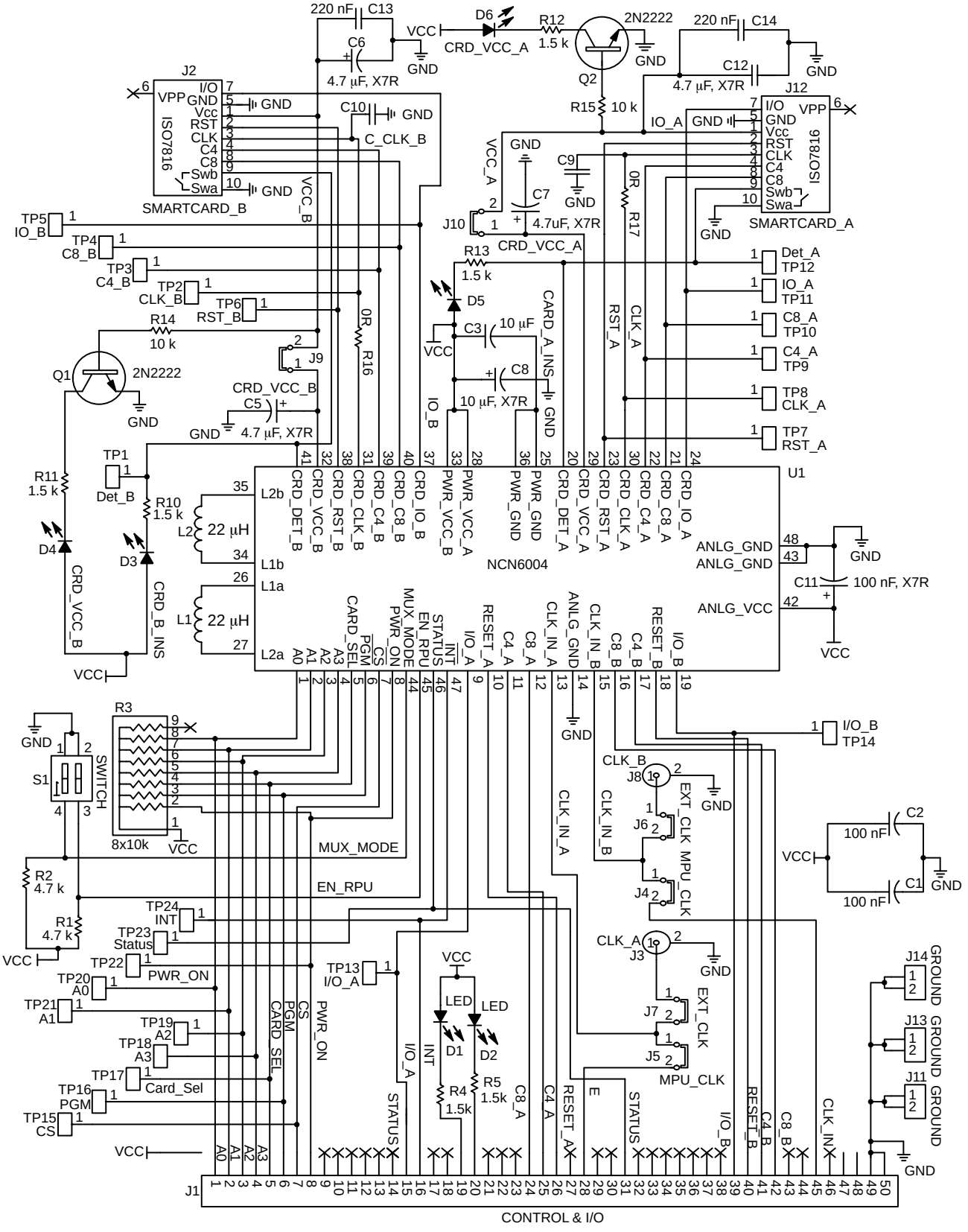


Figure 35. Test Board Schematic Diagram

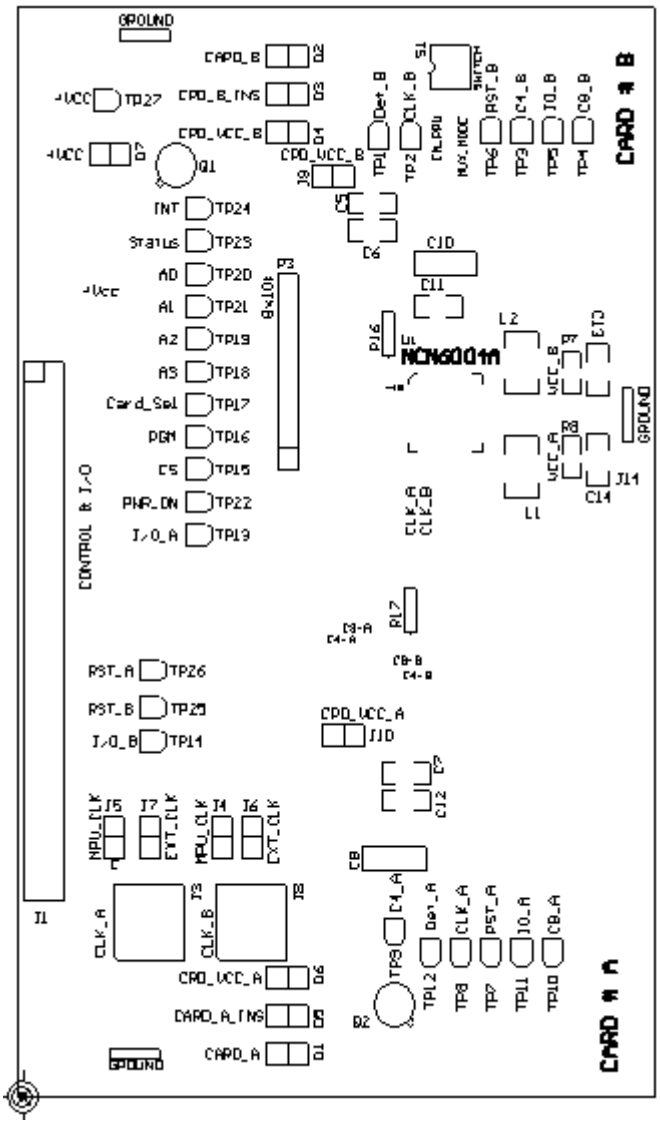


Figure 36. Demo Board PCB Top Overlay

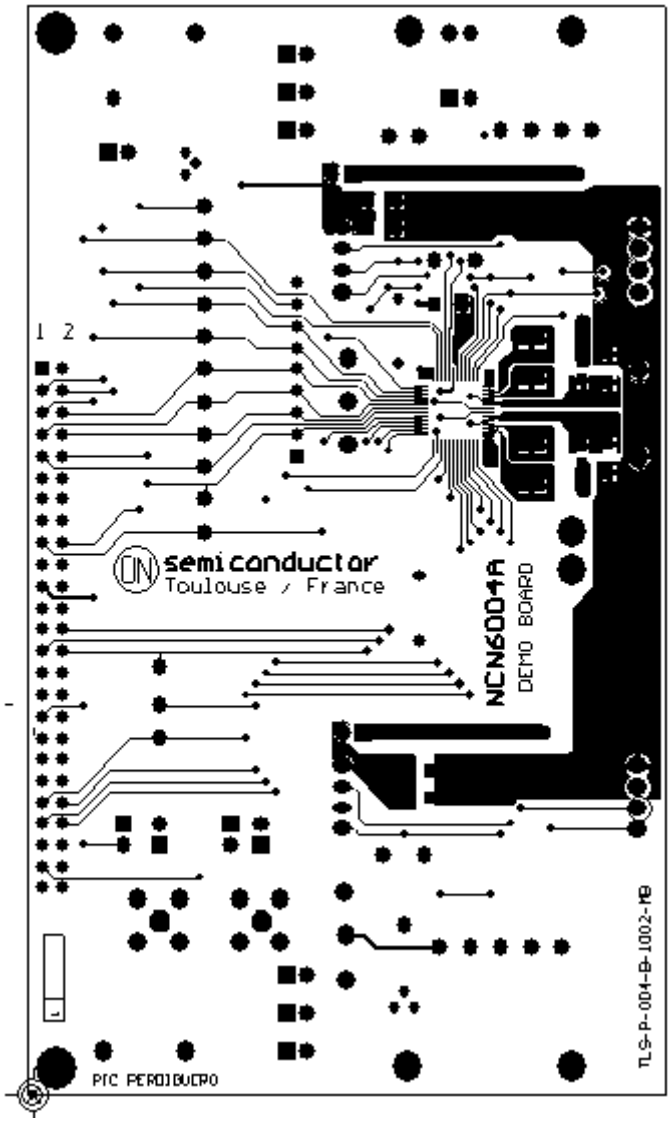


Figure 37. Demo Board PCB Top Layer

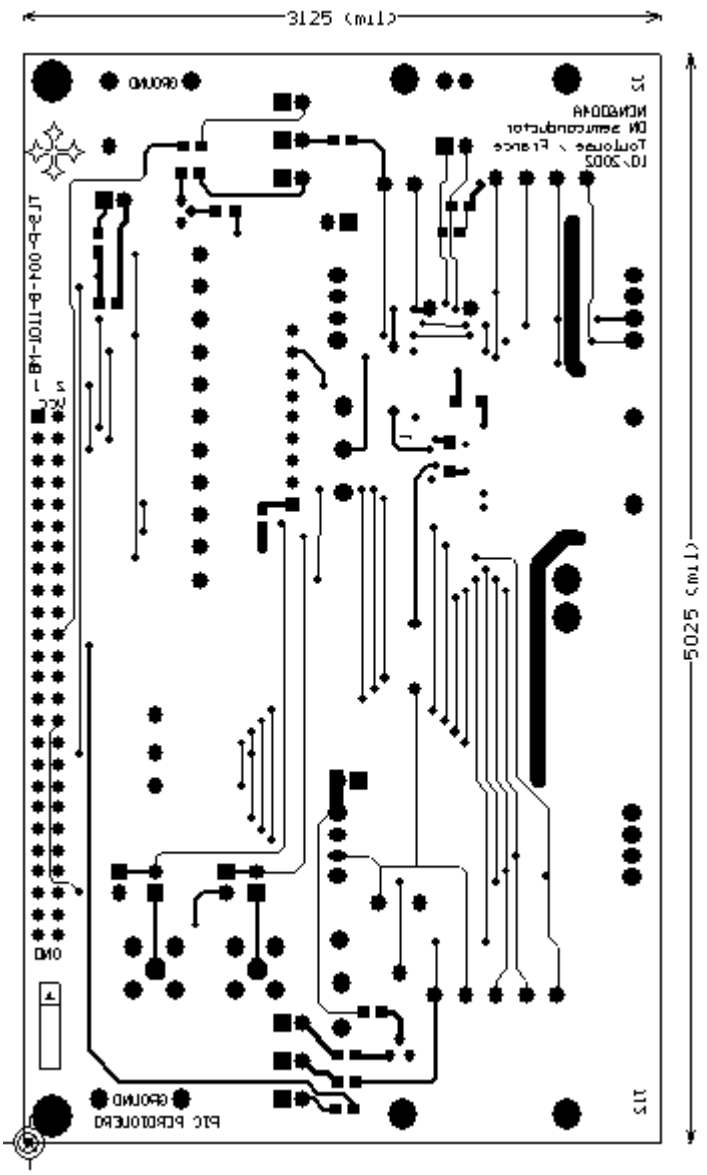


Figure 38. Demo Board PCB Bottom Layer

NOTE: Note: the demo board is built with a four layers PCB, the internal ones being dedicated to V_{CC} and GND planes.

ABBREVIATIONS

L1a and L1b	DC/DC external inductor #A	**CRD_VCC_A**	Interface IC Card #A Power Supply Line
L2a and L2b	DC/DC external inductor #B	**CRD_CLK_A**	Interface IC Card #A Clock Input
Cout	Output Capacitor	**CRD_RST_A**	Interface IC Card #A RESET Input
CRD_VCC	Card Power Supply Input	**CRD_IO_A**	Interface IC Card #A Data link
VCC	MPU Power Supply Voltage	**CRD_C4_A**	Interface IC Card #A Data Control
Icc	Current at card VCC pin	**CRD_C8_A**	Interface IC Card #A Data Control
Class A	5 V Smart Card	**CRD_DET_A**	Card insertion/extraction detection
$\overline{\text{CS}}$	Chip Select	**CARD_SEL**	Card #A/B Selection bit
CRD_CLK_B	Interface IC Card #B Clock Input		
CRD_IO_B	Interface IC Card #B Data link	**EN_RPU**	Enable/Disable internal pull up
CRD_IO_B	Interface IC Card #B RESET Input	**$\overline{\text{PGM}}$**	Chip Programming Mode
EMV	Euro Card Master Card Visa	**ISO**	International Standards Organization
Class B	3 V Smart Card	**CRD_VCC_B**	Interface IC Card #B Power Supply Line
ANLG_VCC = VCC = V_{bat}	Input Voltage	**CRD_C4_B**	Interface IC Card #B Data Control
PWR_ON	Chip Power On bit	**CRD_C8_A**	Interface IC Card #B Data Control
MUX_MODE	Card Multiplex or Parallel Op.		
CRD_DET_B	Card insertion/extraction detection	**T0**	Smart Card Data transfer procedure by bytes
T1	Smart Card Data transfer procedure by strings	**μC**	Microcontroller

48 LEADS, TQFP EP
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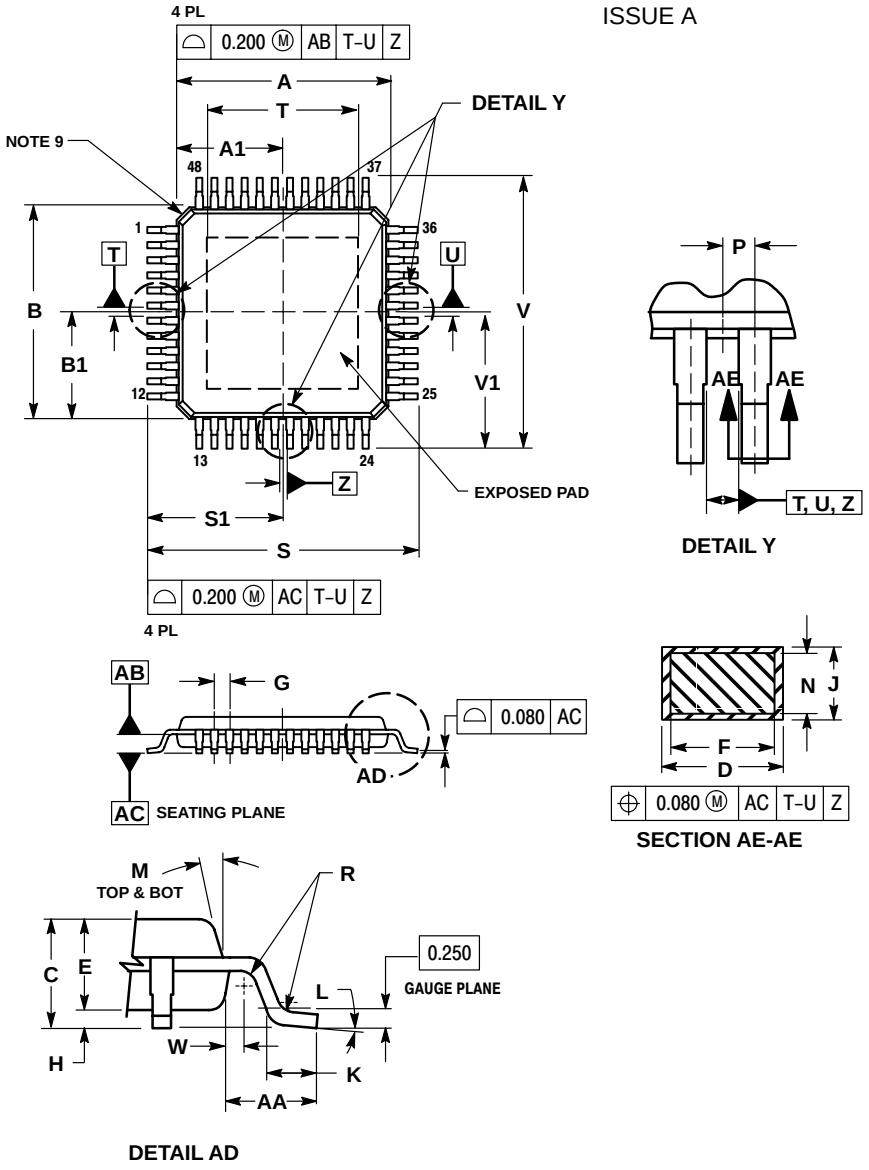

NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS S AND AB TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	0.900	1.100
D	0.170	0.270
E	0.950	1.250
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0 °	7 °
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
T	5.000 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	

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