FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21351-1E

ASSP

Dual Serial Input PLL Frequency Synthesizer

MB15F05L

■ DESCRIPTION

The Fujitsu MB15F05L is a serial input Phase Locked Loop (PLL) frequency synthesizer with a 1800MHz and a 233.15MHz prescalers. A 64/65 or a 128/129 for the 1800MHz prescaler, and a 16/17 for the 233.15MHz prescaler can be selected that enables pulse swallow operation.

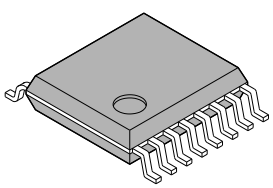
The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 5.0mA typ. at a supply voltage of 3.0V.
Furthermore, a super charger circuit is included to provide a fast tuning as well as low noise performance. As a result of this, MB15F05L is ideally suitable for digital mobile communications, such as PHS(Personal Handy Phone System).

■ FEATURES

- High frequency operationRF synthesizer: 1800MHz max. / IF synthesizer: 233.15MHz fixed
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 5.0 mA typ. (Vcc = 3V)
- Power saving function : Supply current at power saving mode Typ.0.1µA (Vcc=3V), Max.10µA (I_{PS1}=I_{PS2})
- Dual modulus prescaler : 1800MHz prescaler(64/65,128/129)
- Serial input 14–bit programmable reference divider: R = 5 to 16,383
- Serial input 18–bit programmable divider consisting of:
  - Binary 7–bit swallow counter: 0 to 127
  - Binary 11–bit programmable counter: 5 to 2,047
- On–chip high performance charge pump circuit and phase comparator, achieving high–speed lock–up and low phase noise
- On–chip phase control for phase comparator
- Wide operating temperature: Ta = -40 to 85˚C

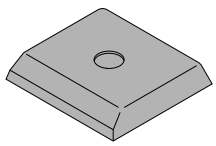
■ PACKAGES

16-pin, Plastic SSOP



(FPT-16P-M05)

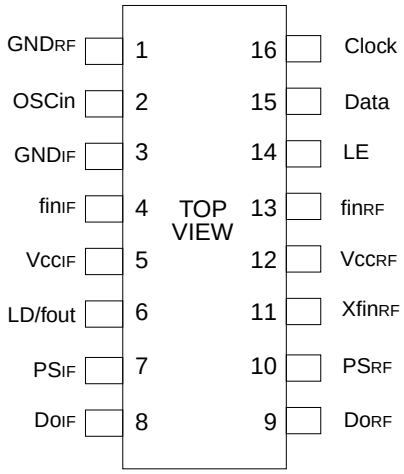
16-pin,plastic BCC



(LCC-16P-M03)

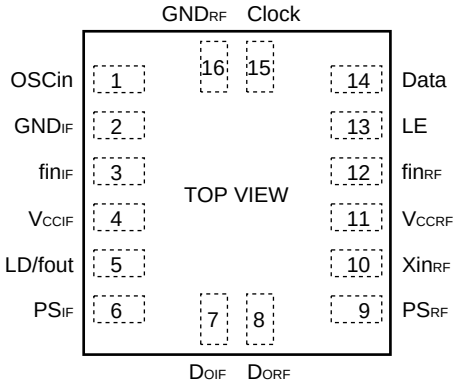
■ PIN ASSIGNMENTS

SSOP-16pin



(FPT-16P-M05)

BCC-16pin

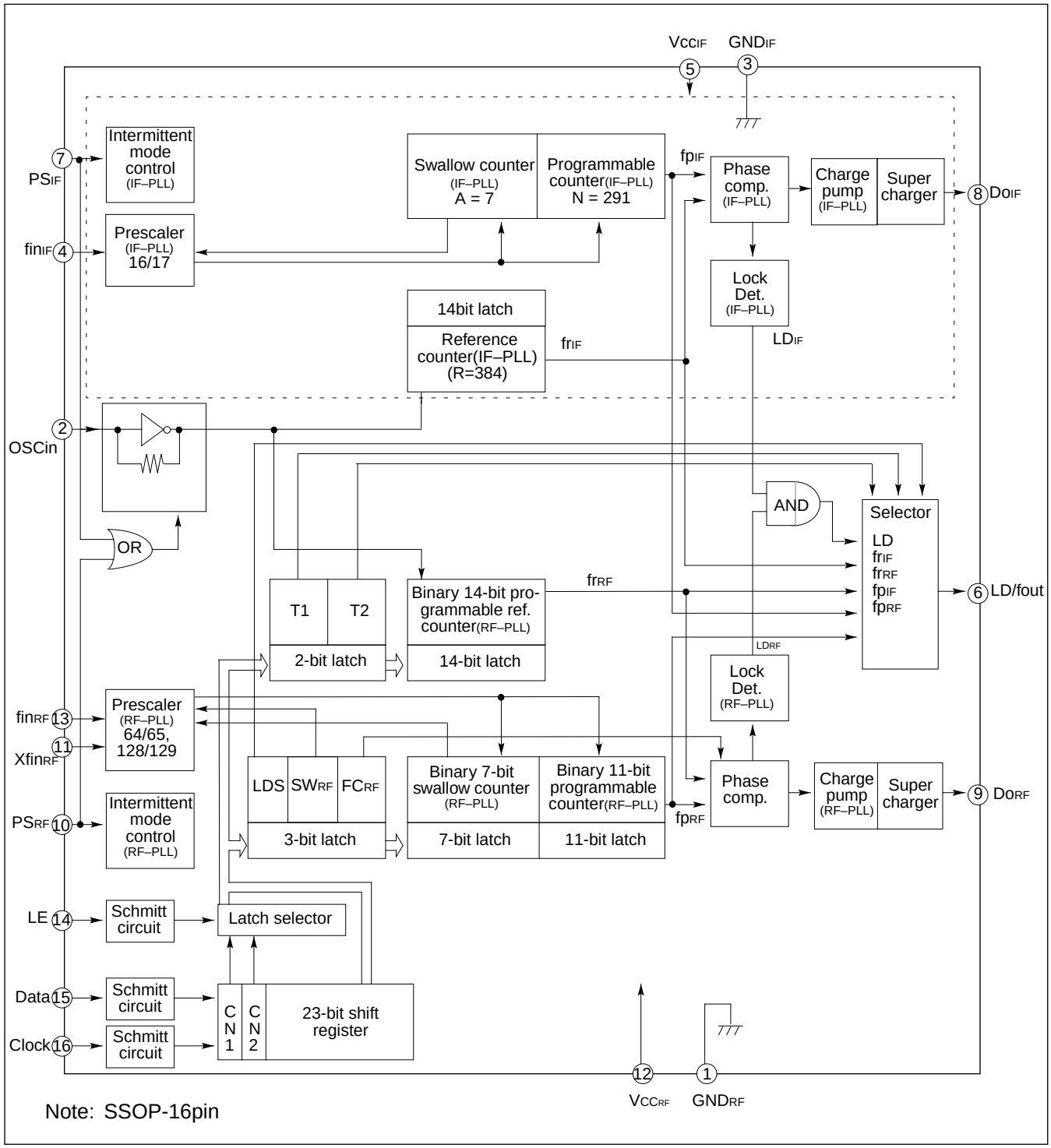


(LCC-16P-M03)

■ PIN DESCRIPTION

Pin No.		Pin name	I/O	Descriptions
SSOP16	BCC16			
1	16	GND_{RF}	–	Ground for RF–PLL section.
2	1	OSCin	I	The programmable reference divider input. TCXO should be connected with a AC coupling capacitor.
3	2	GND_{IF}	–	Ground for the IF-PLL section.
4	3	fin_{IF}	I	Prescaler input pin for the IF-PLL. The connection with VCO should be AC coupling.
5	4	Vcc_{IF}	–	Power supply voltage input pin for the IF-PLL section.
6	5	LD/fout	O	Lock detect signal output (LD) / phase comparator monitoring output (fout) The output signal is selected by a LDS bit in a serial data. LDS bit = ”H” ; outputs fout signal LDS bit = ”L” ; outputs LD signal
7	6	PS_{IF}	I	Power saving mode control for the IF-PLL section. This pin must be set at ”L” Power-ON. (Open is prohibited.) PS_{IF} = ”H” ; Normal mode PS_{IF} = ”L” ; Power saving mode
8	7	Do_{IF}	O	Charge pump output for the IF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
9	8	Do_{RF}	O	Charge pump output for the RF-PLL section. Phase characteristics of the phase detector can be reversed by FC-bit.
10	9	PS_{RF}	I	Power saving mode control for the RF-PLL section. This pin must be set at ”L” Power-ON. (Open is prohibited.) PS_{RF} = ”H” ; Normal mode PS_{RF} = ”L” ; Power saving mode
11	10	$Xfin_{RF}$	I	Prescaler complimentary input for the RF-PLL section. This pin should be grounded via a capacitor.
12	11	Vcc_{RF}	–	Power supply voltage input pin for the RF-PLL section, the shift register and the oscillator input buffer. When power is OFF, latched data of RF-PLL is cancelled.
13	12	fin_{RF}	I	Prescaler input pin for the RF-PLL. The connection with VCO should be AC coupling.
14	13	LE	I	Load enable signal input (with the schmitt trigger circuit.) When LE is ”H”, data in the shift register is transferred to the corresponding latch according to the control bit in a serial data.
15	14	Data	I	Serial data input (with the schmitt trigger circuit.) A data is transferred to the corresponding latch (IF-ref counter, IF-prog. counter, RF-ref. counter, RF-prog. counter) according to the control bit in a serial data.
16	15	Clock	I	Clock input for the 23-bit shift register (with the schmitt trigger circuit.) One bit data is shifted into the shift register on a rising edge of the clock.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	–0.5 to +4.0	V	
Input voltage	V_I	–0.5 to V_{CC} +0.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Output Current	Io	-10 to +10	mA	Except Do
	Ido	-25to+25	mA	Do output
Storage temperature	T_{STG}	–55 to +125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Note
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
Input voltage	V_i	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always yse semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with repect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

Handling Precautions

- This device should be transported and stored in anti-static containers.
- This is a static-sensitive device; take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workerbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boards with devices.

■ ELECTRICAL CHARACTERISTICS

(Vcc=2.7V to 3.6V, Ta=-40°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current		I_{CCIF}*1	fin_{IF} = 233.15MHz, fosc = 19.2MHz	–	1.5	–	mA
		I_{CCRF}*2	fin_{RF} = 1800MHz, fosc = 19.2MHz	–	3.5	–	
Power saving current		Ips_{IF}	Vcc_{IF} current at PS_{IF} ="L"	–	0.1*3	10	µA
		Ips_{RF}	Vcc_{RF} current at $PS_{IF/RF}$ ="L"	–	0.1*3	10	
Operating frequency	fin_{IF}*3	fin_{IF}	IF–PLL	233.15MHz(fosc=19.2MHz,fr=50kHz)			
	fin_{RF}*3	fin_{RF}	RF–PLL	100	–	1800	MHz
	OSCin	f_{OSC}	–	–	19.2	–	
Input sensitivity	fin_{IF}	$Vfin_{IF}$	IF–PLL, 50Ω termination	–10	–	+2	dBm
	fin_{RF}	$Vfin_{RF}$	RF–PLL, 50Ω termination	–10	–	+2	dBm
	OSCin	V_{OSC}	–	0.5	–	V_{CC}	Vp-p
Input voltage	Data, Clock, LE	V_{IH}	Schmitt trigger input	V_{CC}x0.7 + 0.4	–	–	V
		V_{IL}	Schmitt trigger input	–	–	V_{CC}x0.3–0.4	
	PS_{IF}, PS_{RF}	V_{IH}	–	V_{CC}x0.7	–		V
		V_{IL}	–	–	–	V_{CC}x0.3	
Input current	Data, Clock, LE, PS_{IF}, PS_{RF}	I_{IH}*5		–1.0		+1.0	µA
		I_{IL}*5		–1.0	–	+1.0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}*5		–100	–	0	
Output voltage	LD/fout	V_{OH}	I_{OH} = –1.0mA	V_{CC}–0.4	–		V
		V_{OL}	I_{OL} = 1.0mA	–	–	0.4	
	Do_{IF}, Do_{RF}	V_{DOH}	I_{DOH} = –1.0mA	V_{CC}–0.4	–		V
		V_{DOL}	I_{DOL} = 1.0mA	–	–	0.4	
High impedance cutoff current	Do_{IF}, Do_{RF}	I_{OFF}	V_{CC}=3.0V, V_{OFF}=GND to V_{CC}	–	–	3.0	nA

(Continued)

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(Vcc=2.7V to 3.6V, Ta=-40°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Output current	LD/fout	I_{OH}*5	Vcc = 3.0V	–1.0	–	–	mA
		I_{OL}	Vcc = 3.0V	–	–	1.0	
	D_{OIF}, D_{ORF}	I_{DOH}*5	Vcc = 3.0V, V_{DOH} = 2.0V , Ta=25°C	–11	–	–6	mA
		I_{DOL}	Vcc = 3.0V, V_{DOL} = 1.0V, Ta=25°C	8	–	15	

*1: Conditions ; Vcc_{IF} = 3V, Ta = 25°C, in locking state.
*2: Conditions ; Vcc_{RF} = 3V, Ta = 25°C, in locking state.
*3: fosc = 19.2 MHz , Vcc = 3.0V, Ta = 25°C, in locking state.
*4: AC coupling with a 1000pF capacitor connected.
*5: The symbol "-"(minus) means direction of current flow.

■ FUNCTIONAL DESCRIPTIONS

The divide ratio can be calculated using the following equation:

$f_{VCO} = \{(P \times N) + A\} \times f_{OSC} \div R \quad (A < N)$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)
P: Preset divide ratio of dual modulus prescaler (16 for IF-PLL, 64 or 128 for RF-PLL)
N: Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
A: Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
f_{OSC}: Reference oscillation frequency
R: Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)

Note: IF-PLL P = 16, N = 291, A = 7, R = 384, f_{OSC} = 19.2 MHz, f_{VCO} = 233.15 MHz, fr = 50 kHz (Fixed)

Serial Data Input

Serial data is entered using three pins, Data pin, Clock pin, and LE pin. Programmable dividers of IF/RF–PLL sections, programmable reference dividers of IF/RF PLL sections are controlled individually.
Serial data of binary data is entered through Data pin.
On rising edge of clock, one bit of serial data is transferred into the shift register. When load enable signal is high, the data stored in the shift register is transferred to one of latch of them depending upon the control bit data setting.

Table1. Control Bit

Control bit		Destination of serial data
CN1	CN2	
H	L	The programmable reference counter for the RF-PLL.
H	H	The programmable counter and the swallow counter for the RF-PLL

Shift Register Configuration

Programmable Reference Counter

LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	T1	T2	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	X	X	X	X	X

CN1, 2 : Control bit [Table. 1]
R1 to R14: Divide ratio setting bits for the programmable reference counter (5 to 16,383) [Table. 2]
T1, 2 : Test purpose bit [Table.3]
X : Dummy bits(Set "0" or "1")
NOTE: Data input with MSB first.

Programmable Counter

LSB ← Data Flow → MSB

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
CN1	CN2	LDS	SW_{RF}	FC_{RF}	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

CN1, 2 : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 4]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 5]
SW_{RF} : Divide ratio setting bit for the RF prescaler0 [Table. 6}
FC_{RF} : Phase control bit for the RF phase detector [Table. 7]
LDS : LD/fout signal select bit [Table. 8]

Note: Data input with MSB first.

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Test Purpose Bit Setting

T1	T2	LD/fout pin state
L	L	Outputs $fr_{IF.}$
H	L	Outputs $fr_{RF.}$
L	H	Outputs $fp_{IF.}$
H	H	Outputs $fp_{RF.}$

Table.4 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.5 Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 6 Prescaler Data Setting

		SW = "H"	SW = "L"
Prescaler divide ratio	RF-PLL	64/65	128/129

Table. 7 Phase Comparator Phase Switching Data Setting

Phase Comparator input	FCRF = H	FCRF = L
	DORF	DORF
fr > fp	H	L
fr = fp	Z	Z
fr < fp	L	H
VCO polarity	(1)	(2)

Phase Comparator input	FCIF = H
	DOIF
fr > fp	H
fr = fp	Z
fr < fp	L

- Z = High–impedance
- Depending upon the VCO and LPF polarity, FC bit should be set.

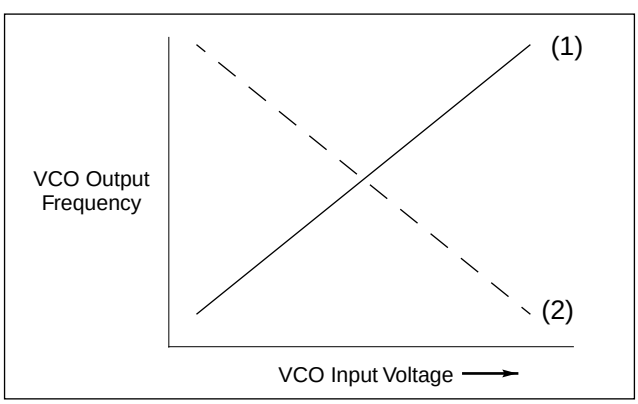
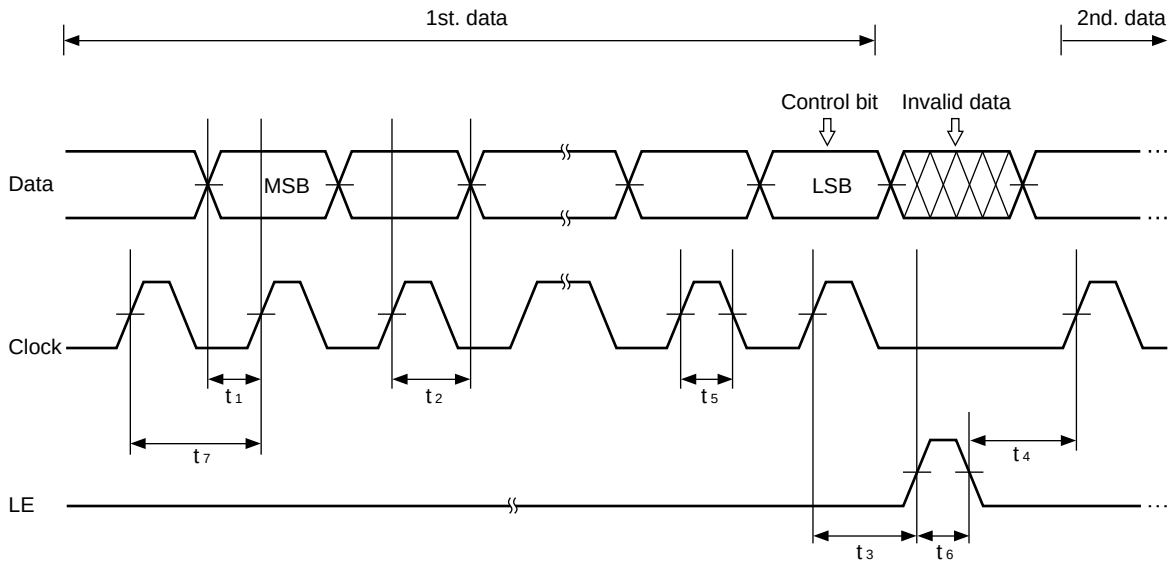


Table. 8 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signals
L	LD signal

Serial Data Input Timing

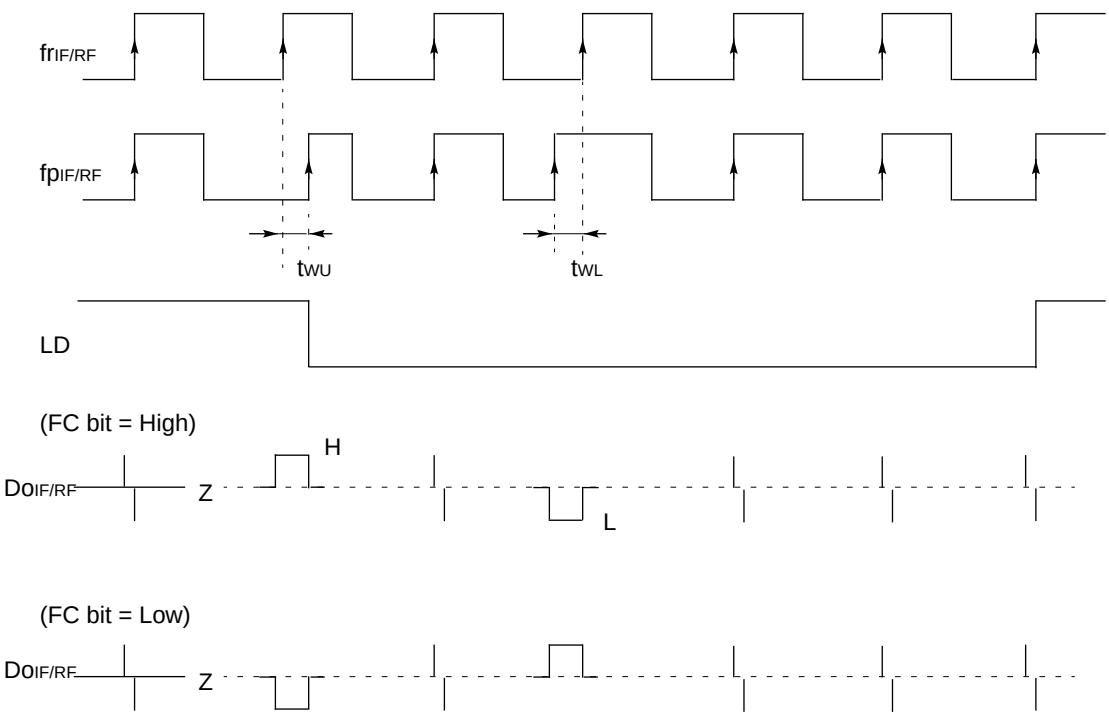


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min	Typ.	Max	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

Parameter	Min	Typ	Max	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

■ PHASE DETECTOR OUTPUT WAVEFORM



LD Output Logic Table

IF–PLL section	RF–PLL section	LD output
Locking state / Power saving state	Locking state / Power saving state	H
Locking state / Power saving state	Unlocking state	L
Unlocking state	Locking state / Power saving state	L
Unlocking state	Unlocking state	L

Note: •Phase error detection range = –2π to +2π
•Pulses on $Do_{IF/RF}$ signals are output to prevent dead zone.
•LD output becomes low when phase error is t_{WU} or more.
•LD output becomes high when phase error is t_{WL} or less and continues to be so for three cycles or more.
•t_{WU} and t_{WL} depend on OSCin input frequency as follows.
$t_{WU} \geq 4/fosc$: i.e. $t_{WU} \geq 312.5ns$ when foscin = 12.8 MHz
$t_{WL} \leq 8/fosc$: i.e. $t_{WL} \leq 625.0ns$ when foscin = 12.8 MHz

■ POWER SAVING MODE (INTERMITTENT MODE CONTROL CIRCUIT)

Setting a $PS_{IF(RF)}$ pin to Low, IF-PLL (RF-PLL) enters into power saving mode resultant current consumption can be limited to 10μA (typ.). Setting PS pin to High, power saving mode is released so that the device works normally.

In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (fr) and comparison frequency (fp) and may in the worst case take longer time for lock up of the loop.

To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up. Thus keeping the loop locked.

PS pin must be set "L" at Power-ON.

Allow 1 μs after frequency stabilization on power-up for exiting the power saving mode (PS: L to H)

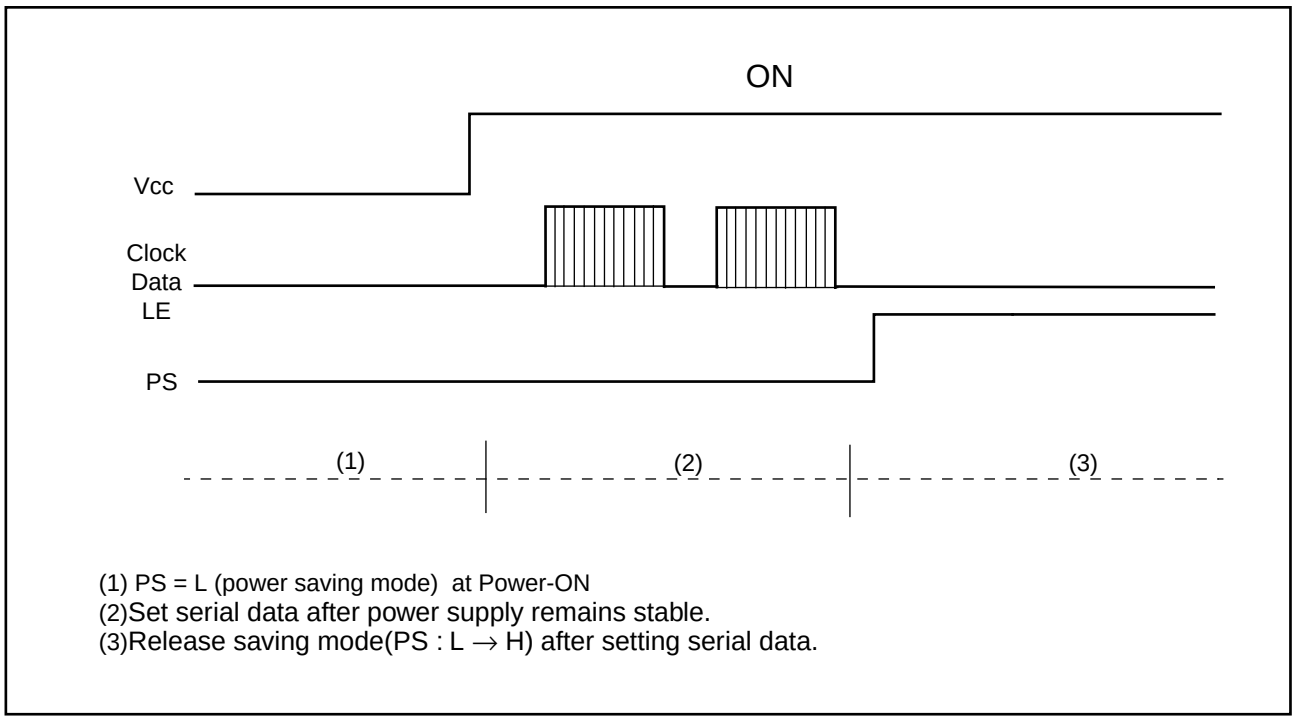
Serial data can be entered during the power saving mode.

During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10μA per one PLL section.

At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.

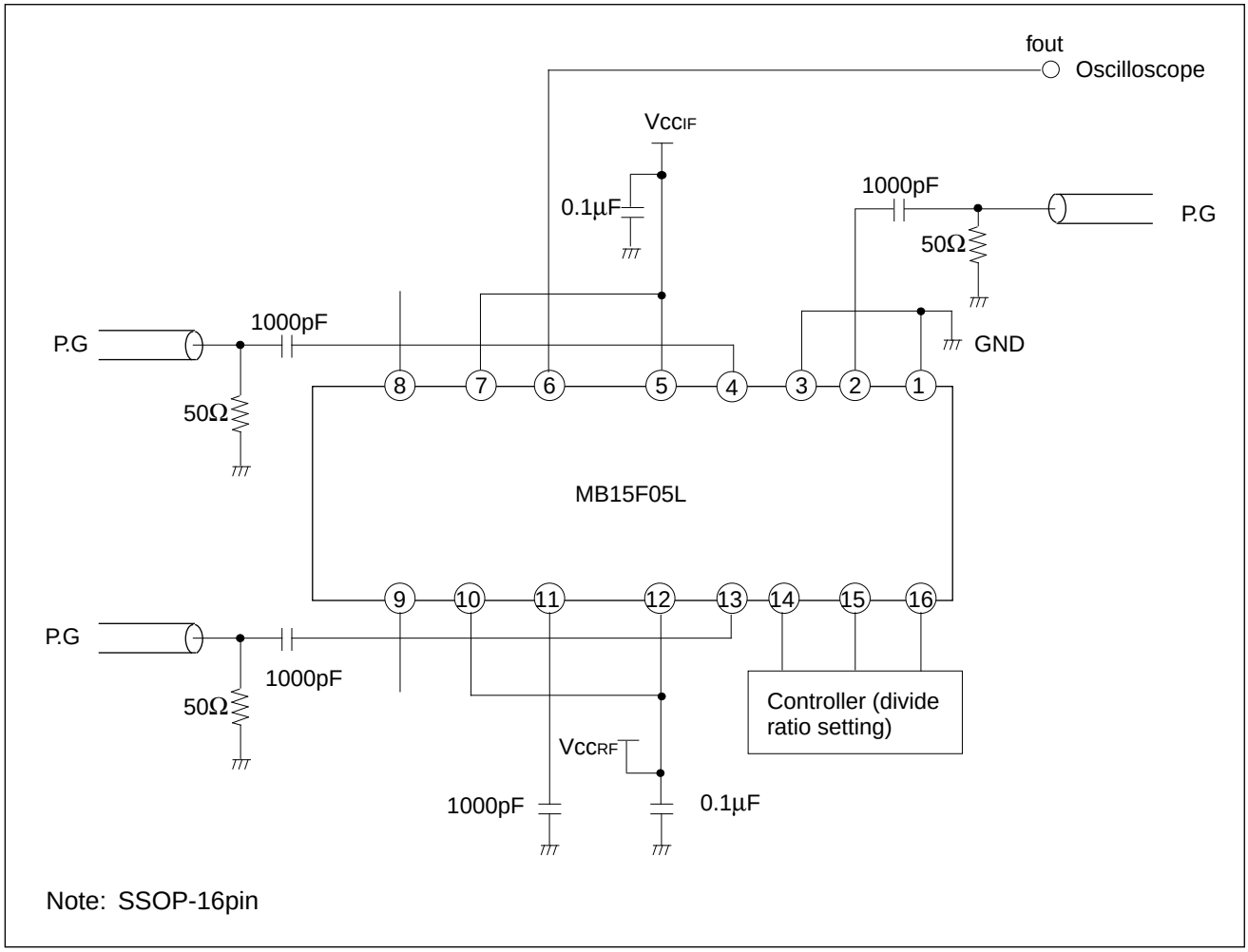
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF's time constant. As a result of this, VCO's frequency is kept at the locking frequency.

PS_{IF}	PS_{RF}	IF-PLL counters	RF-PLL counters	OSC input buffer
L	L	OFF	OFF	OFF
H	L	ON	OFF	ON
L	H	OFF	ON	ON
H	H	ON	ON	ON



(1) PS = L (power saving mode) at Power-ON
(2)Set serial data after power supply remains stable.
(3)Release saving mode(PS : L → H) after setting serial data.

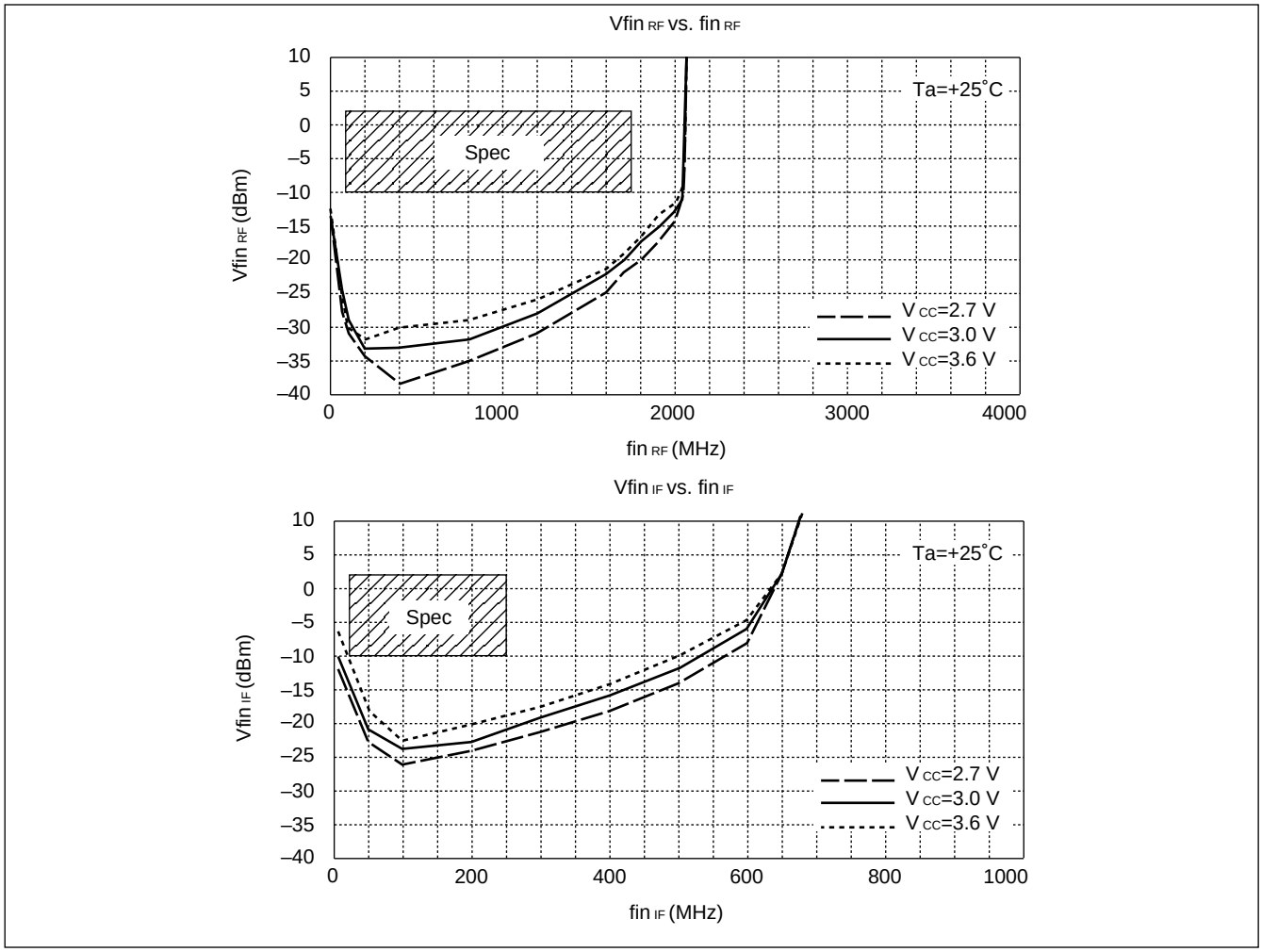
■ TEST CIRCUIT (Prescaler Input/Programmable Reference Divider Input Sensitivity Test)



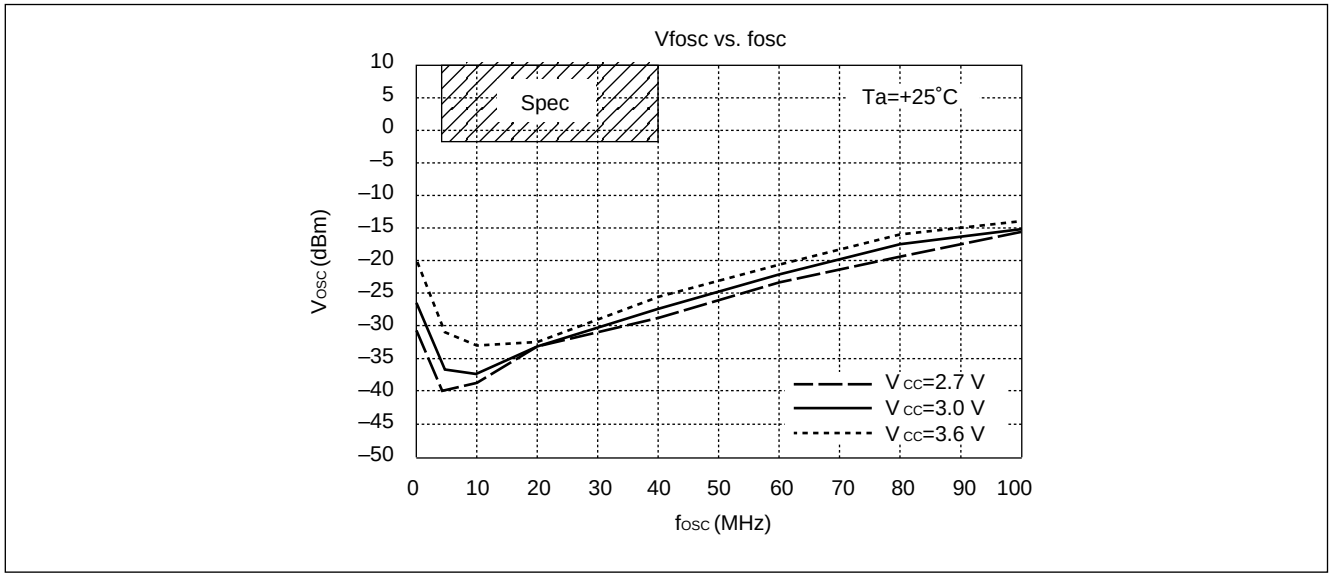
Note: SSOP-16pin

■ TYPICAL CHARACTERISTICS

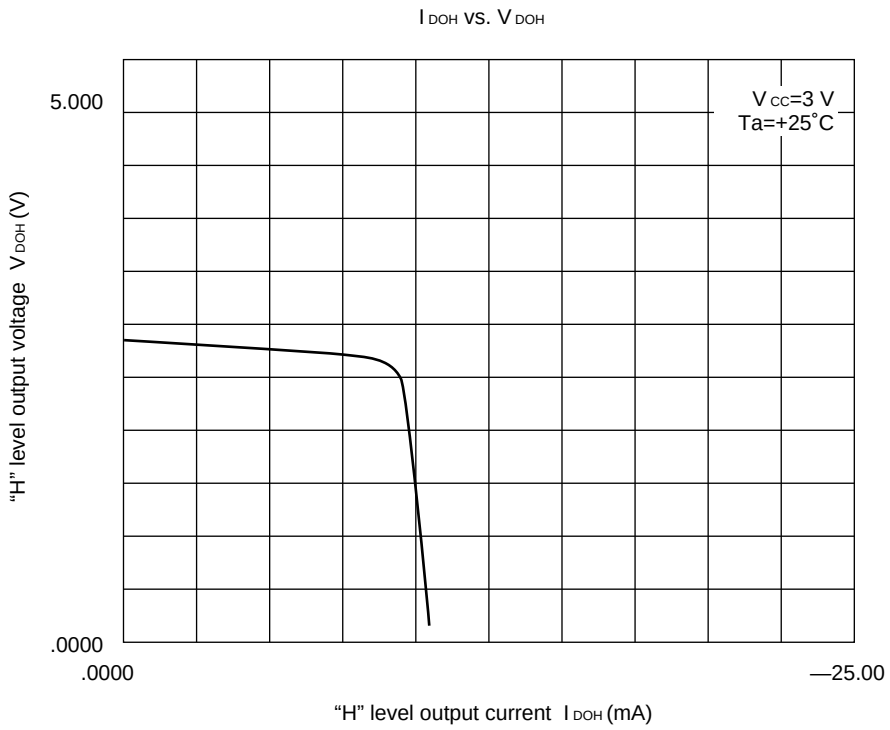
1. fin Input Sensitivity

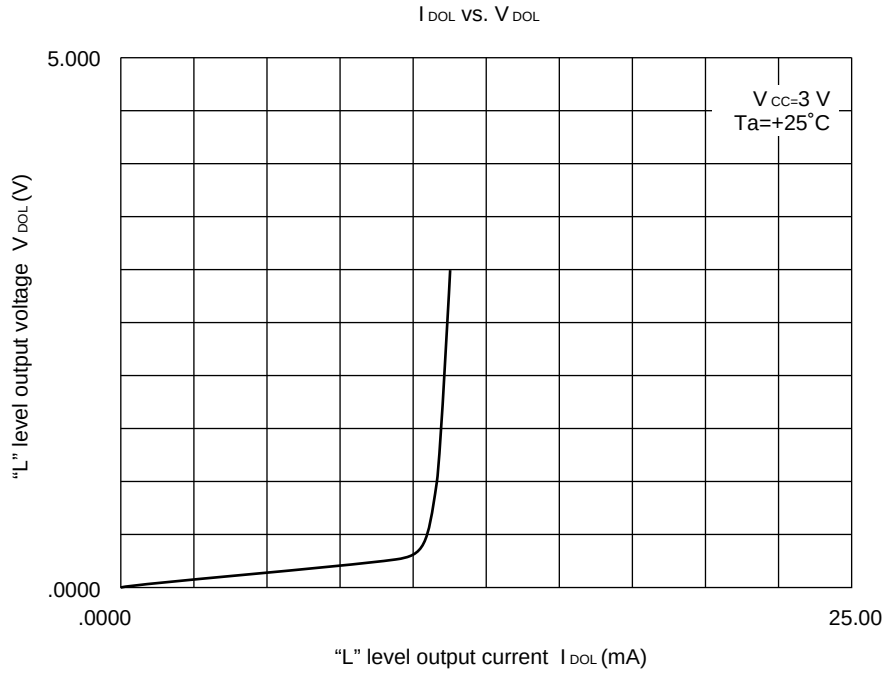


2. OSCIN Input Characteristics

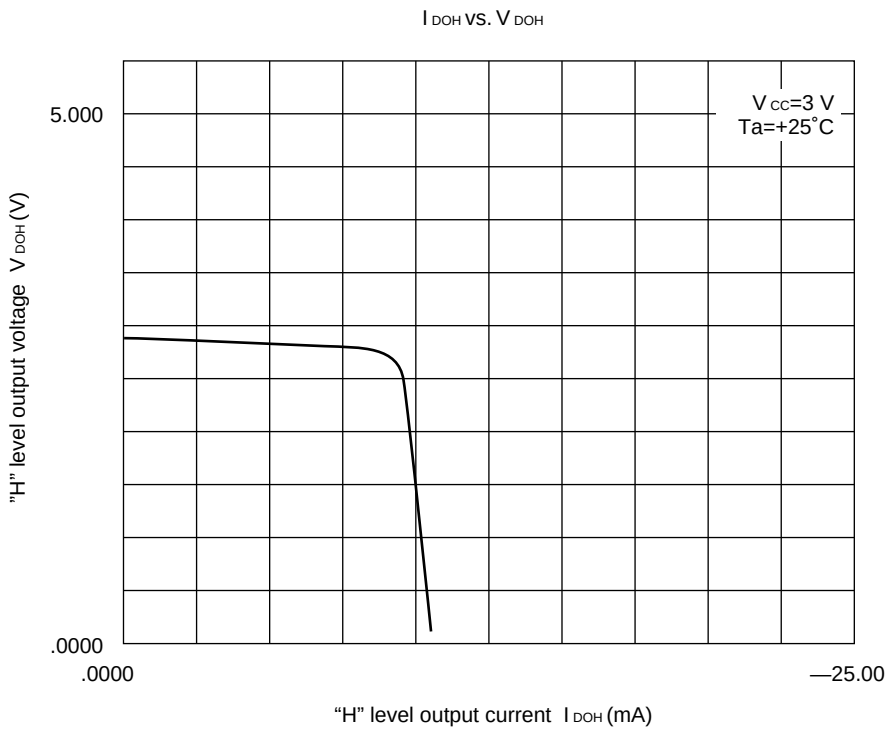


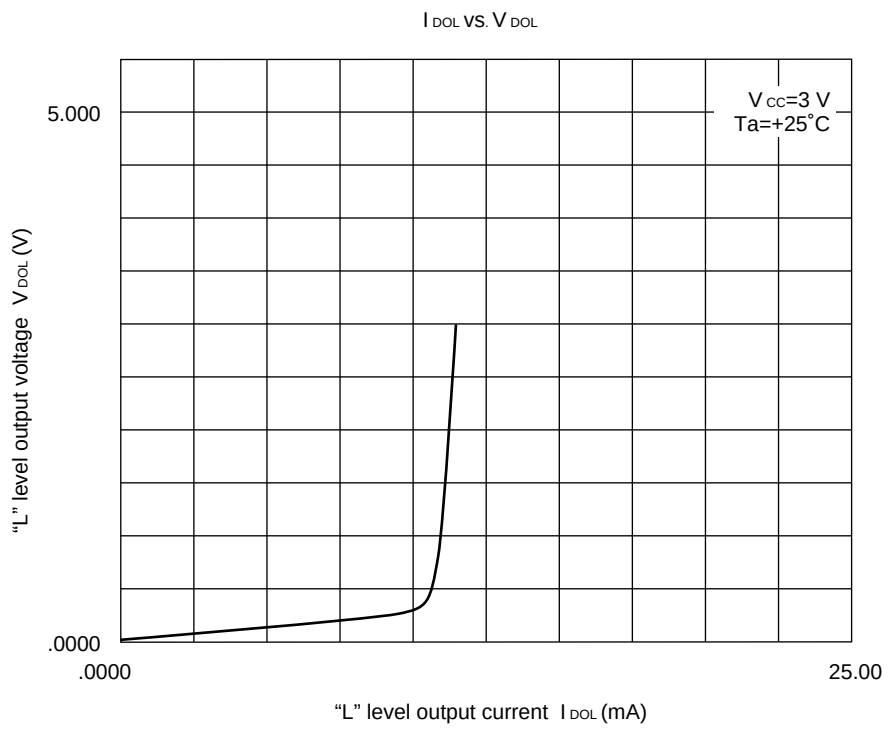
3. D_{ORF} Output Current



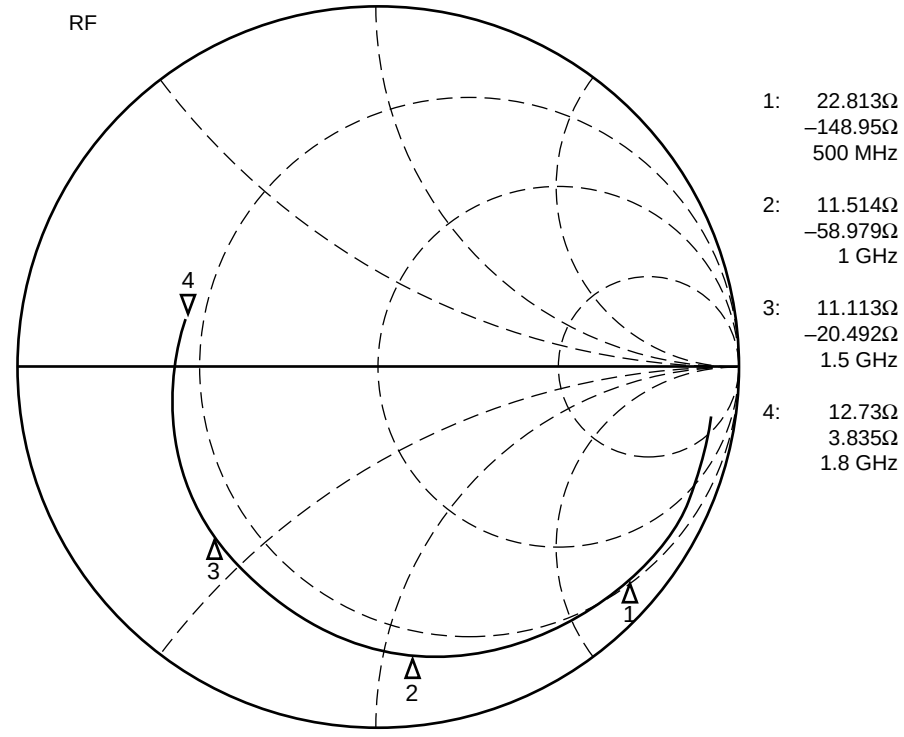


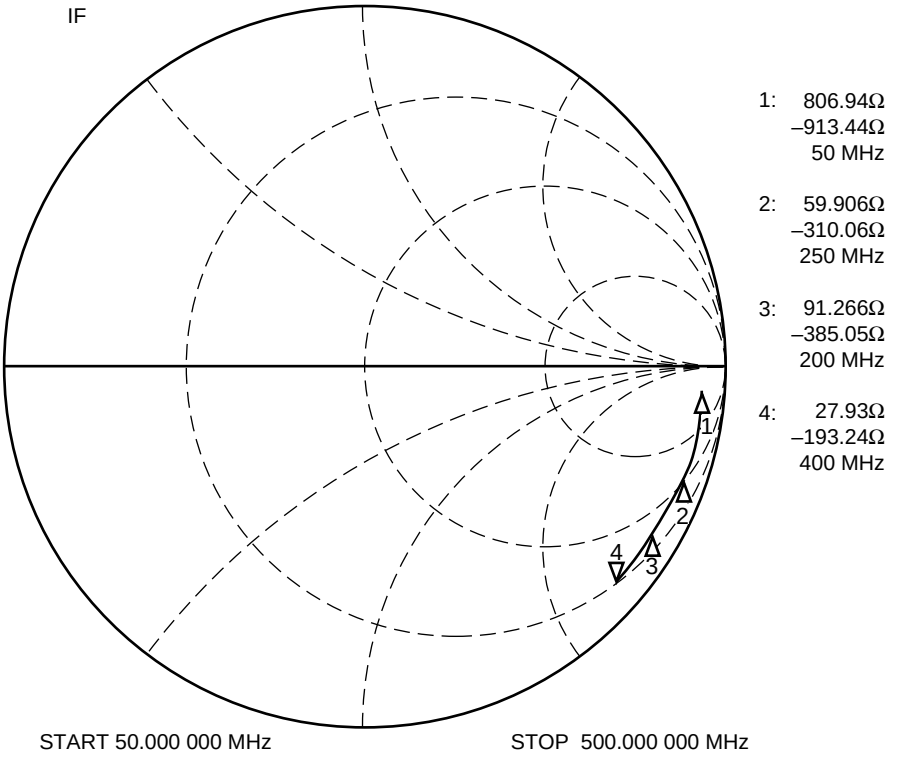
4. DOIF Output Current





5. Input Impedance





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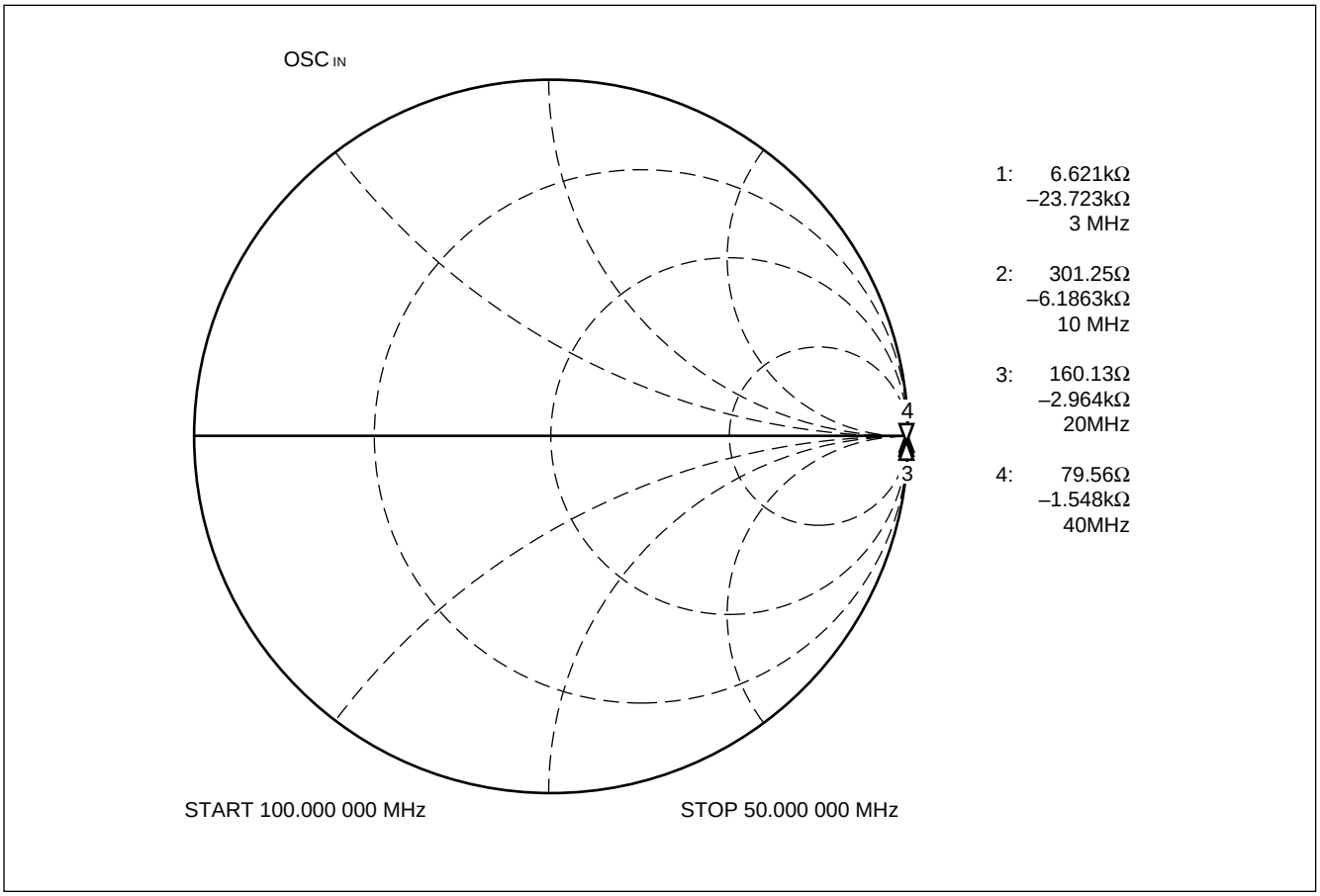
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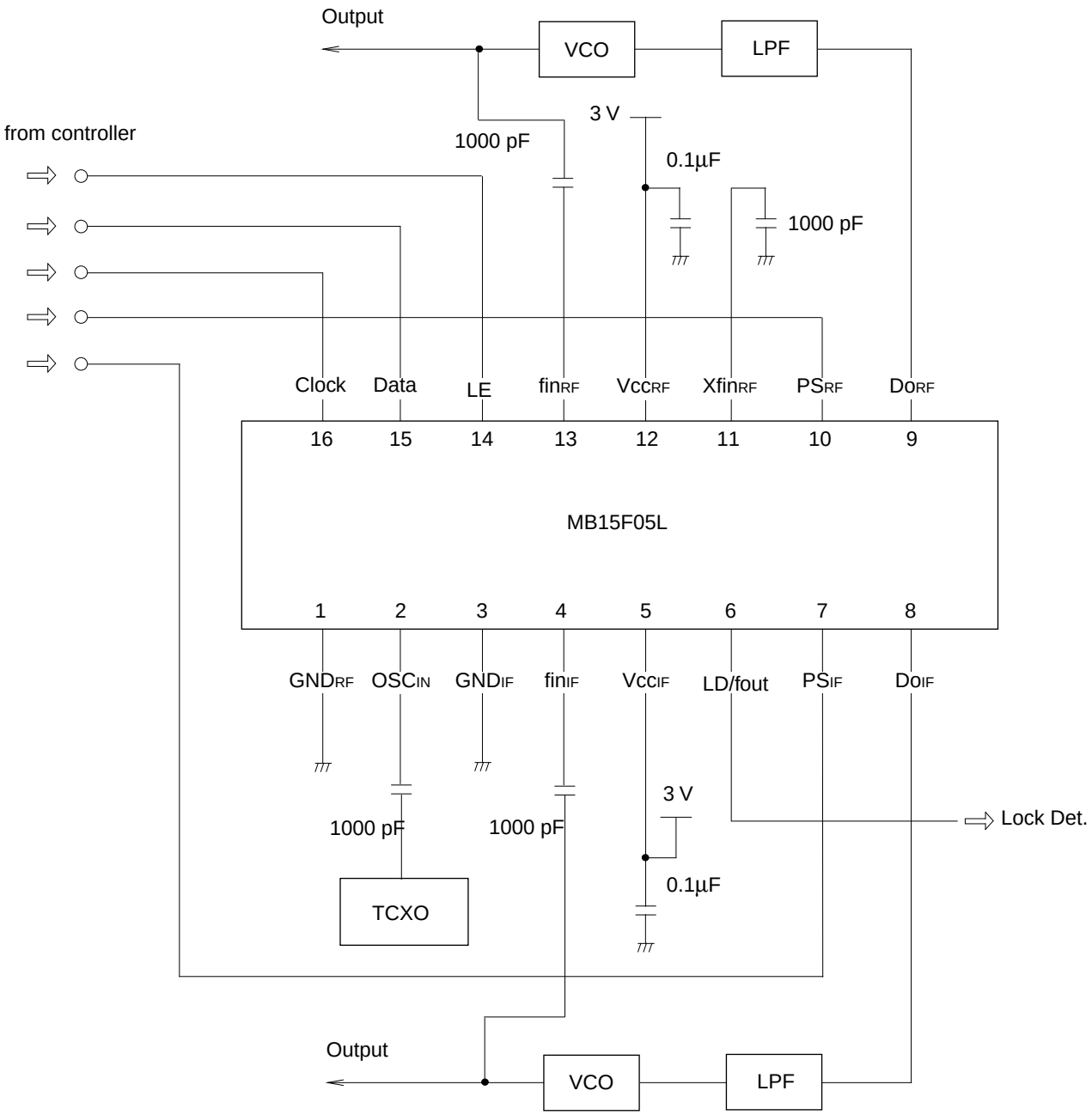
4
3
1: 6.621kΩ
–23.723kΩ
3 MHz
2: 301.25Ω
–6.1863kΩ
10 MHz
3: 160.13Ω
–2.964kΩ
20MHz
4: 79.56Ω
–1.548kΩ
40MHz
START 100.000 000 MHz
STOP 50.000 000 MHz

■ APPLICATION EXAMPLE



Clock, Data, LE: Schmitt trigger circuit is provided (insert a pull-down or pull-up resistor to prevent oscillation when open-circuited in the input).

Note: SSOP-16pin

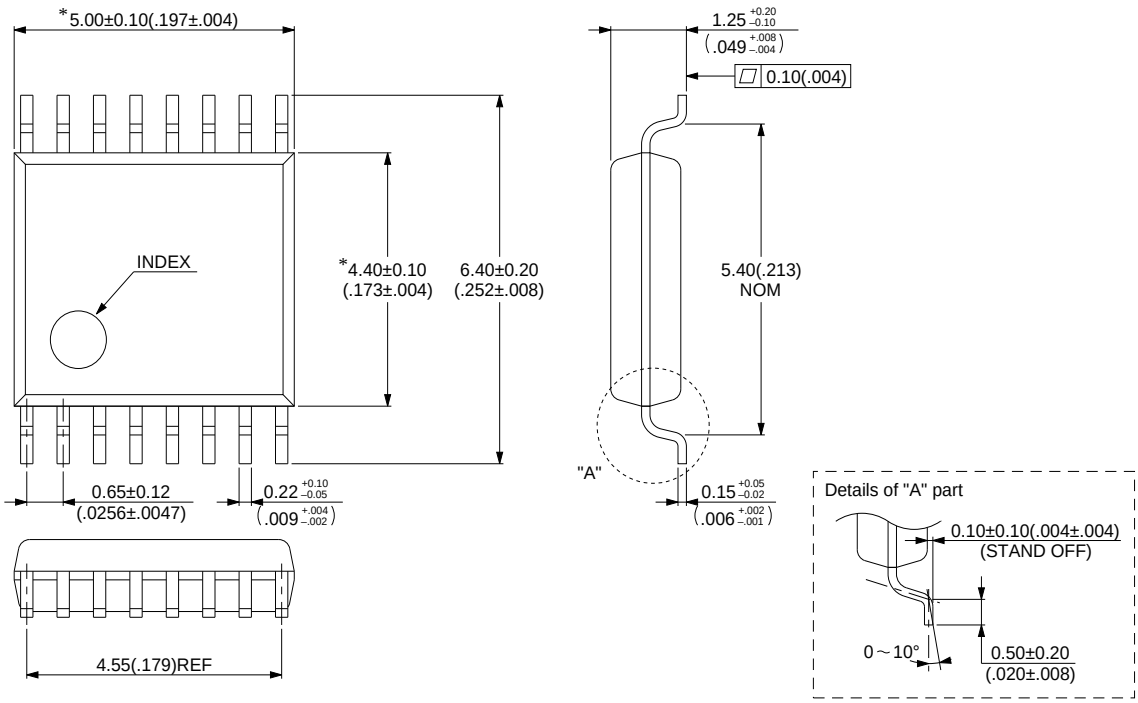
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15F05L PFV	16pin, Plastic SSOP (FPT-16P-M05)	
MB15F05L PV	16pin, Plastic BCC (LCC-16P-M03)	

■ PACKAGE DIMENSIONS

16 pins, Plastic SSOP
(FPT-16P-M05)

* : These dimensions do not include resin protrusion.

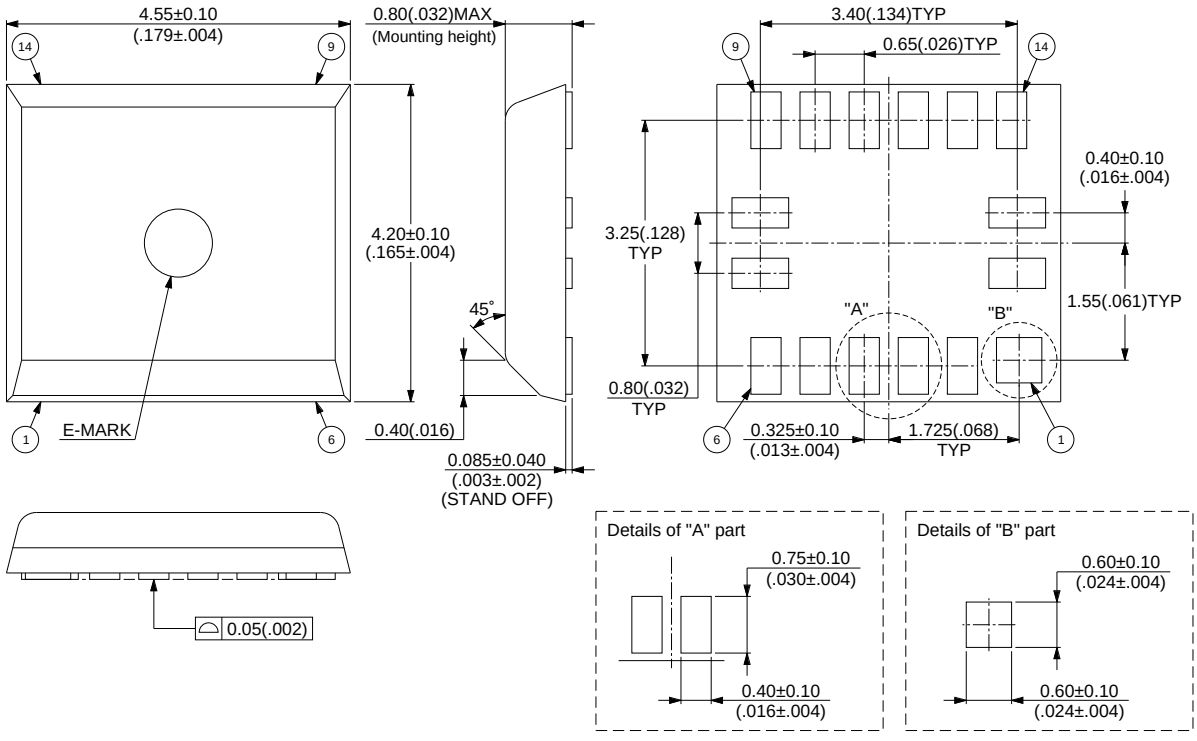


Dimensions in mm (inches)

(Continued)

16 pins, Plastic BCC
(LCC-16P-M03)

* : These dimensions do not include resin protrusion.



Dimensions in mm (inches)

FUJITSU LIMITED

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