PRELIMINARY

Integrated Circuit Systems, Inc.

ICS844003I-01

FEMTOCLOCKS™ CRYSTAL-TO-LVDS FREQUENCY SYNTHESIZER

GENERAL DESCRIPTION

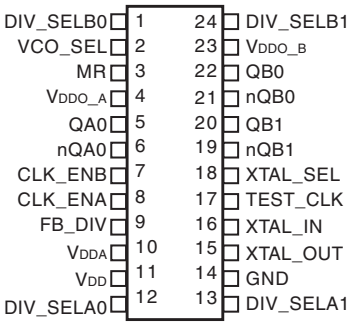
The ICS844003I-01 is a 3 differential output LVDS Synthesizer designed to generate Ethernet reference clock frequencies and is a member of the HiPerClocks™ family of high performance clock solutions from ICS. Using a 19.53125MHz or 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of 4 frequency select pins (DIV_SEL[A1:A0], DIV_SEL[B1:B0]): 625MHz, 312.5MHz, 156.25MHz, and 125MHz. The 844003I-01 has 2 output banks, Bank A with 1 differential LVDS output pair and Bank B with 2 differential LVDS output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The ICS844003I-01 uses ICS' 3rd generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS844003I-01 is packaged in a small 24-pin TSSOP package.

FEATURES

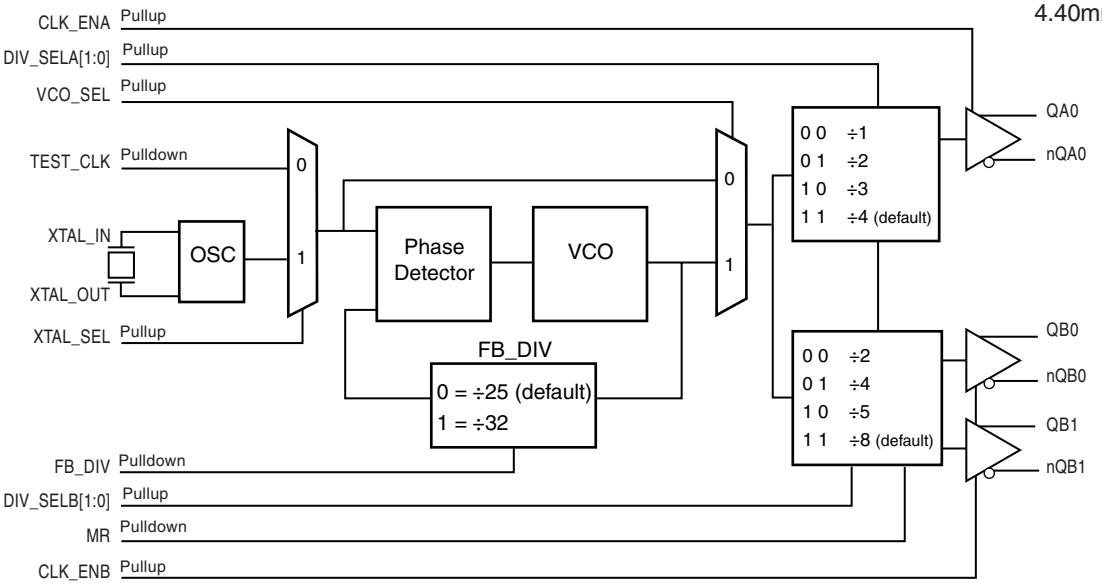
- Three LVDS outputs on two banks, A Bank with one LVDS pair and B Bank with 2 LVDS output pairs
- Using a 19.53125MHz or 25MHz crystal, the two output banks can be independently set for 625MHz, 312.5MHz, 156.25MHz or 125MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz to 680MHz
- RMS phase jitter @ 156.25MHz (1.875MHz - 20MHz): 0.56ps (typical)
- 3.3V output supply mode
- -40°C to 85°C ambient operating temperature

PIN ASSIGNMENT



ICS844003I-01
24-Lead TSSOP
4.40mm x 7.8mm x 0.92mm
package body
G Package
Top View

BLOCK DIAGRAM



The Preliminary Information presented herein represents a product in prototyping or pre-production. The noted characteristics are based on initial product characterization. Integrated Circuit Systems, Incorporated (ICS) reserves the right to change any circuitry or specifications without notice.

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 24	DIV_SELB0, DIV_SELB1	Input	Pullup	Division select pin for Bank B. Default = HIGH. LVCMOS/LVTTL interface levels. See Table 3C.
2	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or TEST_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. Has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
4	V_{DDO_A}	Power		Output supply pin for Bank A outputs.
5, 6	QA0, nQA0	Ouput		Differential output pair. LVDS interface levels.
7	CLK_ENB	Input	Pullup	Synchronizing clock enable for Bank B outputs. Active High output enable. When logic HIGH, the output pair in Bank B is enabled. When logic LOW, the QB outputs are LOW and nQB outputs are HIGH. Has an internal pullup resistor so the default power-up state of output is enabled. LVCMOS/LVTTL interface levels. See Figure 1.
8	CLK_ENA	Input	Pullup	Synchronizing clock enable for Bank A outputs. Active High output enable. When logic HIGH, the output pair in Bank A is enabled. When logic LOW, the QA output is LOW and nQA output is HIGH. Has an internal pullup resistor so the default power-up state of output is enabled. LVCMOS/LVTTL interface levels. See Figure 1.
9	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷25. When HIGH, the feedback divider is set for ÷32. LVCMOS/LVTTL interface levels. See Table 3D.
10	V_{DDA}	Power		Analog supply pin.
11	V_{DD}	Power		Core supply pin.
12, 13	DIV_SELA0, DIV_SELA1	Input	Pullup	Division select pin for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels. See Table 3C.
14	GND	Power		Power supply ground.
15, 16	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
17	TEST_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.
18	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended TEST_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
19, 20	nQB1, QB1	Output		Differential output pair. LVDS interface levels.
21, 22	nQB0, QB0	Output		Differential output pair. LVDS interface levels.
23	V_{DDO_B}	Power		Output supply pin for Bank B outputs.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pullup Resistor			51		kΩ

TABLE 3A. BANK A FREQUENCY TABLE

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0/nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELA1	DIV_SELA0				
25	0	0	0	25	1	25	625
25	0	0	1	25	2	12.5	312.5
20	0	0	1	25	2	12.500	250
22.5	0	1	0	25	3	8.333	187.5
25	0	1	1	25	4	6.25	156.25
24	0	1	1	25	4	6.25	150
20	0	1	1	25	4	6.25	125
19.44	1	0	0	32	1	32	622.08
19.44	1	0	1	32	2	16	311.04
15.625	1	0	1	32	2	16	250
18.75	1	1	0	32	3	10.667	200
19.44	1	1	1	32	4	8	155.52
18.75	1	1	1	32	4	8	150
15.625	1	1	1	32	4	8	125

TABLE 3B. BANK B FREQUENCY TABLE

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QB0/nQB0 Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELB1	DIV_SELB0				
25	0	0	0	25	2	12.5	312.5
20	0	0	0	25	2	12.5	250
25	0	0	1	25	4	6.25	156.25
24	0	0	1	25	4	6.25	150
20	0	0	1	25	4	6.25	125
25	0	1	0	25	5	5	125
25	0	1	1	25	8	3.125	78.125
24	0	1	1	25	8	3.125	75
20	0	1	1	25	8	3.125	62.5
19.44	1	0	0	32	2	16	311.04
15.625	1	0	0	32	2	16	250
19.44	1	0	1	32	4	8	155.52
18.75	1	0	1	32	4	8	150
15.625	1	0	1	32	4	8	125
15.625	1	1	0	32	5	6.4	100
19.44	1	1	1	32	8	4	77.76
18.75	1	1	1	32	8	4	75
15.625	1	1	1	32	8	4	62.5

TABLE 3C. OUTPUT BANK CONFIGURATION SELECT FUNCTION TABLE

Inputs		Outputs
DIV_SELA1	DIV_SELA0	QA, nQA
0	0	÷1
0	1	÷2
1	0	÷3
1	1	÷4 (default)

Inputs		Outputs
DIV_SELB1	DIV_SELB0	QBx, nQBx
0	0	÷2
0	1	÷4
1	0	÷5
1	1	÷8 (default)

TABLE 3D. FEEDBACK DIVIDER CONFIGURATION SELECT FUNCTION TABLE

Inputs	
FB_DIV	Feedback Divide
0	÷25
1	÷32

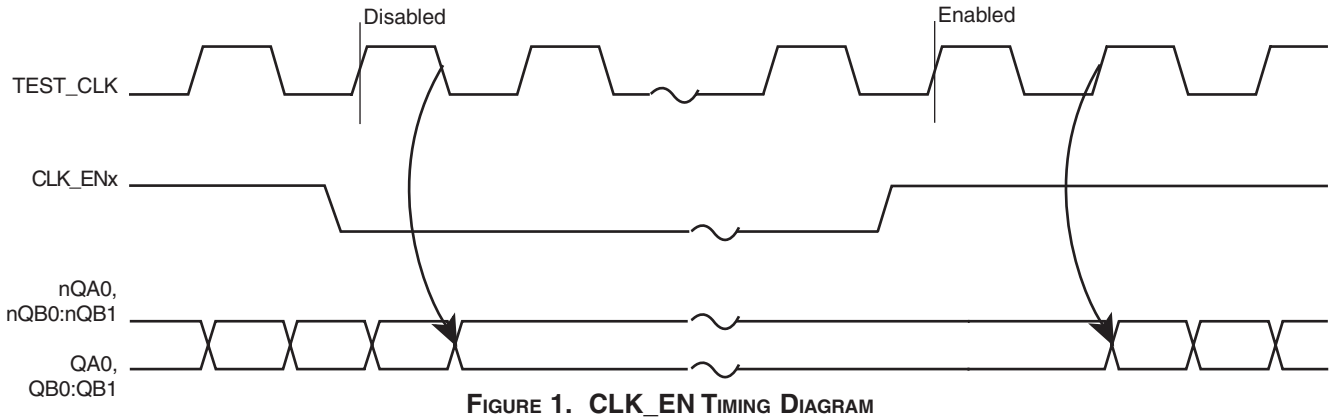


FIGURE 1. CLK_EN TIMING DIAGRAM

TABLE 3E. CLK_ENA SELECT FUNCTION TABLE

Inputs	Outputs	
CLK_ENA	QA0	nQA0
0	LOW	HIGH
1	Active	Active

TABLE 3F. CLK_ENB SELECT FUNCTION TABLE

Inputs	Outputs	
CLK_ENB	QB0:QB1	nQB0:nQB1
0	LOW	HIGH
1	Active	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	70°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO\_A, B}$	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			102		mA
I_{DDA}	Analog Supply Current			10		mA
$I_{DDO\_A, B}$	Output Supply Current			50		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	TEST_CLK, MR, FB_DIV	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		DIV_SELB0, DIV_SELB1, DIV_SELA0, DIV_SELA1, VCO_SEL, XTAL_SEL, CLK_ENA, CLK_ENB	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	TEST_CLK, MR, FB_DIV	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		DIV_SELB0, DIV_SELB1, DIV_SELA0, DIV_SELA1, VCO_SEL, XTAL_SEL, CLK_ENA, CLK_ENB	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, TA = -40°C TO 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			0	50	mV
V_{OS}	Offset Voltage			1.35		V
ΔV_{OS}	V_{OS} Magnitude Change			0	50	mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷25		19.6		27.2	MHz
	FB_DIV = ÷32		15.313		21.25	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF
Drive Level					1	mW

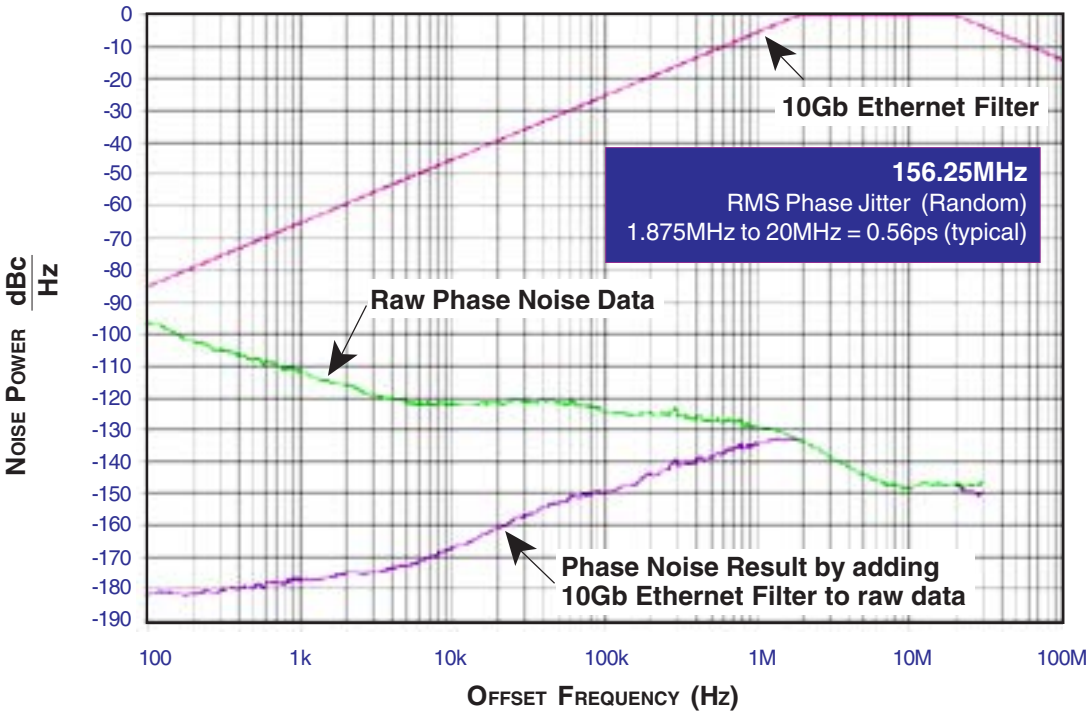
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO\_A} = V_{DDO\_B}$ = 3.3V±5%, TA = -40°C TO 85°C

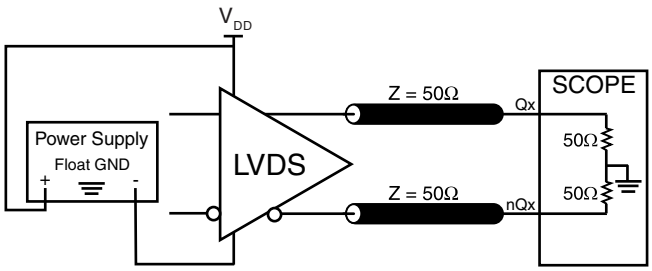
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency Range	Output Divider = ÷1	490		680	MHz
		Output Divider = ÷2	245		340	MHz
		Output Divider = ÷3	163.33		226.67	MHz
		Output Divider = ÷4	122.5		170	MHz
		Output Divider = ÷5	98		136	MHz
		Output Divider = ÷8	61.25		85	MHz
*t*sk(b)	Bank Skew, NOTE 1			8		ps
*t*sk(o)	Output Skew; NOTE 2, 4	Outputs @ Same Frequency		11		ps
		Outputs @ Different Frequencies		109		ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	625MHz (1.875MHz - 20MHz)		0.53		ps
		312.5MHz (1.875MHz - 20MHz)		0.53		ps
		156.25MHz (1.875MHz - 20MHz)		0.56		ps
		125MHz (1.875MHz - 20MHz)		0.58		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		325		ps
odc	Output Duty Cycle			50		%

NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Please refer to the Phase Noise Plots.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

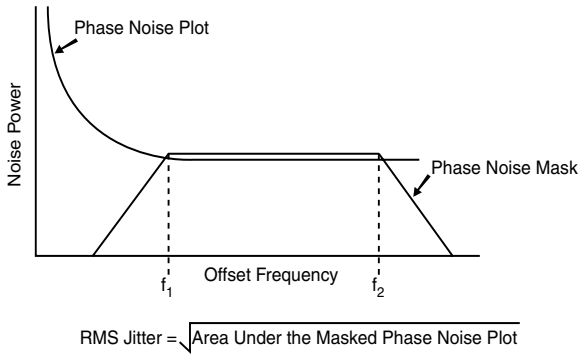
TYPICAL PHASE NOISE AT 156.25MHZ



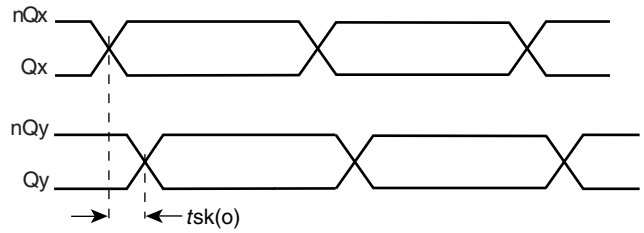
PARAMETER MEASUREMENT INFORMATION



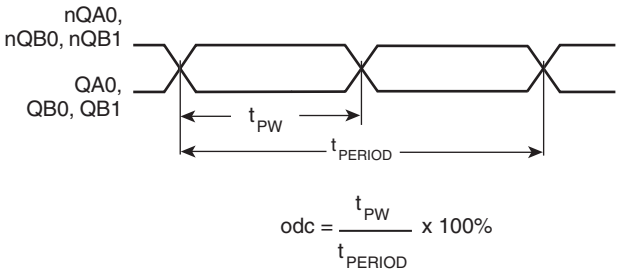
LVDS 3.3V OUTPUT LOAD AC TEST CIRCUIT



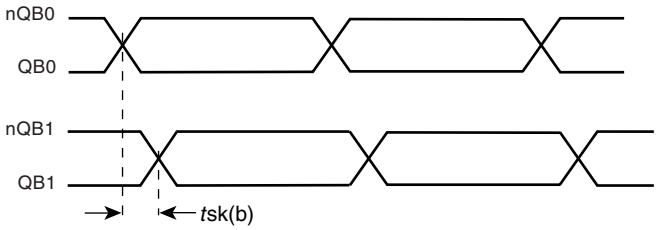
RMS PHASE JITTER



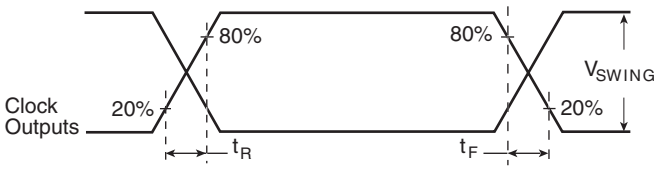
OUTPUT SKEW



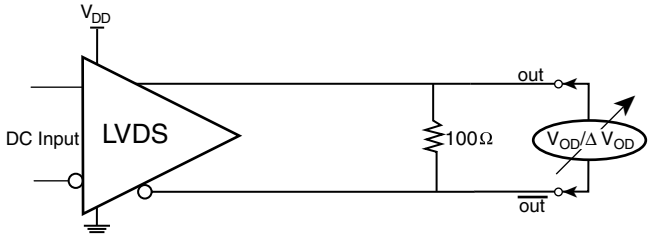
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



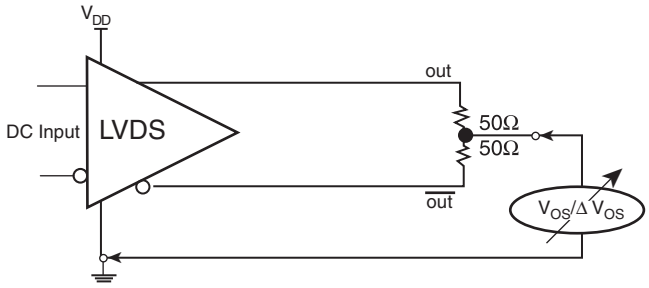
BANK SKEW



OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS844003I-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, and V_{DDOx} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 2* illustrates how a 10Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

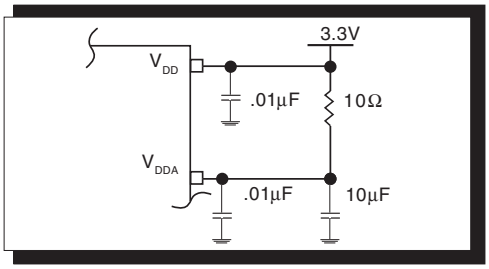


FIGURE 2. POWER SUPPLY FILTERING

CRYSTAL INPUT INTERFACE

The ICS844003I-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 3* below were determined using a 19.53125MHz or 25MHz 18pF parallel resonant crystal and were chosen to minimize the ppm error.

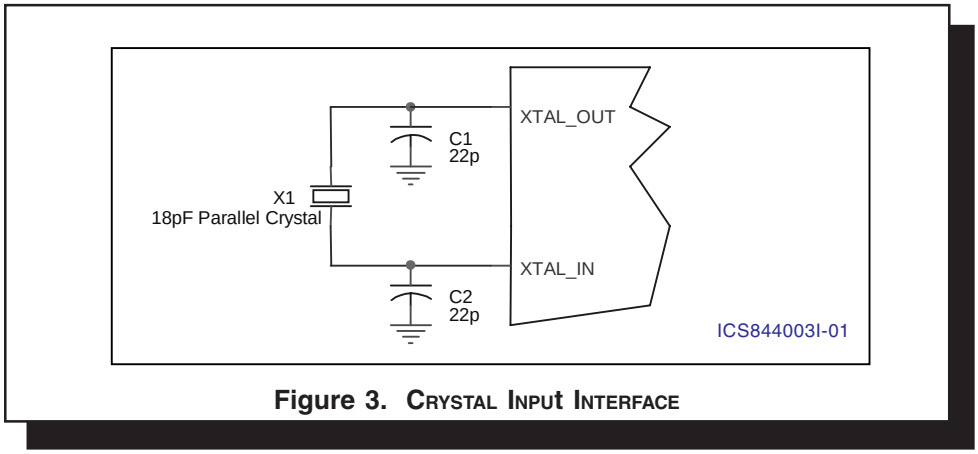


Figure 3. CRYSTAL INPUT INTERFACE

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

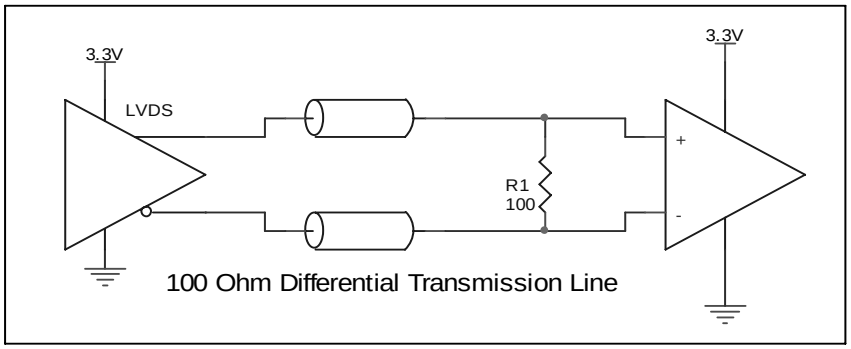


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	70°C/W	65°C/W	62°C/W

TRANSISTOR COUNT

The transistor count for ICS844003I-01 is: 3537

PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

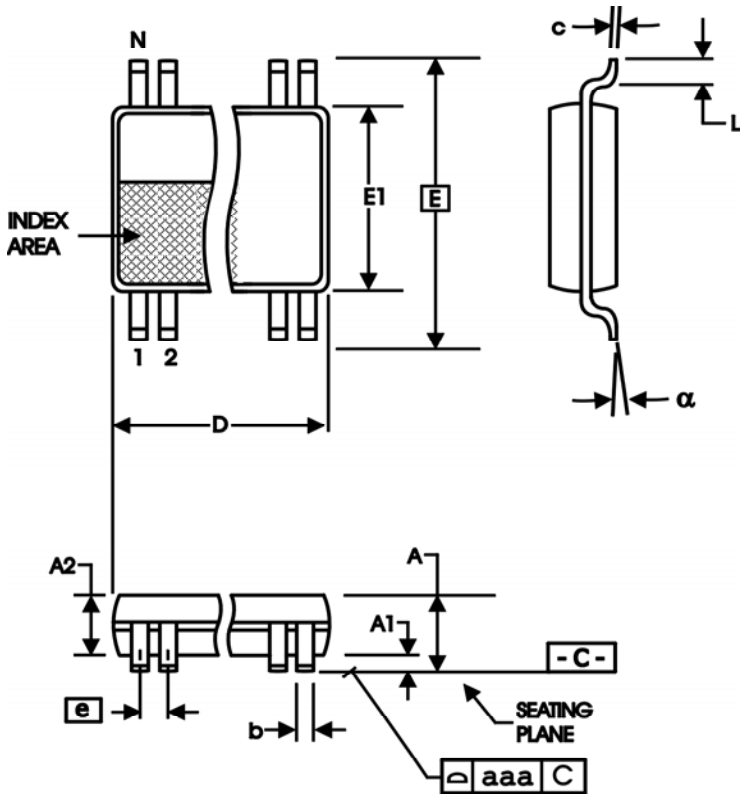


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS844003AGI-01	ICS844003AI01	24 Lead TSSOP	tube	-40°C to 85°C
ICS844003AGI-01T	ICS844003AI01	24 Lead	2500 tape & reel	-40°C to 85°C