PRELIMINARY | Data Sheet | July 2000 | File Number 4903

Multi-Output System Electronics Regulator for Mobile PCs

The IPM6220 provides the power control and protection for five output voltages required in high-performance notebook PC applications. The IC integrates three fixed frequency pulse-width-modulation (PWM) controllers and two linear regulators along with monitoring and protection circuitry into a single 24 lead SSOP package.

The two PWM controllers regulate the system main +5V and +3.3V voltages with synchronous-rectified buck converters. Synchronous rectification and hysteretic operation at light loads contributes to a high efficiency over a wide range of load variation. Efficiency is even further enhanced by using FETs $r_{DS(ON)}$ as a current sense resistor. Feed-forward ramp modulation, current mode control scheme, internal feed-back compensation provide fast and firm transients handling when powering advanced CPUs and chip sets.

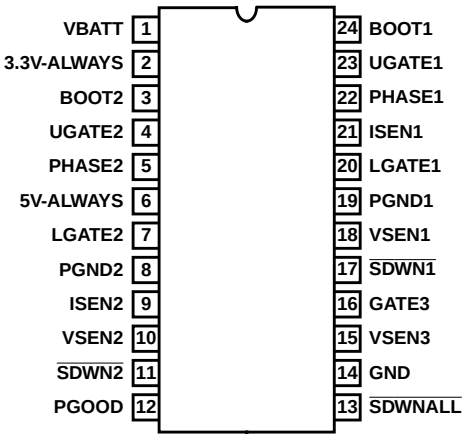
The third PWM controller regulates output voltage of +12V boost converter.

Two linear regulators provide +5-ALWAYS and +3.3-ALWAYS low current outputs required by the notebook system controller.

The IPM6220 monitors all the output voltages. A single Power-Good signal is issued when soft start is completed and all outpovervoltage protection latches the chip off to prevent output voltages from going above 115% of their settings. Undervoltage protection latches the chip off when any of the output drops below 75% of its setting value after soft-start sequence is completed. The PWM controller's over-current circuitry monitor the output currents by sensing the voltage drop across the lower MOSFETs. If precision current-sensing is required, an external current-sense resistors may optionally be used.

Pinout

IPM6220 (SSOP)
TOP VIEW



Features

- Provides Five Regulated Voltages
  - +5V-ALWAYS
  - +3.3V-ALWAYS
  - +5V-MAIN
  - +3.3V-MAIN
  - +12V
- High Efficiency Over Wide Load Range
  - Synchronous Buck Converters on Main Outputs
  - Hysteretic Operation at Light Load
- No Current-Sense Resistor Required
  - Uses MOSFET's $r_{DS(ON)}$
  - Optional Current-Sense Resistor for Precision Overcurrent
- Operates Directly From Battery 5.6V to 24V Input
- Input Undervoltage Lock-Out (UVLO)
- Excellent Dynamic Response
  - Combined Voltage Feed-Forward and Current Mode Control
- Power-Good Output Voltages Monitor
- Out of Phase Clock Generator
- Separate Shutdown Pins for Advanced Configuration Power Interface (ACPI) Compliance
- 300kHz Fixed Switching Frequency
- Thermal Shutdown

Applications

- Mobile PCs
- Hand-Held Portable Instruments

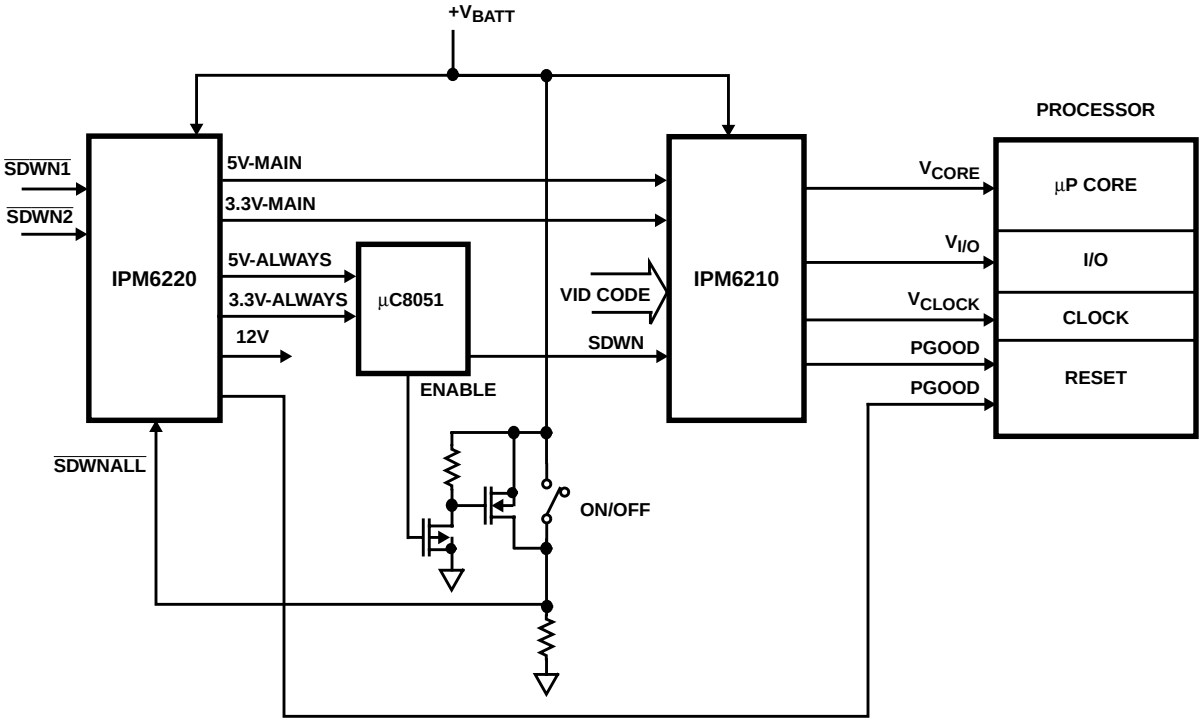
Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

Ordering Information

PART NUMBER	TEMP. (^{o}C)	PACKAGE	PKG. NO.
IPM6220CB	0 to 70	24 Ld SSOP	M24.15-P

Generic Mobile Power System Diagram



Absolute Maximum Ratings

Input Voltage, VBATT . . . . . +30.0V
Phase, Isen and $\overline{SDWNALL}$ Pins . . . . . GND-0.3V to +30.0V
BOOT and UGATE Pins . . . . . +35.0V
IBOOT1,2 with Respect to PHASE1,2 . . . . . +7.0V
$\overline{SDWN1}$, $\overline{SDWN2}$ Pins . . . . . +7.0V
All other pins . . . . . GND -0.3V to 15V
ESD Classification . . . . . Class 2

Recommended Operating Conditions

Input Voltage, VBAT . . . . . +5.6V to +24.0V
Ambient Temperature Range . . . . . 0^oC to 70^oC
Junction Temperature Range . . . . . 0^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SSOP Package	88
SSOP Package (with 3 in^2 of copper)	TBD
Thermal Resistance (Typical, Note 1)	θ_{JC} ($^oC/W$)
SSOP Package	28.5

Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SSOP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY						
VBATT			5.6	14	24	V
Quiescent Current	I_{CC}	LGATE1, LGATE2, UGATE1, UGATE2, GATE3 Open	-	-	1.4	mA
Standby Current	I_{CCSB}		-	-	60	µA
Shutdown Current	I_{CCSN}		-	-	10	µA
INPUT UVLO						
Rising VBATT Threshold			4.4	4.5	4.6	V
Falling VBATT Threshold			3.9	4.0	4.1	V
OSCILLATOR						
PWM1,2 Oscillator Frequency	$F_{c1,2}$		255	300	345	kHz
Ramp Amplitude, Peak to Peak	V_{R1}	Vin=16V	-	2	-	V
Ramp Offset	V_{ROFF}		-	0.5	-	V
Ramp/V_{BAT} Gain	G_{RB}		-	125	-	mV/V
REFERENCE AND SOFT START						
Internal Reference Voltage	V_{REF}		-	2.5	-	V
Reference Voltage Accuracy			-1.0	-	+1.0	%
Soft-Start Current During Startup	I_{SS}		-	5	-	µA
PWM 1 CONVERTER, 5V MAIN						
Output Voltage	V_{OUT1}		4.9	4.97	5.1	V
Load Regulation		100mA < I_{VOUT1} < 5.0A; 5.6V < V_{BATT} < 24.0V	-2.0	-0.6	+2.0	%
Undervoltage Shutdown Level	V_{UV1}	2µs delay	-	-	3.75	V
Overcurrent Comparator Threshold	V_{OC1}		-	-	TBD	V
Overvoltage Shutdown	V_{OVP1}		5.75	-	-	V
Switchover to Hysteretic Operation Threshold	V_{HYST1}		TBD	-	-	V
PWM 2 CONVERTER, 3.3V MAIN						
Output Voltage	V_{OUT2}		3.234	3.29	3.366	V
Load Regulation		100mA < I_{VOUT2} < 5.0A; 5.6V<V_{BATT}< 24.0V	-2.0	-0.3	+2.0	%
Undervoltage Shutdown Level	V_{UV2}	2µs Delay	-	-	2.48	V
Overcurrent Comparator Threshold	V_{OC2}		-	-	TBD	V

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. Refer to Figures 1, 2 and 3 **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Shutdown	V_{OVP2}		3.80	-	-	V
Switchover to Hysteretic Operation	V_{HYST1}		TBD	-	-	V
PWM1, 2 CONTROLLER GATE DRIVERS						
Upper Drive Source Current	I_{2UGON}		-	0.5	-	A
Upper Drive Pullup Resistance	R_{2UGPUP}		-	3	10	Ω
Upper Drive Sink Current	I_{2UGOFF}		-	0.75	-	A
Upper Drive Pulldown Resistance	R_{2UGPDN}		-	2	10	Ω
Lower Gate Source Current	I_{2LGON}		-	0.5	-	A
Lower Drive Pullup Resistance	R_{2LGPUP}		-	3	5	Ω
Lower Gate Sink current	I_{2LGOFF}		-	1	-	A
Lower Drive Pulldown Resistance	R_{2LGPDN}		-	1.5	5	Ω
PWM 3 CONVERTER						
Output Voltage	VOUT3	Determined by external resistor divider	9	12	15	V
Load Regulation		$10mA < I_{VOUT3} < 120mA$	-2.0	-	2.0	%
Undervoltage Shutdown Level	V_{UV3}	2µs delay	-	-	9	V
Overcurrent Shutdown	I_{oc3}	Maximum current which causes undervoltage shutdown	120	-	360	mA
Overvoltage Shutdown	V_{OVP3}		17.5	-	-	V
PWM3 Oscillator Frequency	F_{C3}		85	100	115	kHz
Ramp Amplitude, Peak to Peak	V_{R3}		-	2		-
Maximum Duty Cycle					33	%
PWM 3 CONTROLLER GATE DRIVERS						
Source, Sink Current	I_{3G}		-	0.5	-	A
Pullup, Pulldown Resistance	R_{3G}		-	3	5	Ω
5V-ALWAYS AND 3.3V-ALWAYS						
Linear Regulator Accuracy		$5.6V < V_{BATT} < 24V; 0 < I_{load} < 50mA$	-2.0		+2.0	%
Maximum Output Current			50			mA
Overcurrent Shutdown					100	mA
Undervoltage Shutdown				75		%
Bypass Switch $r_{DS(ON)}$					1	Ω
POWER GOOD AND CONTROL FUNCTIONS						
Power Good Threshold for PWM1 and PWM2			-14	-12	-10	%
V_{PGD1} Threshold Voltage	V_{PG1}		4.3	4.4	4.5	V
V_{PWM2} Threshold Voltage	V_{PG2}		2.8	2.9	3.0	V
PGOOD Leakage Current	I_{PGLKG}	$V_{PULLUP} = 5.0V$	-	-	10	µA
PGOOD Voltage Low	V_{PGOOD}	$I_{PGOOD} = -4mA$	-	-	0.5	V
PGOOD Min Pulse Width	T_{PGmin}		10	-	-	µs
$\overline{SDWN1, 2, ALL}$- Low (OFF)			-	-	0.8	V
$\overline{SDWN1, 2,}$ - High (ON)			2.0	-	-	V
$\overline{SDWNALL}$ - High (ON)			3.0	-	-	V

Block Diagram

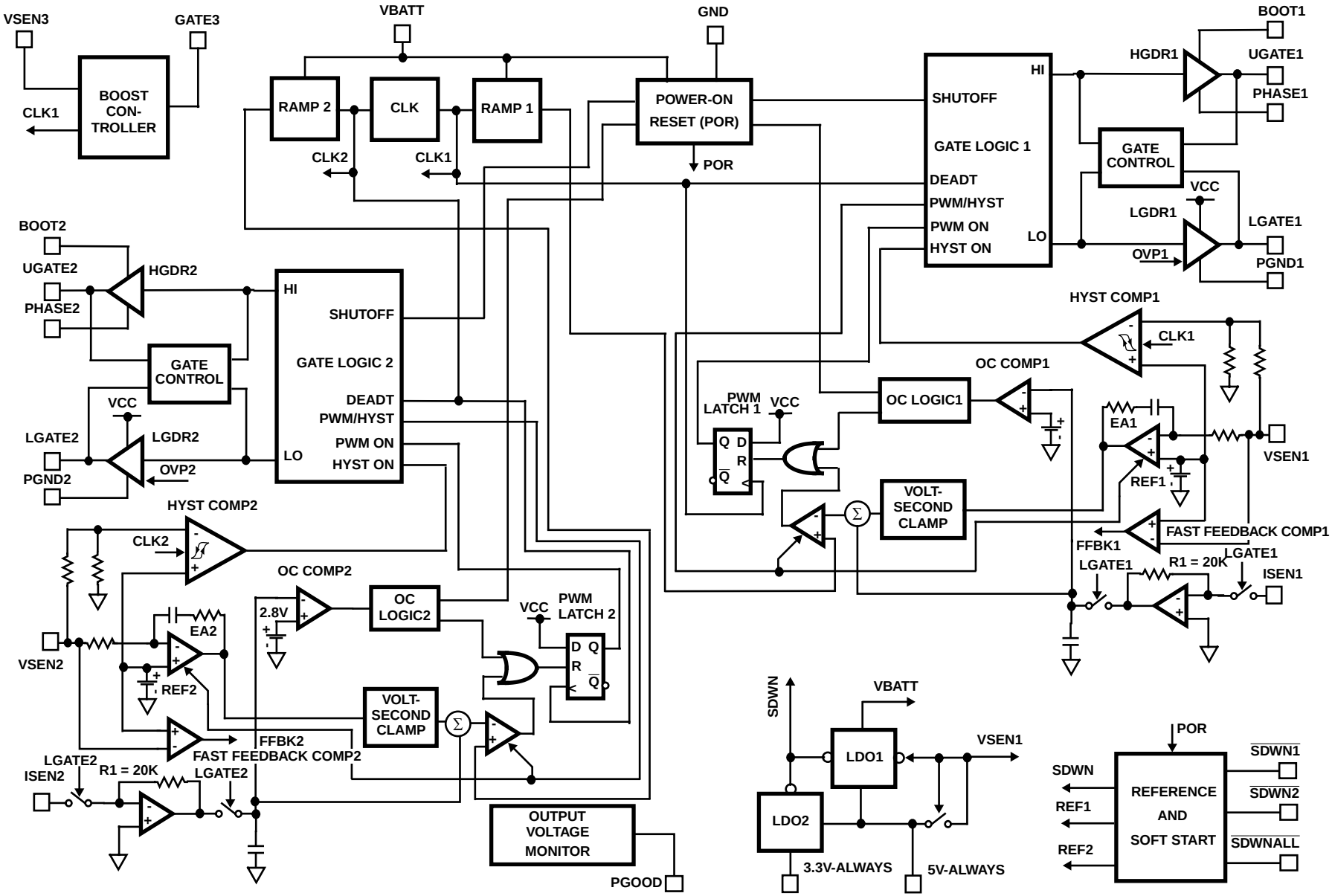


FIGURE 1.

Functional Pin Description

VBATT (Pin 1)

Supplies all the power necessary to operate the chip. IC starts to operate when voltage on this pin exceeds 4.5V and stops to operate when voltage on this pin drops below 4.0V. Also provides battery voltage to the oscillator for feed-forward rejection of the input voltage variation.

3.3V-ALWAYS (Pin 2)

Output of 3.3V-AlWAYS linear regulator.

5V-ALWAYS (Pin 6)

Output of 5V-ALWAYS linear regulator.

BOOT1, BOOT2 (Pins 24 and 3)

Through these pins power is supplied to the upper MOSFET drivers of PWM1 and PWM2 converters. Connect these pins to respective junctions of bootstrap capacitors with the cathodes of the bootstrap diodes. Anodes of the bootstrap diodes are connected to pin 3, 5V-ALWAYS.

UGATE1, UGATE2 (Pins 23 and 4)

These pins provide the gate drive for the upper MOSFETs. Connect UGATE pins to the respective PWM converter's upper MOSFET gate.

PHASE1, PHASE2 (Pins 22 and 5)

The so called PHASE points are the junction points of the upper MOSFET sources, output filter inductors, and lower MOSFET drains. Connect the PHASE pins to the respective PWM converter's upper MOSFET source.

ISEN1, ISEN2 (Pins 21 and 9)

These pins are used to monitor the voltage drop across the lower MOSFETs for current feedback and over-current protection. For precise current detection these inputs could be connected to optional current sense resistors placed in series with sources of the lower MOSFETs. To set the gain of the current sense amplifier, resistor should be placed in series with each of those inputs. Value of the resistor required can be obtained from the following equation:

$$R_{si} = \frac{20k \bullet Iosc \bullet Rcs}{Vth}$$

where: Iosc - desired overload current; Rcs - either $r_{DS(ON)}$ of the lower MOSFET, or the value of the optional current sense resistor; Vth - threshold of the current protection circuitry.

LGATE1, LGATE 2 (Pins 20 and 7)

These pins provide the gate drive for the lower MOSFETs. Connect the lower MOSFET gate of each converter to the corresponding pin.

PGND1, PGND2 (Pins 19 and 8)

These are the power ground connection for PWM1 and PWM2 converters, respectively. Tie each lower MOSFET source to the corresponding pin.

VSEN1, VSEN2 (Pin 18, 10)

These pins are connected to the main outputs and provide voltage feedback signal for respective PWM controllers. The PGOOD and OVP circuits use these signals to report output voltage status and for overvoltage protection.

$\overline{\text{SDWN2}}$ (Pin 11)

This pin provides enable/disable function and soft start for PWM2 controller. Controller is enabled when this pin is pulled high and $\overline{\text{SDWNALL}}$ is high too. Controller is off when the pin is pulled to the ground. To realize the soft-start function, terminate this pin with a capacitor. Soft-start time can be obtained from the following equitation.

$$Tss1 = \frac{3.5V \times Css2}{5\mu A}$$

PGOOD (Pin 12)

PGOOD is an open drain output used to indicate the status of the PWM converters' output voltages. This pin is pulled low when any of the outputs except PWM3 (+12V) is not within ±10% of respective nominal voltages, or when PWM3 (+12V) is not in between its undervoltage and overvoltage thresholds.

$\overline{\text{SDWNALL}}$ (Pin 13)

This pin provides enable/disable function for all outputs. The chip is completely disabled, no output is present when this pin is pulled to the ground. When this pin is pulled high, 5V-ALWAYS and 3.3-ALWAYS outputs are regulated. Status of the other outputs depends on $\overline{\text{SDWN1}}$ and $\overline{\text{SDWN2}}$.

GND (Pin 14)

Signal ground for the IC. All voltage levels are measured with respect to this pin.

VSEN3 (Pin 15)

This pin provides voltage feedback signal for PWM3 controller. The PGOOD and OVP circuits use this pin to report output voltage status and for overvoltage protection. Also, this pin is used to independently disable PWM3 controller when not used. Connect this pin to 5V-ALWAYS if the boost converter is not populated in your design.

GATE3 (Pin 16)

This pins drives the boost MOSFET.

$\overline{\text{SDWN1}}$ (Pin 17)

This pin provides enable/disable function and soft-start for PWM1 controller. Controller is enabled when this pin is pulled high and $\overline{\text{SDWNALL}}$ is high too. Controller is off when the pin is pulled to the ground. To realize the soft-start, terminate this pin with a capacitor. Soft-start time can be obtained from the following equation.

$$Tss1 = \frac{3.5V \times Css1}{5\mu A}$$

Description

Operation

The IIPM6220 addresses system electronics power needs of modern notebook and sub-notebook PCs. The IC integrates control circuits for two synchronous buck converters for +5.0V and +3.3V busses, two linear regulators for 3.3V-ALWAYS and 5V-ALWAYS, and control circuit for +12V boost converter.

The PWM converters use the same clock generator with two out-of-phase outputs. This reduces input current ripple and requirements to the input filter.

The +12V boost controller uses 100kHz clock derived from the main clock. This controller uses front edge PWM scheme with maximum duty factor limited to 33%.

The chip has three input lines $\overline{SDWN1}$, $\overline{SDWN2}$ and $\overline{SDWNALL}$ for advanced control power interface (ACPI) to allow turn on and off all outputs, as well as independently control +3.3V and +5V outputs.

To maximize efficiency, current sense technique based on MOSFET $r_{DS(ON)}$ voltage drop is used. If accurate current protection is desired, current sense resistors can optionally be used. Light load efficiency is enhanced by a hysteretic mode of operation which is automatically engaged when inductor current becomes discontinuous.

3.3V and 5V Architecture

Main outputs are generated from the unregulated DC source by two independent synchronous buck converters. IC integrates all the components required for output adjustment and feedback compensation significantly reducing the number of external parts.

These buck PWM controllers are identical and employ fixed frequency current mode control scheme with addition of feed-forward ramp programming for better rejection of the input voltage variation. They use out-off-phase sequences from the same unadjusted frequency clock oscillator to reduce input current ripple.

Current Sensing and Overcurrent Protection

Both PWM converters employ the lower MOSFET on-state resistance, $r_{DS(ON)}$ as a current sensing element. This technique eliminates need in a current sense resistor and power losses usually associated with it.

The sensed voltage drop is used for the current feedback and the overcurrent protection. The $r_{DS(ON)}$ voltage drop is sampled after about 200ns after the lower MOSFET is turned on.

The sampled voltage after amplification is compared with internally set overcurrent threshold. To accommodate wide range of the $r_{DS(ON)}$ variation, the value of the overcurrent threshold should represent overload current about 180% of the nominal value. This could lead to the situation where the converter continuously delivers power about two times the nominal without significant drop in the output voltage.

To eliminate this, the time delay circuit (8:1 counter which counts the clock cycles) is activated when the overcurrent condition is detected for the first time. This limits the inductor current buildup and essentially switches the converter into current regulation mode for a short period of time (eight clock cycles). If after the delay the overcurrent condition is still present, the converter shuts down. If not - the normal operation restores.

This overcurrent scheme has been proven to be very robust in applications like portable computers where fast inductor current buildup is common due to a big difference between input and output voltages and a low value of the inductor.

Operation Mode Control

The mode control circuit changes the converter's mode of operation depending on the level of the load current. At nominal current converter operates in fixed frequency PWM mode. When the load current drops lower than the critical value, inductor current becomes discontinuous and the operation mode is changed to hysteretic.

The mode control circuit consists of a flip-flop which outputs provide HYST and NORMAL signals. These signals inhibit normal PWM operation and activate hysteretic comparator and diode emulation mode of the synchronous FET.

The inputs of the flip-flop are controlled by outputs of two delay circuits, which constantly monitor output of the phase node comparator. High level on the comparator output during $\overline{PWM}$ cycle is associated with continuous mode of operation. The low level - corresponds to the discontinuous mode of operation. When the low level on the comparator output is detected eight times in a row, the mode control flip-flop is set and converter is commanded to operate in the hysteretic mode. If during this pulse counting process the comparator's output happens to be high, the counter of the delay circuit will be reset and circuit will continue to monitor for eight low level pulses in a row from the very beginning.

TABLE 1. POWER CONTROL

SDWNALL	SDWN1	SDWN2	3V AND 5V ALWAYS	3V MAIN	5V MAIN
0	X	X	0	0	0
1	0	0	1	0	0
1	1	0	1	0	1
1	0	1	1	1	0
1	1	1	1	1	1

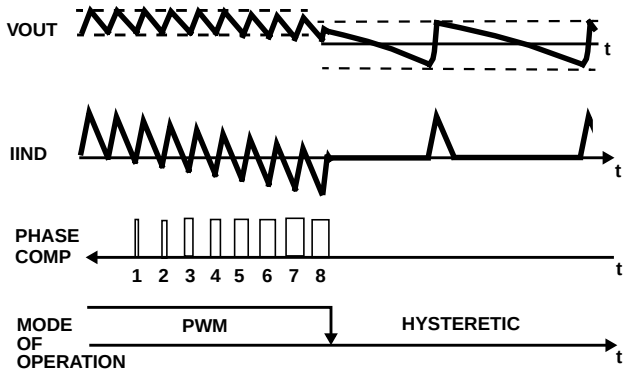


FIGURE 2.

The circuit which restores normal PWM operation mode works in the same way and is looking for eight in a row high level pulses on the comparator's output. If during this counting process the comparator's output happens to be low, the counter will be reset and the mode control flip-flop will not change the state. The operation mode will only be changed when eight pulses in a row fill the counter. This technique prevents jitter and chatter of the operation mode at the load levels close to the critical.

Light Load (Hysteretic) Operation

In the light load (hysteretic) mode the output voltage is regulated by the hysteretic comparator which forces the upper gate driver high when the output voltage drops lower the certain level. When the output voltage rises above the set point the upper gate driver is inhibited.

Voltage on the non-inverting input of the hysteretic comparator is a reference voltage with a small addition of the clock frequency pulses. Such a scheme allows to synchronize the upper MOSFET turn-on with the main clock and contributes positively to the seamless transition between the operation modes.

3.3V and 5V Soft Start, Sequencing and Standby

The 5V and 3.3V converters are enabled if $\overline{SDWN1}$ and $\overline{SDWN2}$ are high (open) and $\overline{SDWNALL}$ is also high. The standby mode is defined as a condition when $\overline{SDWN1}$ and $\overline{SDWN2}$ are low and PWM converters are disabled but $\overline{SDWNALL}$ is high (3.3V-ALWAYS and 5V-ALWAYS outputs are enabled).

Soft start of the 3.3V and 5V converters is accomplished by means of the capacitors connected from pins $\overline{SDWN1}$ and $\overline{SDWN2}$ to the ground. In conjunction with pull up to +VCC 5µA current sources they provide controlled rise of the voltage on these pins. The output voltage of the converter should reach the regulation before the voltage on the soft start capacitor reaches the threshold of 3.5V. The value of the soft start capacitors can be calculated from the following expression.

$$Css = \frac{5\mu A \times t_{SS}}{3.5V}$$

Where: t_{SS} - is a desired soft start time, and 3.5V is a voltage on the soft start capacitor when undervoltage protection is enabled.

By varying the values of soft start capacitors it is possible to provide sequencing of the main outputs at startup.

Gate Control Logic

The gate control logic translates generated PWM control signals into the MOSFET gate drive signals providing necessary amplification, level shift and shoot-trough protection. Also, it bears some functions that help optimize the IC performance over a wide range of the operational conditions. As MOSFET switching time can very dramatically from type to type and with the input voltage, gate control logic provides adaptive dead time by monitoring gate voltages of both upper and lower MOSFETs.

12V Converter Architecture

The 12V boost converter generates its output voltage from the main 5V output. An external inductor, a diode and a capacitor are required to complete the circuit. The output signal is fed back to the controller via an external resistive divider. The divider allows to adjust the output voltage as necessary. For example, to accommodate the linear regulator if higher level of regulation is required. The boost controller can be disabled in the systems where there is no need for 12V power by connecting VSEN3 pin to 5V-ALWAYS rail.

The control circuit for the 12V converter consists of a 3:1 frequency divider which drives a ramp generator and resets a PWM latch (Figure 2). The length of the CLK/3 pulses is equal to the period of the main clock. Thus, duty factor of the pulse sequence after the divider is limited to 1/3. An output of a non-inverting error amplifier is compared with the rising ramp voltage. When the ramp voltage becomes higher than the error signal, the PWM comparator sets the latch and the output of the gate driver is pulled high. The rising edge of the $\overline{CLK/3}$ pulses resets the latch and pulls the output of the gate driver low. Operation of the circuit repeats after two idle periods of the main clock.

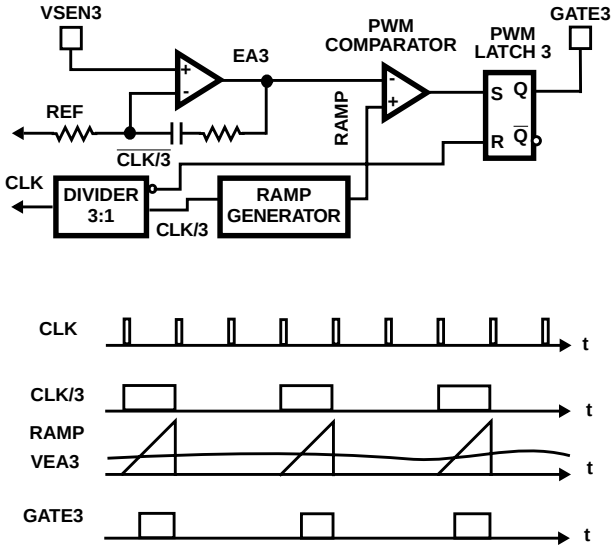


FIGURE 3.

The fact that the maximum duty factor of the converter is limited to 1/3 allows for guaranteed discontinuous inductor current operation over the all operation conditions. The inductor should be kept lower some critical value.

$$Lmax = \frac{Vinmin^2 \times Dmax^2 \times Ro}{2 \times Vo^2 \times F}$$

where, Vinmin -- minimum input voltage; Dmax=1/3 -- maximum duty factor; Ro -- nominal load resistance; Vo -- nominal output voltage; F -- the switching frequency.

The boost converter with the limited duty factor in the discontinuous inductor current mode can deliver to the load and correspondingly draw from the source only certain amount of energy. The output voltage starts to drop when the maximum duty factor is reached.

$$Vo = Vin \times Dmax \times \sqrt{\frac{Ro}{2 \times L \times F}}$$

Thus, providing automatic output overcurrent limiting. If the value of the inductor is chosen properly, the output current twice as high as a nominal will pull the output voltage down to the point were the undervoltage protection comes into effect.

The 12V converter starts to operate at the same time as the 5V converter. The softly rising voltage on the 5V output accompanied with limited to 33% maximum duty factor provides softly rising 12V output. The total capacitance on the 12V output should be chosen appropriately, so that the output voltage can buildup higher than the undervoltage limit (9V) during the soft start time in order to avoid triggering of the undervoltage protection.

Over Temperature Protection

The chip incorporates an over temperature protection circuit that shuts all the outputs down when the die temperature of 150^oC is reached. Normal operation restores at the die temperatures below 125^oC trough the full soft-start by cycling the input voltage.

3V-ALWAYS, 5V-ALWAYS Linear Regulators

The 3.3V-ALWAYS and 5V-ALWAYS outputs are derived from the battery voltage and are the first voltages available in the notebook when the power button is pushed down (Figure 2). The 5V-ALWAYS output is generated directly from the battery voltage by a linear regulator and is used to power the chip itself, the CPU regulator and their gate drivers. The 3.3V-ALWAYS output is used to power the keyboard controller and is generated from the 5V-ALWAYS output. The total current capability of these outputs is 50mA. When the system 5V rail is enabled and regulated, the 5V-ALWAYS output is connected to it via an internal 1Ω switch. Simultaneously, the 5V-AWAYS linear regulator is disabled to protect the chip from the excessive power dissipation.

IPM6220 DC-DC Converter Application Circuit

Figure 4 shows an application circuit of a power supply for a notebook PC microprocessor system. The power supply provides +5V_ALWAYS, +3.3V_ALWAYS, +5.0V, +3.3V, and +12.0V from +5.6-24V_{DC} battery voltage. For detailed information on the circuit, including a Bill-of-Materials and circuit board description, see Application Note ANXXXX. Also see Intersil's web site (www.intersil.com) or Intersil AnswerFAX (321-724-7800) for the latest information.

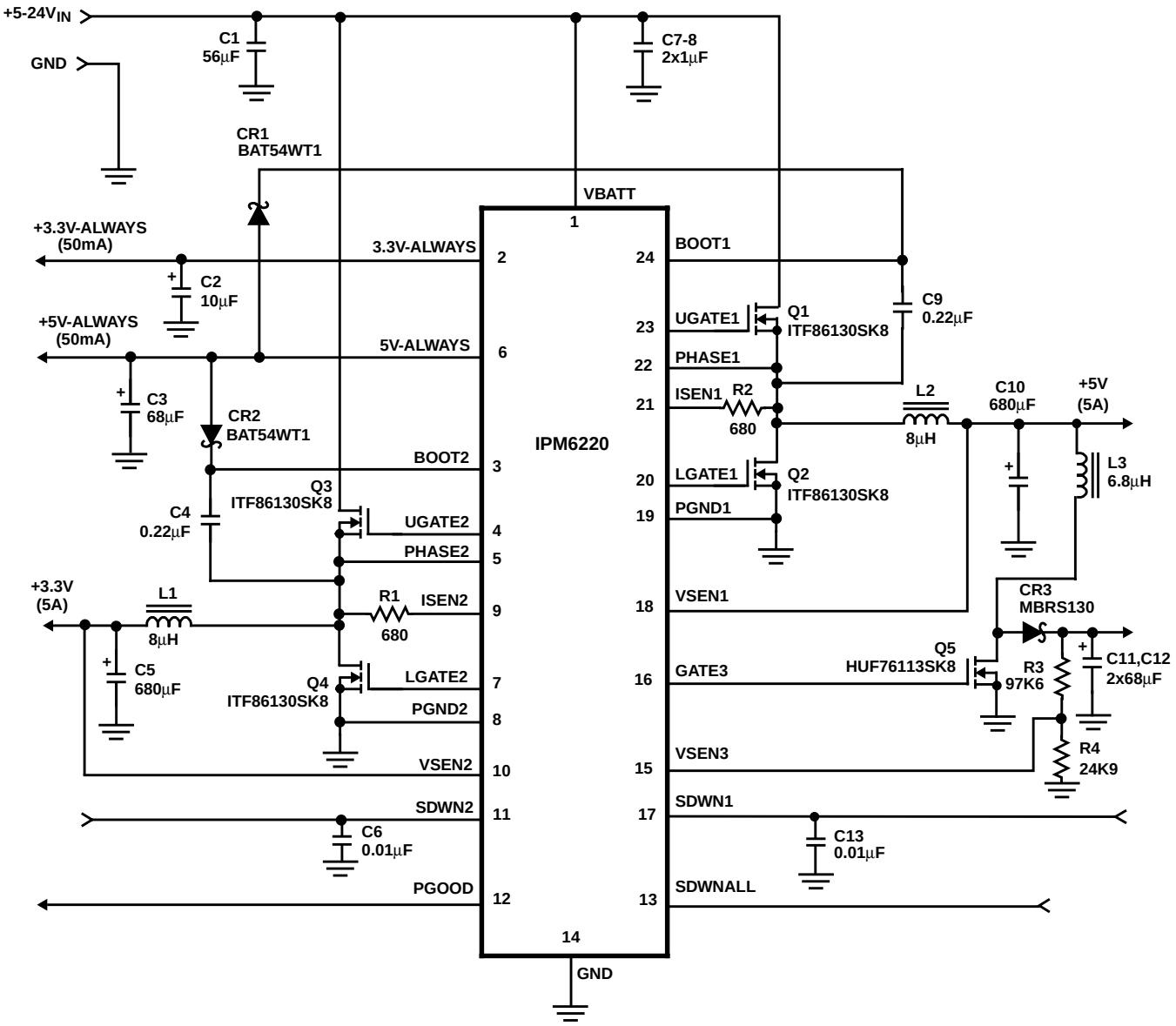
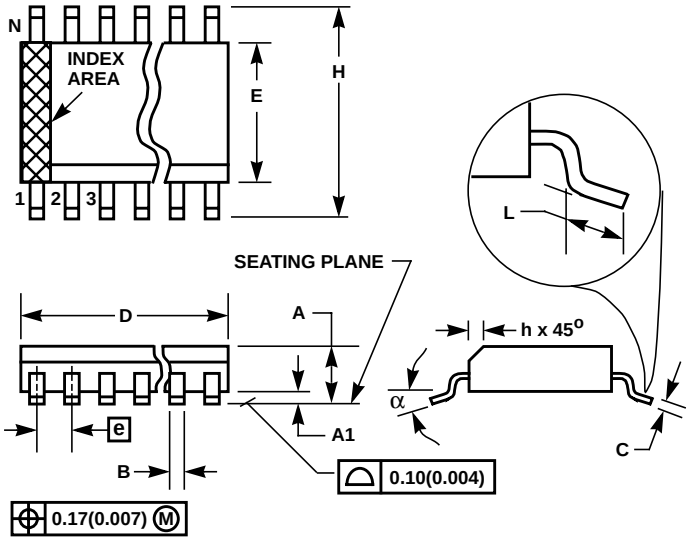


FIGURE 4. APPLICATION CIRCUIT

Shrink Small Outline Plastic Packages (SSOP/QSOP)



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24 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.007	0.011	0.178	0.279	-
B	0.008	0.012	0.203	0.305	-
C	0.007	0.010	0.178	0.254	-
D	0.337	0.344	8.56	8.74	1
E	0.149	0.157	3.78	3.99	2
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.79	6.20	-
h	0.015		0.38		-
L	0.016	0.050	0.41	1.27	3
N	24		24		4
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs.
2. Dimension “E” does not include interlead flash or protrusions.
3. “L” is the length of terminal for soldering to a substrate.
4. “N” is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

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