INTEGRATED CIRCUITS

DATA SHEET

74LVT32374

3.3 V 32-bit edge-triggered D-type flip-flop; 3-state

Product specification

2002 Mar 20

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FEATURES

- 32-bit edge-triggered flip-flop
- 3-state buffers
- Output capability: +64 mA/–32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA in accordance with JEDEC std 17
- ESD protection exceeds 2000 V in accordance with MIL STD 883 method 3015 and 200 V in accordance with Machine Model.

DESCRIPTION

The 74LVT32374 is a high-performance BICMOS product designed for V_{CC} operation at 3.3 V.

The 74LVT32374 is a 32-bit edge-triggered D-type flip-flop featuring non-inverting 3-state outputs. The device can be used as four 8-bit flip-flops, or two 16-bit flip-flops or one 32-bit flip-flop. On the positive transition of the clock (CP), the Q outputs of the flip-flop take on the logic levels set-up at the D inputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f \leq 2.5$ ns.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay nCP to nQ_n	C_L = 50 pF; V_{CC} = 3.3 V	2.9	ns
C_I	input capacitance	V_I = 0 or 3.0 V	3	pF
C_O	output capacitance	outputs disabled; V_O = 0 or 3.0 V	9	pF
I_{CCZ}	total supply current	output disabled; V_{CC} = 3.6 V	140	μA

FUNCTION TABLE

See note 1.

OPERATING MODE	INPUTS			INTERNAL REGISTER	OUTPUTS
	nOE	nCP	nDn		nQn
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Hold	L	not ↑	X	NC	NC
Disable outputs	H	not ↑	X	NC	Z
	H	↑	nDn	nDn	Z

Note

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW OE transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW OE transition;
   NC = not connected;
   X = don't care;
   Z = high-impedance OFF-state;
   ↑ = LOW-to-HIGH CP transition;
   not ↑ = not a LOW-to-HIGH CP transition.

ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE RANGE	PACKAGE			
		PINS	PACKAGE	MATERIAL	CODE
74LVT32374EC	–40 to +125 °C	96	LFBGA96	plastic	SOT536-1

PINNING

SYMBOL	DESCRIPTION
nDn	data input
nCP	clock input
nQn	flip-flop output
GND	ground (0 V)
nOE	output enable input (active LOW)
V_{CC}	supply voltage

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	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	$1D_1$	$1D_3$	$1D_5$	$1D_7$	$2D_1$	$2D_3$	$2D_5$	$2D_7$	$3D_1$	$3D_3$	$3D_5$	$3D_7$	$4D_1$	$4D_3$	$4D_5$	$4D_6$
5	$1D_0$	$1D_2$	$1D_4$	$1D_6$	$2D_0$	$2D_2$	$2D_4$	$2D_6$	$3D_0$	$3D_2$	$3D_4$	$3D_6$	$4D_0$	$4D_2$	$4D_4$	$4D_7$
4	1CP	GND	V_{CC}	GND	GND	V_{CC}	GND	2CP	3CP	GND	V_{CC}	GND	GND	V_{CC}	GND	4CP
3	$1\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$2\overline{OE}$	$3\overline{OE}$	GND	V_{CC}	GND	GND	V_{CC}	GND	$4\overline{OE}$
2	$1Q_0$	$1Q_2$	$1Q_4$	$1Q_6$	$2Q_0$	$2Q_2$	$2Q_4$	$2Q_6$	$3Q_0$	$3Q_2$	$3Q_4$	$3Q_6$	$4Q_0$	$4Q_2$	$4Q_4$	$4Q_7$
1	$1Q_1$	$1Q_3$	$1Q_5$	$1Q_7$	$2Q_1$	$2Q_3$	$2Q_5$	$2Q_7$	$3Q_1$	$3Q_3$	$3Q_5$	$3Q_7$	$4Q_1$	$4Q_3$	$4Q_5$	$4Q_6$

Fig.1 Pin configuration.

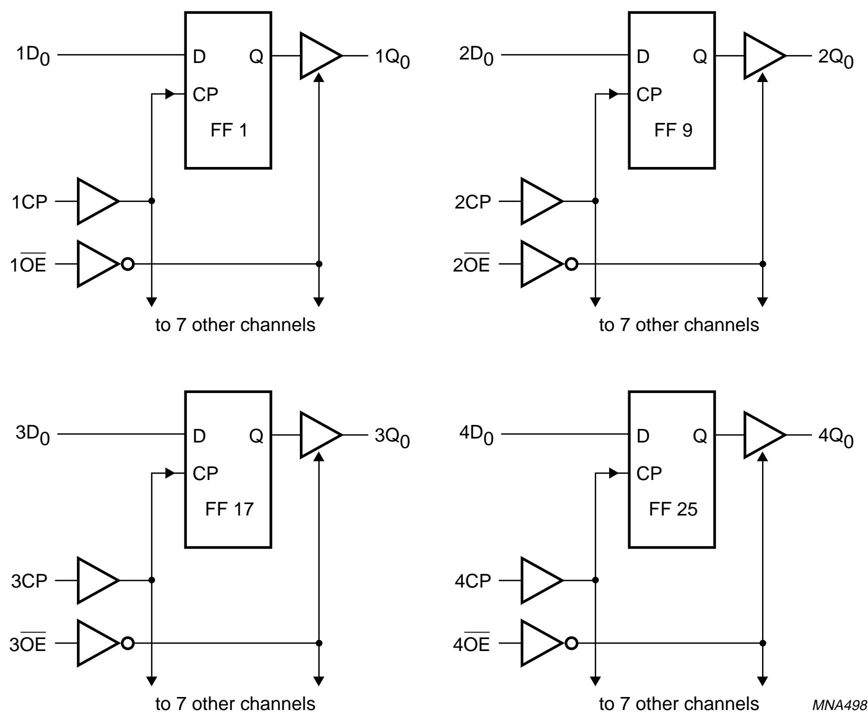


Fig.2 Logic symbol.

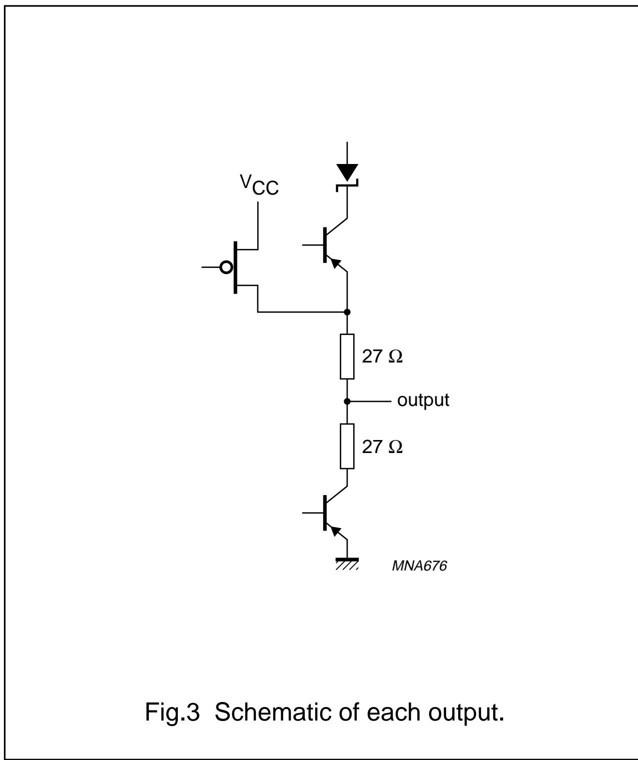


Fig.3 Schematic of each output.

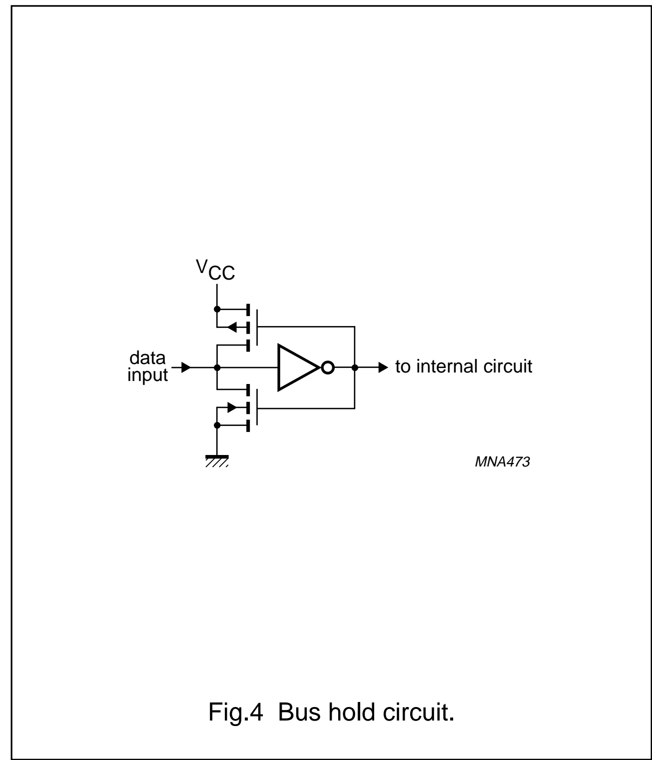


Fig.4 Bus hold circuit.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–2.7	+3.6	V
V_I	input voltage	note 1	0	5.5	V
V_{IH}	HIGH-level input voltage		2.0	–	V
V_{IL}	LOW-level input voltage		–	0.8	V
I_{OH}	HIGH-level output current		–	–32	mA
I_{OL}	LOW-level output current		–	32	mA
		current duty cycle ≤ 50%; f ≥ 1 kHz	–	64	mA
Δt/ΔV	input transition rise or fall times	outputs enabled	–	10	ns/V
T_{amb}	operating ambient temperature		–40	+125	°C
P_D	power dissipation per package	note 2	–	–	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 70 °C the value of P_D derates linearly with 1.8 mW/K.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	–	+4.6	V
I_{IK}	input diode current	$V_I < 0$	–	–50	–	mA
V_I	input voltage	note 2	–0.5	–	+7.0	V
I_{OK}	output diode current		–	–50	–	mA
V_O	output voltage	output in OFF or HIGH state; note 2	–0.5	–	+7.0	V
I_O	output current	output in LOW state	–	128	–	mA
		output in HIGH state	–	–64	–	mA
T_{stg}	storage temperature		–65	–	+150	°C

Notes

1. The performance capability of a high-performance integrated circuit in conjuction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.
2. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		T_{amb} (°C)			UNIT
		OTHER	V_{CC} (V)	–40 to +85			
				MIN.	TYP.[1]	MAX.	
V_{IK}	input clamp voltage	I_{IK} = –18 mA	2.7	–	–0.85	–1.2	V
V_{OH}	HIGH-level output voltage	I_{OH} = –32 mA	3.0	2.0	2.3	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 64 mA	3.0	–	0.4	0.55	V
V_{RST}	power-up output LOW voltage	I_O = –1 mA; V_I = GND or V_{CC}; note 2	3.6	–	0.1	0.55	V
I_I	input leakage current	V_I = V_{CC} or GND; control pins	3.6	–	0.1	±1	μA
		V_I = 5.5 V	0 or 3.6	–	0.4	10	μA
		V_I = V_{CC}; data pins; note 3	3.6	–	0.1	1	μA
		V_I = 0 V; data pins; note 3	3.6	–	–0.4	–5	μA
I_{off}	output OFF current	V_I or V_O = 0 to 4.5 V	0	–	0.1	±100	μA
I_{hold}	bus hold current D inputs	V_I = 0.8 V; note 4	3.0	75	135	–	μA
		V_I = 2.0 V; note 4	3.0	–75	–135	–	μA
		V_{CC} = 3.6 V; note 4	0 to 3.6	±500	–	–	μA
I_{EX}	current into an output in the HIGH state when $V_O > V_{CC}$	V_O = 5.5 V	3.0	–	50	125	μA
$I_{pu/pd}$	power-up/down 3-state output current	V_O = 5.5 V to V_{CC}; V_I = GND or V_{CC}; V_{OE} = don't care; note 5	≤ 1.2 V	–	1	±100	μA
I_{OZH}	3-state output HIGH current	V_O = 3.0 V; V_I = V_{IH} or V_{IL}	3.6	–	0.5	5	μA
I_{OZL}	3-state output LOW current	V_O = 0.5 V; V_I = V_{IH} or V_{IL}	3.6	–	+0.5	–5	μA
I_{CCH}	quiescent supply current	outputs HIGH; I_O = 0; V_I = GND or V_{CC}	3.6	–	0.14	0.24	mA
I_{CCL}	quiescent supply current	outputs LOW; I_O = 0; V_I = GND or V_{CC}	3.6	–	8	12	mA
I_{CCZ}	quiescent supply current	outputs disabled; I_O = 0; V_I = GND or V_{CC}; note 6	3.6	–	0.14	0.24	mA
ΔI_{CC}	additional supply current per input pin	one input at V_{CC} – 0.6 V; other inputs at GND or V_{CC}; note 7	3.0 to 3.6	–	0.1	0.2	μA

Notes

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
3. Unused pins at V_{CC} or GND.
4. This is the bus hold overdrive current required to force the input to the opposite logic state.
5. This parameter is valid for any V_{CC} between 0 and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 ±0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
6. I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
7. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$.

SYMBOL	PARAMETER	WAVEFORMS	$V_{CC} = 3.3 \pm 0.3$ V			$V_{CC} = 2.7$ V	UNIT
			MIN.	TYP.[1]	MAX.	MAX.	
t_{PLH}/t_{PHL}	propagation delay nCP to nQ_n	see Fig.5	1.5	3.0	5.3	6.2	ns
			1.5	3.0	4.9	5.1	ns
t_{PZH}/t_{PZL}	output enable time to HIGH and LOW level	see Figs 7 and 8	1.5	3.5	5.6	6.9	ns
			1.5	3.2	4.9	6.0	ns
t_{PHZ}/t_{PLZ}	output disable time from HIGH and LOW level	see Figs 7 and 8	1.5	3.5	5.4	5.7	ns
			1.5	3.2	5.0	5.1	ns
f_{max}	maximum clock pulse frequency	see Fig.5	150	–	–	–	MHz

Note

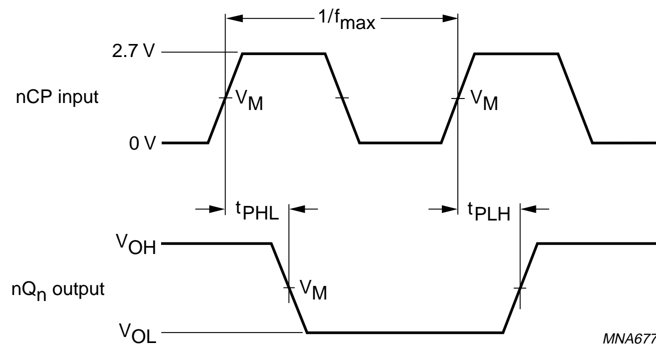
1. All typical values are measured at $V_{CC} = 3.3$ V and $T_{amb} = 25$ °C.

AC SETUP REQUIREMENTS

GND = 0 V; $t_r = t_f = 2.5$ ns; $C_L = 50$ pF; $R_L = 500\ \Omega$; $T_{amb} = -40$ to $+125$ °C.

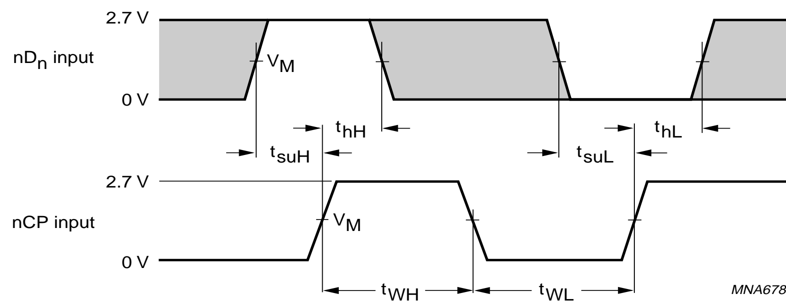
SYMBOL	PARAMETER	WAVEFORMS	$V_{CC} = 3.3 \pm 0.3$ V		$V_{CC} = 2.7$ V	UNIT
			MIN.	TYP.[1]	MIN.	
t_{suH}	set-up time nD_n HIGH to nCP	see Fig.6	2.5	0.7	2.5	ns
t_{suL}	set-up time nD_n LOW to nCP	see Fig.6	2.5	0.7	2.5	ns
t_{hH}	hold time nD_n HIGH to nCP	see Fig.6	0.5	0	0	ns
t_{hL}	hold time nD_n LOW to nCP	see Fig.6	0.5	0	0	ns
t_{WH}	nCP HIGH pulse width	see Fig.6	1.5	0.6	1.5	ns
t_{WL}	nCP LOW pulse width	see Fig.6	3.0	1.6	3.0	ns

AC WAVEFORMS



V_M = 1.5 V;
V_M = GND to 3.0 V.

Fig.5 Clock (nCP) to output (nQ_n) propagation delays, the clock pulse width and the maximum clock pulse frequency.



The shades areas indicate when the input is permitted to change for predicable output performance.

Fig.6 Set-up and hold times for inputs (nD_n) to inputs (nCP).

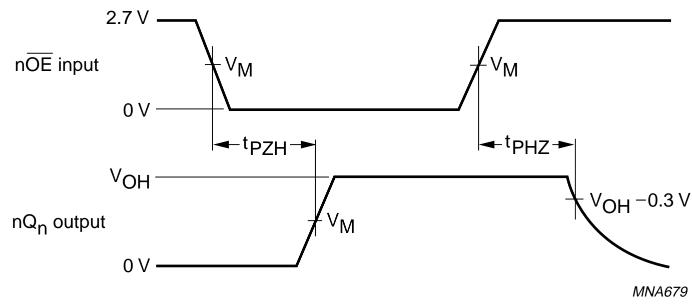


Fig.7 3-state output enable time to HIGH level and output disable time from HIGH level.

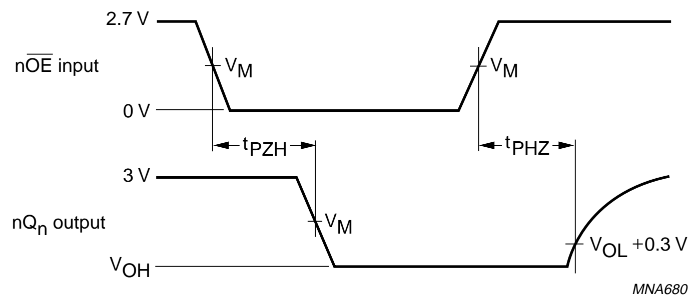
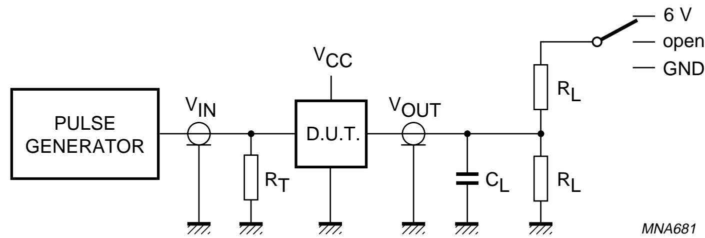


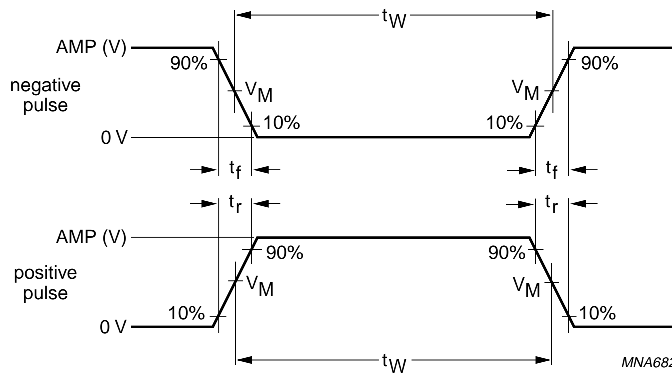
Fig.8 3-state output enable time to LOW level and output disable time from LOW level.



TEST	S_1
t_{PLH}/t_{PHL}	open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

Definitions for test circuit:
R_L = Load resistor.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig.9 Load circuitry for switching times.

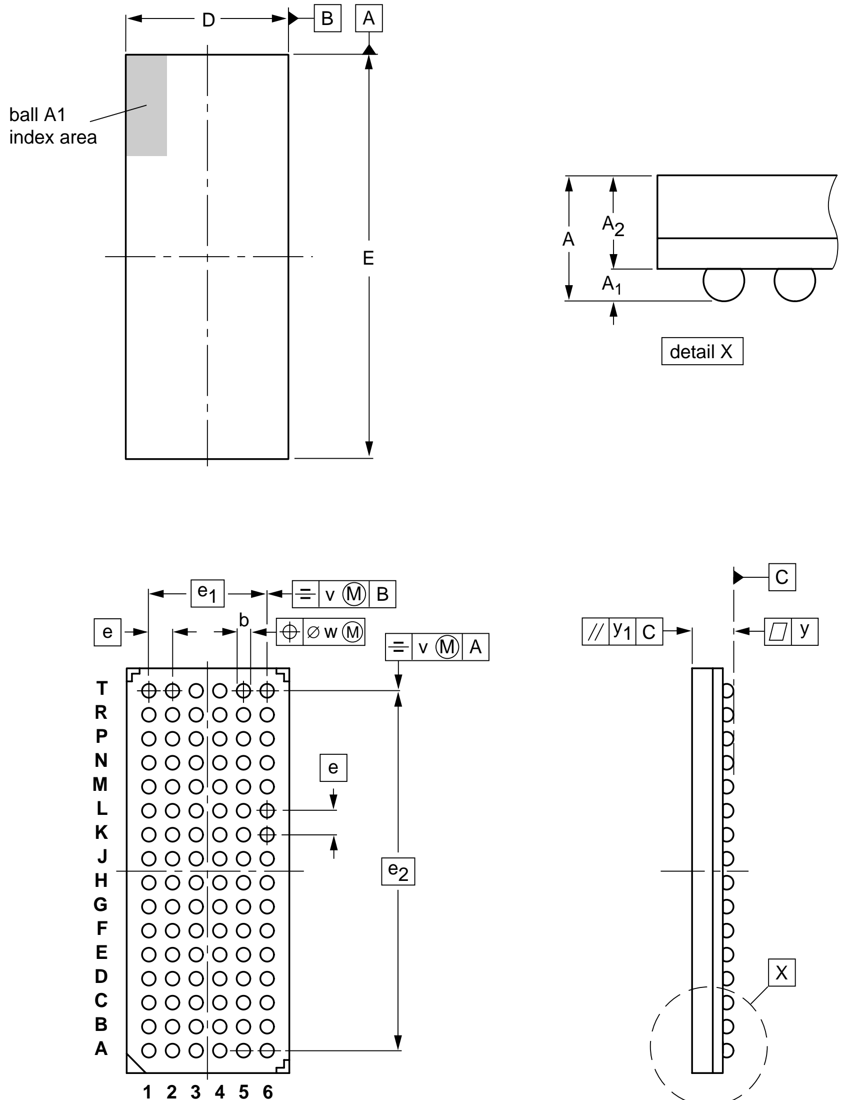


FAMILY	INPUT PULSE REQUIREMENTS				
	AMPLITUDE	PULSE RATE	t_W	t_r	t_f
74LVT32xxx	2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	≤ 2.5 ns

Fig.10 Input pulse definition.

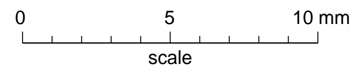
PACKAGE OUTLINE

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.5	0.41 0.31	1.2 0.9	0.51 0.41	5.6 5.4	13.6 13.4	0.8	4.0	12.0	0.15	0.1	0.1	0.2



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT536-1						~~99-12-02~~ 00-03-04

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[(1)]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[(2)]	suitable
PLCC[(3)], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[(3)(4)]	suitable
SSOP, TSSOP, VSO	not recommended[(5)]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS[1]	PRODUCT STATUS[2]	DEFINITIONS
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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