OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM6222B-xx

DOT MATRIX LCD CONTROLLER WITH 16-DOT COMMON DRIVER AND 40-DOT SEGMENT DRIVER

GENERAL DESCRIPTION

The MSM6222B-xx is a dot matrix LCD controller which is fabricated in low power CMOS silicon gate technology. Character display on the dot matrix character type LCD can be controlled in combination with a 4-bit/8-bit microcontroller. This LSI consists of 16-dot COMMON driver, 40-dot SEGMENT driver, display data RAM, character generator RAM, character generator ROM and control circuit.

The MSM6222B-xx is the equivalent of Hitachi's HD44780. There is, however, a slight difference between the two devices as described in the table on the last page.

The MSM6222B-xx has the character generator ROM that can be programmed by custom mask. MSM6222B-01 is a standard version having 160 characters with lowercase (5 x 7 dots), and 32 characters with uppercase (5 x 10 dots) in this ROM.

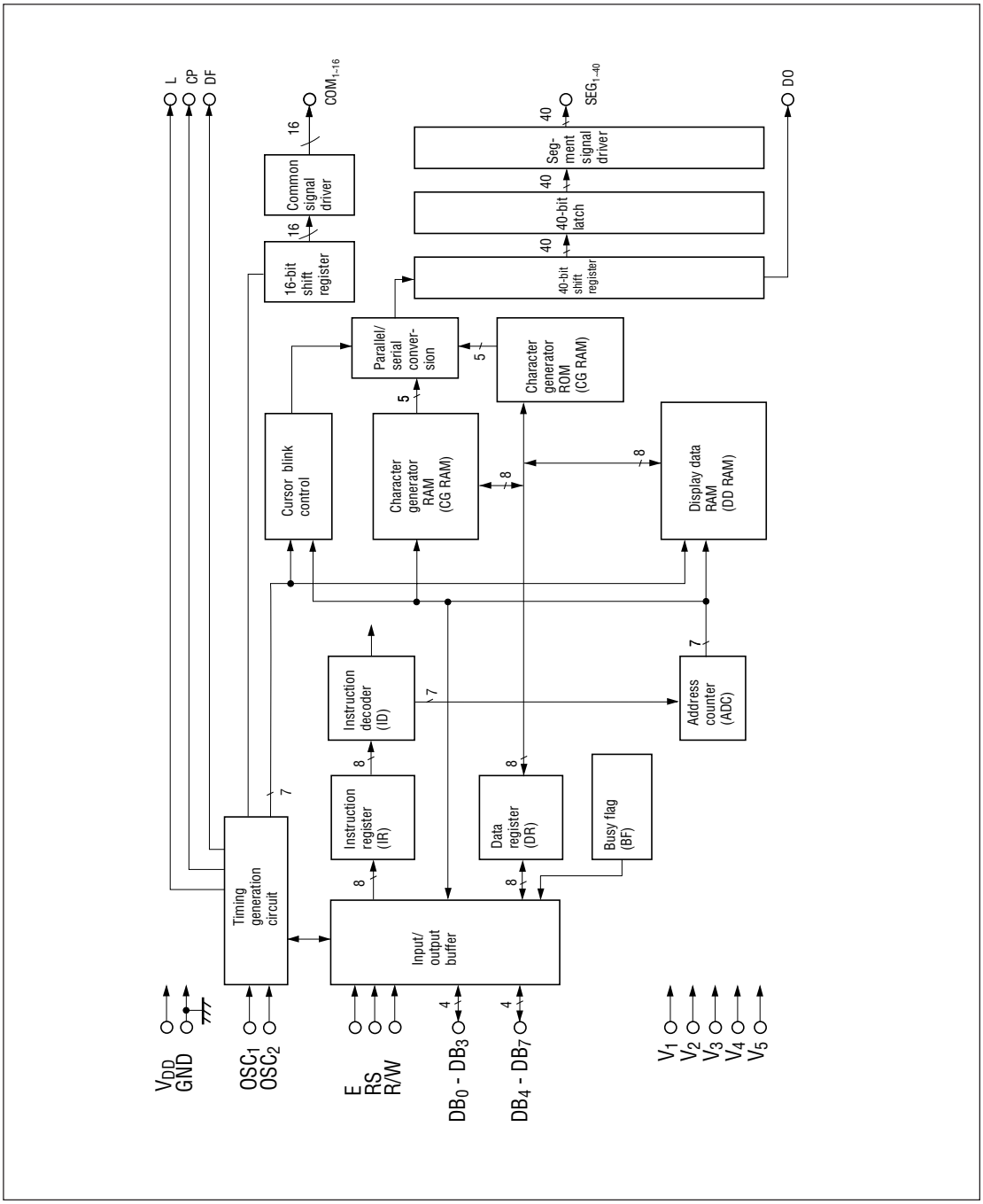
FEATURES

- Easy interface with an 8-bit or 4-bit microcontroller.
- Dot matrix LCD controller/driver for lowercase (5 x 7 dots) or uppercase (5 x 10 dots).
- Automatic power ON reset.
- COMMON signal drivers (16) and SEGMENT signal drivers (40).
- Can control up to 80 characters when used in combination with MSM5259.
- Character generator ROM for 160 characters with lowercase (5 x 7 dots) and 32 characters with uppercase (5 x 10 dots).
- Character patterns are programmable by character generator RAM. (Lowercase: 5 x 8 dots, 8 kinds, uppercase: 5 x 11 dots, 4 kinds).
- Oscillation circuit for external resistor or ceralock.
- 1/8 duty (1 line; 5 x 7 dots + cursor), 1/11 duty (1 line; 5 x 10 dots + cursor), or 1/16 duty (2 lines; 5 x 7 dots + cursor), selectable.
- Clear display even at 1/5 bias, 3.0V LCD driving voltage.
- Package options:

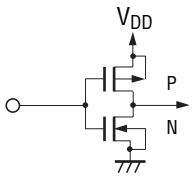
  80-pin plastic QFP (QFP80-P-1420-0.80-L) (Product name: MSM6222B-xxGS-L)
  80-pin plastic QFP (QFP80-P-1420-0.80-BL) (Product name: MSM6222B-xxGS-BL)

  xx indicates code number.

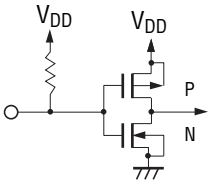
BLOCK DIAGRAM



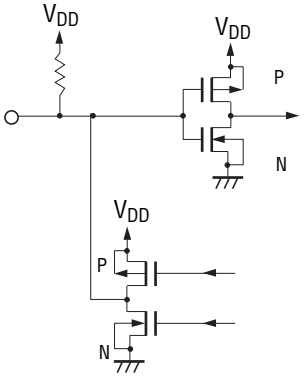
INPUT AND OUTPUT CONFIGURATION



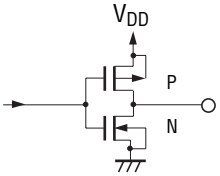
Applicable to pin E.



Applicable to pins R/W and RS.

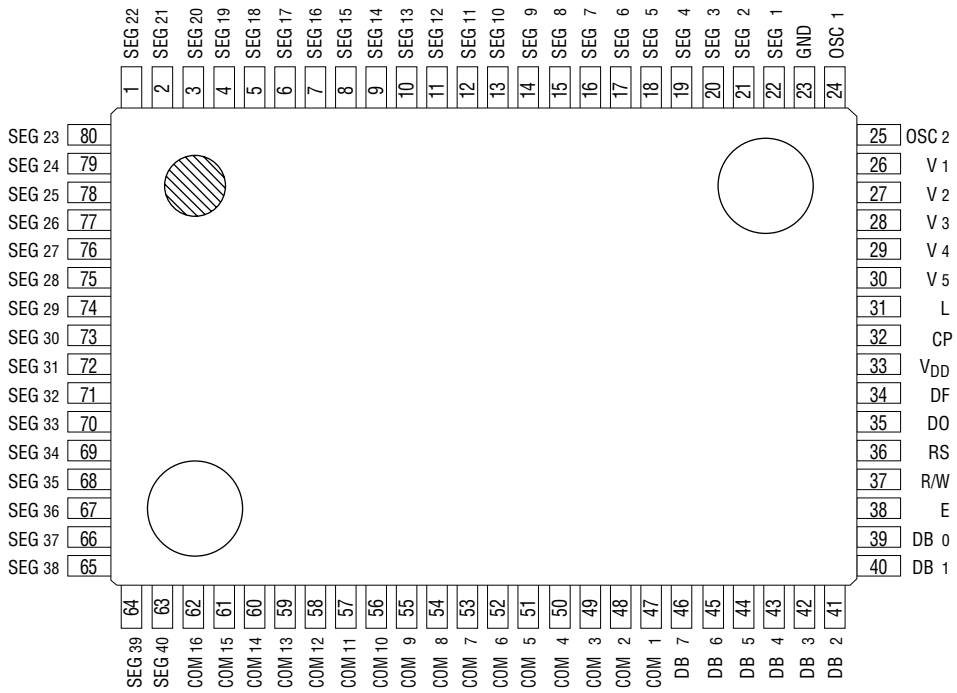


Applicable to pins DB_0 - DB_7.



Applicable to pins DO, CP, L, and DF.

PIN CONFIGURATION



80-Pin Plastic QFP

Note : The figure for Type L shows the configuration viewed from the reverse side of the package. Pay attention to the difference in pin arrangement.

PIN DESCRIPTIONS

Symbol	Description
R/W	Read/write selection input pin. "H" : Read, and "L" : Write
RS	Register selection input pin. "H" : Data register, and "L" : Instruction register
E	Input pin for data input/output between CPU and MSM6222B-xx and for instruction register activation.
DB_0 - DB_7	Input/output pins for data send/receive between CPU and MSM6222B-xx.
OSC_1, OSC_2	Clock oscillating pins required for internal operation upon receipt of the LCD drive signal and CPU instruction.
COM_1 - COM_{16}	LCD COMMON signal output pins.
SEG_1 - SEG_{40}	LCD SEGMENT signal output pins.
DO	Output pin to be connected to MSM5259 to expand the number of characters to be displayed.
CP	Clock output pin used when DO pin data output shifts inside of MSM5259.
L	Clock output pin for the serially transferred data to be latched to MSM5259.
DF	The alternating current signal (Display Frequency) output pin.
V_{DD}	Power supply pin.
GND	Ground pin.
V_1, V_2, V_3, V_4, V_5	Bias voltage input pins to drive the LCD.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable pin
Supply Voltage	V_{DD}	Ta = 25°C	–0.3 to + 7.0	V	V_{DD}, GND
LCD Driving Voltage	V_1, V_2, V_3 V_4, V_5	Ta = 25°C	V_{DD} – 9.0 to V_{DD} + 0.3	V	V_1, V_2, V_3 V_4, V_5
Input Voltage	V_I	Ta = 25°C	–0.3 to V_{DD} + 0.3	V	R/W, RS, E, DB_0 - DB_7 OSC_1
Power Dissipation	P_D	—	500	mW	—
Storage Temperature	T_{STG}	—	–55 to + 150	°C	—

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit	Applicable pin
Supply Voltage	V_{DD}	—	4.5 to 5.5	V	V_{DD}, GND
LCD Driving Voltage	V_{LCD}*1	1/4 bias, V_{DD}–V_5*2	3.0 to 8.0	V	V_{DD}, V_5
		1/5 bias, V_{DD}–V_5*3	3.0 to 8.0	V	
Operating Temperature	T_{op}	—	–20 to + 75	°C	—

*1 Voltage between V_{DD} and V_5.

*2 Voltages applicable to V_1, V_2, V_3 and V_4 are as follows.
$V_1 = V_{DD} - 1/4\ (V_{DD} - V_5)$
$V_2 = V_3 = V_{DD} - 1/2\ (V_{DD} - V_5)$
$V_4 = V_{DD} - 3/4\ (V_{DD} - V_5)$

*3 Voltages applicable to V_1, V_2, V_3 and V_4 are as follows.
$V_1 = V_{DD} - 1/5\ (V_{DD} - V_5)$
$V_2 = V_{DD} - 2/5\ (V_{DD} - V_5)$
$V_3 = V_{DD} - 3/5\ (V_{DD} - V_5)$
$V_4 = V_{DD} - 4/5\ (V_{DD} - V_5)$

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 to 5.5V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
"H" Input Voltage	V_{IH1}	—	2.2	—	V_{DD}	V	R/W, RS, E,
"L" Input Voltage	V_{IL1}	—	–0.3	—	0.6	V	DB_0 - DB_7
"H" Input Voltage	V_{IH2}	—	V_{DD} – 1.0	—	V_{DD}	V	OSC_1
"L" Input Voltage	V_{IL2}	—	–0.3	—	1.0	V	
"H" Output Voltage	V_{OH1}	I_O = –0.205mA	2.4	—	—	V	DB_0 - DB_7
"L" Output Voltage	V_{OL1}	I_O = 1.2mA	—	—	0.4	V	
"H" Output Voltage	V_{OH2}	I_O = –40µA	$0.9V_{DD}$	—	—	V	DO, CP, L,
"L" Output Voltage	V_{OL2}	I_O = 40µA	—	—	$0.1V_{DD}$	V	DC, OSC_2
COM Voltage Drop	V_C	I_O = ±50µA *1	—	—	2.9	V	COM_1 - COM_{16}
SEG Voltage Drop	V_S	I_O = ±50µA *1	—	—	3.8	V	SEG_1 - SEG_{40}
Input Leakage Current	I_{IL}	$V_I = V_{SS}$	—	—	–1	µA	E
		$V_I = V_{DD}$	—	—	1	µA	
Input Current	I_{IL2}	V_{DD} = 5.0V $V_I = V_{SS}$	–50	–125	–250	µA	R/W, RS DB_0 - DB_7
		$V_I = V_{DD}$, excluding current flowing over pullup resistor and output drive MOS	—	—	2	µA	

*1 Applicable to the voltage drop (V_C) occurring in pins V_{DD}, V_1, V_4, and V_5 to each COMMON pin (COM1 to COM16) when 50 µA flows in or out of all COM and SEG pins. Also applicable to voltage drop (V_S) occurring in pins V_{DD}, V_2, V_3, and V_5 to each SEG pin (SEG1 to SEG40). When output level is at V_{DD}, V_1 or V_2 level, 50 µA flows out, while 50 µA flows in when the output level is at V_3, V_4 or V_5 level.
This occurs when +5V is input to V_{DD}, V_1, and V_2, and when –3V is input to V_3, V_4, and V_5.

(V_{DD} = 4.5 to 5.5V, Ta = –20 to +75°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Applicable pin
Supply Current (1)	I_{DD1}	V_{DD} = 5.0V, resistor oscillation or external clock input via OSC_1. f_{OSC} = 270kHz. E is in "L" level. Other inputs are open. Output pins are all no load. *2		—	0.35	0.6	mA	V_{DD}
Supply Current (2)	I_{DD2}	V_{DD} = 5.0V, ceramic oscillation, f_{OSC} = 250kHz. E is in "L" level. Other pins are open. Output pins are all no load. *2		—	0.55	0.8	mA	V_{DD}
LCD Driving Bias Input Voltage	V_{LCD1}	V_{DD}–V_5 *7	1/5 bias	3.0	—	8.0	V	V_{DD}, V_1, V_2, V_3, V_4, V_5
	V_{LCD2}		1/4 bias	3.0	—	8.0		

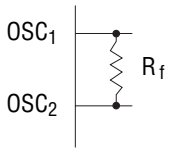
*2 Applicable to the current that flows in pin V_{DD} when power is input as follows: V_{DD} = 5V, GND = 0V, V_1 = 3.4V, V_2 = 1.8V, V_3 = 0.2V, V_4 = –1.4V, and V_5 = –3V.

AC Characteristics

(V_{DD} = 4.5 to 5.5V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable pin
R_f Clock Oscillation Frequency	f_{OSC1}	R_f = 91kΩ ± 2% *3	175	250	350	kHz	OSC_1 OSC_2
Clock Input Frequency	f_{IN}	OSC_2 is open. Input from OSC_1	125	250	350	kHz	OSC_1
Input Clock Duty	f_{DUTY}	*4	45	50	55	%	OSC_1
Input Clock Rise Time	t_r	*5	—	—	0.2	µs	OSC_1
Input Clock Fall Time	t_f	*5	—	—	0.2	µs	OSC_1
Ceramic Filter Oscillation Frequency	f_{OSC}	R_f = 510kΩ, C_1 = C_2 = 200 pF, R_d = 30kΩ, and Ceralock CSB250A. *6	245	250	255	kHz	OSC_1 OSC_2

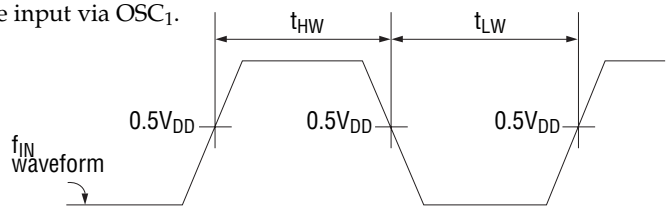
*3



$R_f = 91k\Omega \pm 2\%$

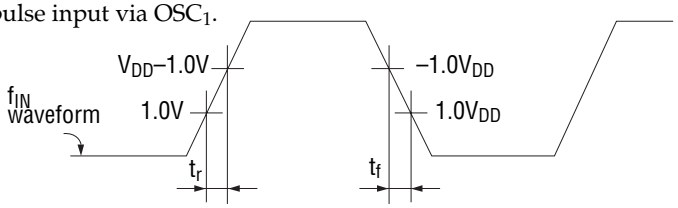
Minimum wiring is required between OSC_1 and R_f and between OSC_2 and R_f.

*4 Applied to pulse input via OSC_1.

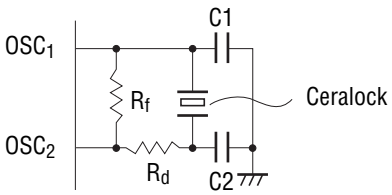


$f_{DUTY} = t_{HW} / (t_{HW} + t_{LW}) \times 100(\%)$

*5 Applied to pulse input via OSC_1.



*6



Ceralock : CSB250A (mfd. by MURATA MFG.Co.)
R_f : 510kΩ ±5%
R_d : 30kΩ ±5%
C_1 : 200pF ±10%
C_2 : 200pF ±10%
Please contact us when using this circuit.

*7 Input the voltage listed in the table below to V_1 - V_5:

Pin \ N (LCD lines)	1-line mode	2-line mode
V_1	$V_{DD} - \frac{V_{LCD}}{4}$	$V_{DD} - \frac{V_{LCD}}{5}$
V_2	$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{2V_{LCD}}{5}$
V_3	$V_{DD} - \frac{V_{LCD}}{2}$	$V_{DD} - \frac{3V_{LCD}}{5}$
V_4	$V_{DD} - \frac{3V_{LCD}}{4}$	$V_{DD} - \frac{4V_{LCD}}{5}$
V_5	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

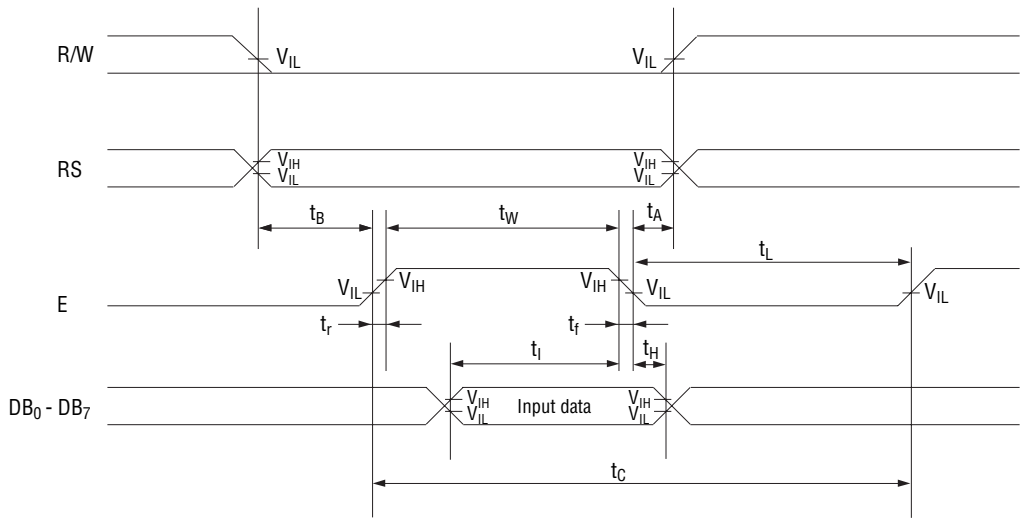
V_{LCD} is an LCD driving voltage. (For "N" (number of LCD lines), refer to the initial set of the instruction code.)

Switching Characteristics

• Timing for input from the CPU

(V_{DD} = 4.5 to 5.5V, Ta = –20 to +75°C)

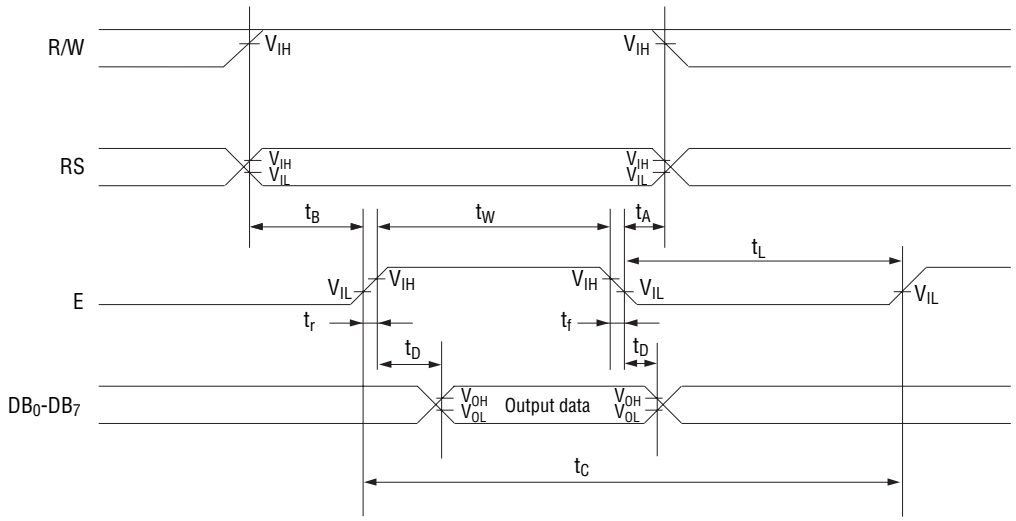
Parameter	Symbol	Min.	Typ.	Max.	Unit
R/W and RS set-up time	t_B	140	—	—	ns
E "H" pulse width	t_W	280	—	—	ns
R/W and RS holding time	t_A	10	—	—	ns
E rise time	t_r	—	—	25	ns
E fall time	t_f	—	—	25	ns
E "L" pulse width	t_L	280	—	—	ns
E cycle time	t_C	667	—	—	ns
DB_0 to DB_7 input data set-up time	t_I	180	—	—	ns
DB_0 to DB_7 input data holding time	t_H	10	—	—	ns



• Timing for output to the CPU

(V_{DD} = 4.5 to 5.5V, Ta = –20 to +75°C)

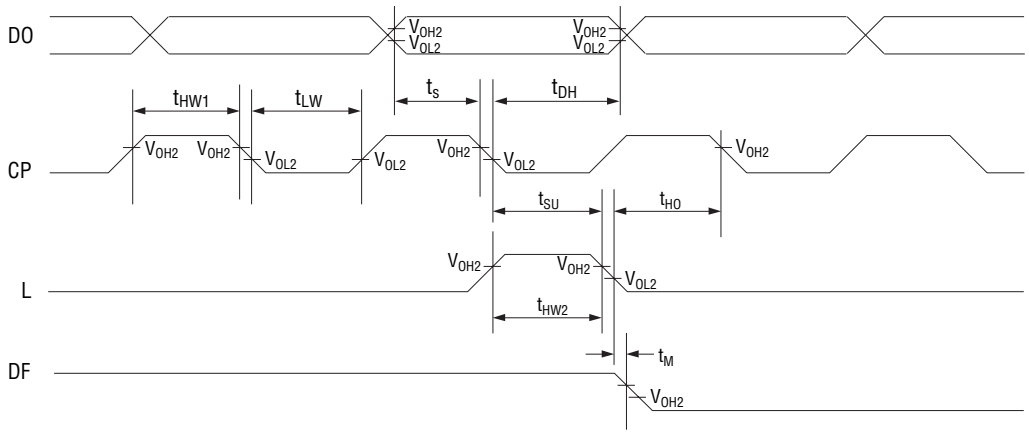
Parameter	Symbol	Min.	Typ.	Max.	Unit
R/W and RS set-up time	t_B	140	—	—	ns
E "H" pulse width	t_W	280	—	—	ns
R/W and RS holding time	t_A	10	—	—	ns
E rise time	t_r	—	—	25	ns
E fall time	t_f	—	—	25	ns
E "L" pulse width	t_L	280	—	—	ns
E cycle time	t_C	667	—	—	ns
DB_0 to DB_7 data output delay time	t_D	—	—	220	ns
DB_0 to DB_7 data output holding time	t_O	20	—	—	ns



• Timing for output to MSM5259

(V_{DD} = 4.5 to 5.5V, Ta = –20 to +75°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CP "H" pulse width	t_{HW1}	800	—	—	ns
CP "L" pulse width	t_{LW}	800	—	—	ns
DO set-up time	t_S	300	—	—	ns
DO holding time	t_{DH}	300	—	—	ns
L clock set-up time	t_{SU}	500	—	—	ns
L clock holding time	t_{HO}	100	—	—	ns
L "H" pulse width	t_{HW2}	800	—	—	ns
DF delay time	t_M	–1000	—	1000	ns



FUNCTIONAL DESCRIPTION

Instruction Register (IR) and Data Register (DR)

These two registers are selected by the REGISTER SELECTOR (RS) pin.
The DR is selected when the "H" level is input to the RS pin and IR is selected when the "L" level is input.
The IR is used to store the address of the display data RAM (DD RAM) or character generator RAM (CG RAM) and instruction code.
The IR can be written, but not be read by the microcomputer (CPU).
The DR is used to write and read the data to and from the DD RAM or CG RAM.
The data written to DR by the CPU is automatically written to the DD RAM or CG RAM as an internal operation.
When an address code is written to IR, the data (of the specified address) is automatically transferred from the DD RAM or CG RAM to the DR. Next, when the CPU reads the DR, it is possible to verify DD RAM or CG RAM data from the DR data.
After the writing of DR by the CPU, the next adress in the DD RAM or CG RAM is selected to be ready for the next CPU writing.
Likewise, after the reading out of DR by the CPU, DD RAM or CG RAM data is read out by the DR to be ready for the next CPU reading.
Write/read to and from both registers is carried out by the READ/WRITE (R/W) pin.

Table 1 RS and R/W pins functions

R/W	RS	Function
L	L	IR write
H	L	Read of busy flag (BF) and address counter (ADC)
L	H	DR write
H	H	DR read

Busy Flag (BF)

When the busy flag is at "H", it indicates that the MSM6222B-xx is engaged in internal operation.
When the busy flag is at "H", any new instruction is ignored.
When R/W = "H" and RS = "L", the busy flag is output from DB_7.
New instruction should be input when busy flag is "L" level.
When the busy flag is at "H", the output code of the address counter (ADC) is undefined.

Address Counter (ADC)

The address counter (ADC) allocates the address for the DD RAM and CG RAM write/read and also for the cursor display.
When the instruction code for a DD RAM address or CG RAM address setting is input to IR, after deciding whether it is DD RAM or CG RAM, the address code is transferred from IR to ADC. After writing (reading) the display data to (from) the DD RAM or CG RAM, the ADC is incremented (decremented) by 1 internally.
The data of the ADC is output to DB_0 - DB_6 on the conditions that R/W = "H", RS = "L", and BF = "L".

Timing Generator Circuit

This circuit is used to generate timing signals to activate internal operations upon receipt of CPU instruction and also from such internal circuits as the DD RAM, CG RAM, and CG ROM.

It is designed so that the internal operation caused by accessing from the CPU will not interfere with the internal operation caused by LCD driving. Consequently, when data is written from the CPU to DD RAM, flickering does not occur in a display area other than the display area where the data is written.

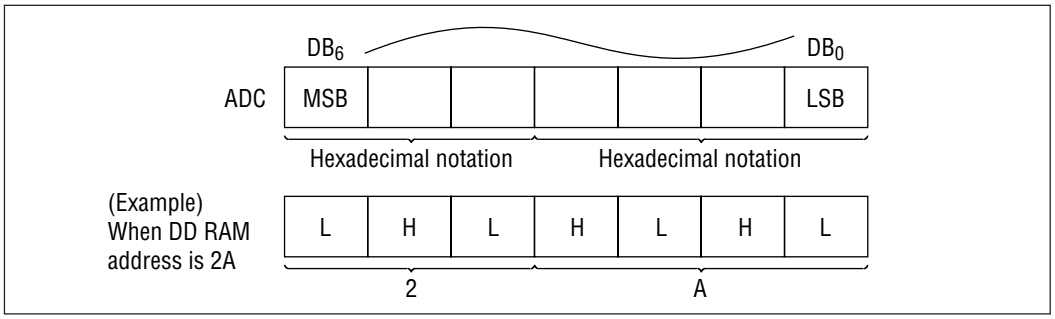
In addition, this circuit generates the transfer signal to MSM5259 for display character expansion.

Display Data RAM (DD RAM)

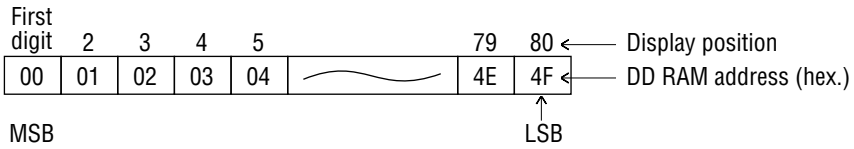
This RAM is used to store display data of 8-bit character codes (see Table 2).

DD RAM address corresponds to the display position of the LCD. The correspondence between the two is described in the following.

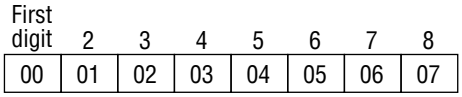
DD RAM address (set to ADC) is expressed in hexadecimal notation as shown below:



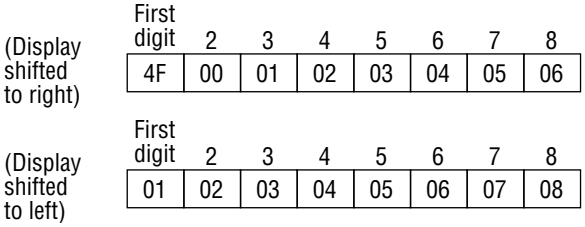
(1) Correspondence between address and display position in the 1-line display mode



- When the MSM6222B-xx alone is used, up to 8 characters can be displayed from the first to eighth digit.



When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:



- When the MSM6222B-xx is used with one MSM5259, up to 16 characters can be displayed from the first to sixteenth digit as shown below:

First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F

MSM6222B-xx display MSM5259 display

When the display is shifted by instruction, the correspondence between the LCD display and the DD RAM address changes as shown below:

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
(Display shifted to right)	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
(Display shifted to left)	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10

MSM6222B-xx display MSM5259 display

- Since the MSM6222B-xx has a DD RAM capacity of up to 80 characters, up to 9 MSM5259 devices can be connected to MSM6222B-xx so that 80 characters can be displayed.

First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		73	74	75	76	77	78	79	80
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	~	42	49	4A	4B	4C	4D	4E	4F

MSM6222B-xx display MSM5259 (1) display MSM5259 (2) - (8) display MSM5259 (9) display

(2) Correspondence between address and display position in the 2-line display mode

	First digit	2	3	4	5		39	40	
									← Display position
First line	00	01	02	03	04		26	27	← DD RAM address (hex.)
Second line	40	41	42	43	44		66	67	

(Note) The last address of the first line is not consecutive to the head address of the second line.

- When MSM6222B-xx alone is used, up to 16 characters (8 characters x 2 lines) can be displayed from the first to eighth digit.

	First digit	2	3	4	5	6	7	8
First line	00	01	02	03	04	05	06	07
Second line	40	41	42	43	44	45	46	47

When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit	2	3	4	5	6	7	8
First line	27	00	01	02	03	04	05	06
Second line	67	40	41	42	43	44	45	46

(Display shifted to left)

	First digit	2	3	4	5	6	7	8
First line	01	02	03	04	05	06	07	08
Second line	41	42	43	44	45	46	47	48

- When the MSM6222B-xx is used with one MSM5259, up to 32 characters (16 characters x 2 lines) can be displayed from the first to the sixteenth digit.

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
Second line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
	MSM6222B-xx display								MSM5259 display							

When the display is shifted by instruction, the correspondence between the LCD display position and the DD RAM address changes as shown below:

(Display shifted to right)

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
Second line	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E

MSM6222B-xx display MSM5259 display

(Display shifted to left)

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
First line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
Second line	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50

MSM6222B-xx display MSM5259 display

- Since the MSM6222B-xx has a DD RAM capacity of up to 80 characters, up to 4 MSM5259 devices can be connected to the MSM6222B-xx in the 2-line display mode.

	First digit	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18		33	34	35	36	37	38	39	40
First line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11		20	21	22	23	24	25	26	27
Second line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51		60	61	62	63	64	65	66	67

MSM6222B-xx display MSM5259 (1) display MSM5259 (2) - (3) display MSM5259 (4) display

Character Generator ROM (CG ROM)

The CG ROM is used to generate 5 x 7 dots (160 kinds) or 5 x 10 dots (32 kinds) character patterns from an 8-bit DD RAM character code signal.
The correspondence between 8-bit character codes and character patterns is shown in Table 2.
When the 8-bit character code of the CG ROM is written to the DD RAM, the character pattern of the CG ROM corresponding to the code is displayed on the LCD display position corresponding to the DD RAM address.

Table 2 Relationship Between Character Codes and Characters (Character Patterns) of MSM6222B -01

Upper 4 bits / Lower 4 bits	MSB 0000	0010		0011		0100		0101		0110		0111		1010		1011		1100		1101		1110		1111	
0000 LSB	CG RAM (1)			0		@		P		\		p				—		タ		ミ		α		P	
0001	(2)	!		1		A		Q		a		q		。		ア		チ		ム		ä		q	
0010	(3)	″		2		B		R		b		r		「		イ		ツ		メ		β		Θ	
0011	(4)	#		3		C		S		c		s		」		ウ		テ		モ		ε		∞	
0100	(5)	$		4		D		T		d		t		、		エ		ト		ヤ		μ		Ω	
0101	(6)	%		5		E		U		e		u		•		オ		ナ		ユ		σ		ü	
0110	(7)	&		6		F		V		f		v		ヲ		カ		ニ		ヨ		ρ		Σ	
0111	(8)	’		7		G		W		g		w		ァ		キ		ヌ		ラ		g		π	
1000	(1)	(		8		H		X		h		x		ィ		ク		ネ		リ		√		$\overline{X}$	
1001	(2)	)		9		I		Y		i		y		ゥ		ケ		ノ		ル		–1		*y*	
1010	(3)	*		:		J		Z		j		z		ェ		コ		ハ		レ		*j*		千	
1011	(4)	+		;		K		[		k		{		ォ		サ		ヒ		ロ		x		万	
1100	(5)	,		<		L		¥		l		|		ャ		シ		フ		ワ		¢		円	
1101	(9)	–		=		M		]		m		}		ュ		ス		ヘ		ン		£		÷	
1110	(7)	.		>		N		^		n		→		ョ		セ		ホ		゙		$\overline{n}$			
1111	(8)	/		?		O		_		o		←		ッ		ソ		マ		゜		ö		■	

Character Generator RAM (CG RAM)

The CG RAM is used to display user's original character patterns other than character patterns in the CG ROM.
The CG RAM has a capacity (64 bytes = 512 bits) of writing 8 kinds of characters for 5 x 7 dots and 4 kinds of characters for 5 x 10 dots.
When displaying character patterns stored in the CG RAM, write 8-bit character codes (00 to 07 or 08 to 0F; hex.) on the left side as shown in Table 2. Then it is possible to output the character pattern to the LCD display position corresponding to the DD RAM address.
The following explains how to write and read character patterns to and from the CG RAM.

(1) When the character pattern is 5 x 7 dots (see Table 3-1).

- A method of writing character pattern to the CG RAM by CPU:
  Three bits of CG RAM addresses 0-2 correspond to the line position of the character pattern.
  First, set increment or decrement by the CPU, and then input the CG RAM address. After this, write character patterns to the CG RAM through DB_0 - DB_7 line by line. DB_0 to DB_7 correspond to CG RAM data 0-7 in Table 3-1.
  It is displayed when "H" is set as input data and is not displayed when "L" is set as input data.
  Since the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.
  The line, in which the CG RAM addresses 0-2 are all "H" ("7" in hexadecimal notation), is the cursor position. It is ORed with the cursor at the cursor position and displayed to LCD.
  For this reason, it is necessary to set all input data that become cursor positions to "L".
  Although CG RAM data 0-4 bits are output to the LCD as display data, CG RAM data bits 5-7 are not output. The latter can be written and read to and from the RAM, it is therefore allowed to be used as data RAM.

- A method of displaying the CG RAM character pattern to the LCD:
  The CG RAM is selected when upper 4 bits of the character codes are all "L".
  As character code bit 3 is invalid, the display of "0" in Table 3-1, is selected by character code "00" (hex.) or "08" (hex.).
  When the 8-bit character code of the CG RAM is written to the DD RAM, the character pattern of the CG RAM is displayed on the LCD display position corresponding to the DD RAM address. (DD RAM data, bits 0-2 correspond to CG RAM address, bits 3-5.)

(2) When character pattern is 5 x 10 dots (see Table 3-2).

- A method of writing character pattern into the CG RAM by the CPU:
  Four bits of CG RAM address, bits 0-3, correspond to the line position of the character pattern.
  First, set increment or decrement with the CPU, and then input the address of the CG RAM.
  After this, write the character pattern code into the CG RAM, line by line from DB_0-DB_7.
  DB_0 to DB_7 correspond to CG RAM data, bits 0-7, in Table 3-2.
  It is displayed when "H" is set as input data, while it is not displayed when "L" is set as input data.
  As the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.
  The line, the CGRAM addresses 0-3 of which are "A" in hexadecimal notation, is the cursor position. The CGRAM data is 0Red with the cursor at the cursor position and displayed to LCD. For this reason, it is necessary to set all input data that become cursor positions to "L".
  When the CG RAM data, bits 0-4, and CG RAM addresses, bits 0-3, are "0" to "A", they are displayed on the LCD as the display data. When the CG RAM data, bits of 5-7, and CG RAM, bit data is 0-4 and CG RAM address data is "B" to "F", it is not output to the LCD.
  But in this case, CG RAM can be used as RAM and it can be written into/read out. So, it can be used as the data RAM.

- A method of displaying the CG RAM character pattern to the LCD:
  The CG RAM is selected when 4-upper order bits of the character code are all "L". As character code bits 0 and 3 are invalid, the display of "μ" is selected by character codes "00", "01", "08", and "09" (hex.) as in Table 3-2.
  When the CG RAM character code is written to the DD RAM, the CG RAM character pattern is displayed on the LCD display position corresponding to the DD RAM address.
  (DD RAM data bits 1 and 2 correspond to CG RAM address bits 4 and 5.)

Table 3-1 Relationship between CG RAM data (character pattern), CG RAM address and DD RAM data when the character pattern is 5 x 7 dots.
The example below indicates "OKI".

CG RAM address	CG RAM data (character pattern)		DD RAM data (character code)
5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB		7 6 5 4 3 2 1 0 MSB LSB
L L L L L L L L H L H L L H H H L L H L H H H L H H H	X X X L H H H L H L L L H H L L L H H L L L H H L L L H H L L L H L H H H L L L L L L		L L L L X L L L
L L H L L L L L H L H L L H H H L L H L H H H L H H H	X X X H L L L H H L L H L H L H L L H H L L L H L H L L H L L H L H L L L H L L L L L		L L L L X L L H
H H H L L L L L H L H L L H H H L L H L H H H L H H H	X X X L H H H L L L H L L L L H L L L L H L L L L H L L L L H L L L H H H L L L L L L		L L L L X H H H

X : Don't Care

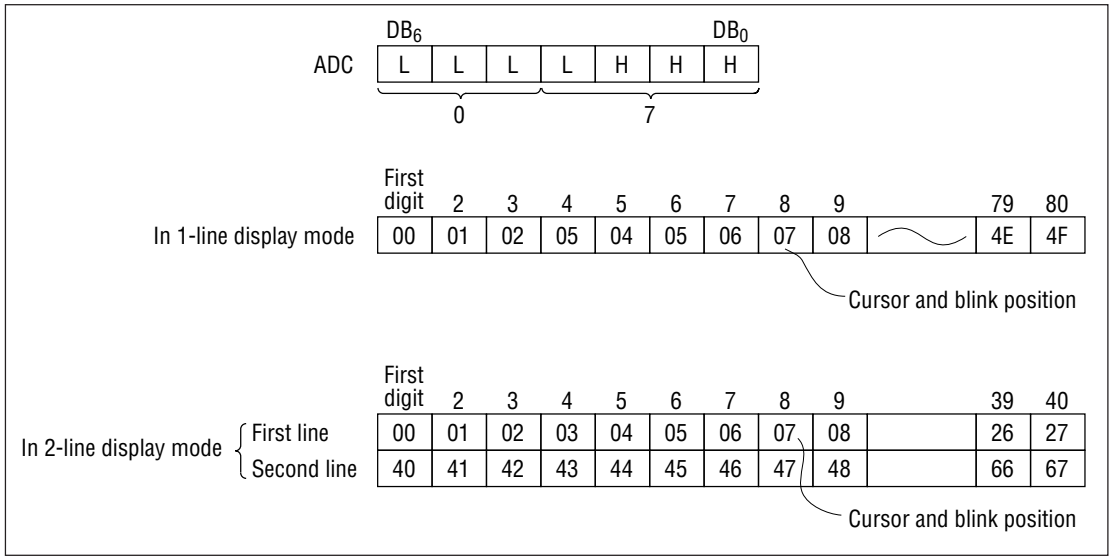
Table 3-2 Relationship between CG RAM data (character pattern), CG RAM address and DD RAM data when the character pattern is 5 x 10 dots. The examples below indicate μ, g and ʊ.

CG RAM address	CG RAM data (character pattern)		DD RAM data (character code)
5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB		7 6 5 4 3 2 1 0 MSB LSB
L L L L L L L L L H L L H L L L H H L H L L L H L H L H H L L H H H H L L L H L L H H L H L H L H H H H L L H H L H H H H L H H H H	X X X L L L L L H L L L H H L L L H H L L L H H L L H H H H H L H H L L L L H L L L L H L L L L L L L L L X X X X X		L L L L X L L X
L H L L L L L L L H L L H L L L H H L H L L L H L H L H H L L H H H H L L L H L L H H L H L H L H H H H L L H H L H H H H L H H H H	X X X L L L L L L L L L L L H H H H H L L L H H L L L H H L L L H L H H H H L L L L H L L L L H L H H H L L L L L L X X X X X		L L L L X L H X
L L L L L L L L L H L L H L L L H H L H L L L H L H L H H L L H H H H L L L H L L H H L H L H L H H H H L L H H L H H H H L H H H H	X X X L L L L L L L L L L H H L H H L H L H L H L L L H H L L L H L H H H L L L L L L L L L L L L L L L L X X X X X		L L L L X H H X

X : Don't Care

Cursor/Blink Control Circuit

This is a circuit that generates the LCD cursor and blink.
This circuit is under the control of the CPU program.
The display of the cursor and blink on the LCD is made at a position corresponding to the DD RAM address that is set in the ADC.
The figure below shows an example of the cursor/blink position when the value of ADC is set to "07" (hex.).



(Note) The cursor and blink are displayed even when the CG RAM address is set in the ADC. For this reason, it is necessary to inhibit the cursor and blink display while the CG RAM address is set in the ADC.

LCD Display Circuit (COM_1 to COM_{16}, SEG_1 to SEG_{40}, L, CP, DO, and DF)

As the MSM6222B-xx provides the COM signal outputs (16 outputs) and the SEG signal outputs (40 outputs), it can display 8 characters (1-line display) or 16 characters (2-line display) as a unit.
SEG_1 to SEG_{40} are used to display 8-digit display on the LCD. To expand the display, an MSM5259 is used.
The MSM5259, 40-dot segment driver, is used for expansion of the SEG signal output.
Interface with the MSM5259 is made through data output pin (DO), clock output pin (CP), latch output pin (L), and display frequency pin (DF). The character pattern data is serially transferred to MSM5259 through DO and CP. When the data of 72 characters 360-bit (= 5-bit/ch. x 72 ch. = 1-line display) or 32 characters 160-bit (5-bit/ch. x 32 ch. = 2-line display) is output, the latch pulse is also output through pin L. By this latch pulse, the data transferred serially to MSM5259 is latched to be used as display data. The display frequency signal (DF) required when LCD is displayed is also output from DF pin synchronously with this latch pulse.

Built-in Reset Circuit

The MSM6222B-xx is automatically initialized when the power is turned on.
During initialization, the busy flag (BF) holds "H" and does not accept instructions (other than the busy flag read).
The busy flag holds "H" for 15 ms after V_{DD} reaches 4.5V or more.
During initialization, the MSM6222B-xx executes the follwing instructions:

- Display clear
- Data length of interface with CPU: 8 bits (8B/4B = "H")
- LCD: 1-line display (N = "L")
- Character font: 5 x 7 dots (F = "L")
- ADC: Increment (I/D = "H")
- No display shift (SH = "L")
- Display: Off (DI = "L")
- Cursor: Off (C = "L")
- No blink (B = "L")

It is required to satisfy the following power supply conditions.

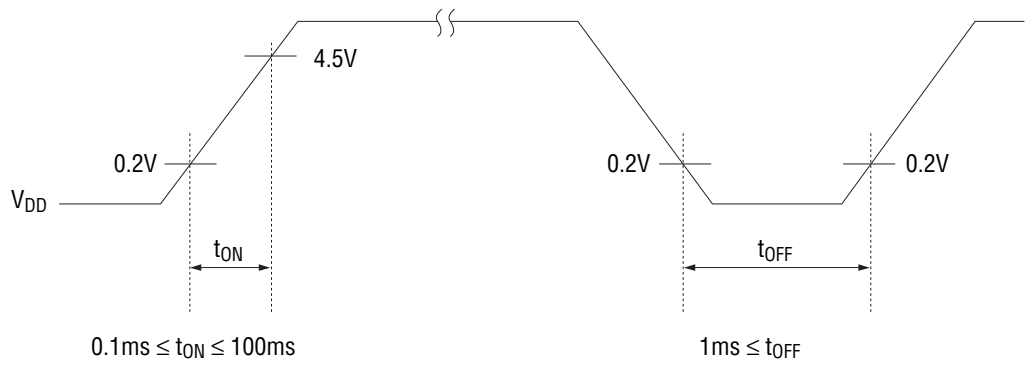


Fig. 1. Power ON/OFF Waveform

Data Bus Connected with CPU

The data bus connected with CPU is available either once for 8 bits or twice for 4 bits. This allows the MSM6222B-xx to be interfaced with either an 8-bit or 4-bit CPU.

(1) When the interface data length is 8 bits
Data buses DB_0 to DB_7 (8 buses) are all used and data input/output is carried out in one step.

(2) When the interface data length is 4 bits
The 8-bit data input/output is carried out in two steps by using only high-order 4 bits of data buses DB_4 to DB_7 (4 buses)
The first time data input/output is made for 4-high order bits (DB_4 to DB_7 when the interfaces data length is 8 bits) and the second time data input/output is made for low-order 4 bits (DB_0 to DB_3 when the interface data length is 8 bits). Even when the data input/output can be completely made through high-order 4 bits, be sure to make another input/output of low-order 4 bits. (Example: Busy flag Read).
Since the data input/output is carried out in two steps but as one execution, no normal data transfer is executed from the next input/output if accessed only once.

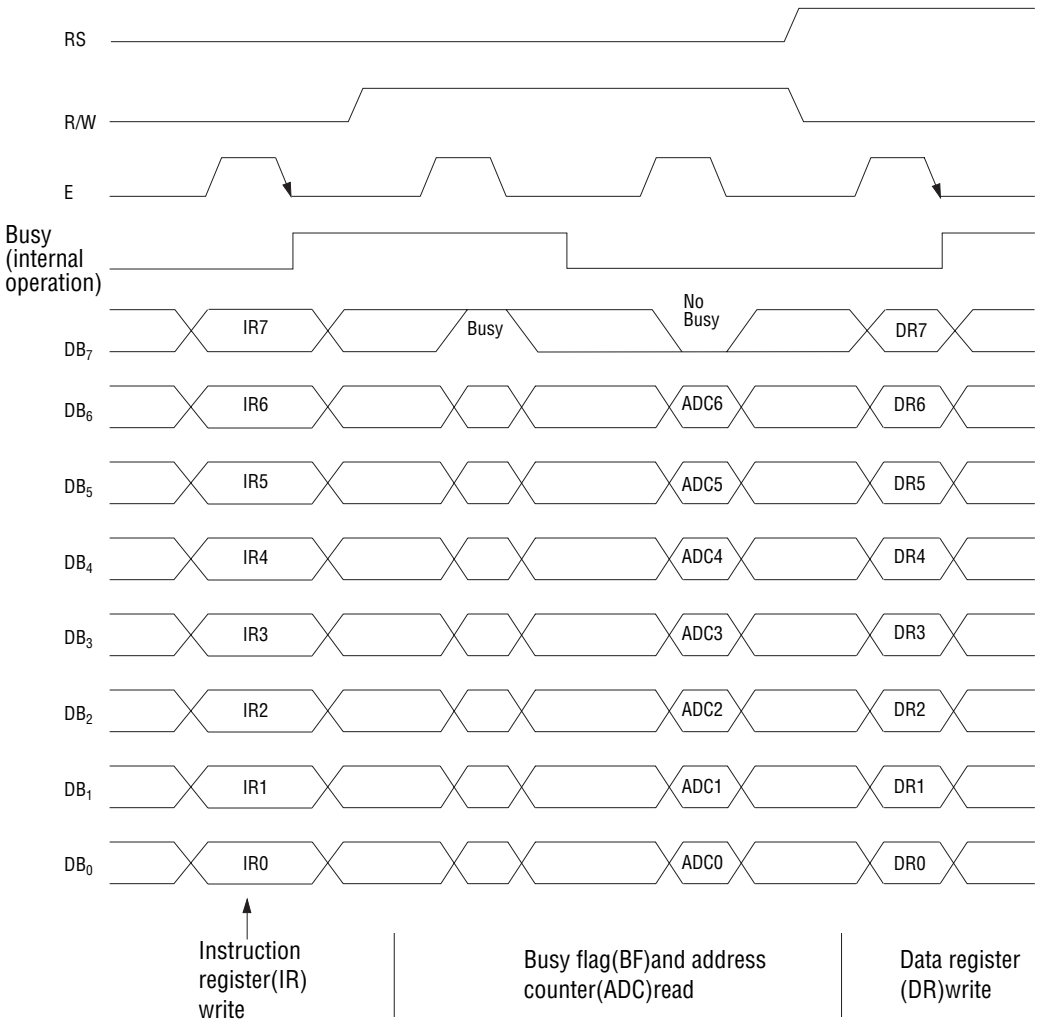


Fig. 2 8-Bit Data Transfer

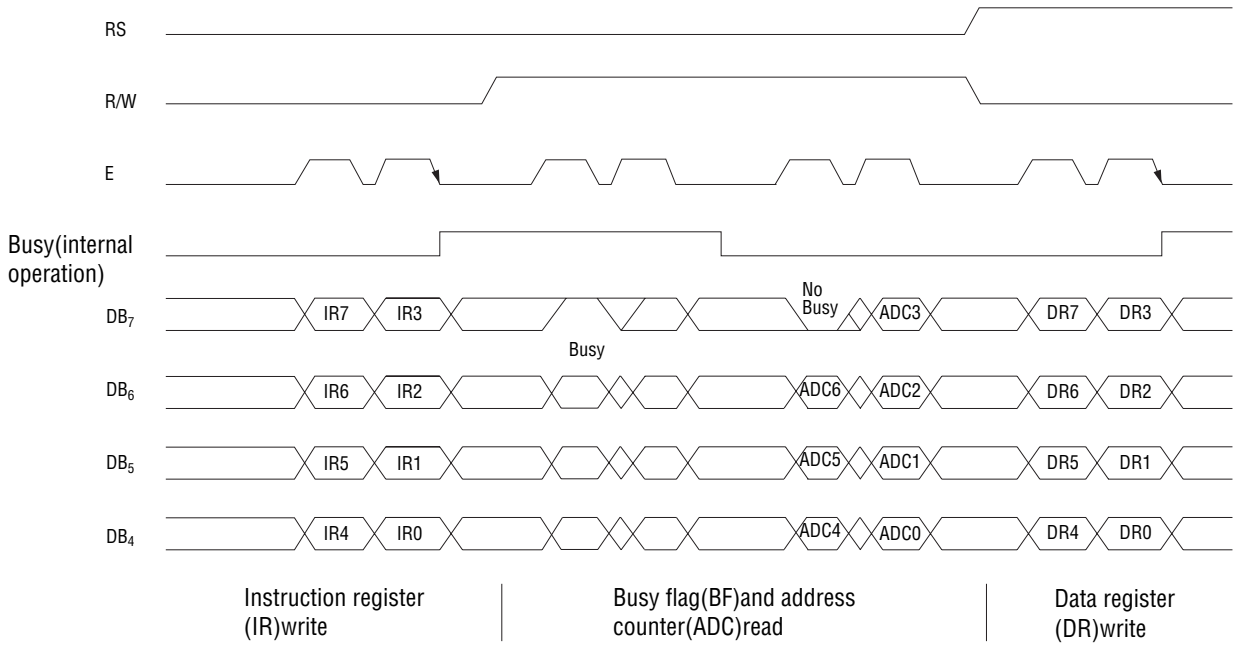


Fig. 3 4-Bit Data Transfer

Instruction Code

The instruction code is defined as the signal through which the MSM6222B-xx is accessed by the CPU.
The MSM6222B-xx begins operation upon receipt of the instruction code input.
As the internal processing operation of MSM6222B-xx starts in a timing that does not affect the LCD display, the busy status continues for longer than the CPU cycle time.
Under the busy status (when the busy flag is set to "H"), the MSM6222B-xx does not execute any instructions other than the busy flag read.
Therefore, the CPU has to verify that the busy flag is set to "L" prior to the input of the instruction code.

(1) Display clear:

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	L	H

When this instruction is executed, the LCD display is cleared.
I/D in the entry mode setting is set to "H" (increment). SH does not change.
When the cursor and blink are in display, the blinking position moves to the left end of the LCD (the left end of the first line in the 2-line display mode).

(Note) All DD RAM data goes to "20" (hex.), while the address counter (ADC) goes to "00" (hex.). The execution time is 1.64 ms (max.), when the OSC oscillation frequency is 250 kHz.

(2) Cursor home

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	H	X

X : Don't Care

When this instruction is executed, the blinking position moves to the left end of the LCD (to the left end of the first line in the 2-line display mode) as the cursor and blink are being displayed.
When the display is in shift, the display returns to its original position before shifting.

(Note) The address counter (ADC) goes to "00" (hex.). The execution time is 1.64 ms (max.), when the OSC oscillation frequency is 250 kHz.

(3) Entry mode setting

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	H	I/D	SH

① When the I/D is set, the 8-bit character code is written or read to and from the DD RAM, the cursor and blink shift to the right by 1 character position (I/D = "H"; increment) or to the left by 1 character position (I/D = "L"; decrement).
The address counter is incremented (I/D = "H") or decremented (I/D = "L") by 1 at this time. Even after the character pattern code is written or read to and from the CG RAM, the address counter (ADC) is incremented (I/D = "H") or decremented (I/D = "L") by 1.

② When SH = "H" is set, the character code is written to the DD RAM. Then the cursor and blink stop and the entire display shifts to the left (I/D = "H") or to the right (I/D = "L") by 1 character position.
When the character is read from the DD RAM during SH = "H", or when the character pattern data is written or read to or from the CG RAM during SH = "H", the entire display does not shift, but normal write/read is performed (the entire display does not shift, but the cursor and blink shift to the right (I/D = "H") or to the left (I/D = "L") by 1 character position.
When SH = "L" is set, the display does not shift, but normal write/read is performed.
The execution time when the OSC oscillation frequency is 250 kHz is 40 µs.

(4) Display mode setting

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	H	DI	C	B

① The DI bit controls whether the character pattern is displayed or not displayed.
When DI is "H", this bit makes the LCD display the character pattern.
When DI is "L", the LCD character pattern is not displayed. The cursor and blink are also cancelled at this time.

(Note) Unlike the display clear, the character code is not rewritten at all.

② The cursor is not displayed when C = "L" and is displayed when DI = "H" and C = "H".

③ The blink is cancelled when B = "L" and is executed when DI = "H" and B = "H".
In the blink mode, all dots (including the cursor), displaying character pattern, and cursor are displayed alternately at 409.6 ms (in 5 x 7 dots character font) or 563.2 ms (in 5 x 10 dots character font) when the OSC oscillation frequency is 250 kHz. The execution time when the OSC oscillation frequency is 250 kHz is 40 µs.

(5) Cursor and display shift

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	H	D/C	R/L	X	X

X : Don't Care

When D/C = "L" and R/L = "L", the cursor and blink positions are shifted to the left by 1 character position (ADC is decremented by 1).
When D/C = L and R/L = "H", the cursor and blink positions are shifted to the right by 1 character position (ADC is incremented by 1).
When D/C = "H" and R/L = "L", the entire display is shifted to the left by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).
When D/C = "H" and R/L = "H", the entire display is shifted to the right by 1 character position. The cursor and blink positions are also shifted with the display (ADC remains unchanged).
In the 2-line display mode, the cursor and blink positions are shifted from the first to the second line when the cursor is shifted to the right next to the fortieth digit (27; hex.) in the first line. No such shifting is made in other cases.
When shifting the entire display, the display pattern, cursor, and blink positions are in no case shifted between lines (from the first to the second line or vice versa).
The execution time, when the OSC oscillation frequency is 250 kHz, is 40 µs.

(6) Initial setting

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	H	8B/4B	N	F	X	X

X : Don't Care

① When 8B/4B = "H", the data input/output to and from the CPU is carried out simultaneously by means of 8 bits DB_7 to DB_0.
When 8B/4B = "L", the data input/output to and from the CPU is carried out in two steps through 4 bits of DB_7 to DB_4.

② The 2-line display mode of the LCD is selected when N = "H", while the 1-line display mode is selected when N = "L".

③ The 5 x 7 dots character font is selected when F = "L", while the 5 x 10 dots character font is selected when F = "H" and N = "L".
This initial setting has to be accessed prior to other instructions except for the busy flag read after the power is supplied to the MSM6222B-xx.

N	F	Number of display lines	Character font	Duty ratio	Number of biases	Number of COMMOM signals
L	L	1 - line	5 x 7 dots	1/8	4	8
L	H	1 - line	5 x 10 dots	1/11	4	11
H	L	2 - line	5 x 7 dots	1/16	5	16
H	H	2 - line	5 x 7 dots	1/16	5	16

Generate biases externally and input them to the MSM6222B-xx (V_{DD}, V_1, V_2, V_3, V_4, and V_5).
When the number of biases is 4, input the same potential to V_2 and V_3. The execution time, when the OSC oscillation frequency is 250 kHz, is 40 µs.

(7) CG RAM address setting

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	H	C_5	C_4	C_3	C_2	C_1	C_0

When CG RAM addresses, bits C_5 to C_0 (binary), are set, the CG RAM is specified, until the DD RAM address is set.
Write/read of the character pattern to and from the CPU begins with addresses, bits C_5 to C_0, starting from CG RAM selection.
The execution time, when the OSC oscillation frequency is 250 kHz, is 40 µs.

(8) DD RAM address setting

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	H	D_6	D_5	D_4	D_3	D_2	D_1	D_0

When the DD RAM addresses D_6 to D_0 (binary) are selected, the DD RAM is specified until the DD RAM address is set.
Write/read of the character code to and from the CPU begins with addresses D_6 to D_0 starting from DD RAM selection.
In the 1-line display mode (N = H), however, D_6 to D_0 (binary) must be set to one of the values among "00" to "4F" (hex.).
Likewise, in the 2-line mode, D_6 to D_0 (binary) must be set to one of the values among "00" to "27" (hex.) or "40" to "67" (hex.).
When any value other than the above is input, it is impossible to make a normal write/read of character codes to and from the DD RAM.
The execution time, when the OSC oscillation frequency is 250 kHz, is 40 µs.

(9) DD RAM and CG RAM data write

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	H	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0

When E_7 to E_0 (binary) codes are written to the DD RAM or CG RAM, the cursor and display move as described in "(5) Cursor and display shift". The execution time, when the OSC oscillation frequency is 250 kHz, is 40 µs.

(10) Busy flag and address counter read (Execution time is 1 μs.)

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	L	BF	O_6	O_5	O_4	O_3	O_2	O_1	O_0

The busy flag (BF) is output by this instruction to indicate whether the MSM6222B-xx is engaged in internal operations (BF = "H") or not (BF = "L").
When BF = "H", no new instruction is accepted. It is therefore necessary to verify BF = "L" before inputting a new instruction.
When BF = "L", a correct address counter value is output. The address counter value must match the DD RAM address or CG RAM address. The decision of whether it is a DD RAM address or CG RAM address is made by the address previously set.
Since the address counter value when BF = "H" is sometimes incremented or decremented by 1 during internal operations, it is not always a correct value.

(11) DD RAM and CG RAM data read

	R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	H	P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Character codes (bits P_7 to P_0) are read from the DD RAM, while character patterns (P_7 to P_0) from the CG RAM.
Selection of DD RAM or CG RAM is decided by the address previously set.
After reading those data, the address counter (ADC) is incremented or decremented by 1 as set by the shift mode mentioned in item "(3) shift mode set".
The execution time, when the OSC oscillation frequency is 250 kHz, is 40 μs.

(Note) Conditions for the reading of correct data:
① When the DD RAM address set or CG RAM address set is input before inputting this instruction.
② When the cursor/display shift is input before inputting this instruction in case the character code is read.
③ Data after the second reading from RAM when read more than 2 times. Correct data is not output in any other case.

Interface with LCD and MSM5259

Display examples when setting the 5 x 7 dots character font 1-line mode, 5 x 10 dots character font 1-line mode, and 5 x 7 dots character font 2-line mode through instructions are shown in Figures 4, 5, and 6, respectively.
When the 5 x 7 dots character font is set in the 1-line display mode, the COM signals COM_9 to COM_{16} are output for extinguishing.
Likewise, when the 5 x 10 dots character font (1-line is set), the COM signals COM_{12} to COM_{16} are output for display-off.
The display example shows a combination of 16 characters (32 characters for the 2-line display mode) and the LCD. When the number of MSM5259s are increased according to the increase in the number of characters, it is possible to display a maximum of 80 characters.
Besides, it is necessary to generate bias voltage required for LCD operation by splitting resistors outside the IC to input it to MSM6222B-xx and MSM5259.
Examples of these bias voltages are shown in Figures 7, 8, 9, and 10. Basically, this can be done by dividing the voltage by the resistors as shown in Figures 7 and 8. If the value of resistor R is made larger to reduce system power consumption, the LCD operating margin decreases and the LCD driving waveform is distorted. To prevent this, a by-pass capacitor is serially connected to the resistor to lower voltage division impedance caused by the splitting of resistors as shown in Figures 9 and 10.
As the values of R, VR, and C vary according to the LCD size used and V_{LCD} (LCD drive voltage), these values have to be determined through actual experimentation in combination with the LCD.
(Example set values: R = 3.3 to 10kΩ, V_R = 10 to 30kΩ, and C = 0.0022 µF to 0.047 µF)
Figure 17 shows an application circuit for the MSM6222B-xx and MSM5259 including a bias circuit.
The bias voltage has to maintain the following potential relation:

$$V_{DD} > V_1 > V_2 \geq V_3 > V_4 > V_5$$

- In the case of 1-line 16 characters display (5 x 7 dots/font)

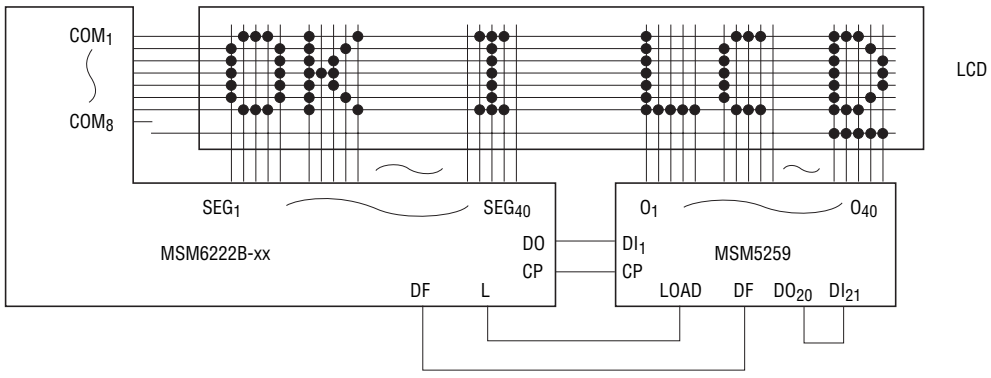


Figure 4

• In the case of 16-character (1 line) display (5 x 10 dots/font)

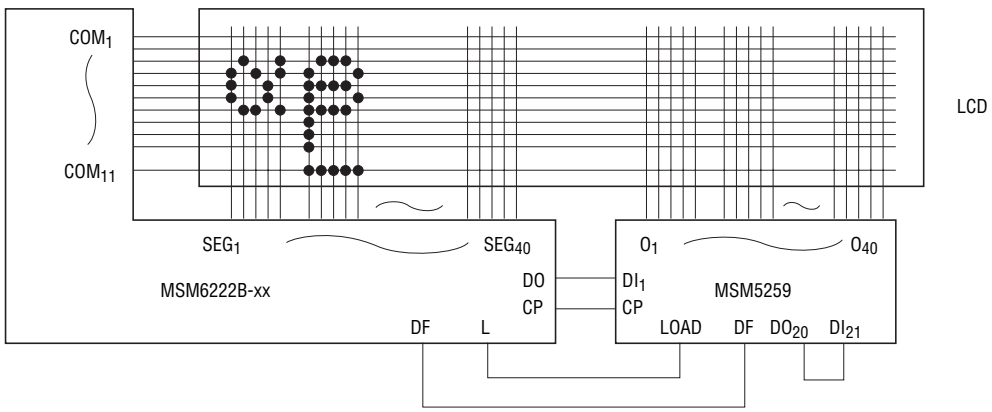


Figure 5

• In the case of 16-character (2 lines) display (5 x 7 dots/font)

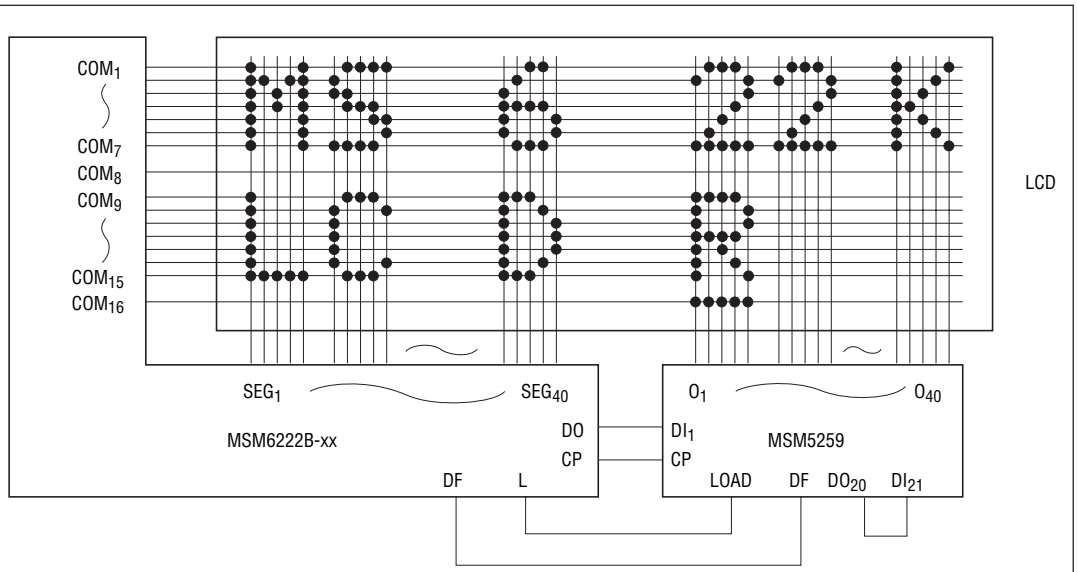


Figure 6

• Bias voltage circuit (1-line display mode)

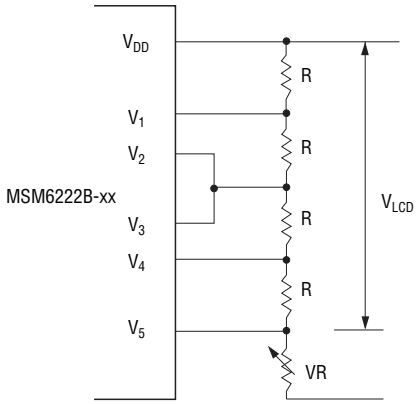


Figure 7

• Bias voltage circuit (2-line display mode)

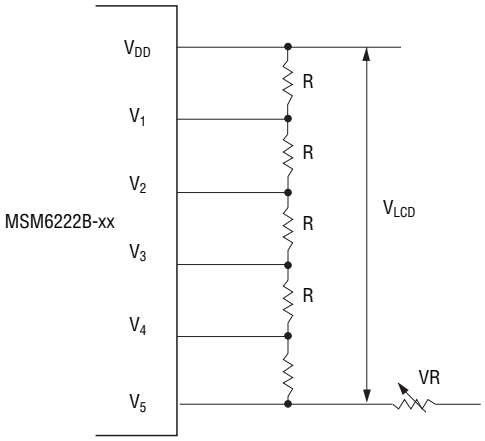


Figure 8

• Bias voltage circuit (1-line display mode)

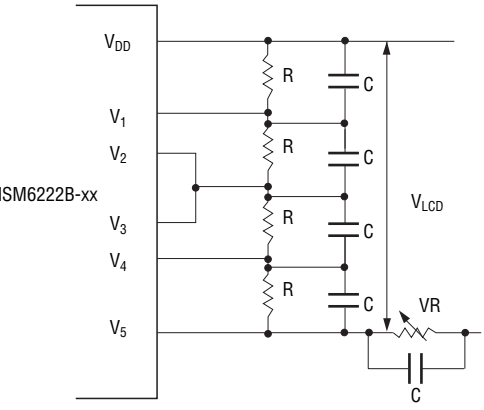


Figure 9

• Bias voltage circuit (2-line display mode)

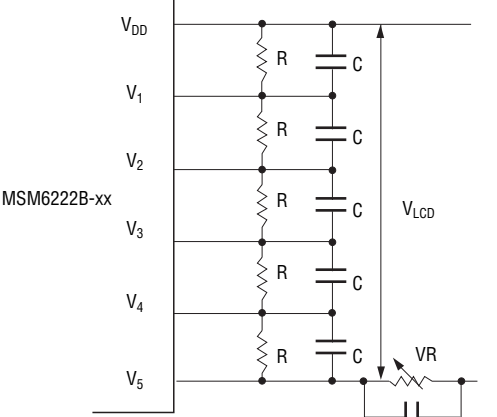


Figure 10

(V_{LCD} : LCD driving voltage)

• Application circuit

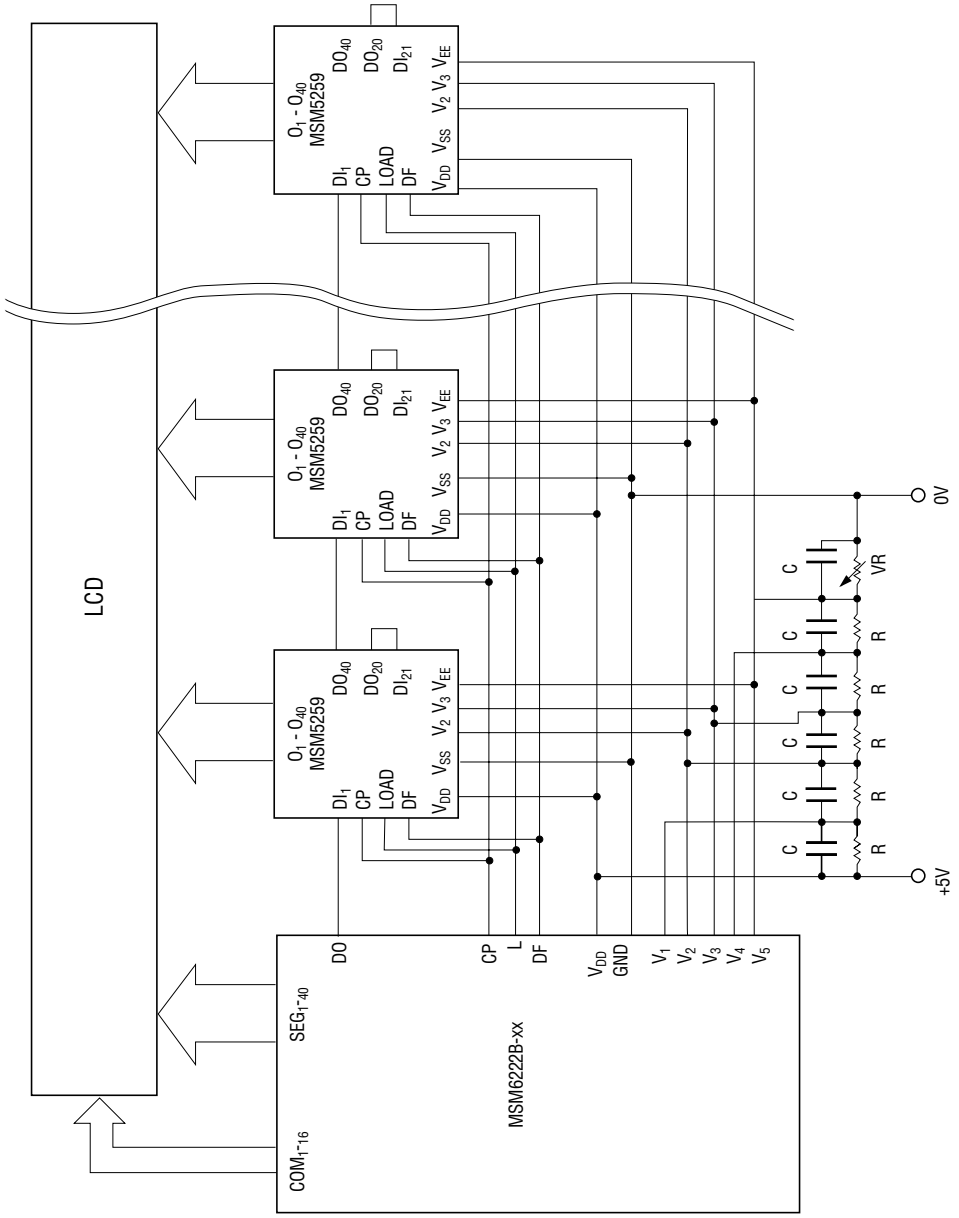


Figure 11

LCD Drive Waveforms

Figures 12, 13 and 14 show the LCD driving waveforms consisting of COM signal, SEG signal, DF signal and L (latch pulse waveform) signal, in the duty of 1/8, 1/11 and 1/16 respectively. The relation between duty and frame frequency is described in the table below.

Duty	Frame frequency
1/8	78.1 Hz
1/11	56.8 Hz
1/16	78.1 Hz

(Note) The OSC oscillation frequency is assumed to be 250 kHz.

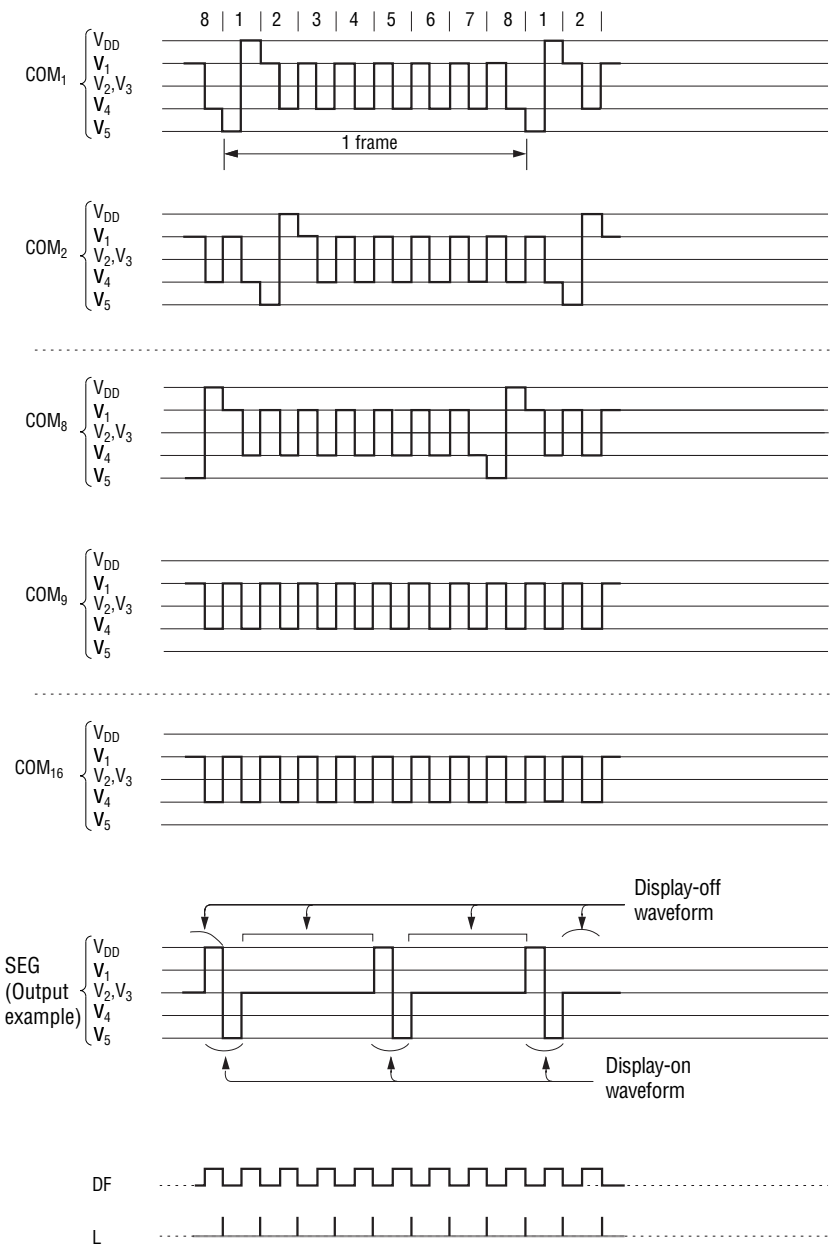


Figure 12. LCD Driving Waveform at 1/8 Duty

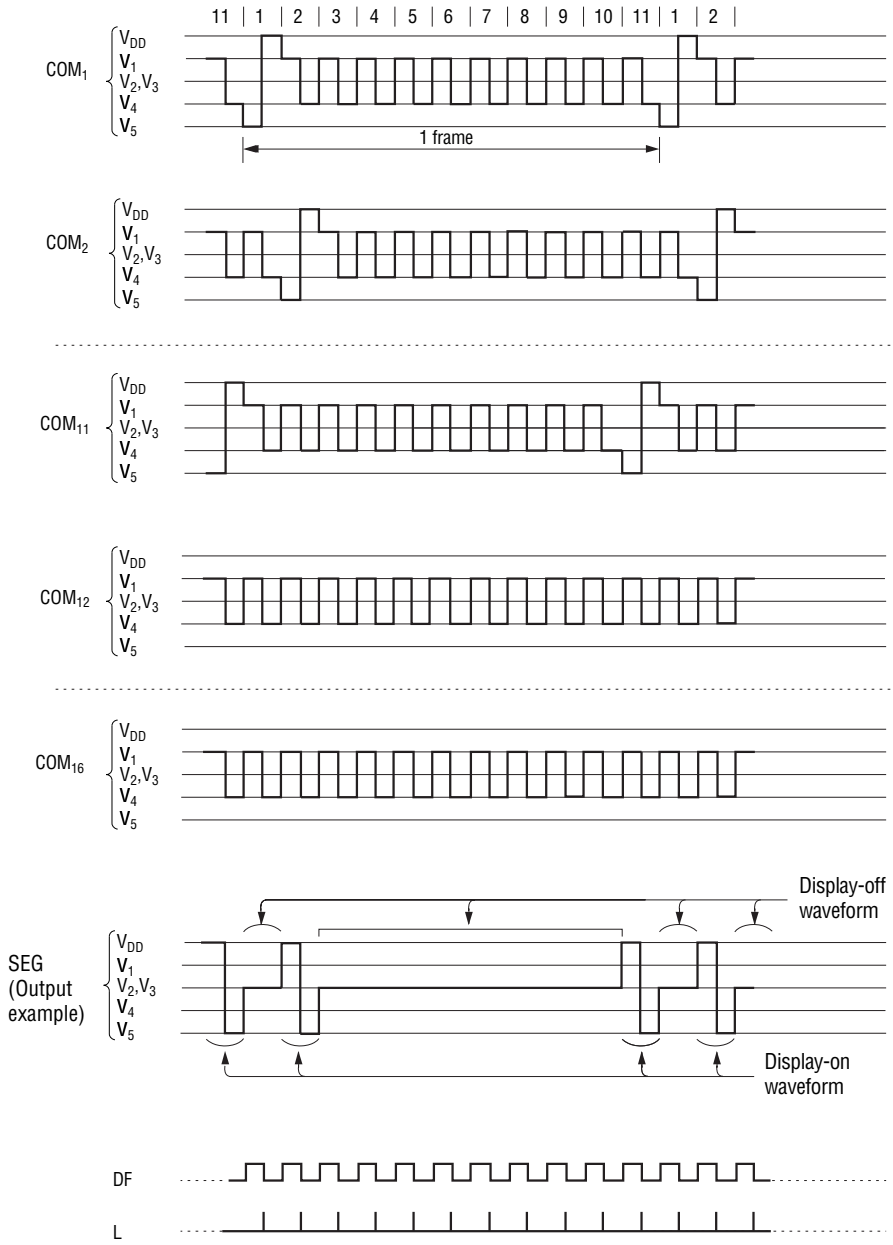


Figure 13. LCD Driving Waveform at 1/11 Duty

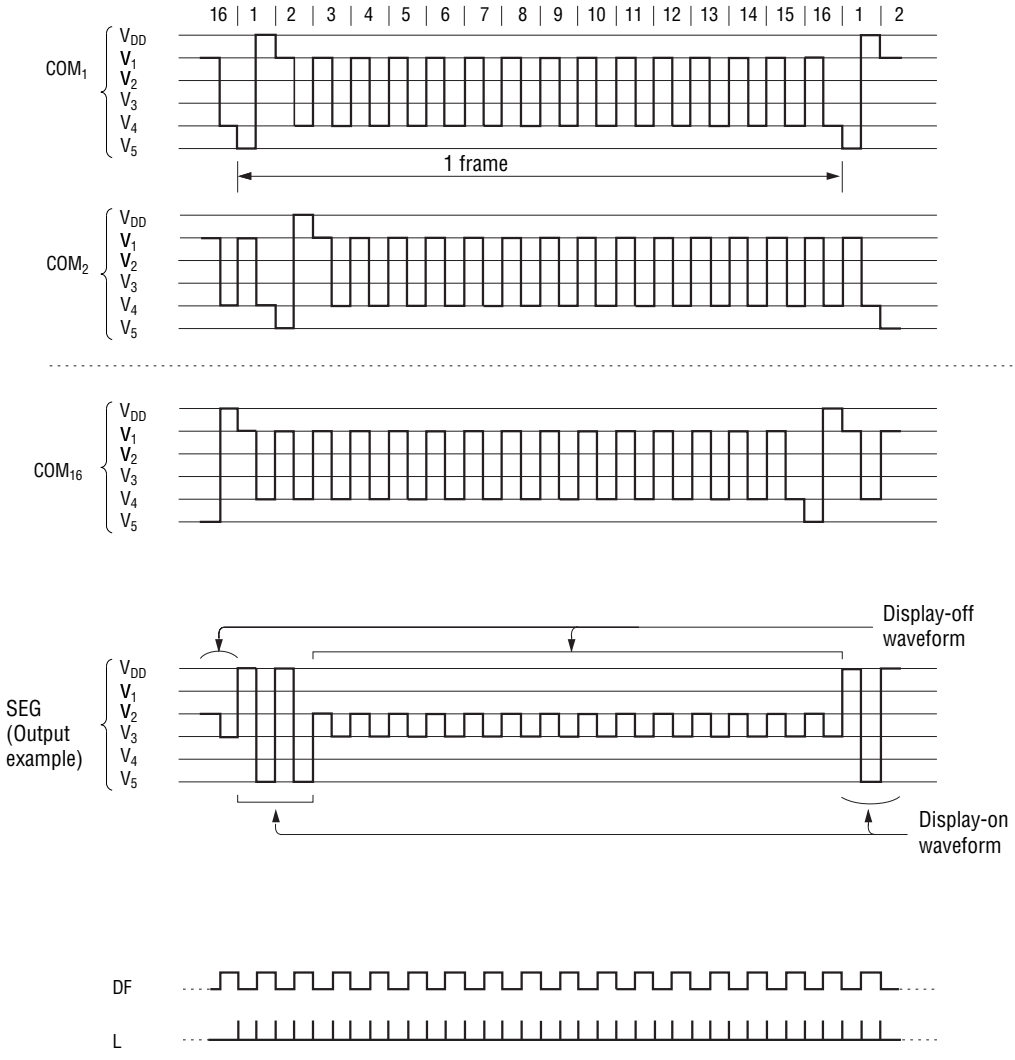


Figure 14. LCD Driving Waveform at 1/16 Duty

Initial Setting of Instruction

(1) When data input/output to and from the CPU is carried out by 8 bits (DB_0 to DB_7):

① Turn on the power.
② Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
③ Set 8B/4B at "H" by initial setting of instruction.
④ Wait for 4.1 ms or more.
⑤ Set 8B/4B at "H" by initial setting of instruction.
⑥ Wait for 100 µs or more.
⑦ Set 8B/4B at "H" by initial setting of instruction.
⑧ Check the busy flag as No Busy.
⑨ Set 8B/4B at "H". Set LCD line number (N) and character font (F).
(After this, do not change the LCD line number and character font.)
⑩ Check No Busy.
⑪ Clear the display by setting the display mode.
⑫ Check No Busy.
⑬ Clear the display.
⑭ Check No Busy.
⑮ Set the shift mode.
⑯ Check No Busy.
⑰ Initial setting completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
L	L	L	L	H	H	X	X	X	X

X : Don't Care

(2) When data input/output to and from the CPU is carried out by 4 bits (DB_4 to DB_7):

① Turn on the power.
② Wait for 15 ms or more after V_{DD} has reached 4.5V or more.
③ Set 8B/4B at "H" by initial setting of instruction.
④ Wait for 4.1 ms or more.
⑤ Set 8B/4B at "H" by initial setting of instruction.
⑥ Wait for 100 µs or more.
⑦ Set 8B/4B at "H" by initial setting of instruction.
⑧ Check the busy flag as No Busy.
⑨ Set 8B/4B at "L". Set LCD line number (N) and character font (F).
⑩ Wait for 100 µs or more.
⑪ Set 8B/4B at "L". Set LCD line number (N) and character font (F).
⑫ Check No Busy.
⑬ Clear the display by setting the display mode.
⑭ Check No Busy.
⑮ Clear the display.
⑯ Check No Busy.
⑰ Set the shift mode.
⑱ Check No Busy.
⑲ Initialization completed.

Example of Instruction Code for Steps ③, ⑤, and ⑦.

R/W	RS	DB_7	DB_6	DB_5	DB_4
L	L	L	L	H	H

Example of Instruction Code for Step ⑧.

R/W	RS	DB_7	DB_6	DB_5	DB_4
H	L	BF	O_6	O_5	Q_4

Example of Instruction Code for Step ⑨.

R/W	RS	DB_7	DB_6	DB_5	DB_4
L	L	L	L	H	L

Execute two-step accesses in 4 bits from Step ⑪ to Step ⑱.

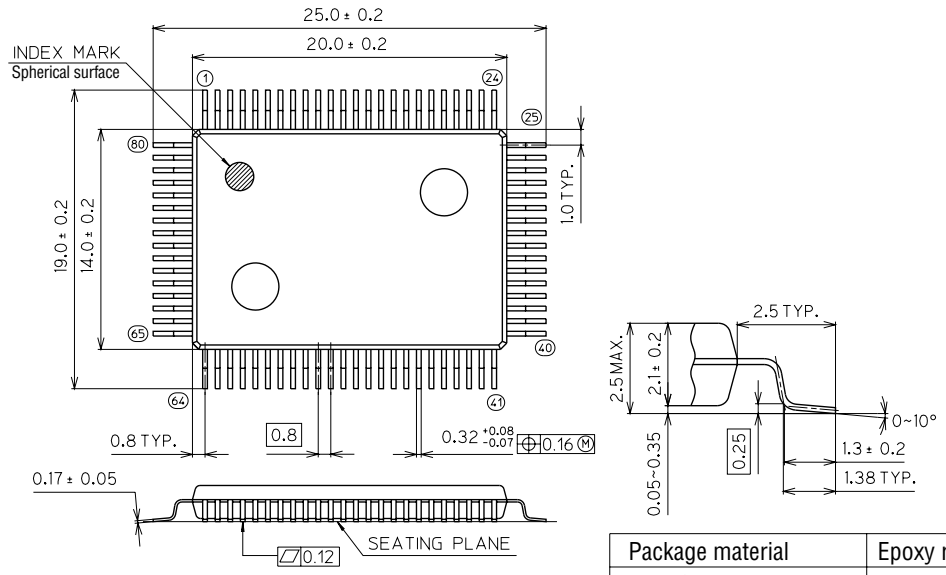
Differences Between HD44780 and MSM6222B-xx

Item	HD44780	MSM6222B - xx
LCD driving voltage (V_{LCD}) 1/4 bias 1/5 bias	 3.0 to 11.0 (V) 4.6 to 11.0 (V)	 3.0 to 8.0 (V) 3.0 to 8.0 (V)
Bus interface speed with CPU	1 MHz (1000 ns)	1.5 MHz (667 ns) Since signal rise/fall time is quite fast, the electromagnetic induction between lines of the PCB and the cable assignment should be noted.
The increment and decrement of the address counter in writing/ reading the data to/from the CGRAM/DDRAM.	The address counter is incremented or decremented 6 μsec (when f_{OSC} = 250 KHz) after the busy condition is released. (Period of busy condition is 40 μs) So, the data cannot be written into/ read out from the RAM for 6 μsec after the busy condition was over.	The address counter is incremented or decremented during the busy condition. So, data can be written into/read out from the RAM immediately after the busy condition was over.
The repeated input frequency (oscillation frequency=250kHz) of display clear instruction	610 Hz or less (1.64 ms or more)	78 Hz or less in 5×7 dots (12.8 ms or more), 56Hz or less in 5×10 dots (17.9 ms or more)

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-L



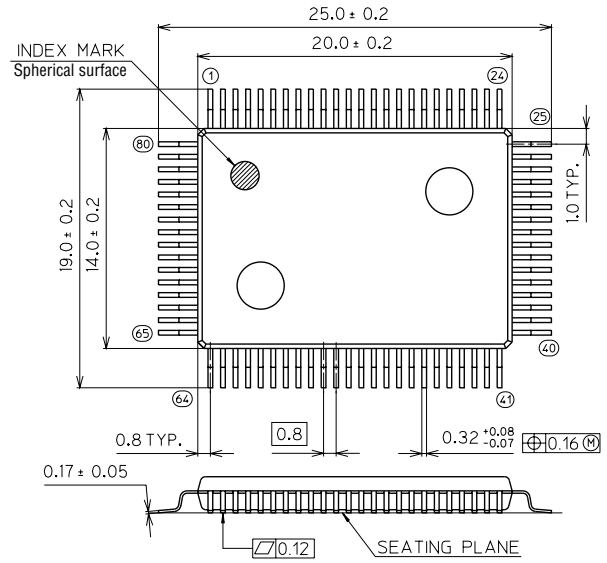
Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

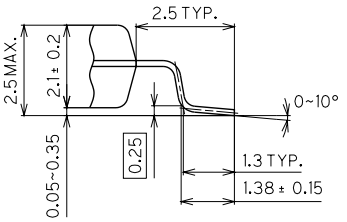
Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

(Unit : mm)

QFP80-P-1420-0.80-BL





Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

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