

### 32 x 32 Video Crosspoint

The ISL59532 is a 32 x 32 integrated video crosspoint switch matrix with input and output buffers and On-Screen Display (OSD) insertion. The ISL59532 is ideal for routing video signals in security and video-on-demand systems. This device operates from a single +5V supply. Any output can be switched to any of the 32 input video signal sources. OSD information can be inserted into any output through an internal, dedicated fast 2:1 mux (15ns switching times) located before the output buffer. Also, any input can be broadcast to all 32 outputs. Each output can be tri-stated and its gain set to +1 or +2.

The ISL59532 offers a -3dB signal bandwidth of 320MHz. The differential gain and differential phase of 0.025%, along with 0.1dB flatness out to 50MHz, make the ISL59532 suitable for many video applications.

The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible three-wire serial interface. The ISL59532 interface is set up to facilitate both fast updates and initialization. On power-up, all outputs are initialized in the disabled state to avoid output conflicts within the user system. For capacitor-coupled applications, the inputs include a clamp circuit that restores the input level to an externally applied reference.

The ISL59532 is available in a 356 Ld BGA package and specified over an extended -40°C to +85°C temperature range.

The ISL59532 has single-supply signal operation. It can accommodate voltages from 0V to 3.5V at the inputs and 0V to 4V at the outputs. It also has an input clamp with external group reference that can be used for AC-coupled applications.

A fully differential input version of this device is also available, ISL59533.

### Features

- 32 x 32 non-blocking switch with buffered inputs and outputs
- Operates from a single +5V supply
- Output gain switchable x1 or x2
- SPI digital interface
- Tri-state output
- -90dB Isolation at 6MHz
- 0.025%/0.05° dG/dP
- Pb-free plus anneal available (RoHS compliant)

### Applications

- Security camera switching
- RGB routing
- HDTV routing

### Ordering Information

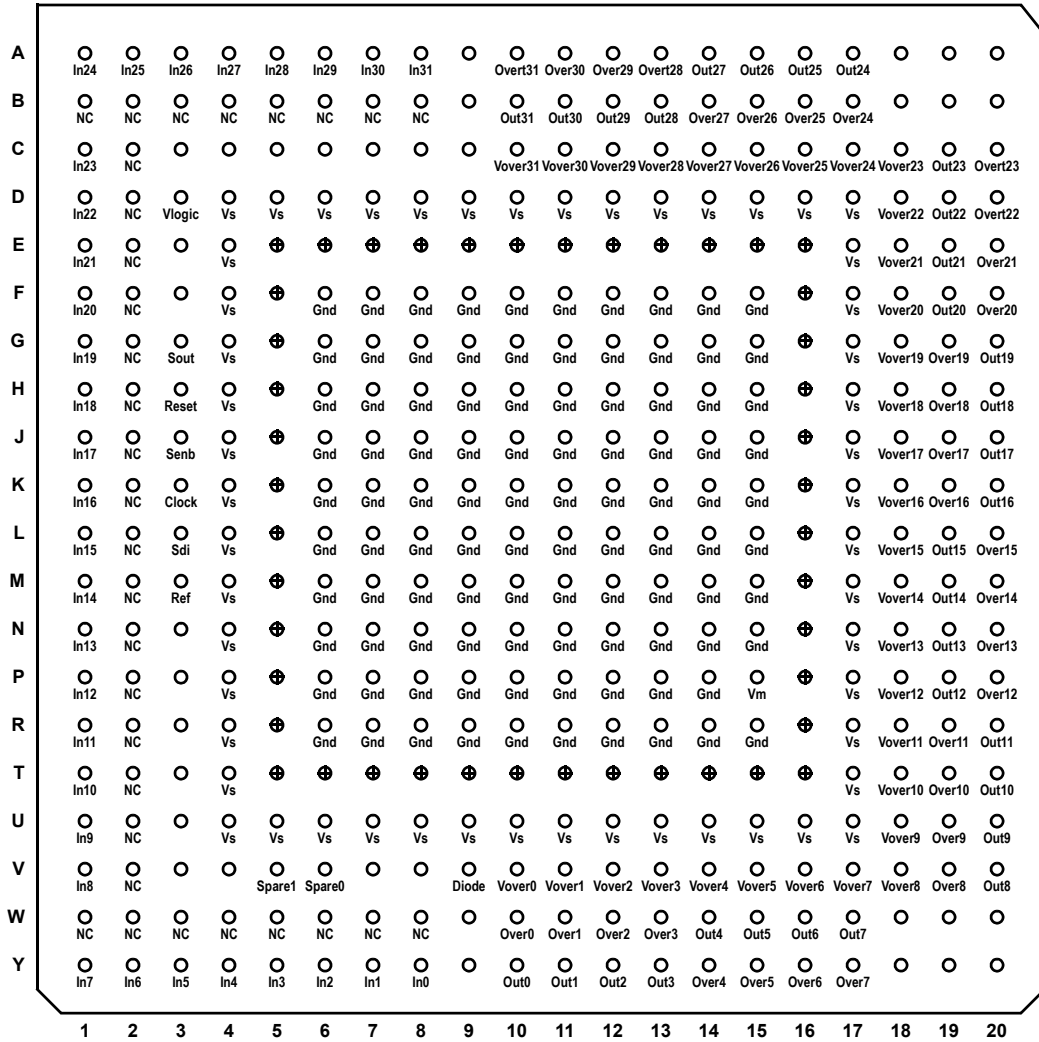
PART NUMBER	TAPE & REEL	PACKAGE	PKG. DWG. #
ISL59532IKEZ (See Note)	-	356 Ld BGA (Pb-free)	V356.27x27A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

# ISL59532

## Pinout

### ISL59532 (356 LD BGA) TOP VIEW



⊕ = NO BALLS

PAD NAME "GND" IS THE SAME AS PACKAGE OR BALL NAME "GROUND" OR "G"

PAD NAME "VS" IS THE SAME AS PACKAGE OR BALL NAME "POWER" OR "P"

PAD X, Y IS FROM PAD CENTER

ALL PADS ARE 70µ x 70µ

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Supply Voltage between $V_S$ and GND	5.5V	Maximum Die Temperature	+125°C
Maximum Continuous Output Current	40mA	Storage Temperature	-65°C to +150°C
Ambient Operating Temperature	-40°C to +85°C		

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**DC Electrical Specifications**  $V_S = 5V$

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
$V_S$	Supply Range		4.5		5.5	V
$V_D$	Digital Supply	Establishes serial output high level	1.2		5.5	V
$A_V$	Gain	$A_V = 1, R_L = 500\Omega$	0.97	1	1.03	V/V
		$A_V = 2, R_L = 150\Omega$	1.94	2	2.06	V/V
GM	Gain Matching (to average of all other outputs)	$A_V = 1$	-1.5	1	1.5	%
		$A_V = 2$		0.5	1.0	%
$V_{IN}$	Input Voltage Range	$A_V = 1$	0		3.5	V
$V_{OUT}$	Output Voltage Range	$A_V = 2, R_L = 150\Omega$	0		4.0	V
$I_B$	Input Bias Current	Clamp off	-10	-5	0	$\mu\text{A}$
		Clamp enabled, $V_{IN} = V_{REF} + 0.5V$	-10	-7	-5	$\mu\text{A}$
$V_{OS}$	Output Offset Voltage	$A_V = 1$	-25	0	25	mV
		$A_V = 2$	-70	0	70	mV
$I_{OUT}$	Output Current	Sourcing, $R_L = 10\Omega$ to GND	60	100		mA
		Sinking, $R_L$ to 2.5V	25	35		mA
PSRR	Power Supply Rejection Ratio			80		dB
$I_S$	Supply Current	Enabled, no load current		600	700	mA
		Disabled		1.6	2.2	mA

**AC Electrical Specifications**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
BW -3dB	3dB Bandwidth	$V_{OUT} = 200mV_{P-P}, A_V = 2$		320		MHz
BW 0.1dB	0.1dB Bandwidth	$V_{OUT} = 200mV_{P-P}, A_V = 2$		50		MHz
SR	Slew Rate	$V_{OUT} = 2V_{P-P}, A_V = 2$	360	520		V/ $\mu\text{s}$
$T_S$	Settling Time to 0.1%	$V_{OUT} = 2V_{P-P}, A_V = 2$		12		ns
Glitch	Switching Glitch, Peak	$A_V = 1$		40		mV
$T_{over}$	Overlay Delay Time	Beginning of output transition		6		ns
dG	Diff Gain	$A_V = 2, R_L = 150\Omega$		0.025		%
dP	Diff Phase	$A_V = 2, R_L = 150\Omega$		0.05		°
Xt	Hostile Crosstalk	6MHz		-85		dB
$V_N$	Input Noise Voltage			18		nV/ $\sqrt{\text{Hz}}$

**Pin Descriptions**

NAME	NUMBER	DESCRIPTION
IN4	Y4	Input
IN5	Y3	Input
IN6	Y2	Input
IN7	Y1	Input
REF	M3	Clamp reference input
GND	GND	Ground
SDI	L3	Serial data input
VS	VS	Power supply
IN8	V1	Input
IN9	U1	Input
IN10	T1	Input
IN11	R1	Input
VS	VS	Power supply
GND	GND	Ground
IN12	P1	Input
IN13	N1	Input
IN14	M1	Input
IN15	L1	Input
SCLK	K3	Serial data clock
VS	VS	Power supply
$\overline{\text{ENA}}$	J3	Serial enable-inverted
GND	GND	Ground
IN16	K1	Input
IN17	J1	Input
IN18	H1	Input
IN19	G1	Input
VS	VS	Power supply
GND	GND	Ground
IN20	F1	Input
IN21	E1	Input
IN22	D1	Input
IN23	C1	Input
RESET	H3	Reset input
VS	VS	Power supply
SDO	G3	Serial data output
GND	GND	Ground
IN24	A1	Input
IN25	A2	Input
IN26	A3	Input

**Pin Descriptions (Continued)**

NAME	NUMBER	DESCRIPTION
IN27	A4	Input
$\overline{\text{INPUTTEST}}$	NONE	Manufacturing test pin - leave open
GND	GND	Ground
GND	GND	Ground
VS	VS	Power supply
VS	VS	Power supply
VLOGIC	D3	Logic power supply for serial output driver
IN28	A5	Input
IN29	A6	Input
IN30	A7	Input
IN31	A8	Input
VSL	VS	Power supply
VGL	GND	Ground
VS	VS	Power supply
GND	GND	Ground
OVER31	A10	Overlay logic control
VOVER31	C10	Overlay analog input
OUT31	B10	Output
OVER30	A11	Overlay logic control
VOVER30	C11	Overlay analog input
OUT30	B11	Output
OVER29	A12	Overlay logic control
VOVER29	C12	Overlay analog input
OUT29	B12	Output
OVER28	A13	Overlay logic control
VOVER28	C13	Overlay analog input
OUT28	B13	Output
GND	GND	Ground
VS	VS	Power supply
OUT27	A14	Output
VOVER27	C14	Overlay analog input
OVER27	B14	Overlay logic control
OUT26	A15	Output
VOVER26	C15	Overlay analog input
OVER26	B15	Overlay logic control
OUT25	A16	Output
VOVER25	C16	Overlay analog input
OVER25	B16	Overlay logic control
OUT24	A17	Output

**Pin Descriptions** (Continued)

NAME	NUMBER	DESCRIPTION
VOVER24	C17	Overlay analog input
OVER24	B17	Overlay logic control
GND	GND	Ground
OUTTEST3	NONE	Manufacturing test pin-leave open
VS	VS	Power supply
OVER23	C20	Overlay logic control
VOVER23	C18	Overlay analog input
OUT23	C19	Output
OVER22	D20	Overlay logic control
VOVER22	D18	Overlay analog input
OUT22	D19	Output
OVER21	E20	Overlay logic control
VOVER21	E18	Overlay analog input
OUT21	E19	Output
OVER20	F20	Overlay logic control
VOVER20	F18	Overlay analog input
OUT20	F19	Output
GND	GND	Ground
VS	VS	Power supply
OUT19	G20	Output
VOVER19	G18	Overlay analog input
OVER19	G19	Overlay logic control
OUT18	H20	Output
VOVER18	H18	Overlay analog input
OVER18	H19	Overlay logic control
OUT17	J20	Output
VOVER17	J18	Overlay analog input
OVER17	J19	Overlay logic control
OUT16	K20	Output
VOVER16	K18	Overlay analog input
OVER16	K19	Overlay logic control
OUTTEST2	NONE	Manufacturing test pin-leave open
GND	GND	Ground
VS	VS	Power supply
OVER15	L20	Overlay logic control
VOVER15	L18	Overlay analog input
OUT15	L19	Output
OVER14	M20	Overlay logic control
VOVER14	M18	Overlay analog input
OUT14	M19	Output

**Pin Descriptions** (Continued)

NAME	NUMBER	DESCRIPTION
OVER13	N20	Overlay logic control
VOVER13	N18	Overlay analog input
OUT13	N19	Output
OVER12	P20	Overlay logic control
VOVER12	P18	Overlay analog input
OUT12	P19	Output
GND	GND	Ground
VS	VS	Power supply
OUT11	R20	Output
VOVER11	R18	Overlay analog input
OVER11	R19	Overlay logic control
OUT10	T20	Output
VOVER10	T18	Overlay analog input
OVER10	T19	Overlay logic control
OUT9	U20	Output
VOVER9	U18	Overlay analog input
OVER9	U19	Overlay logic control
OUT8	V20	Output
VOVER8	V18	Overlay analog input
OVER8	V19	Overlay logic control
VS	VS	Power supply
OUTTEST1	NONE	Manufacturing test pin-leave open
GND	GND	Ground
OVER7	Y17	Overlay logic control
VOVER7	V17	Overlay analog input
OUT7	W17	Output
OVER6	Y16	Overlay logic control
VOVER6	V16	Overlay analog input
OUT6	W16	Output
OVER5	Y15	Overlay logic control
VOVER5	V15	Overlay analog input
OUT5	W15	Output
OVER4	Y14	Overlay logic control
VOVER4	V14	Overlay analog input
OUT4	W14	Output
VS	VS	Power supply
GND	GND	Ground
OUT3	Y13	Output
VOVER3	V13	Overlay analog input
OVER3	W13	Overlay logic control

**Pin Descriptions** (Continued)

NAME	NUMBER	DESCRIPTION
OUT2	Y12	Output
VOVER2	V12	Overlay analog input
OVER2	W12	Overlay logic control
OUT1	Y11	Output
VOVER1	V11	Overlay analog input
OVER1	W11	Overlay logic control
OUT0	Y10	Output
VOVER0	V10	Overlay analog input
OVER0	W10	Overlay logic control
VS	VS	Power supply
OUTTEST0	NONE	Manufacturing test pin-leave open
GND	GND	Ground
IN0	Y8	Input
IN1	Y7	Input
IN2	Y6	Input
IN3	Y5	Input
DIODE	V9	Anode of a ground-connected diode: useful for measuring die temperature
VS	VS	Power supply
GND	GND	Ground
VS	VS	Power supply
GND	GND	Ground
SPARE0	V6	Not assigned-do not connect
SPARE1	V5	Not assigned-do not connect
INPUTTEST BUS	NONE	Manufacturing test pin-leave open

Typical Performance Curves

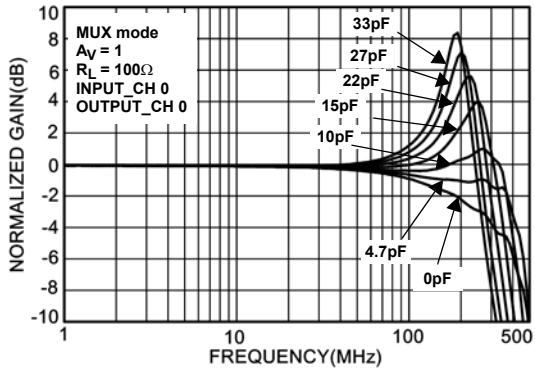


FIGURE 1. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 1$ , MUX MODE

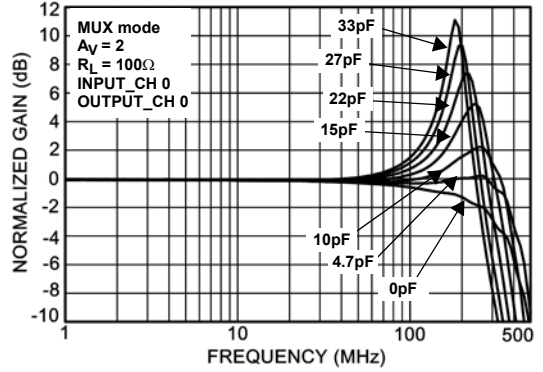


FIGURE 2. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 2$ , MUX MODE

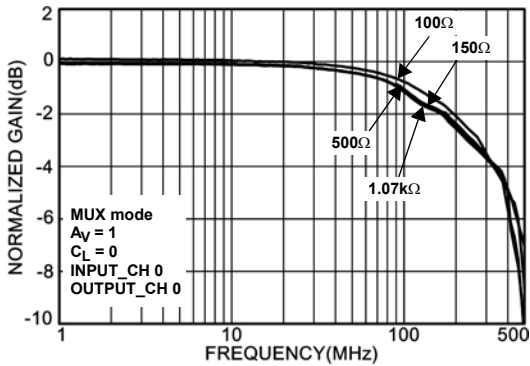


FIGURE 3. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 1$ , MUX MODE

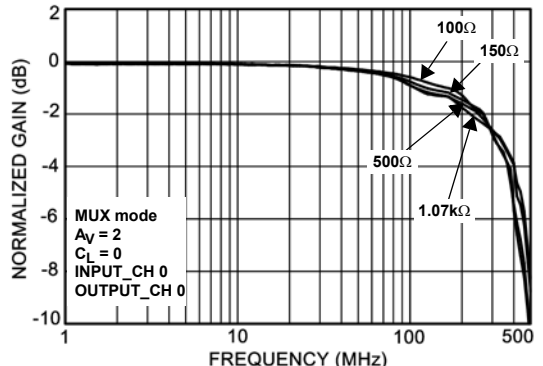


FIGURE 4. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 2$ , MUX MODE

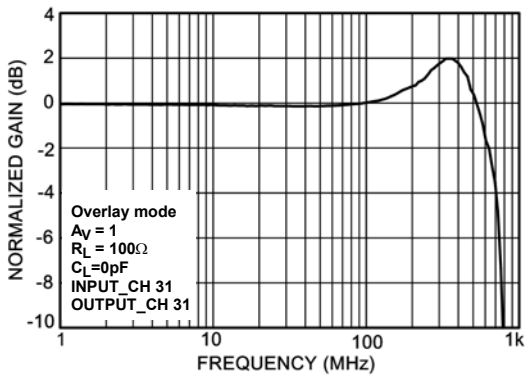


FIGURE 5. FREQUENCY RESPONSE - OVERLAY INPUT,  $A_V = 1$

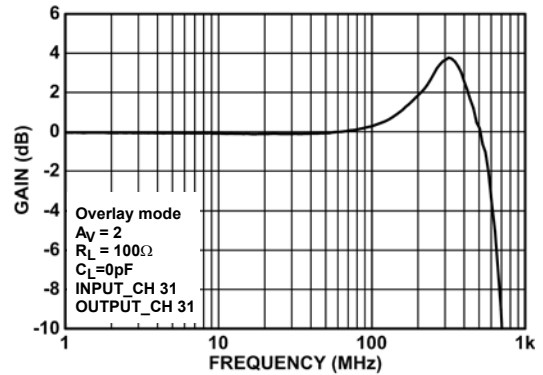


FIGURE 6. FREQUENCY RESPONSE - OVERLAY INPUT,  $A_V = 2$

Typical Performance Curves (Continued)

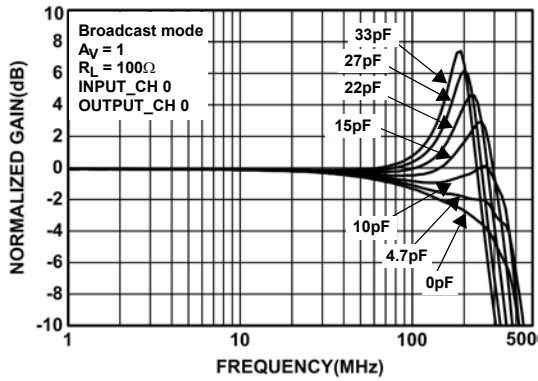


FIGURE 7. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 1$ , BROADCAST MODE

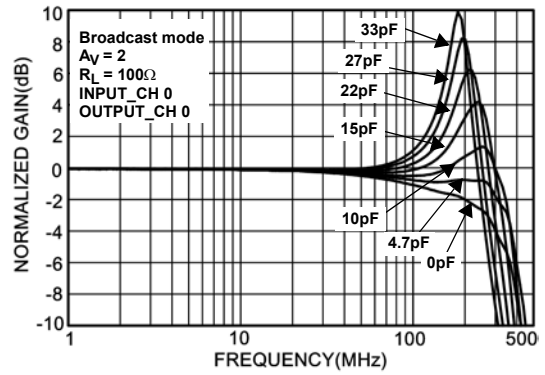


FIGURE 8. FREQUENCY RESPONSE - VARIOUS  $C_L$ ,  $A_V = 2$ , BROADCAST MODE

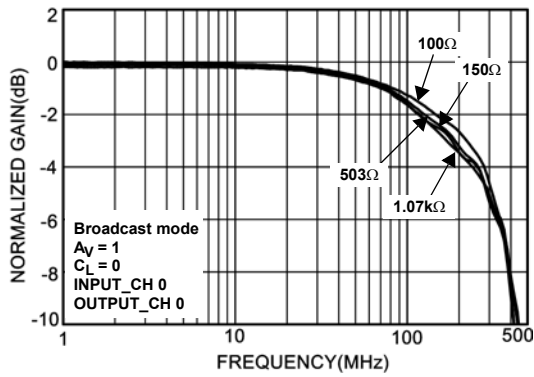


FIGURE 9A. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 1$ , BROADCAST MODE

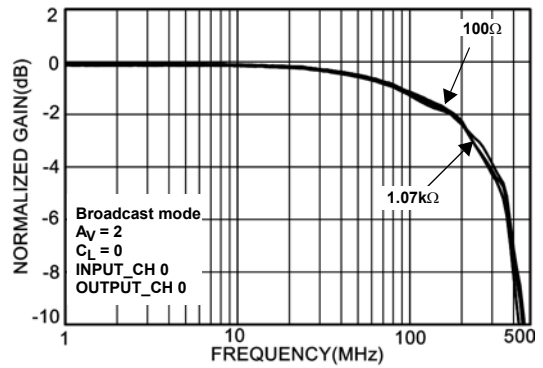


FIGURE 10. FREQUENCY RESPONSE - VARIOUS  $R_L$ ,  $A_V = 2$ , BROADCAST MODE

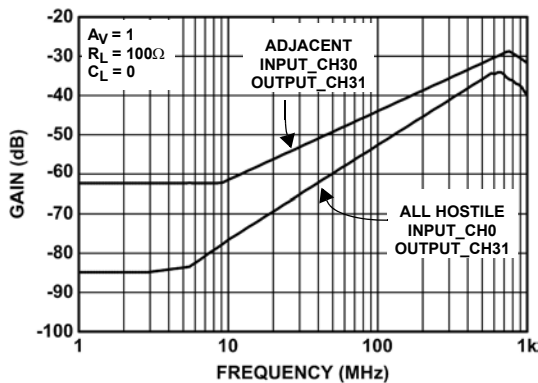


FIGURE 11. CROSSTALK -  $A_V = 1$

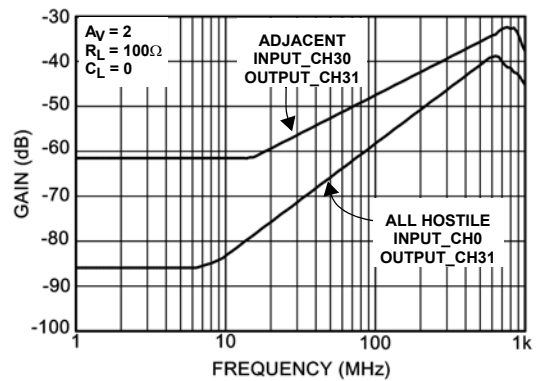


FIGURE 12. CROSSTALK -  $A_V = 2$



Typical Performance Curves (Continued)

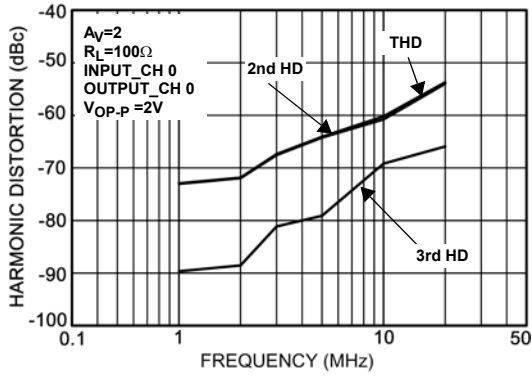


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

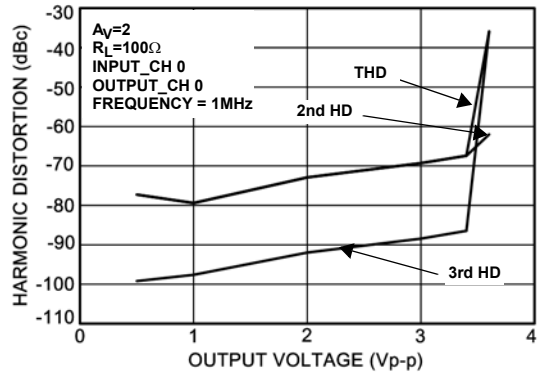


FIGURE 14. HARMONIC DISTORTION vs  $V_{OUT\_P\_P}$

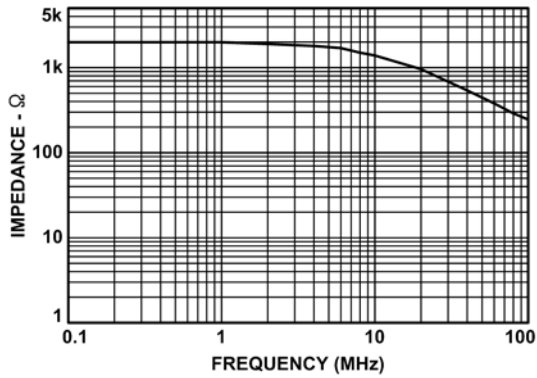


FIGURE 15. DISABLE OUTPUT IMPEDANCE

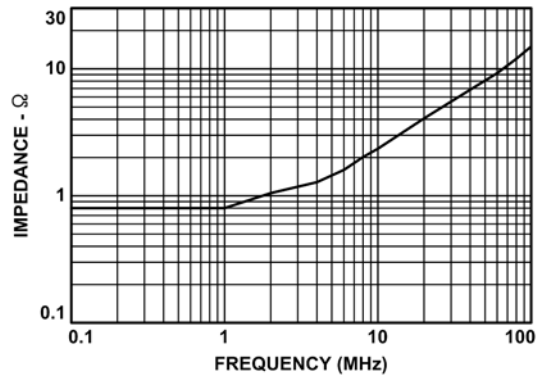


FIGURE 16. ENABLE OUTPUT IMPEDANCE

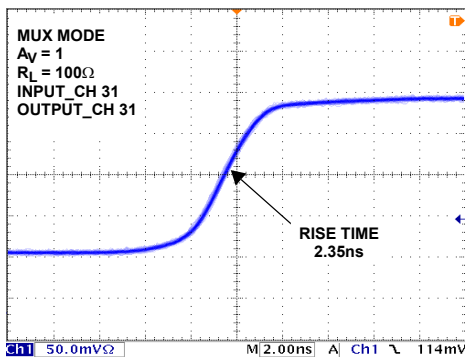


FIGURE 17. RISE TIME -  $A_V = 1$

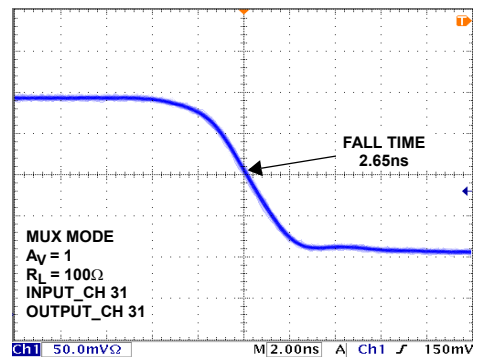


FIGURE 18. FALL TIME -  $A_V = 1$

Typical Performance Curves (Continued)

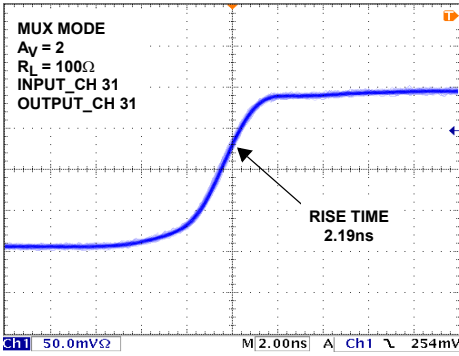


FIGURE 19. RISE TIME -  $A_V = 2$

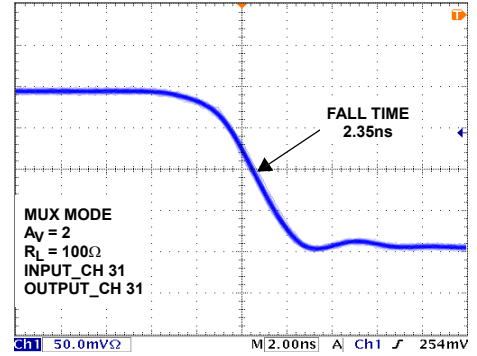


FIGURE 20. FALL TIME -  $A_V = 2$

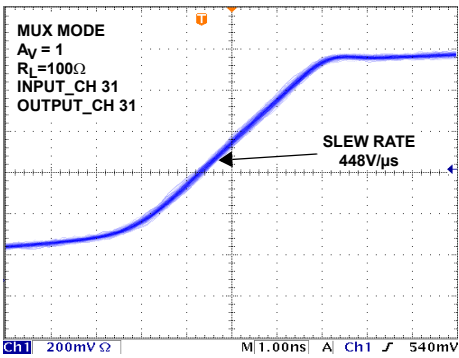


FIGURE 21. RISING SLEW RATE -  $A_V = 1$

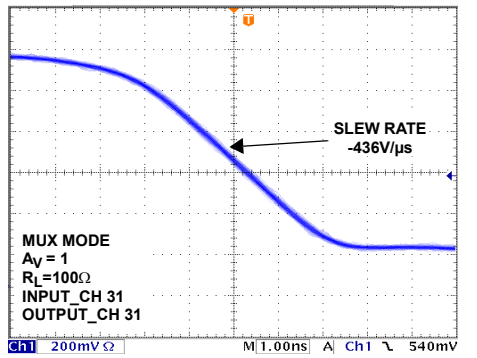


FIGURE 22. FALLING SLEW RATE -  $A_V = 1$

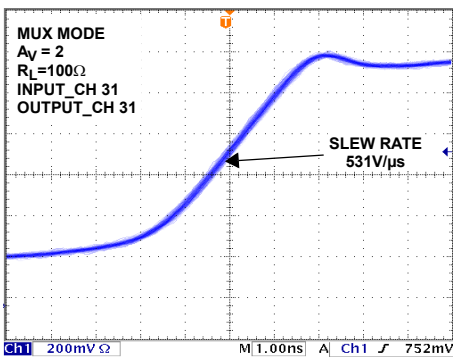


FIGURE 23. RISING SLEW RATE -  $A_V = 2$

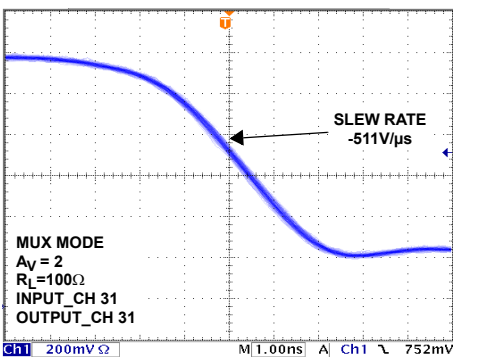


FIGURE 24. FALLING SLEW RATE -  $A_V = 2$

Typical Performance Curves (Continued)

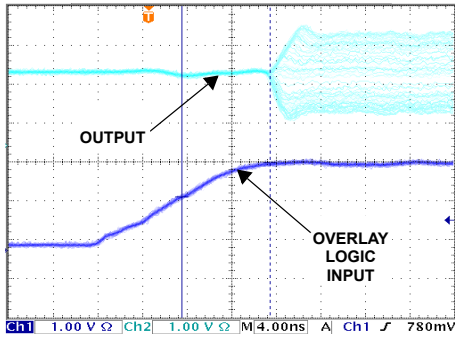


FIGURE 25. OVERLAY SWITCH TURN-ON DELAY TIME

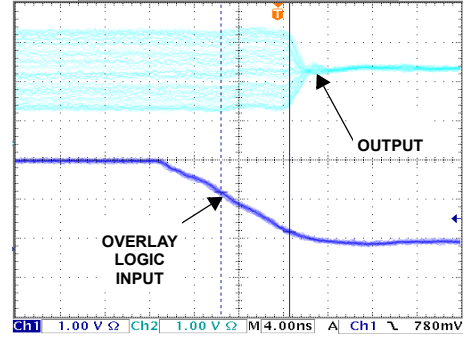


FIGURE 26. OVERLAY SWITCH TURN-OFF DELAY TIME

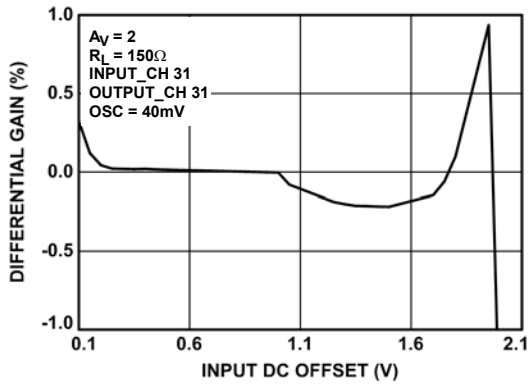


FIGURE 27. DIFFERENTIAL GAIN,  $A_V = 2$

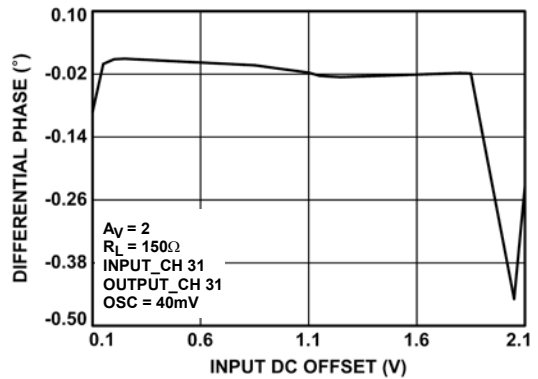


FIGURE 28. DIFFERENTIAL PHASE,  $A_V = 2$

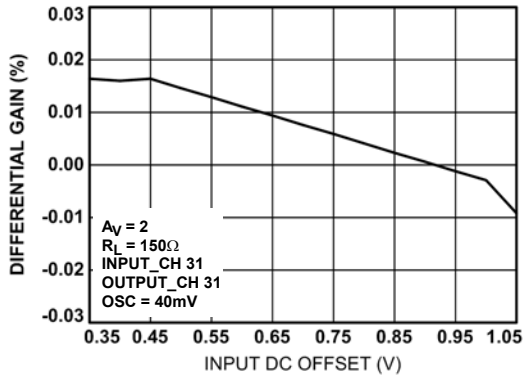


FIGURE 29. DIFFERENTIAL GAIN,  $A_V = 2$

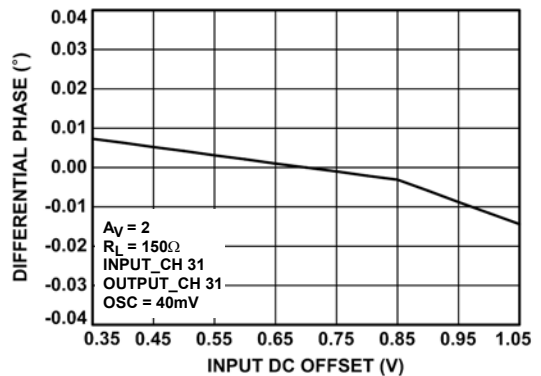


FIGURE 30. DIFFERENTIAL PHASE,  $A_V = 2$

Typical Performance Curves (Continued)

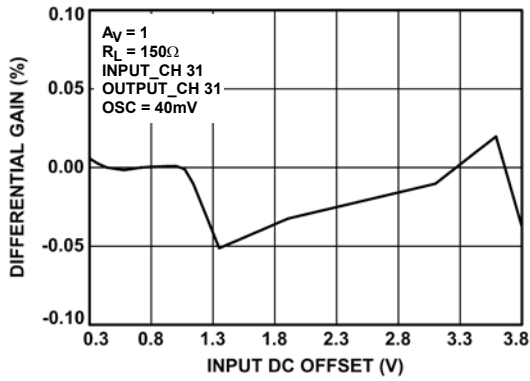


FIGURE 31. DIFFERENTIAL GAIN,  $A_V = 1$

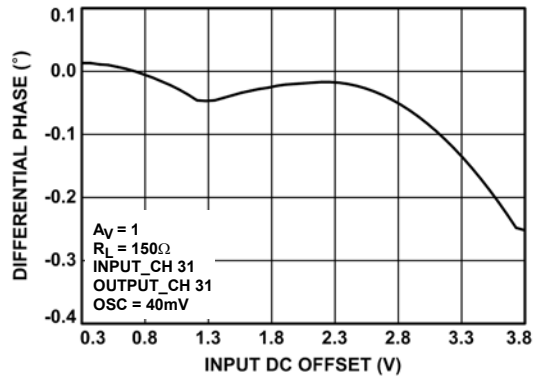


FIGURE 32. DIFFERENTIAL PHASE,  $A_V = 1$

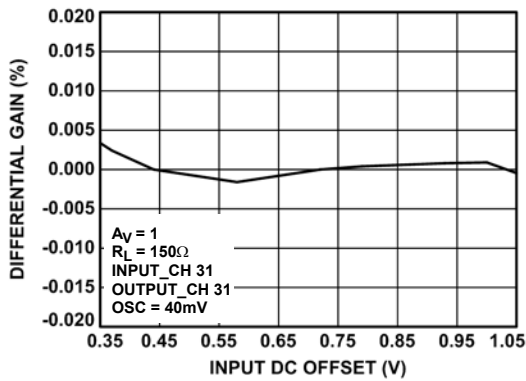


FIGURE 33. DIFFERENTIAL GAIN,  $A_V = 1$

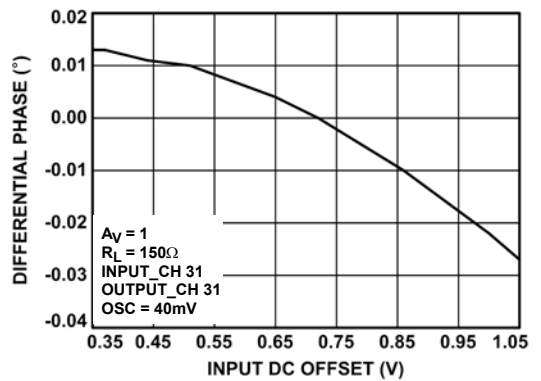


FIGURE 34. DIFFERENTIAL PHASE,  $A_V = 1$

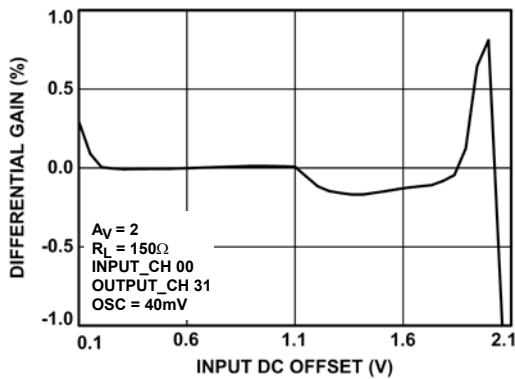


FIGURE 35. DIFFERENTIAL GAIN,  $A_V = 2$

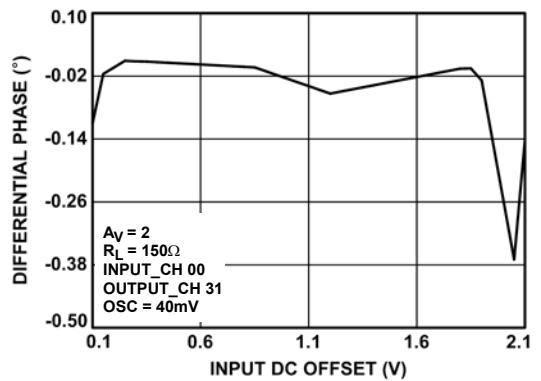


FIGURE 36. DIFFERENTIAL PHASE,  $A_V = 2$

Typical Performance Curves (Continued)

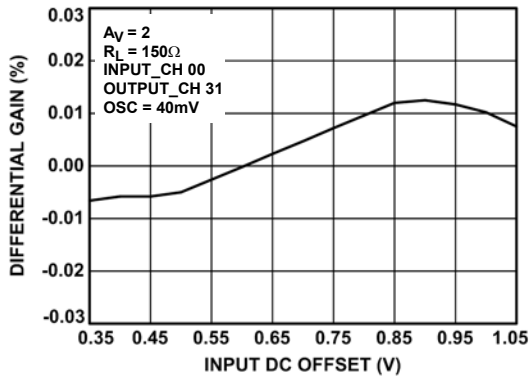


FIGURE 37. DIFFERENTIAL GAIN,  $A_V = 2$

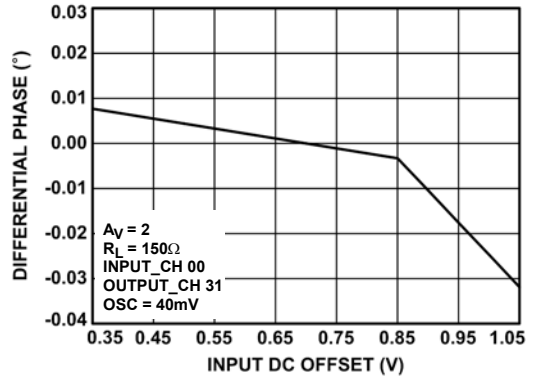


FIGURE 38. DIFFERENTIAL PHASE,  $A_V = 2$

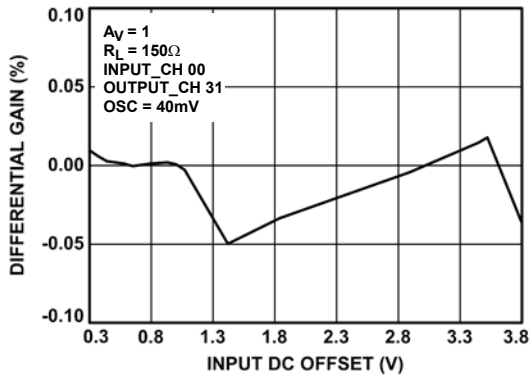


FIGURE 39. DIFFERENTIAL GAIN,  $A_V = 1$

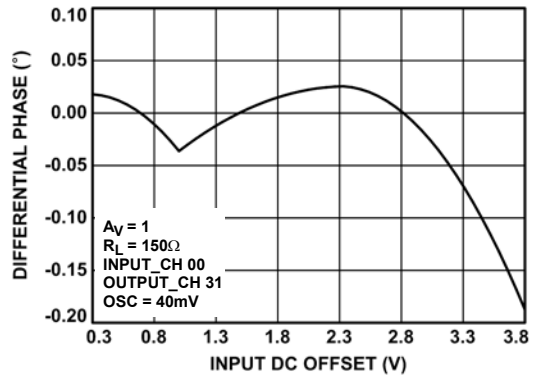


FIGURE 40. DIFFERENTIAL PHASE,  $A_V = 1$

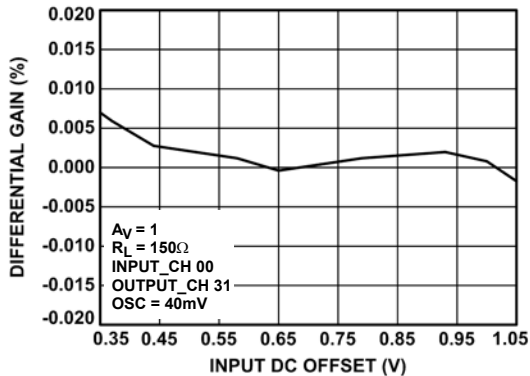


FIGURE 41. DIFFERENTIAL GAIN,  $A_V = 1$

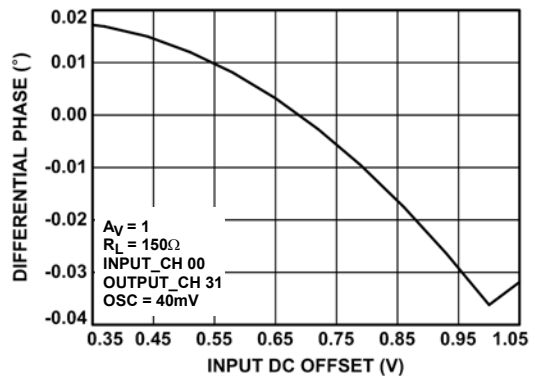


FIGURE 42. DIFFERENTIAL PHASE,  $A_V = 1$

Typical Performance Curves (Continued)

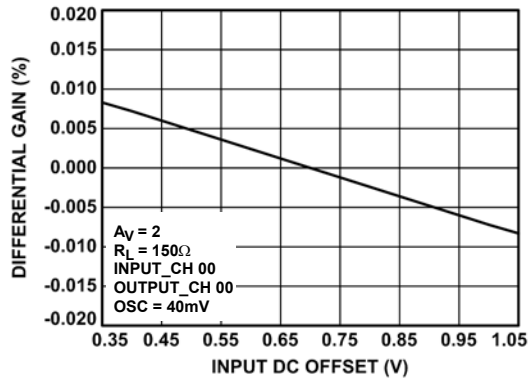


FIGURE 43. DIFFERENTIAL GAIN, OVERLAY,  $A_V = 2$

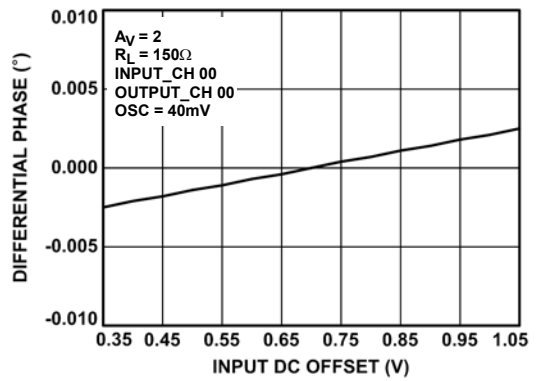


FIGURE 44. DIFFERENTIAL PHASE, OVERLAY,  $A_V = 2$

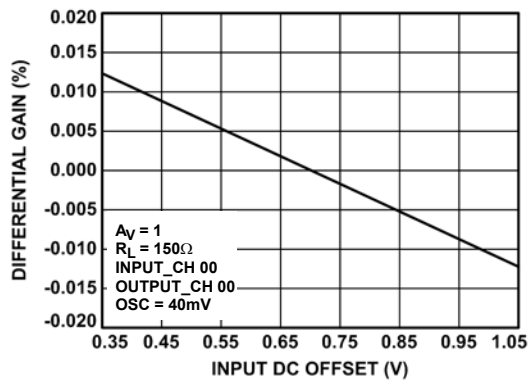


FIGURE 45. DIFFERENTIAL GAIN, OVERLAY,  $A_V = 1$

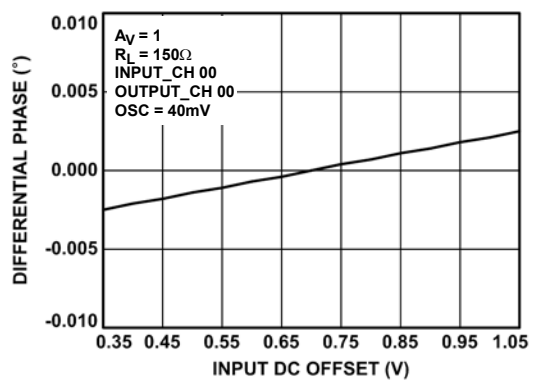


FIGURE 46. DIFFERENTIAL PHASE, OVERLAY,  $A_V = 1$



3dB Bandwidth, MUX Mode,  $A_V = 2$ ,  $R_L = 100\Omega$  [MHz]

		INPUT CHANNELS																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
OUTPUT CHANNELS	0	304				323					324					305					313					320						308		
	1		291																												290			
	2			290																										294				
	3				302																									295				
	4					353																						348						
	5	346					349										310											348				331		
	6							371																			370							
	7								372																	376								
	8									360																366								
	9										363														363									
	10	351										350					317										350					340		
	11												337																					
	12														348																			
	13															340																		
	14																327			341														
	15	360	353	348	349	366	360	366	363	280	366	357	360	348	348	343	337	348	352	358	353	356	364	372	366	173	364	367	368	348	354	352	352	
	16																	325	338															
	17																330			345														
	18																																	
	19														344																			
	20	351											350																				348	
	21												347																					
	22													371																				
	23																																	
	24																											334						
	25	354																300															353	
	26																																	
	27																																	
	28																																	
	29																																	318
	30																																	308
	31	311																																314



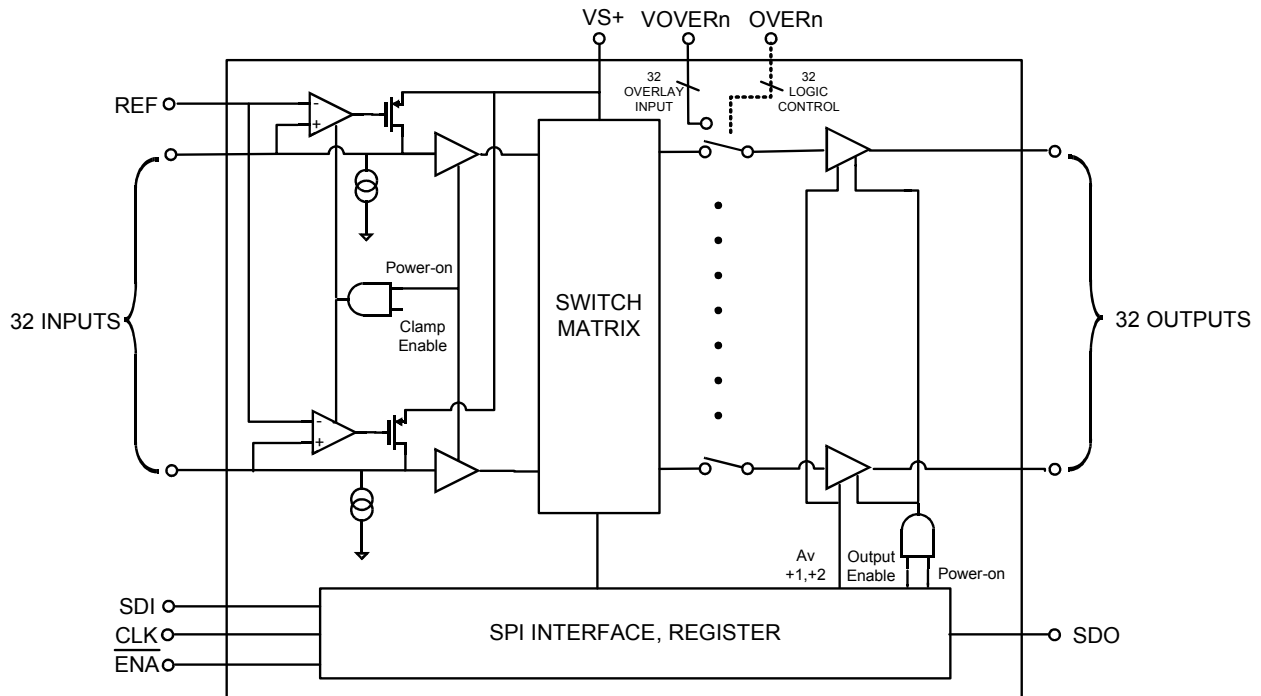
3dB Bandwidth, Broadcast Mode,  $A_V = 1$ ,  $R_L = 100\Omega$  [MHz]

		INPUT CHANNELS																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
OUTPUT CHANNELS	0	196	204	193	175	154	154	158	161	169	157	155	146	125	121	115	109	81	81	79	80	85	85	86	86	83	82	82	77	80	82	85	86	
	1	185	189														104															85	87	
	2	172		163													104															85	87	
	3	161			138												99													81			87	
	4	165				128											99												79				89	
	5	160					126										97												82				89	
	6	152						123									95											81					89	
	7	141							119								91										84						89	
	8	133								113							86									82							89	
	9	133									113						90											85					90	
	10	132										113					91																92	
	11	130											107				90																93	
	12	125												94			87																92	
	13	125													91		88				84												95	
	14	127														90	88		85														97	
	15	125	129	124	118	109	109	110	112	113	110	107	106	95	93	91	89	88	88	88	88	95	94	96	97	93	92	89	86	91	93	95	98	
	16	124															89	88																100
	17	119															85	85		86														100
	18	116													88		84				87												100	
	19	113																				88											100	
	20	114												97			84																102	
	21	112															99																103	
	22	108																94															102	
	23	107																															104	
	24	106																															106	
	25	107																															110	
	26	108																															114	
	27	107																															123	
	28	104																															115	
	29	104																															119	
	30	105	106																														118	125
31	107	110	108	103	98	98	98	99	101	99	97	95	87	86	84	81	113	112	112	114	126	126	128	129	124	118	114	111	120	122	129	131		

3dB Bandwidth, Broadcast Mode,  $A_V = 2$ ,  $R_L = 100\Omega$  [MHz]

		INPUT CHANNELS																																
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31		
OUTPUT CHANNELS	0	270	277	268	247	213	216	227	244	258	223	208	196	147	142	132	123	85	85	85	86	91	91	92	93	90	88	86	85	89	90	92	94	
	1	256	261													117																93	93	
	2	240		223												112															88		92	
	3	219			189											106														86			92	
	4	233				158										108													83				95	
	5	225					152									106												86					95	
	6	204						146								105											88						95	
	7	187							137							99										89							94	
	8	172								128						92									85								94	
	9	171									128					96								93									96	
	10	170										126				97							94										98	
	11	167											119			97						96											101	
	12	152												103		93					89												99	
	13	153													99	93			88														103	
	14	155														96	94		89														105	
	15	151	155	146	134	123	125	126	126	128	123	123	114	103	99	97	94	94	92	92	93	102	102	102	102	102	99	99	93	93	98	99	102	104
	16	146														93	94																	109
	17	138														91	91		92															109
	18	133													94	90			93															109
	19	127												95		90				94														109
	20	129											106			89						106												113
	21	126										106				86							105											114
	22	119									102					84								107										112
	23	118								105						83									106									114
	24	116							103							83										107								117
	25	118						103								84											107							125
	26	120					103									84												108						135
	27	118				103										85													108					142
	28	113			106											82														113				133
	29	114		110												81															123			143
	30	115	116													82																138		155
31	117	121	118	112	105	105	106	108	110	107	104	101	93	91	88	85	130	127	127	130	153	150	158	163	149	140	133	126	140	146	161	164		

## Block Diagram



### General Description

The ISL59532 is a 32 x 32 integrated video crosspoint switch matrix with input and output buffers and On-Screen Display (OSD) insertion. This device operates from a single +5V supply. Any output can be switched to any of the 32 input video signal sources and OSD information through an internal, dedicated fast 2:1 mux located before the output buffer. Also, any one input can be broadcast to all 32 outputs.

The ISL59532 offers a -3dB signal bandwidth of 320MHz. The differential gain and differential phase of 0.025% and 0.05° respectively, along with 0.1dB flatness out to 50MHz. The switch matrix configuration and output buffer gain are programmed through an SPI/QSPI™-compatible, three-wire serial interface. The ISL59532 interface is set up to facilitate both fast updates and initialization. On power-up, all facilities are initialized in the disabled state to avoid output conflicts within the user system.

### Digital Interface

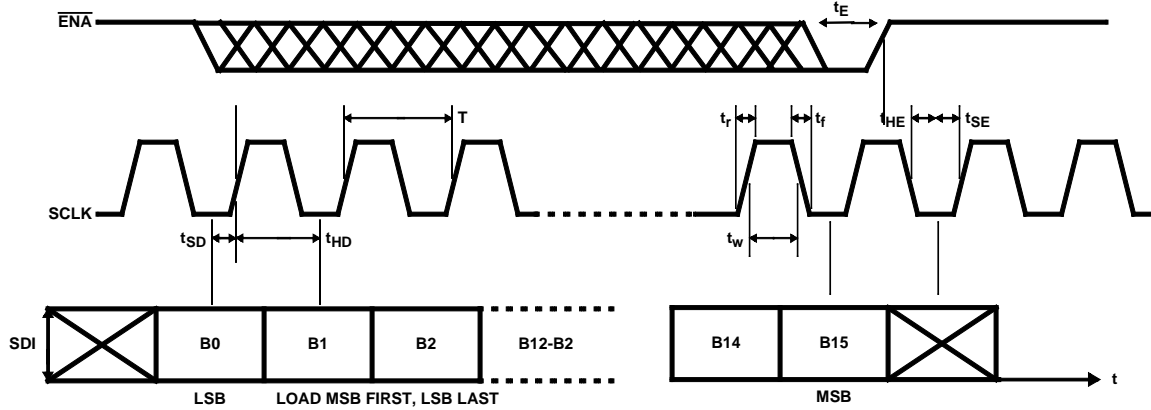
The ISL59532 uses a simple 3-wire SPI compliant digital interface to program the outputs. The ISL59532 can support the clock rate up to 5MHz.

### Serial Interface

The ISL59532 is programmed through a three-wire serial interface. The start and stop conditions are defined by the ENA signal. While the ENA is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The LSB (bit 0) is loaded first and the MSB (bit 15) is loaded last (see Table 1). After the full 16-bit data has been loaded, the ENA is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the ENA is high. The SCLK must be low before the ENA is pulled low.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

**Serial Timing Diagram**



**TABLE 1. SERIAL TIMING PARAMETERS**

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	Clock Period
t <sub>HE</sub>	≥20ns	EN <sub>A</sub> Hold Time
t <sub>SE</sub>	≥20ns	EN <sub>A</sub> Setup Time
t <sub>HD</sub>	≥20ns	Data Hold Time
t <sub>SD</sub>	≥20ns	Data Setup Time
t <sub>w</sub>	0.50 * T	Clock Pulse Width

**Programming Model**

The device has power-on reset that disables outputs, disables test mode, and turns off analog currents. To start up the device the control word is sent:

**TABLE 2. CONTROL WORD FORMAT**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
1	1	1	-	-	-	Clamp	0	0	0	0	0	0	0	Power on	Common output enable

It is important to always program control bits 2-8 as zeros to avoid activating test modes designed for device manufacturing. The clamp bit activates the input clamp and bleed current sink and works only in the single-ended version.

To enable individual outputs, the output enable control word is sent. There are 32 enables to set; this is done with serial words controlling eight at a time. The output enable control word format is:

**TABLE 3. OUTPUT ENABLE FORMAT**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	-	-	-	N1	N0	O <sub>n+7</sub>	O <sub>n+6</sub>	O <sub>n+5</sub>	O <sub>n+4</sub>	O <sub>n+3</sub>	O <sub>n+2</sub>	O <sub>n+1</sub>	O <sub>n</sub>

The O<sub>x</sub> bits represent output enables of eight individual registers. The N1N0 bits represent a two bit binary number which is used in setting n = 2<sup>N1N0</sup>. For instance, to access the control bit of the 11th output enable, we send the word:

**TABLE 4. OUTPUT ENABLE WORD OF 2ND GROUP OF OUTPUTS**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	1	-	-	-	0	1	O <sub>15</sub>	O <sub>14</sub>	O <sub>13</sub>	O <sub>12</sub>	O <sub>11</sub>	O <sub>10</sub>	O <sub>9</sub>	O <sub>8</sub>

Individual output enables are ended with the control register's common output enable bit and the power on bit.

**Gain Setting**

The gain of each output may be set to 1 or 2 using the gain set word. It is in the same format as the output enable control word:

**TABLE 5. GAIN SET FORMAT**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	-	-	-	N1	N0	G <sub>n+7</sub>	G <sub>n+6</sub>	G <sub>n+5</sub>	G <sub>n+4</sub>	G <sub>n+3</sub>	G <sub>n+2</sub>	G <sub>n+1</sub>	G <sub>n</sub>

**Input to Output Selection**

Individual outputs receive their input selection choice using the input/output control word. Its format is:

**TABLE 6. INPUT/OUTPUT WORD**

B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	-	-	-	O <sub>4</sub>	O <sub>3</sub>	O <sub>2</sub>	O <sub>1</sub>	O <sub>0</sub>

For a given binarily selected output, as specified by the O's, an input channel is assigned by the binarily selected I's. Thirty-two transmissions of the input/output control words will be required to set up all outputs.

**Broadcast Mode**

The broadcast mode routs one input to all 32 outputs. It has a memory bit that remembers its state. The configuration of input/output assignments that existed before setting broadcast mode is kept in memory and when broadcast mode is disabled the previous configuration is restored. The broadcast control word format is:

**TABLE 7. BROADCAST WORD**

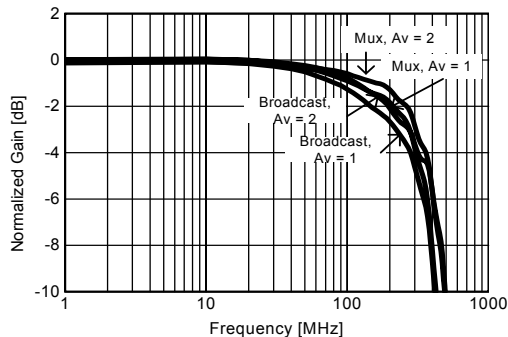
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
0	1	1	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	-	-	-	-	-	-	-	EB

EB sets or resets the broadcast mode memory bit. The I's binarily select the input channel to be broadcast to all outputs.

NOTE: Going from broadcast mode to normal crosspoint mode can alter the input/output configuration. All input/output selections currently must be re-sent after a broadcast-to-non-broadcast transition.

**Bandwidth Considerations**

Wide frequency response (high bandwidth) in a video system means better video resolution. Four sets of frequency response curves are shown in Figure 47. Depending on the switch configurations, one can get between 250MHz to 350MHz bandwidth. A short discussion of the trade-offs follows—including matrix configuration, output buffer gain selection, channel selection, and loading.



**FIGURE 47. FREQUENCY RESPONSE FOR VARIOUS MODES**

In multiplexer mode, the input only drives one output channel, while in broadcast mode the same input drives all 32 outputs. The parasitic capacitance of all 32 channels loads down the input and reduces bandwidth in broadcast

mode. In addition, output buffer gain of +2 has higher bandwidth than gain of +1 due to internal device compensation. Therefore, the highest bandwidth set-up is multiplexer mode and output buffer gain of +2.

The relative location of the input and output channel also has significant impact on the device bandwidth. Again this is due to the layout of the device. When the input and output channels are further away, there are additional parasitics as a result of the distance and lower bandwidth results.

The bandwidth does not change significantly with resistive loading as shown in Figure 3 in the typical performance curves. However, it does change greatly with capacitance loading, Figure 4 in typical performance curves. This is most significant when laying out the PCB. If the PCB trace between the output of the crosspoint switch and the back termination resistor is not minimized, additional parasitic capacitance severely distorts the frequency response.

To emphasize how critical the PCB layout is to performance, let's compare the two boards presented in Figures 48 and 49. Figure 48 shows a larger engineering evaluation board where the termination resistor is far away from the device because of the use of a socket. The board in Figure 48 is a

demoboard without the socket. The parasitic capacitance of the demoboard is about 2.7pF less.

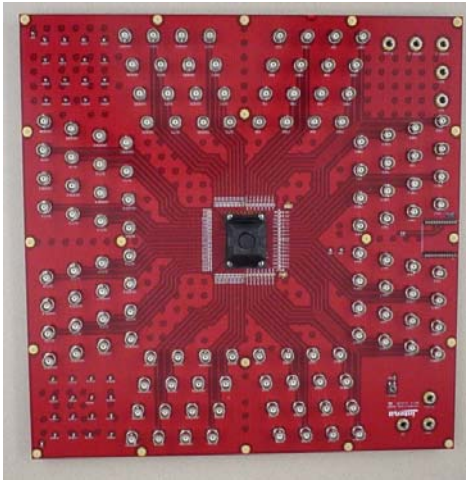


FIGURE 48. ENGINEERING EVALUATION BOARD

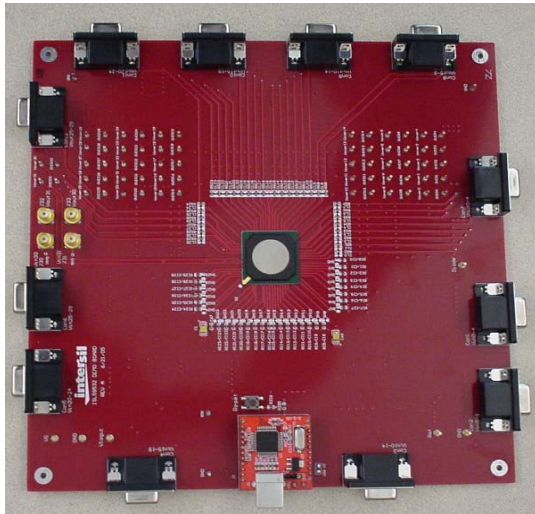


FIGURE 49. CUSTOMER DEMOBOARD

To prove that the parasitic capacitance is the largest contributor to the difference in bandwidth of the two boards, we added 2.7pF at the output of the demoboard. Figure 50 shows the similarity in frequency response of the engineering evaluation board alongside the demoboard piggybacked with 2.7pF.

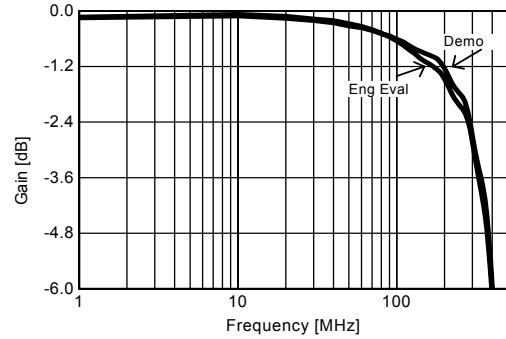


FIGURE 50. FREQUENCY RESPONSE - ENG EVAL BOARD vs DEMO

**Linear Operating Region**

In addition to bandwidth, one must also be very careful with operating the device at its linear operating region. Figure 51 shows differential gain curve. The ISL59532 is a single supply 5V device with its linear region is between 0.1 and 2V. The signal range is fine for most video signals whose nominal signal amplitude is 1V. Both inputs should be maintained at 0.3V or above for best operation. A DC restore circuit is required to put the video signal within the linear operating region of the crosspoint switch.

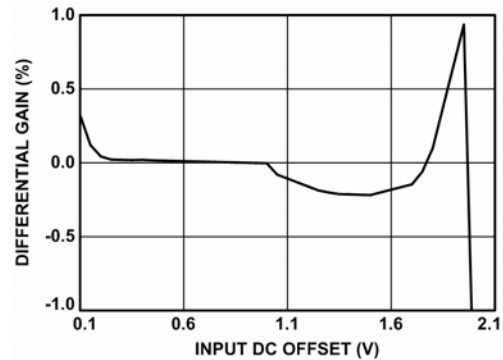


FIGURE 51. DIFFERENTIAL GAIN RESPONSE

The high quality differential gain performance is provided by a DC restore clamp circuit at the input of the device. A discussion of the benefits of the DC-restored system begins by understanding the block diagram of a DC-restore (Figure 52). It consists of 4 simple sections: an input RC network, an op amp configured as a buffer, a FET switch, and a current source. In the absence of an input signal, Rin drains the input node to ground. The discharge current drains the input capacitance of charge to restore the output of the block to ground in preparation for when the FET switch is turned on. This action eliminates any intensity abnormalities.

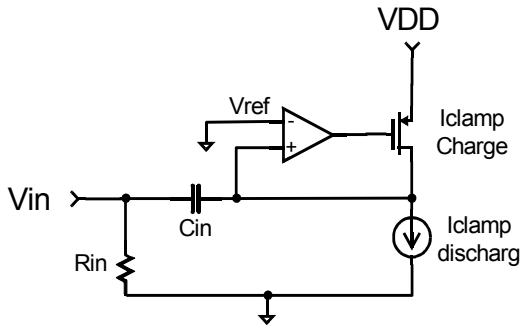


FIGURE 52. DC RESTORE BLOCK DIAGRAM

The pulldown current is necessary to enable the clamp action each sync time but causes the signal to droop during the rest of the video waveform. This droop rate is  $I_B/C_{in}$  volts/second. We generally limit the droop voltage to  $<1$  IRE over a period of video; so for  $1$  IRE =  $7mV$ ,  $I_B = 10\mu A$  maximum, and an NTSC waveform we will set  $C_{in} > 10\mu A * 60\mu s / 7mV = 0.086\mu F$ . Figure 53 shows the result of  $C_{in} = 0.1\mu F$  delivering acceptable droop and  $C_{in} = 0.001\mu F$  producing excessive droop.

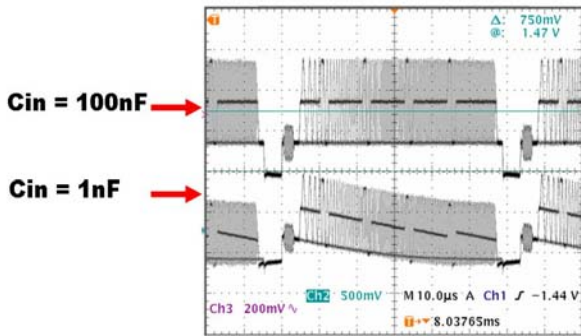


FIGURE 53. DC RESTORE VIDEO WAVEFORMS

**Power Dissipation and Thermal Resistance**

With a large number of switches, it is possible to exceed the  $150^{\circ}C$  absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the crosspoint switch in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation’s quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

*Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.*

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)

Where:

- $T_{JMAX}$  = Maximum junction temperature =  $125^{\circ}C$
- $T_{AMAX}$  = Maximum ambient temperature =  $85^{\circ}C$
- $\theta_{JA}$  = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^n (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}}$$

Where:

- $V_S$  = Supply voltage =  $5V$
- $I_{SMAX}$  = Maximum quiescent supply current =  $700mA$
- $V_{OUT}$  = Maximum output voltage of the application =  $2V$
- $R_{LOAD}$  = Load resistance tied to ground =  $150$
- $N$  =  $1$  to  $32$  channels

$$PD_{MAX} = V_S \times I_{SMAX} + \sum_{i=1}^n (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} = 4.8W$$

The required  $\theta_{JA}$  to dissipate  $4.8W$  is:

$$\theta_{JA} = \frac{T_{JMAX} - T_{AMAX}}{PD_{MAX}} = 8.33(C/W)$$

Table 8 shows  $\theta_{JA}$  thermal resistance results with a Wakefield heatsink and without heatsink and various airflow. At the thermal resistance equation shows, the required thermal resistance depends on the maximum ambient temperature.

TABLE 8.  $\theta_{JA}$  Thermal Resistance [ $^{\circ}C/W$ ]

Airflow [LFM]	0	250	500	750
No Heatsink	18	14.3	13.0	12.6
Wakefield 658-25AB	16.0	7.0	6.0	4.7

# 356 Ld BGA Package

NOTES: UNLESS OTHERWISE SPECIFIED

- ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.
- THE BASIC SOLDER BALL GRID PITCH IS 1.27mm.
- THE MAXIMUM SOLDER BALL MATRIX SIZE IS 20 X 20.
- THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 400.

5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

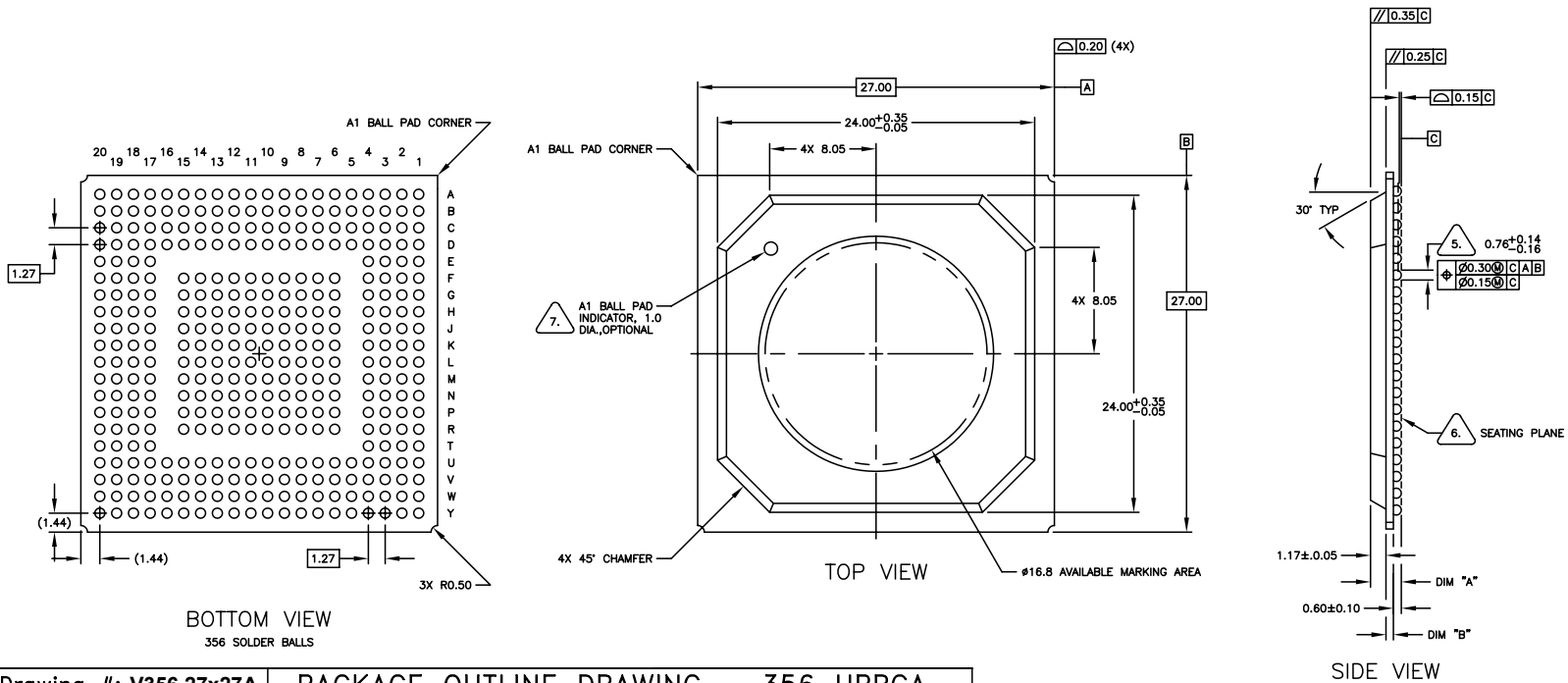



A1 BALL PAD CORNER I.D. FOR PLATE MOLD: TO BE MARKED BY INK.  
AUTO MOLD: DIMPLE TO BE FORMED BY MOLD CAP.

8.

REFERENCE SPECIFICATIONS:

A. THIS DRAWING CONFORMS TO THE JEDEC REGISTERED OUTLINE MS-034/A VARIATION BAL-2.



Drawing #: <b>V356.27x27A</b>	PACKAGE OUTLINE DRAWING - 356 HPBGA 27 x 27 mm x 1.17 mm MOLD CAP 1.27 mm PITCH SUBSTRATE
Rev: 0	
Date: 11/17/05	 SOLUTIONS IN SILICON
Units: mm	

NO. LAYERS	DIM "A"	DIM "B"	NOTES
4	2.38±0.21	0.61±0.06	STANDARD
HPBGA THICKNESS SCHEDULE			

ISL59532