

PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

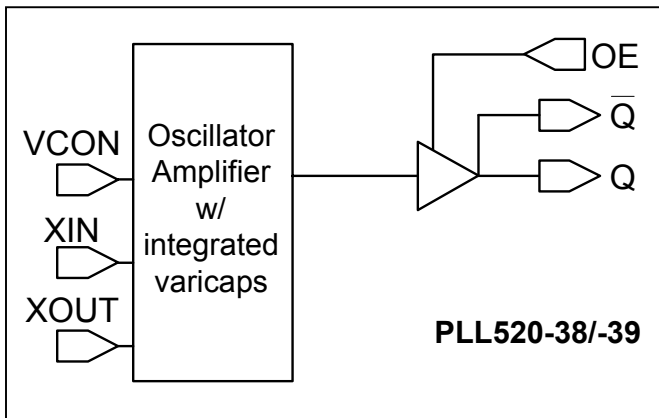
FEATURES

- 65MHz to 130MHz Fundamental Mode Crystal.
- Output range: 65MHz – 130MHz (no PLL).
- Low Injection Power for crystal 50uW.
- PECL (PLL520-38) or LVDS output (PLL520-39).
- Integrated variable capacitors.
- Supports 2.5V or 3.3V-Power Supply.
- Available in 16-Pin (TSSOP or 3x3 QFN).

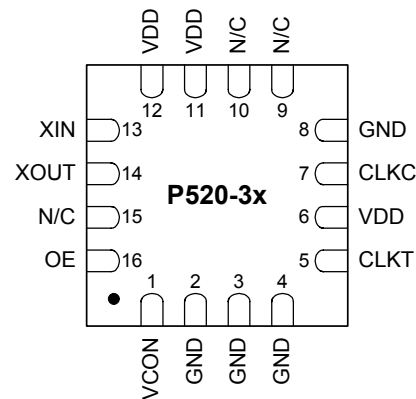
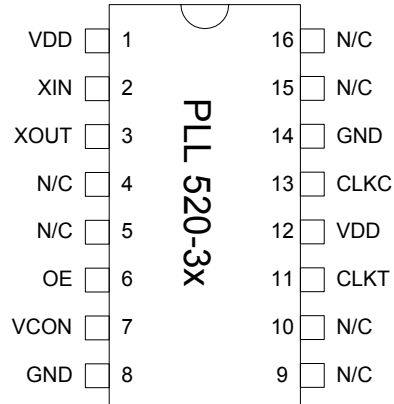
DESCRIPTION

The PLL520-38/-39 is a family of VCXO IC's specifically designed to pull high frequency fundamental crystals from 65MHz to 130MHz, with selectable PECL or LVDS outputs.. They achieve very low current into the crystal resulting in better overall stability. Their internal varicaps allow an on chip frequency pulling, controlled by the VCON input. Their very low jitter makes them ideal for the most demanding timing requirements.

BLOCK DIAGRAM



PIN CONFIGURATION



OUTPUT ENABLE LOGICAL LEVELS

Part #	OE	State
PLL520-38	0 (Default)	Output enabled
	1	Tri-state
PLL520-39	0	Tri-state
	1 (Default)	Output enabled

OE input: Logical states defined by PECL levels for PLL520-38
Logical states defined by CMOS levels for PLL520-39

PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

PIN DESCRIPTIONS

Name	Number	Type	Description
XIN	2	I	Crystal input. See Crystal Specifications on page 2.
XOUT	3	I	Crystal output. See Crystal Specifications on page 2.
OE	6	I	Output enable. See Output Enable Logic table on page 1.
VCON	7	I	Voltage control input.
GND	8, 14	P	Ground.
CLKT	11	O	True output PECL (PLL520-38) or LVDS (PLL520-39).
CLKC	13	O	Complementary output PECL (PLL520-38) or LVDS (PLL520-39).
N/C	4,5,9,10,15,16	-	Not connected.
VDD	1, 12	P	Power supply.

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V _{DD}		4.6	V
Input Voltage, dc	V _I	-0.5	V _{DD} +0.5	V
Output Voltage, dc	V _O	-0.5	V _{DD} +0.5	V
Storage Temperature	T _S	-65	150	°C
Ambient Operating Temperature*	T _A	-40	85	°C
Junction Temperature	T _J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note:** Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Built-in Capacitance	CX+	65MHz to 130MHz (VDD=3.3V)			2	pF
	CX-				2	
Inter-electrode capacitance	C ₀			2.6		
C0/C1 ratio (gamma)	γ				300	-
Oscillation Frequency	OF	Fund.	65		130	MHz

PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

3. Voltage Control Crystal Oscillator (3.3V)

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
VCXO Stabilization Time *	T _{VCXOSTB}	From power valid			10	ms
VCXO Tuning Range		F _{XIN} = 100 – 200MHz; XTAL C ₀ /C ₁ < 250 0V ≤ VCON ≤ 3.3V		200*		ppm
CLK output pullability		VCON=1.65V, ±1.65V	±100*			ppm
On-chip Varicaps control range		VCON = 0 to 3.3V		4 – 18*		pF
Linearity					10*	%
VCXO Tuning Characteristic				65		ppm/V
VCON input impedance				60		kΩ
VCON modulation BW		0V ≤ VCON ≤ 3.3V, -3dB	25			kHz

Note: Parameters denoted with an asterisk (*) represent nominal characterization data and are not production tested to any specific limits.

4. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	I _{DD}	PECL/LVDS			100/80	mA
Operating Voltage	V _{DD}		2.97		3.63	V
Output Clock Duty Cycle		@ 1.25V (LVDS) @ V _{DD} – 1.3V (PECL)	45	50	55	%
Short Circuit Current				±50		mA

5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS	77.76MHz		2.5		ps
Period jitter peak-to-peak	77.76MHz		18.5		ps
Integrated jitter RMS	Integrated 12 kHz to 20 MHz at 77.76MHz		0.5		ps

6. Phase Noise Specifications

PARAMETERS	FREQUENCY	@10Hz	@100Hz	@1kHz	@10kHz	@100kHz	UNITS
Phase Noise relative to carrier	77.76MHz	-75	-95	-125	-145	-155	dBc/Hz

Note: Phase Noise measured at VCON = 0V

PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

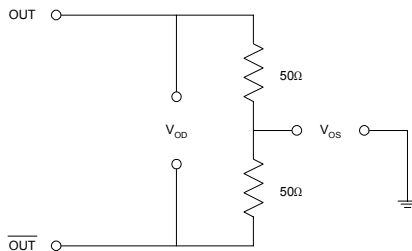
7. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V_{OD}	$R_L = 100 \Omega$ (see figure)	247	355	454	mV
V_{DD} Magnitude Change	ΔV_{OD}		-50		50	mV
Output High Voltage	V_{OH}			1.4	1.6	V
Output Low Voltage	V_{OL}		0.9	1.1		V
Offset Voltage	V_{OS}		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV_{OS}		0	3	25	mV
Power-off Leakage	I_{OXD}	$V_{out} = V_{DD}$ or GND $V_{DD} = 0V$		± 1	± 10	μA
Output Short Circuit Current	I_{OSD}			-5.7	-8	mA

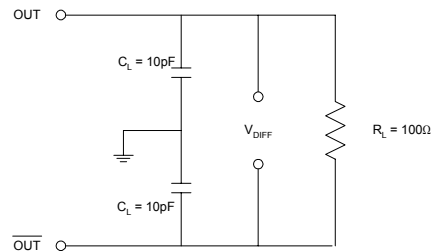
8. LVDS Switching Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	t_r	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	t_f		0.2	0.7	1.0	ns

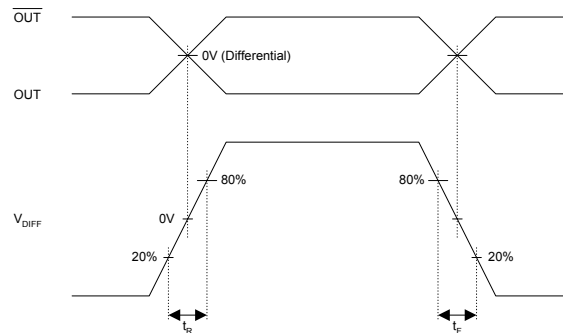
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform



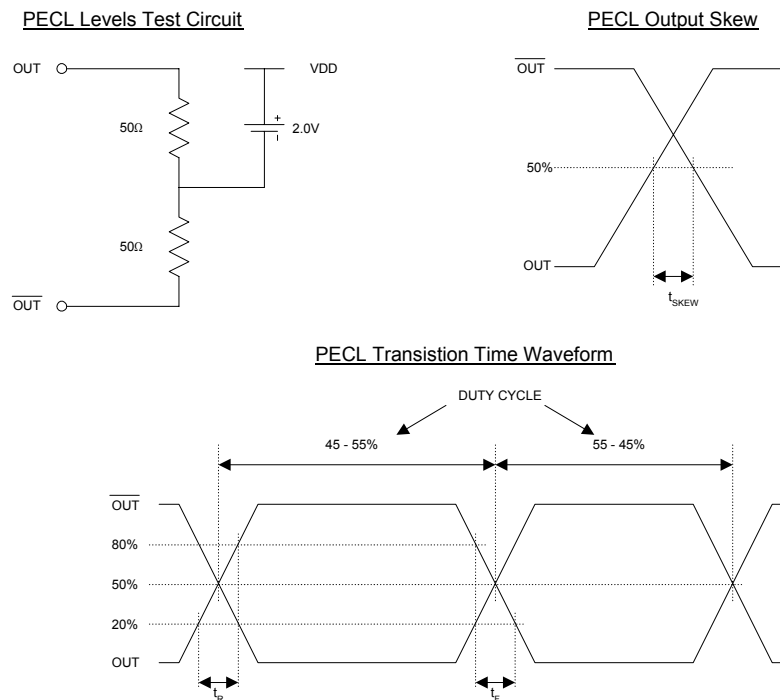
PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

9. PECL Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	V_{OH}	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	V_{OL}			$V_{DD} - 1.620$	V

10. PECL Switching Characteristics

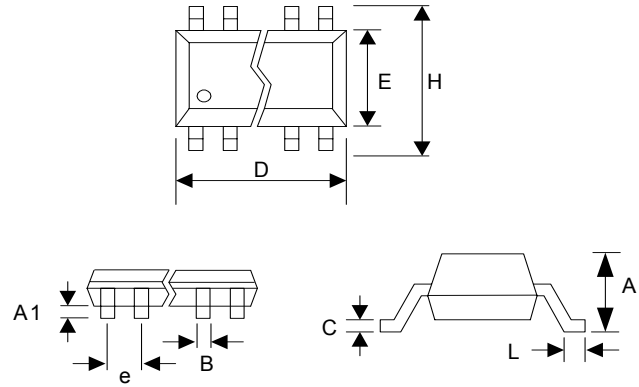
PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	t_r	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	t_f	@80/20% - PECL		0.5	1.5	ns



PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

PACKAGE INFORMATION

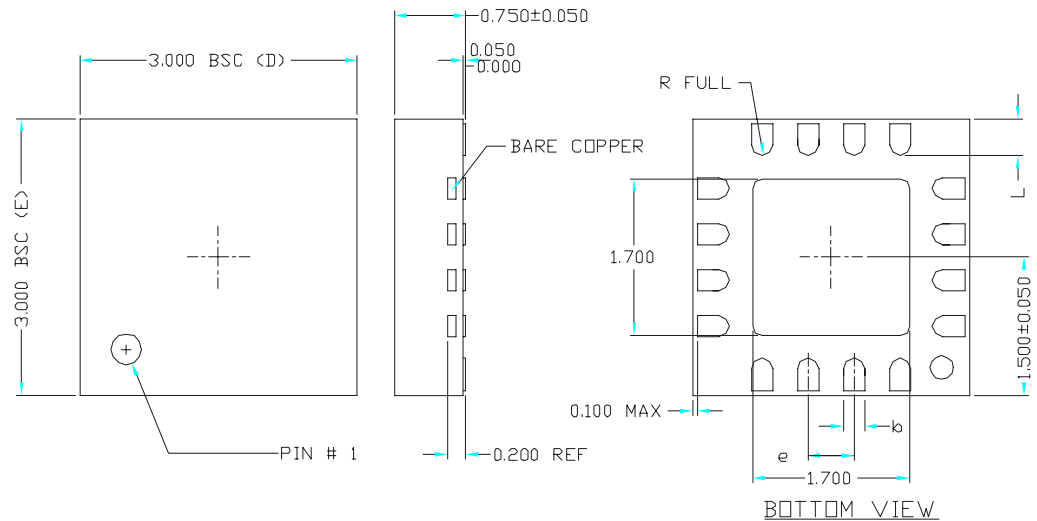
16 PIN TSSOP (mm)		
Symbol	Min.	Max.
A	-	1.20
A1	0.05	0.15
B	0.19	0.30
C	0.09	0.20
D	4.90	5.10
E	4.30	4.50
H	6.40 BSC	
L	0.45	0.75
e	0.65 BSC	



3x3mm QFN

VARIATIONS:

SYMBOL	16 LD		
	MIN	NDM	MAX
e	0.50 BSC		
b	0.18	0.23	0.30
L	0.30	0.40	0.50
ND	4		
NE	4		



PECL and LVDS Low Phase Noise VCXO (for 65-130MHz Fund Xtal)

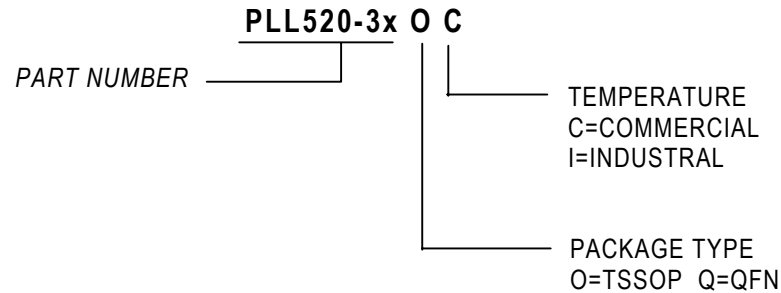
ORDERING INFORMATION

For part ordering, please contact our Sales Department:

47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range



<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
PLL520-38OC	P520-38OC	TSSOP - Tube
PLL520-38OC-R	P520-38OC	TSSOP - Tape & Reel
PLL520-38QC	P520-38QC	QFN - Tube
PLL520-38QC-R	P520-38QC	QFN - Tape & Reel
PLL520-39OC	P520-39OC	TSSOP - Tube
PLL520-39OC-R	P520-39OC	TSSOP - Tape & Reel
PLL520-39QC	P520-39QC	QFN - Tube
PLL520-39QC-R	P520-39QC	QFN - Tape & Reel

PhaseLink Corporation, reserves the right to make changes in its products or specifications, or both at any time without notice. The information furnished by Phaselink is believed to be accurate and reliable. However, PhaseLink makes no guarantee or warranty concerning the accuracy of said information and shall not be responsible for any loss or damage of whatever nature resulting from the use of, or reliance upon this product.

LIFE SUPPORT POLICY: PhaseLink's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of PhaseLink Corporation.