

## Audio

# Monolithic IC MM1407

### Outline

This audio IC was developed for notebook PCs and allows major reduction of amp circuit board area. (To conform to PC98, includes built-in speaker drive amp, headphone amp, line amp. stereo/monaural switching, DC voltage control electronic volume, watchdog, logic control function.)

### Features

- (1) Speaker amp: Stereo BTL output 0.7W (when  $V_{CC} = 5.0V$ ,  $R_L = 8\Omega$ )
- (2) Electronic volume control ( $-60 \sim +20dB$ ). THD = 0.5% (when  $P_{OUT} = 300mW$ ,  $R_L = 8\Omega$ )  
 THD1 = 0.5% (when  $V_{OUT} = 100mV_{rms}$ ,  $R_L = 16\Omega$ )  
 THD2 = 0.1% (when  $V_{OUT} = 1V_{mV_{rms}}$ ,  $R_L = 10k\Omega$ )
- (4) Line amp: Mixes 4 inputs ( 2ch signals and outputs on 3 outputs ( 2ch. Stereo/monaural switching possible on one line. THD = 0.1% (when  $V_{OUT} = 1V_{rms}$ ,  $R_L = 10k\Omega$ )
- (5) Microphone amp: Switch pin selects 1 of 4 inputs
- (6) Logic control: Speaker, headphone and line amp (including microphone amp and mix amp) logic controllable. Current consumption 300 $\mu$ A during power save mode.

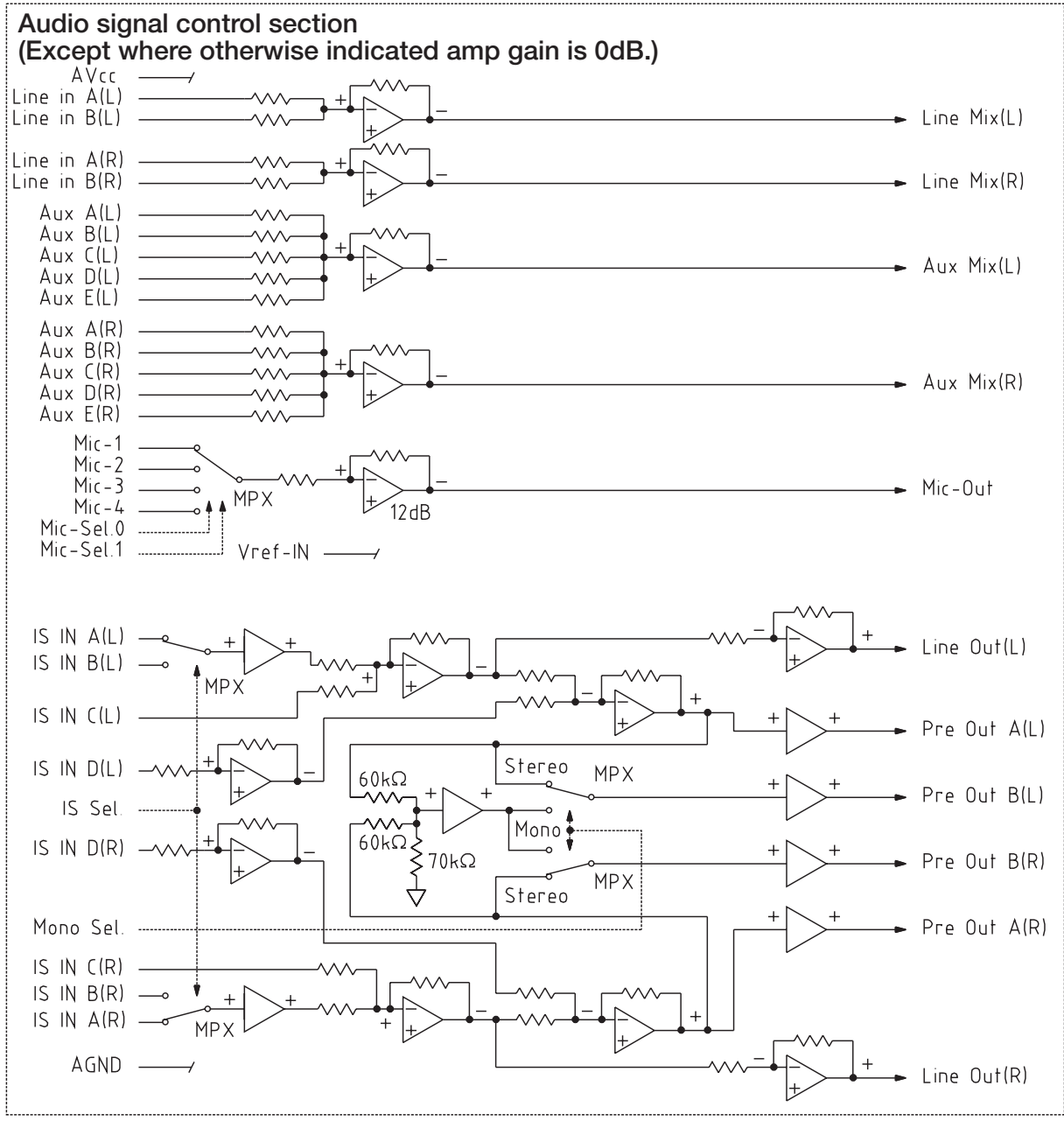
### Package

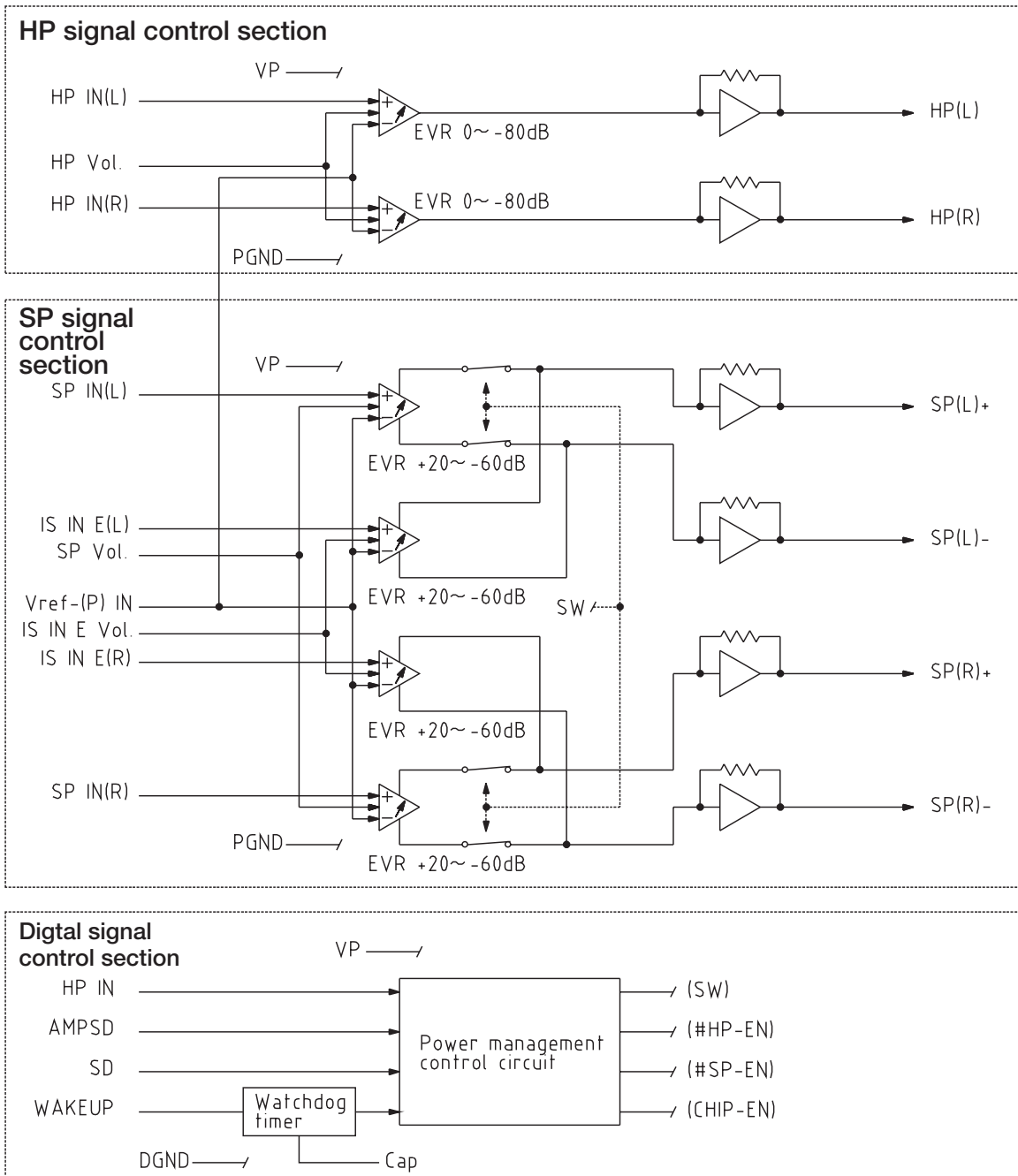
QFP-80B

### Applications

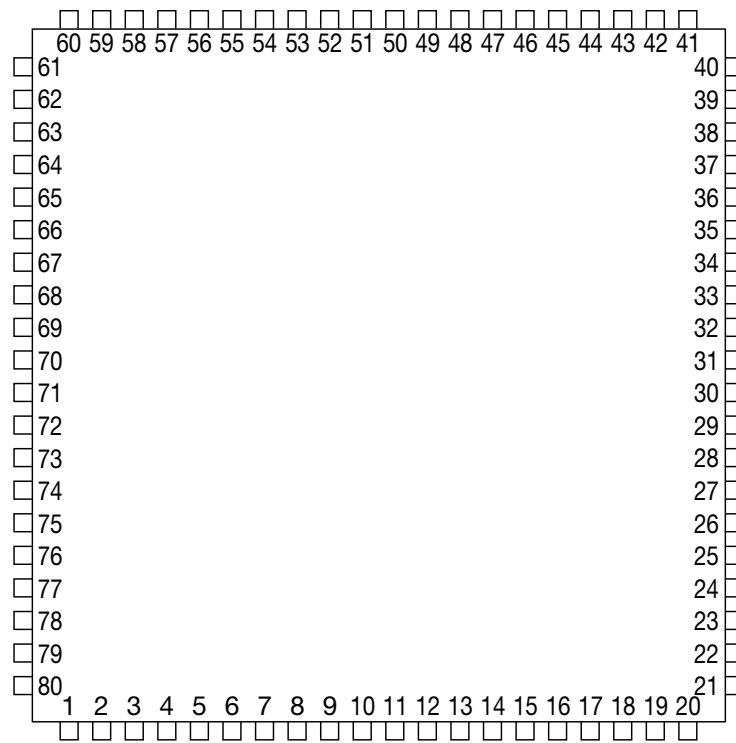
- (1) Notebook PC audio control

Block Diagram





Pin Description



QFP-80B

1	Vref-IN	21	IS IN A (R)	41	HP (R)	61	HP IN (L)
2	Aux E (L)	22	IS IN B (R)	42	Vcc1	62	IS IN E (L)
3	Aux D (L)	23	IS IN C (R)	43	PGND1	63	SP IN (L)
4	Aux C (L)	24	IS IN D (R)	44	SP (R)+	64	HP VOL
5	Aux B (L)	25	IS SEL	45	VP1	65	Mic-sel 0
6	Aux A (L)	26	Line out (R)	46	VP2	66	Mic-sel 1
7	Aux Mix (L)	27	Pre out A (R)	47	SP (R)-	67	Mic-1
8	Line in B (L)	28	Pre out B (R)	48	PGND2	68	Mic-2
9	Line in A (L)	29	Mono SEL	49	GND1	69	Mic-4
10	Line Mix (L)	30	Cap	50	GND2	70	Mic-3
11	AGND1	31	WAKEUP	51	PGND3	71	Mic out
12	Line Mix (R)	32	AMPSD	52	SP (L)+	72	AGND2
13	Line in A (R)	33	SD	53	VP3	73	Pre out B (L)
14	Line in B (R)	34	HP-IN	54	VP4	74	Pre out A (L)
15	Aux Mix (R)	35	DGND	55	SP (L)-	75	Line out (L)
16	Aux A (R)	36	VD	56	PGND4	76	AVcc
17	Aux B (R)	37	Vref (P)-IN	57	Vcc2	77	IS IN D (L)
18	Aux C (R)	38	SP IN (R)	58	HP (L)	78	IS IN C (L)
19	Aux D (R)	39	IS IN E (R)	59	IS IN E VOL	79	IS IN B (L)
20	Aux E (R)	40	HP IN (R)	60	SP VOL	80	IS IN A (L)

**Pin Description**

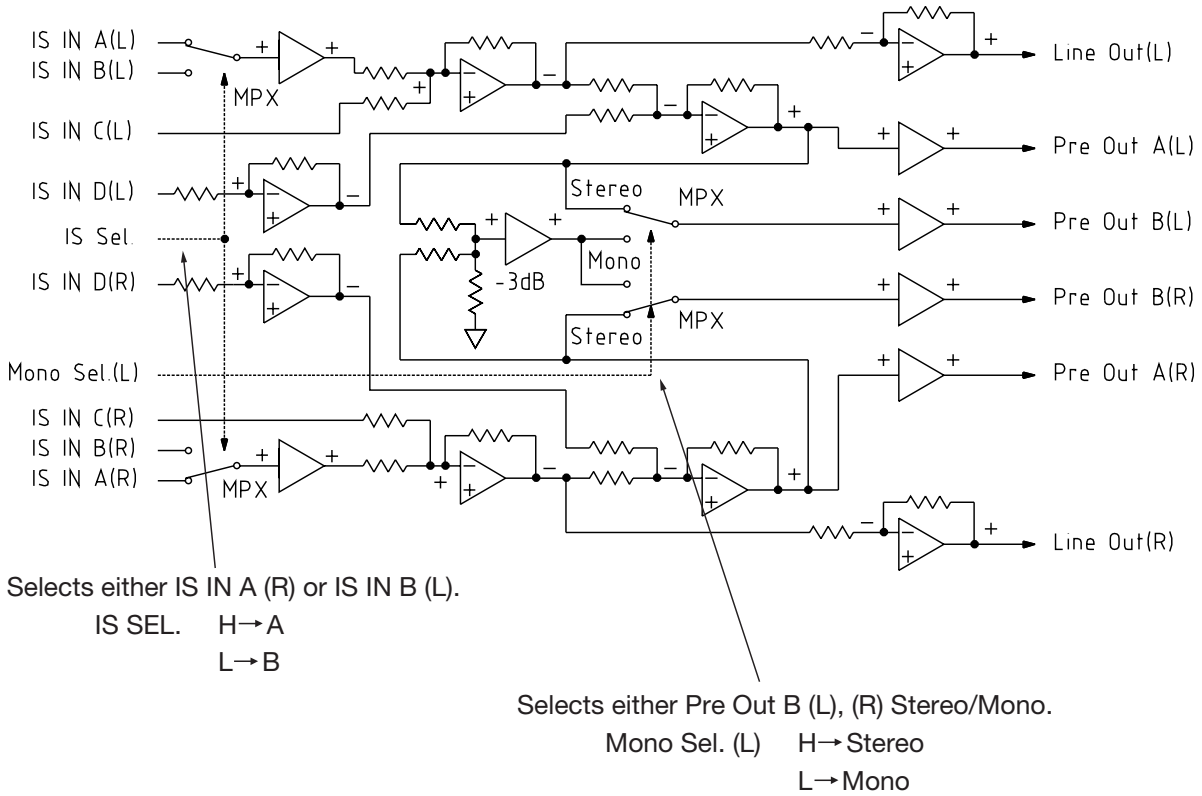
Pin No.	Pin name	Input/Output	Section	Function
1	Vref-IN	Power supply (reference)	Audio signal control	Applies audio signal control reference potential.
2	Aux E (L)	Input	Audio signal control	1 of 5 Aux Mix (L) (add amp) inputs.
3	Aux D (L)	Input	Audio signal control	1 of 5 Aux Mix (L) (add amp) inputs.
4	Aux C (L)	Input	Audio signal control	1 of 5 Aux Mix (L) (add amp) inputs.
5	Aux B (L)	Input	Audio signal control	1 of 5 Aux Mix (L) (add amp) inputs.
6	Aux A (L)	Input	Audio signal control	1 of 5 Aux Mix (L) (add amp) inputs.
7	Aux Mix (L)	Output	Audio signal control	Signal with Aux A ~ E (L) input added is output.
8	Line In B (L)	Input	Audio signal control	1 of 2 Line In (L) (add amp) inputs.
9	Line In A (L)	Input	Audio signal control	1 of 2 Line In (L) (add amp) inputs.
10	Line Mix (L)	Output	Audio signal control	Signal with Aux A ~ B (L) input added is output.
11	AGND1	GND	Audio signal control	Audio signal control ground pin. (except for Mic amp)
12	Line Mix (R)	Output	Audio signal control	Signal with Aux A ~ B (L) input added is output.
13	Line In A (R)	Input	Audio signal control	1 of 2 Line In (R) (add amp) inputs.
14	Line In B (R)	Input	Audio signal control	1 of 2 Line In (R) (add amp) inputs.
15	Aux Mix (R)	Output	Audio signal control	Signal with Aux A ~ E (R) input added is output.
16	Aux A (R)	Input	Audio signal control	1 of 5 Aux Mix (R) (add amp) inputs.
17	Aux B (R)	Input	Audio signal control	1 of 5 Aux Mix (R) (add amp) inputs.
18	Aux C (R)	Input	Audio signal control	1 of 5 Aux Mix (R) (add amp) inputs.
19	Aux D (R)	Input	Audio signal control	1 of 5 Aux Mix (R) (add amp) inputs.
20	Aux E (R)	Input	Audio signal control	1 of 5 Aux Mix (R) (add amp) inputs.
21	IS IN A (R)	Input	Audio signal control	1 pin of 4 amp inputs that output to Line Out (R), Pre Out A (R), Pre Out B (R), (L).
22	IS IN B (R)	Input	Audio signal control	1 pin of 4 amp inputs that output to Line Out (R), Pre Out A (R), Pre Out B (R), (L).
23	IS IN C (R)	Input	Audio signal control	1 pin of 4 amp inputs that output to Line Out (R), Pre Out A (R), Pre Out B (R), (L).
24	IS IN D (R)	Input	Audio signal control	1 pin of 4 amp inputs that output to Pre Out A (R), Pre Out B (R), (L).
25	IS Sel.	Input (SW)	Audio signal control	This pin selects either of two inputs IS IN A (R) or IS IN B (R). (See Figure A)
26	Line Out (R)	Output	Audio signal control	A signal that has IS IN A (R) or B (R) or IS IN C (R) added is output.
27	Pre Out A (R)	Output	Audio signal control	A signal that has IS IN A (R) or B (R) or IS IN C (R) or IS IN D (R) added is output.
28	Pre Out B (R)	Output	Audio signal control	During Mono Sel. R Stereo selection, a signal that has IS IN A (R) or B (R) or IS IN C (R) or IS IN D (R) added is output. During Mono Sel. R Mono selection, a signal that is a mixture of a signal with (R) input added and then lowered 9dB and a signal that with (L) input added and lowered 9dB.
29	Mono Sel.	Input (SW)	Audio signal control	This pin switches Pre Out B (L), (R) Stereo and Mono output. (See Figure A)
30	Cap	Input (logic)	Digital signal control	This pin sets clock monitoring time for the watchdog timer circuit. Clock monitoring time is determined by the capacitor time constant connected to this pin. (See Figure C)
31	WAKEUP	Input (logic)	Digital signal control	1 of 4 logic circuit inputs. (See Figure D)
32	AMPSD	Input (logic)	Digital signal control	1 of 4 logic circuit inputs. (See Figure D)
33	SD	Input (logic)	Digital signal control	1 of 4 logic circuit inputs. (See Figure D)

Pin No.	Pin name	Input/Output	Section	Function
34	HP-IN	Input (logic)	Digital signal control	1 of 4 logic circuit inputs. (See Figure D)
35	DGND	GND	Digital signal control	Digital signal control ground pin.
36	VD	Power supply	Digital signal control	Digital signal control Vcc pin. (*1)
37	Vref- (P) IN	Power supply (reference)	SP, HP signal control	Applies SP, HP signal control section reference potential.
38	SP IN (R)	Input	SP signal control	1 of 2 SP amp (R-ch) inputs. Use music source, etc. input.
39	IS IN E (R)	Input	SP signal control	1 of 2 SP amp (R-ch) inputs. Use beep alarm sound, etc. input.
40	HP IN (R)	Input	HP signal control	HP amp (R-ch) input.
41	HP (R)	Output	HP signal control	HP amp (R-ch) output.
42	Vcc1	Power supply	SP, HP signal control	SP, HP amp input stage, EVR circuit, DC bias circuit Vcc pin. (*2)
43	PGND1	GND	SP, HP signal control	SP, HP amp output stage (power amp) ground pin.
44	SP (R) +	Output	SP signal control	SP amp (R-ch) BTL output (+) pin.
45	VP1	Power supply	SP, HP signal control	SP, HP amp output stage (power amp) Vcc pin.
46	VP2	Power supply	SP, HP signal control	SP, HP amp output stage (power amp) Vcc pin.
47	SP (R) -	Output	SP signal control	SP amp (R-ch) BTL output (-) pin.
48	PGND2	GND	SP, HP signal control	SP, HP amp output stage (power amp) ground pin.
49	GND1	GND	SP, HP signal control	SP, HP amp input stage, EVR circuit, DC bias circuit ground pin. (*3)
50	GND2	GND	SP, HP signal control	SP, HP amp input stage, EVR circuit, DC bias circuit ground pin. (*3)
51	PGND3	GND	SP, HP signal control	SP, HP amp output stage (power amp) ground pin.
52	SP (L) +	Output	SP signal control	SP amp (L-ch) BTL output (+) pin.
53	VP3	Power supply	SP, HP signal control	SP, HP amp output stage (power amp) Vcc pin.
54	VP4	Power supply	SP, HP signal control	SP, HP amp output stage (power amp) Vcc pin.
55	SP (L) -	Output	SP signal control	SP amp (L-ch) BTL output (-) pin.
56	PGND4	GND	SP, HP signal control	SP, HP amp output stage (power amp) ground pin.
57	Vcc2	Power supply	SP, HP signal control	SP, HP amp input stage, EVR circuit, DC bias circuit Vcc pin. (*2)
58	HP (L)	Output	HP signal control	HP amp (R-ch) output pin.
59	IS IN E Vol.	Input	SP signal control	SP amp IS IN E input electronic volume pin. (*4)
60	SP Vol.	Input	SP signal control	SP amp SP IN input electronic volume pin. (*5)
61	HP IN (L)	Input	HP signal control	HP amp (L-ch) input.
62	IS IN E (L)	Input	SP signal control	1 of 2 SP amp (L-ch) inputs. Use beep alarm sound, etc. input.
63	SP IN (L)	Input	SP signal control	1 of 2 SP amp (L-ch) inputs. Use music source, etc. input.
64	HP Vol.	Input	HP signal control	HP amp electronic volume pin. (*6)
65	Mic-Sel.0	Input	Audio signal control	Selects 1 of 4 Mic amp inputs in combination with Mic-Sel. 1 pin. (See Figure E)
66	Mic-Sel.1	Input	Audio signal control	Selects 1 of 4 Mic amp inputs in combination with Mic-Sel. 0 pin. (See Figure E)
67	Mic-1	Input	Audio signal control	1 of 4 Mic amp inputs.
68	Mic-2	Input	Audio signal control	1 of 4 Mic amp inputs.
69	Mic-4	Input	Audio signal control	1 of 4 Mic amp inputs.
70	Mic-3	Input	Audio signal control	1 of 4 Mic amp inputs.
71	Mic-Out	Output	Audio signal control	1 of 4 Mic 1 ~ 4 inputs is output depending on combination of Mic Sel. 0 and Mic Sel. 1 pins.

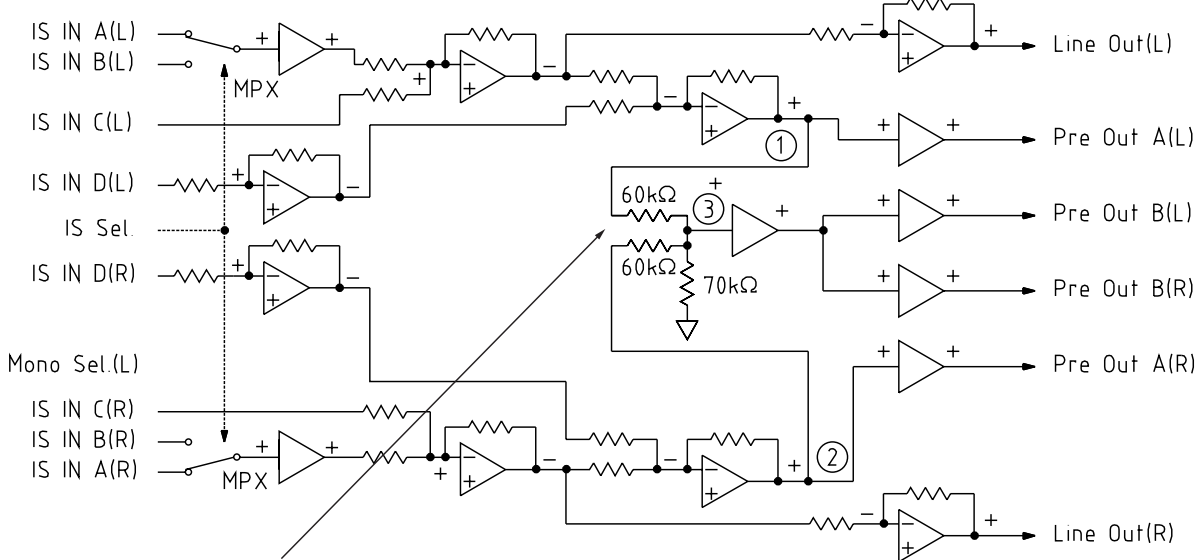
Pin No.	Pin name	Input/Output	Section	Function
72	AGND2	GND	Audio signal control	Mic amp ground pin.
73	Pre Out B (L)	Output	Audio signal control	During Mono Sel. R Stereo selection, a signal that has IS IN A (L) or B (L) or IS IN C (L) or IS IN D (L) added is output. During Mono Sel. R Mono selection, a signal that is a mixture of a signal with (L) input added and then lowered 9dB and a signal that with (R) input added and lowered 9dB. (See Figure B)
74	Pre Out A (L)	Output	Audio signal control	A signal that has IS IN A (R) or B (R) or IS IN C (R) or IS IN D (R) added is output.
75	Pre Out (L)	Output	Audio signal control	A signal that has IS IN A (R) or B (R) or IS IN C (R) added is output.
76	AVcc		Audio signal control	Audio signal control Vcc pin.
77	IS IN D (L)	Input	Audio signal control	1 of 4 amp inputs that is output to Pre Out A (R) or Pre Out B (R), (L).
78	IS IN C (L)	Input	Audio signal control	1 of 4 amp inputs that is output to Line Out (R) or Pre Out A (R), Pre Out B (R), (L).
79	IS IN B (L)	Input	Audio signal control	1 of 4 amp inputs that is output to Line Out (R) or Pre Out A (R), Pre Out B (R), (L).
80	IS IN A (L)	Input	Audio signal control	1 of 4 amp inputs that is output to Line Out (R) or Pre Out A (R), Pre Out B (R), (L).

- \*1 VD power supply and VP power supply must have the same potential.
- \*2 In order to avoid the effects of SP, HP amp interference between L and R, and interference between SP and HP amps on separation characteristics, the wiring connected to this pin should have the same impedance as other Vcc lines (especially lines with large current). (This is not a problem when Vcc1 and Vcc2 lines are bundled.)
- \*3 In order to avoid the effects of SP, HP amp interference between L and R, and interference between SP and HP amps on separation characteristics, the wiring connected to this pin should have the same impedance as other ground lines (especially lines with large current). (This is not a problem when GND1 and GND2 lines are bundled.)
- \*4 The maximum voltage that can be impressed on IS IN E Vol. pin is 2.0V.
- \*5 The maximum voltage that can be impressed on SP Vol. pin is 2.0V.
- \*6 The maximum voltage that can be impressed on HP Vol. pin is 2.0V.

**IS Sel. Pin and Mono Sel. (L) Pin Selection**

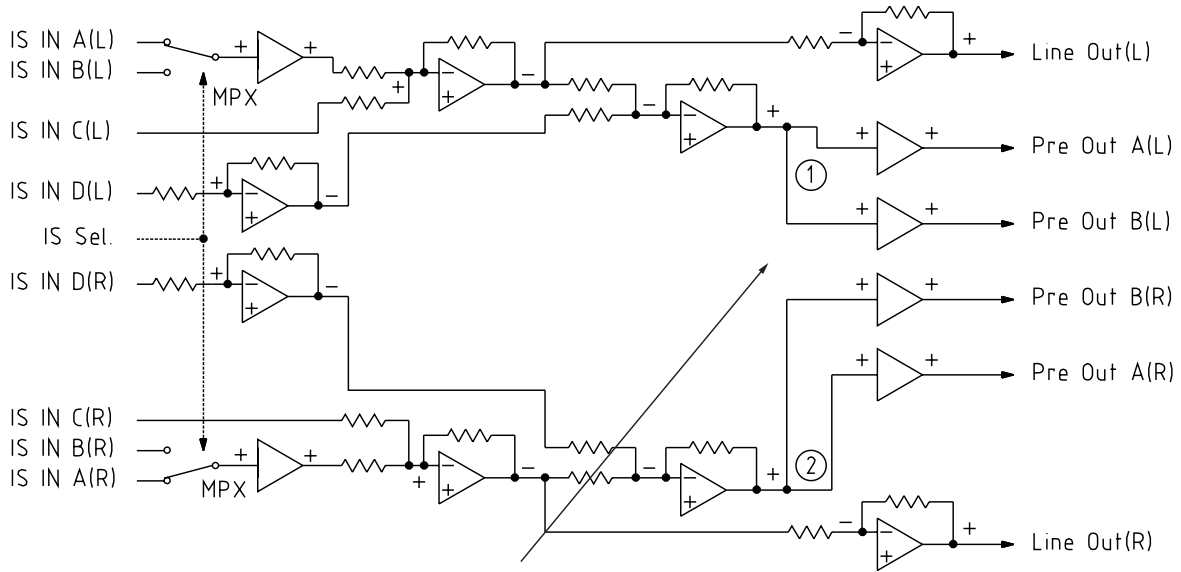


**Figure B. Mono Sel. (L) Pin Pre Out B (L) (R) Signal Route during Mono Selection**



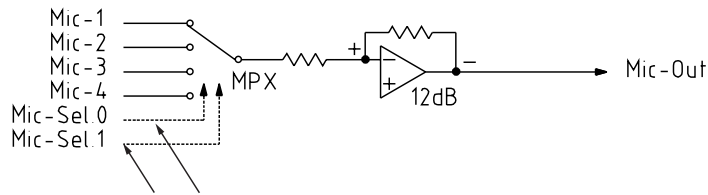


**Mono Sel. (L) Pin Pre Out B (L) (R) Signal Route during Stereo Selection**



During Mono Sel. 1 pin stereo selection, the signal at point 1 is output to Pre Out B (L) and the signal at point 2 is output to Pre Out B (R).

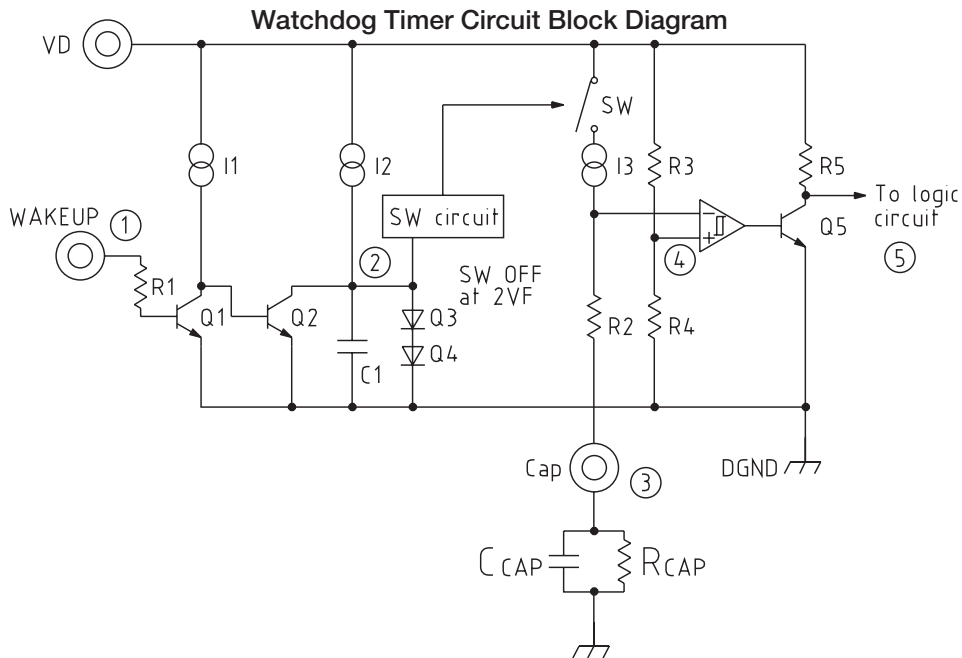
**Mic-Sel. 0, Mic-Sel. 1 pin selection**



1 of 4 Mic 1~4 inputs is selected by Mic-Sel. 0 and Mic-Sel. 1.

	Mic-Sel. 0	Mic-Sel. 1
Mic 1	L	L
Mic 2	L	H
Mic 3	H	L
Mic 4	H	H

Figure C. Watchdog Timer



Basically, the watchdog timer monitors the level (3) of the current it impresses on the external capacitor. The charging time is determined by C1 and I2 in the block diagram, and control is done by input signal (1). When the first "H" trigger (input signal) charges the external capacitor and level (3) goes over (4) "H" threshold value, output is first inverted (L→H). While the input signal is being continuously impressed, the timer repeats charging current impress/stop to the external capacitor, but if input signal (1) is not impressed within the set time (clock monitoring time), charging to the external capacitors is stopped and the capacitor starts discharge operation. Then level (3) falls below "L" threshold value and output (5) is again inverted (H→L).

1. WAKEUP pin input signal cycle limit

Use at 1/Ta or higher, 100Hz or lower.

T1: clock monitoring time (The time from WAKEUP signal input stop until logic truth table WAKEUP switches to low.)

2. WAKEUP pin input signal amplitude limit

Use at 1.5V or higher, 5V or lower.

3. External capacitor time constant (sets clock monitoring time)

Determined by  $T1 = 1.638 \times C \mu F \times R [\Omega]$ .

(E.g.: If C = 1μF, for T1 ≈ 1S, R = 620kΩ, for T1 ≈ 2S, R = 1.2MΩ)

Logic Truth Table

	#SD	#AMPSD	WAKEUP	HP-IN	CHIP-EN	#SP-EN	#HP-EN	SW
(1)			H	H	EN	EN	EN	OFF
(2)			H	L	EN	EN	DIS	ON
(3)	H	H	L	H	EN	DIS	EN	ON
(4)	H	H	L	L	EN	EN	DIS	ON
(5)	H	L	L		EN	DIS	DIS	ON
(6)	L		L		DIS	DIS	DIS	ON

- WAKEUP "H" indicates the state where a pulse is impressed continuously, and "L" means that pulse impression is stopped and level is low. (See Figure C)
- The EN in CHIP-EN means that the audio signal control section in the block diagram is ON, and DIS means that it is OFF.
- The EN in #SP-EN means that the SP signal control section in the block diagram is ON, and DIS means that it is OFF.
- The EN in #HP-EN means that the HP signal control section in the block diagram is ON, and DIS means that it is OFF.
- SW ON and OFF: ON means that SP IN and IS IN E in the SP signal control section in the block diagram are both operating, and OFF means that IS IN E only is operating.

**Absolute Maximum Ratings** (Ta = 25°C)

Item	Signal	Rating	Unit
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Power supply voltage (AV <sub>CC</sub> )	V <sub>CCmax.1</sub>	7	V
Power supply voltage (VP)	V <sub>CCmax.2</sub>	7	V
Power supply voltage (VD)	V <sub>CCmax.3</sub>	7	V
Input pin voltage (AV <sub>CC</sub> )	V <sub>INmax.1</sub>	-0.3~AV <sub>CC</sub> +0.3	V
Input pin voltage (VP)	V <sub>INmax.2</sub>	-0.3~VP+0.3	V
Input pin voltage (VD)	V <sub>INmax.3</sub>	-0.3~VD+0.3	V
Allowable loss	P <sub>d</sub>	680mW (alone) 1.6W (mounted on board)	W

\* When used at over 25, there is a 14mW reduction for every 1°C.  
(Mounting conditions: 40 × 40 × 1.6mm. Glass epoxy, board mounting density 30%.)

**Recommended Operating Conditions** (Ta = 25°C)

Item	Signal	Rating	Unit
Operating temperature	T <sub>OPR</sub>	-20~+75	°C
Operating voltage (AV <sub>CC</sub> )	V <sub>CCOP1</sub>	4.5~5.5	V
Operating voltage (VP)	V <sub>CCOP2</sub>	4.5~5.5	V
Operating voltage (VD)	V <sub>CCOP3</sub>	4.5~5.5	V

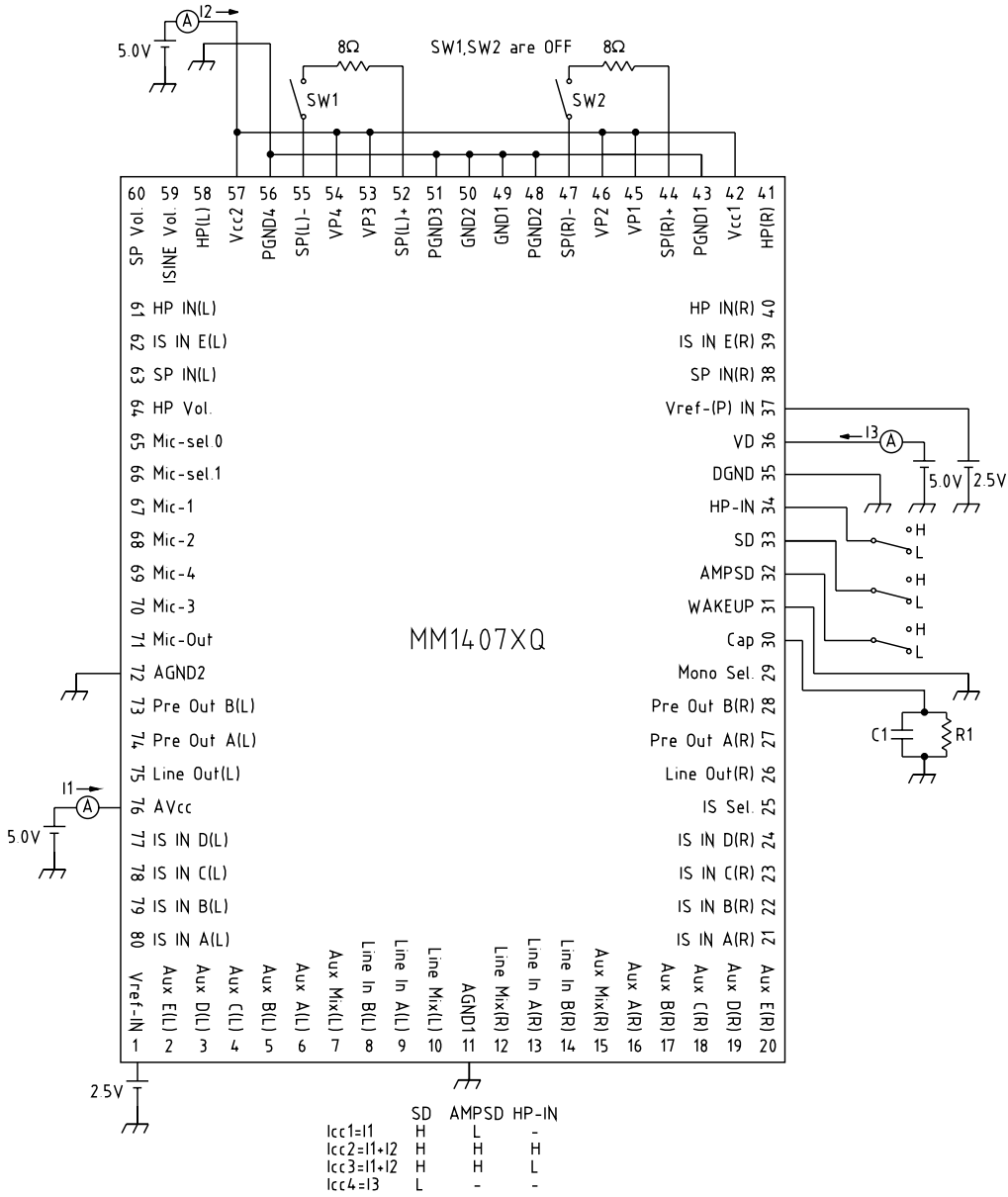
**Electrical Characteristics** (Except where otherwise indicated, Ta = 25°C, AV<sub>CC</sub> = VP = VD = 5V)

Item	Signal	Measurement conditions	Min.	Typ.	Max.	Unit
<b>Consumption Current</b>						
Audio signal control	I <sub>CC1</sub>	For HP AMP, SP AMP OFF		8	12	mA
HP AMP operating	I <sub>CC2</sub>	For Audio ON, SP AMP OFF		18	27	mA
SP AMP operating	I <sub>CC3</sub>	For Audio ON, HP AMP OFF, no load		38	57	mA
During power save	I <sub>CC4</sub>			300	500	µA
<b>Audio signal control Hereafter R<sub>L</sub> = 10k, f<sub>IN</sub> = 1kHz</b>						
Maximum output voltage	V <sub>max.1</sub>	Line Out (L, R), Aux Mix (L, R), Line Mix (L, R) Mic Out THD = 1%	1	1.1		V <sub>rms</sub>
Distortion rate	THD1	Line Out (L, R), Aux Mix (L, R), Line Mix (L, R) Mic Out V <sub>OUT</sub> = 1V <sub>rms</sub>			0.1	%
Gain 1	Gv1	Line Out (L, R), Aux Mix (L, R), Line Mix (L, R)		0		dB
Gain 2	Gv2	Mic Out		12		dB
Input impedance	R <sub>IN</sub>		47			kΩ
Impedance may change during power save, but it will not go below 47k Ω. Signal coupling on input pins may be observed.						
Output impedance	R <sub>OUT</sub>				100	Ω
Separation	CS		60			dB
Output offset 1	V <sub>OFF1</sub>	(V <sub>OUT</sub> ) - (V <sub>ref</sub> -V <sub>IN</sub> )		1	8	mV
Output offset 2 (MIC AMP)	V <sub>OFF2</sub>			1	8	mV
R-Rejection	SVRR	f <sub>r</sub> =100Hz	70	85		dB
Output noise voltage	V <sub>no</sub>	20Hz ~ 20kHz, A curve		30	100	µV <sub>rms</sub>
<b>Phase Relationships</b>						
Line in to Line Mix				Inverted		
Aux A ~ E to Aux Mix				Inverted		
Mic A ~ D to Mic Out				Inverted		
IS IN A ~ D to Line Out				Non-inverted		
IS IN A ~ D to Pre Out				Non-inverted		
IS IN A ~ D to Pre Out phase relationships does not change for Mono Select R Mono or Stereo						

Item	Signal	Measurement conditions	Min.	Typ.	Max.	Unit
<b>Headphone AMP Hereafter <math>R_L = 16\Omega</math>, <math>f_{IN} = 1\text{kHz}</math></b>						
Maximum output voltage 1	Vmax.hp1	PreOutA (L, R) → HP IN (L, R) , $R_L = 10\text{k}\Omega$ , THD = 1%	1	1.1		Vrms
Maximum output voltage 2	Vmax.hp2	PreOutA (L, R) → HP IN (L, R) , $R_L = 16\Omega$ , THD = 1%	350			mVrms
Distortion rate 1	THDhp1	PreOutA (L, R) → HP IN (L, R) EVR = 0dB $V_{OUT} = 1\text{Vrms}$ , $R_L = 10\text{k}\Omega$		0.13	0.25	%
Distortion rate 2	THDhp2	PreOutA (L, R) → HP IN (L, R) EVR = 0dB, $V_{OUT} = 100\text{mVrms}$ , $R_L = 16\Omega$			1	%
Gain 1	Ghp1	EVR; for max. ( $V_{vol1} = 1.25\text{V}$ )		0		dB
Gain 2	Ghp2	EVR; ( $V_{vol1} = 1.0\text{V}$ )		-20		dB
Gain 3	Ghp3	EVR; ( $V_{vol1} = 0.85\text{V}$ )		-40		dB
Gain 4	Ghp4	EVR; ( $V_{vol1} = 0.75\text{V}$ )		-60		dB
Gain 5	Ghp5	EVR; $V_{IN} = 0\text{dBV}$ for MIN ( $V_{vol} = 0.6\text{V}$ ) Mute when $V_{vol} = 0.6\text{V}$ or below			-80	dB
Output level temperature characteristic		EVR setting; gain 1		+3000		ppm/°C
Between-channel gain difference 1	CBhp1	EVR setting; gain 1 ~ 2			±1	dB
Between-channel gain difference 2	CBhp2	EVR setting; gain 3 ~ 4			±3	dB
R-Rejection	SVRRhp	EVR = 0dB, $f_r = 100\text{Hz}$ , $V_{RIPPLE} = -20\text{dBV}$	50	65		dB
Output noise voltage	Vnohp	EVR = 0dB, 20Hz~20kHz, A curve			175	μVrms
Separation	CShp	EVR = 0dB, $f_r = 1\text{kHz}$	50	65		dB
<b>Speaker AMP Hereafter <math>R_L = 8\Omega</math>, BTL connected, <math>f_{IN} = 1\text{kHz}</math></b>						
Maximum output power	Pmax.sp	PreOutB (L, R) → SP IN (L, R) , THD = 10%, EVR = 20dB		0.7		W
Distortion rate	THDsp	PreOutB (L, R) → SP IN (L, R) , EVR = 20dB $P_{OUT} = 300\text{mW}$		1	3	%
Gain 1	Gsp1	EVR; for max. ( $V_{vol} = 1.25\text{V}$ )		20		dB
Gain 2	Gsp2	EVR; ( $V_{vol1} = 1.0\text{V}$ )		0		dB
Gain 3	Gsp3	EVR; ( $V_{vol1} = 0.85\text{V}$ )		-20		dB
Gain 4	Gsp4	EVR; ( $V_{vol1} = 0.75\text{V}$ )		-40		dB
Gain 5	Gsp5	EVR; $V_{IN} = 0\text{dBV}$ for MIN ( $V_{vol} = 0.6\text{V}$ ) Mute when $V_{vol} = 0.6\text{V}$ or below			-60	dB
Output level temperature characteristic		EVR setting; gain 1		+3000		ppm/°C
Between-channel gain difference 1	CBsp1	EVR setting; gain 1 ~ 2			±1	dB
Between-channel gain difference 2	CBsp2	EVR setting; gain 3 ~ 4			±3	dB
R-Rejection	SVRRsp	EVR = 20dBV, $f_r = 100\text{Hz}$ , $V_{RIPPLE} = -20\text{dBV}$	38	45		dB
Output offset	Voffsp	IS IN E VOL = min. SP VOL = 20dB		0	150	mV
Output noise voltage	Vnosp	IS IN E VOL = SP VOL = 20dB, 20Hz~20kHz, A curve			560	μVrms
Separation	CSp	EVR = 20dB, $f_r = 1\text{kHz}$	50	65		dB

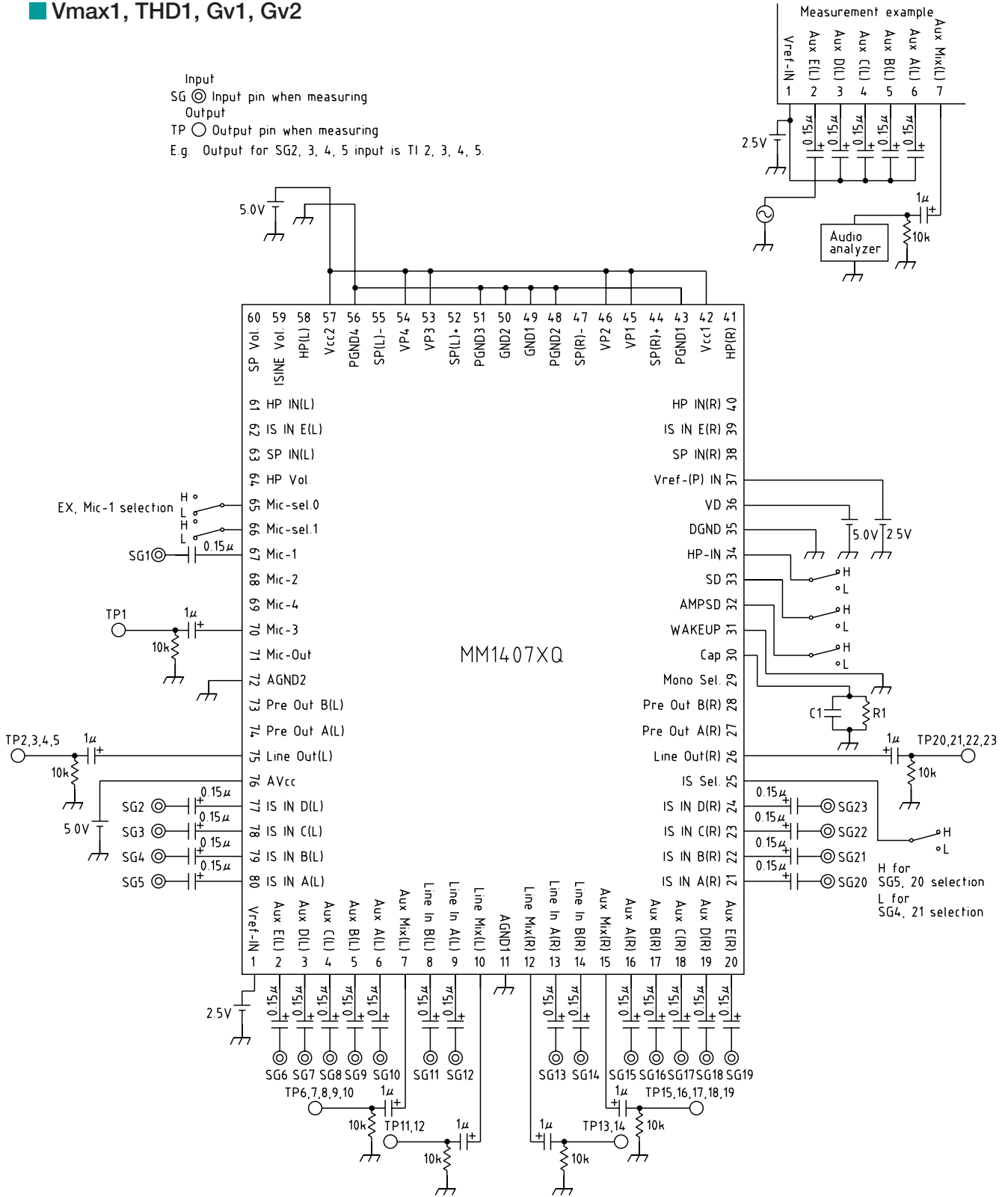
Measuring Circuit

■ Icc1, Icc2, Icc3, Icc4



■ Vmax1, THD1, Gv1, Gv2

Input  
 SG ⊙ Input pin when measuring  
 Output  
 TP ○ Output pin when measuring  
 E.g. Output for SG2, 3, 4, 5 input is TP1, 2, 3, 4, 5.

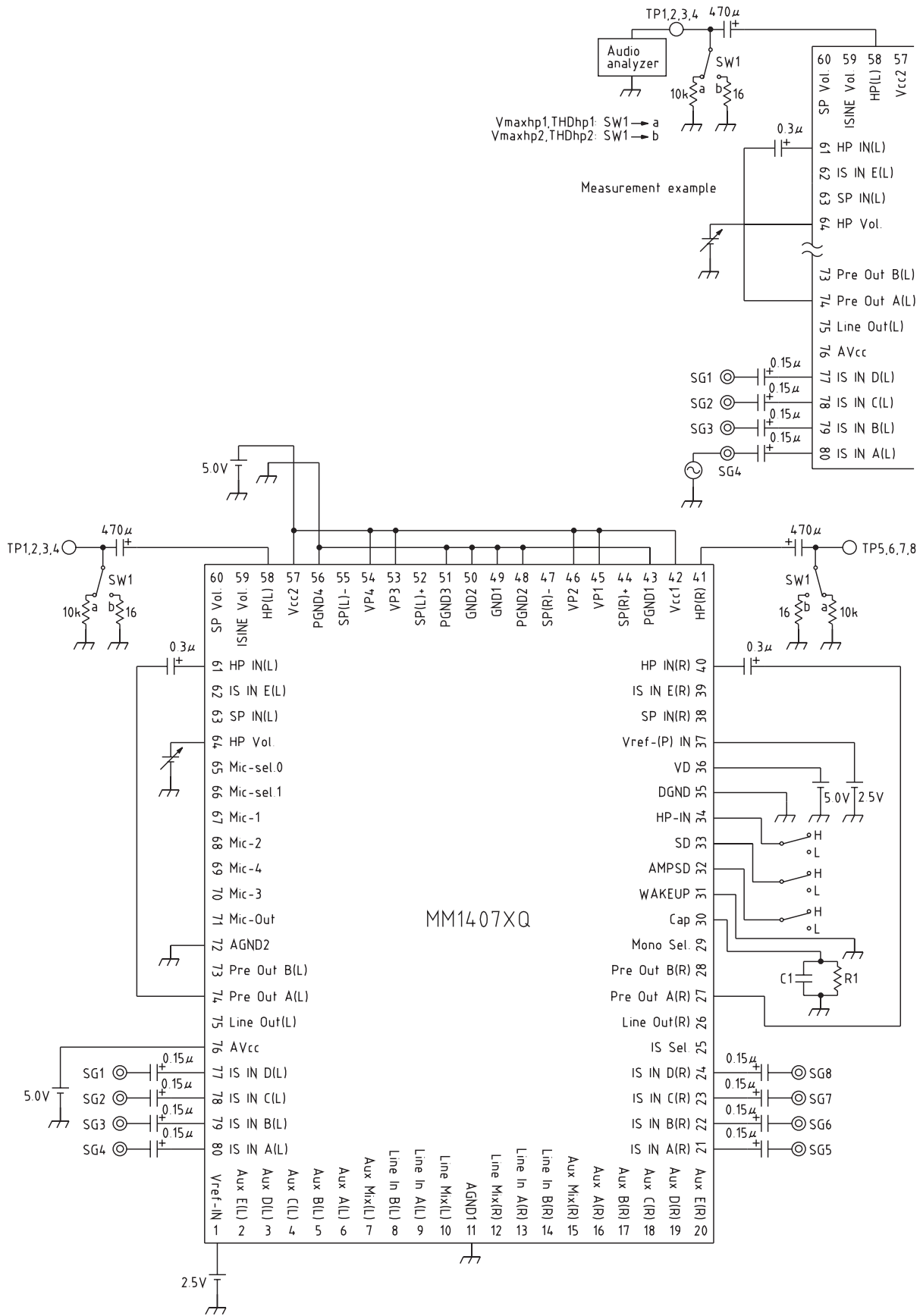




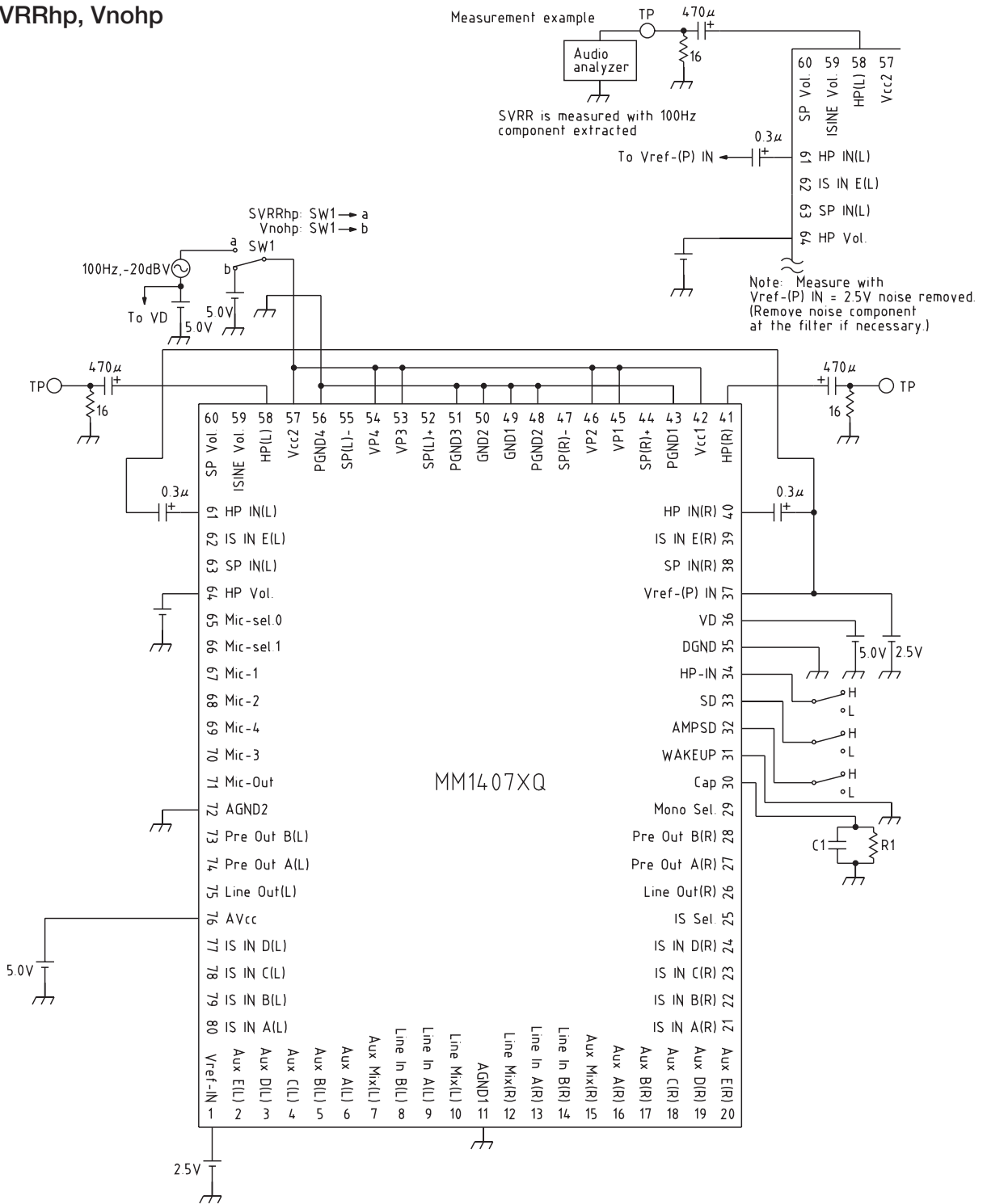




■ Vmaxhp1, Vmaxhp2, THDhp1, THDhp2, Ghp1~5, CBhp1~2

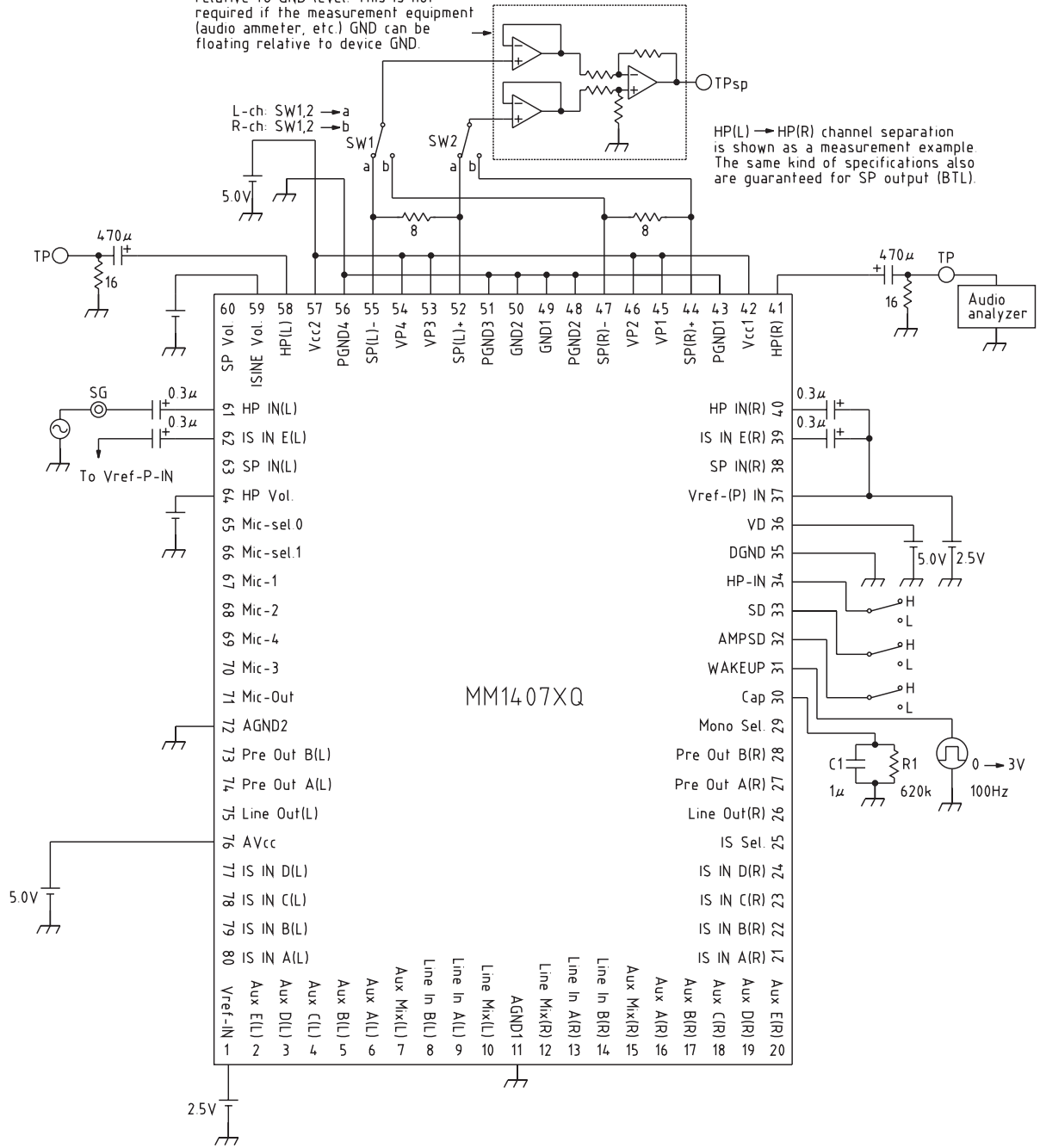


SVRRhp, Vnohp



CSHp

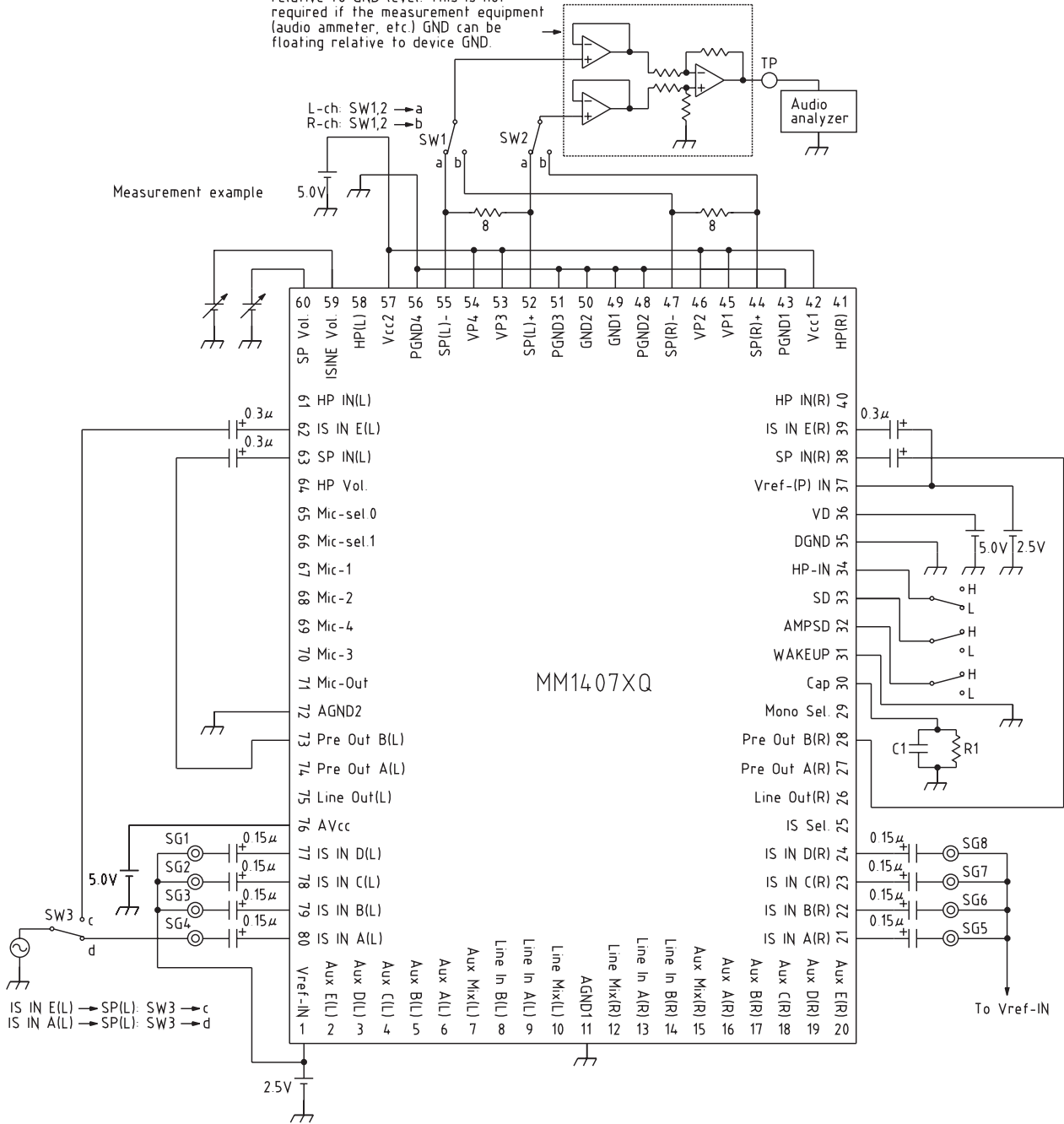
This is an example of a measurement circuit with BTL output measured relative to GND level. This is not required if the measurement equipment (audio ammeter, etc.) GND can be floating relative to device GND.



HP(L) → HP(R) channel separation is shown as a measurement example. The same kind of specifications also are guaranteed for SP output (BTL).

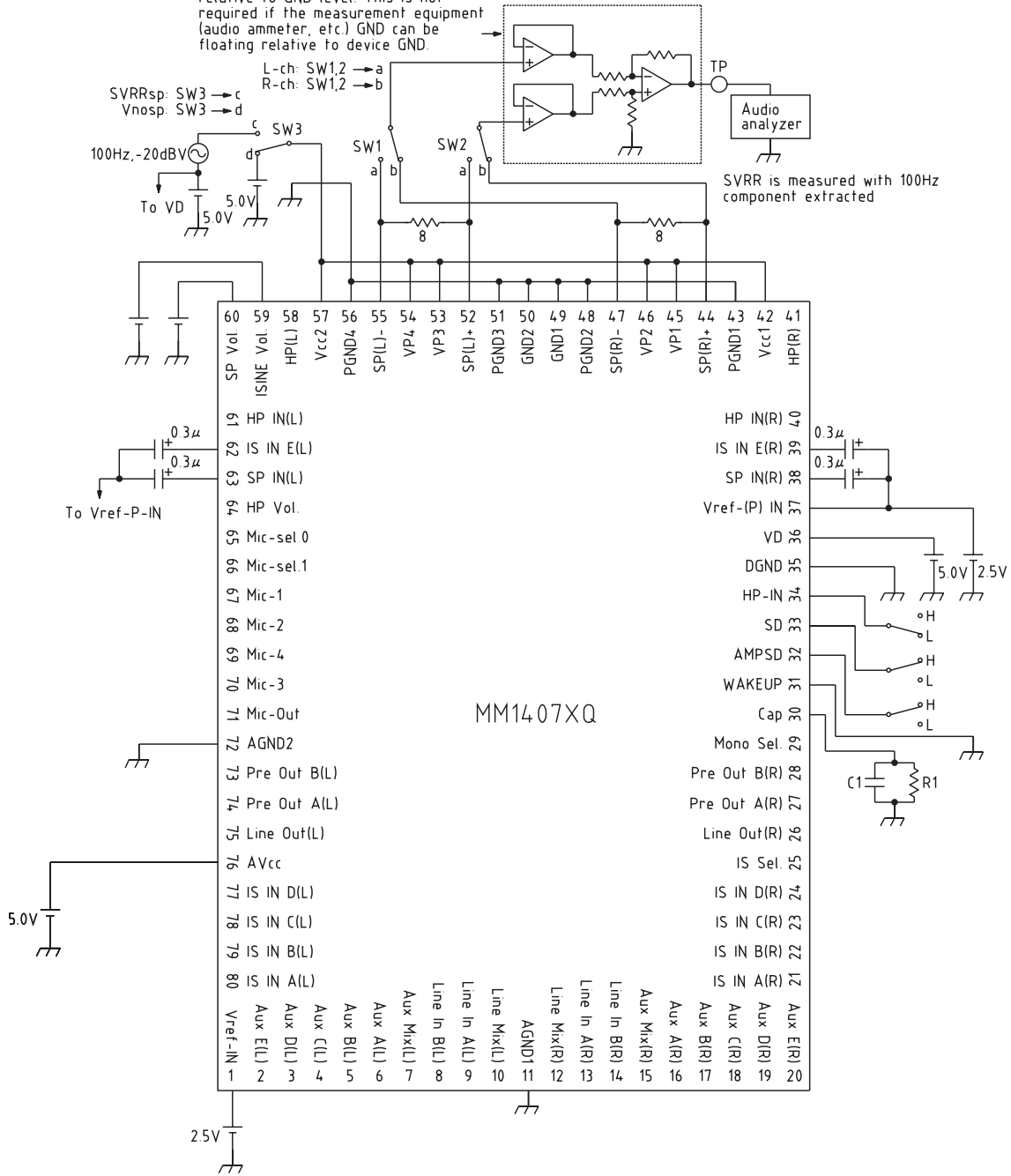
■ Pmaxsp, THDsp, Gsp1~5, CBsp1~2

This is an example of a measurement circuit with BTL output measured relative to GND level. This is not required if the measurement equipment (audio ammeter, etc.) GND can be floating relative to device GND.

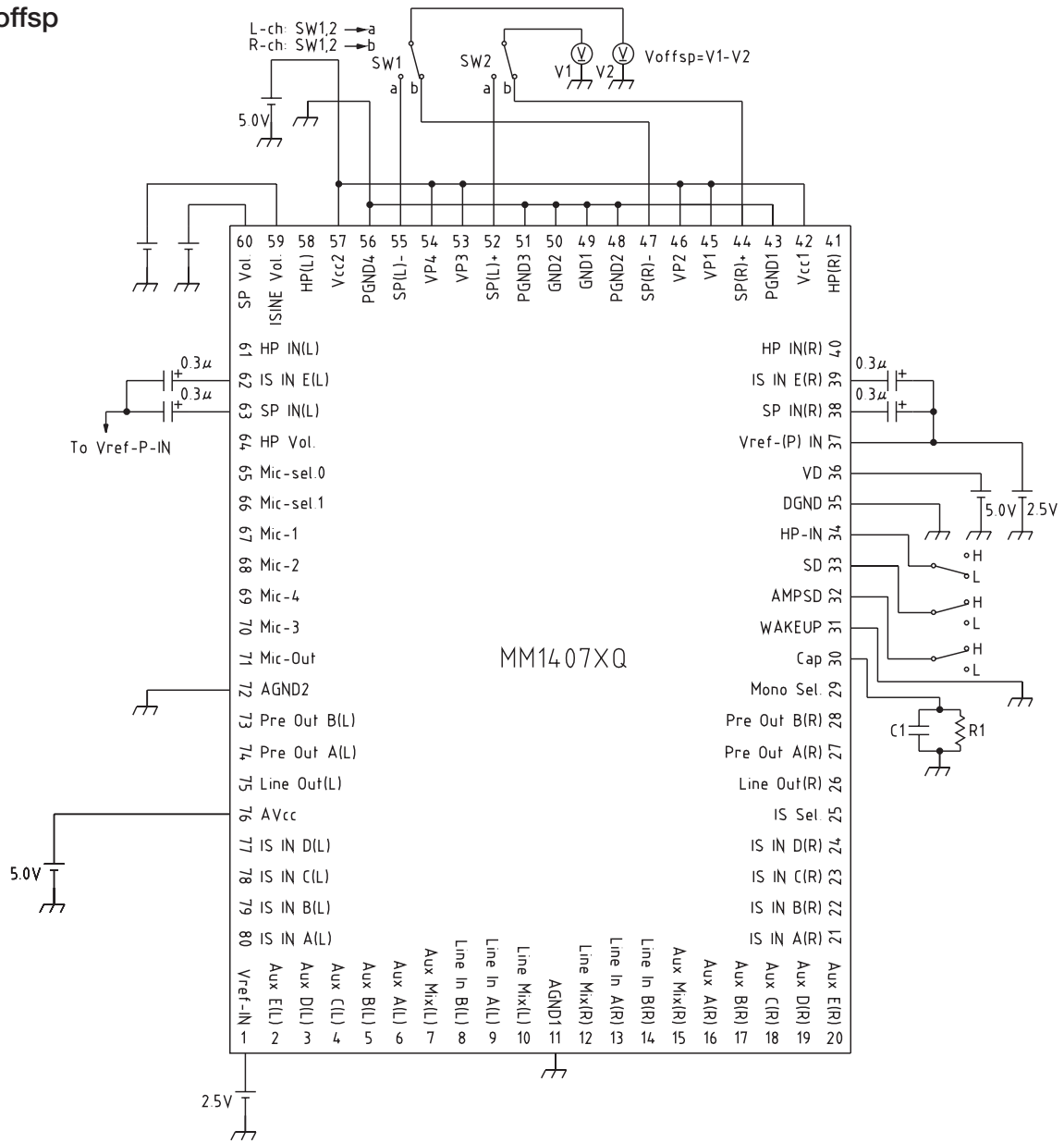


**SVRRsp, Vnosp**

This is an example of a measurement circuit with BTL output measured relative to GND level. This is not required if the measurement equipment (audio ammeter, etc.) GND can be floating relative to device GND.

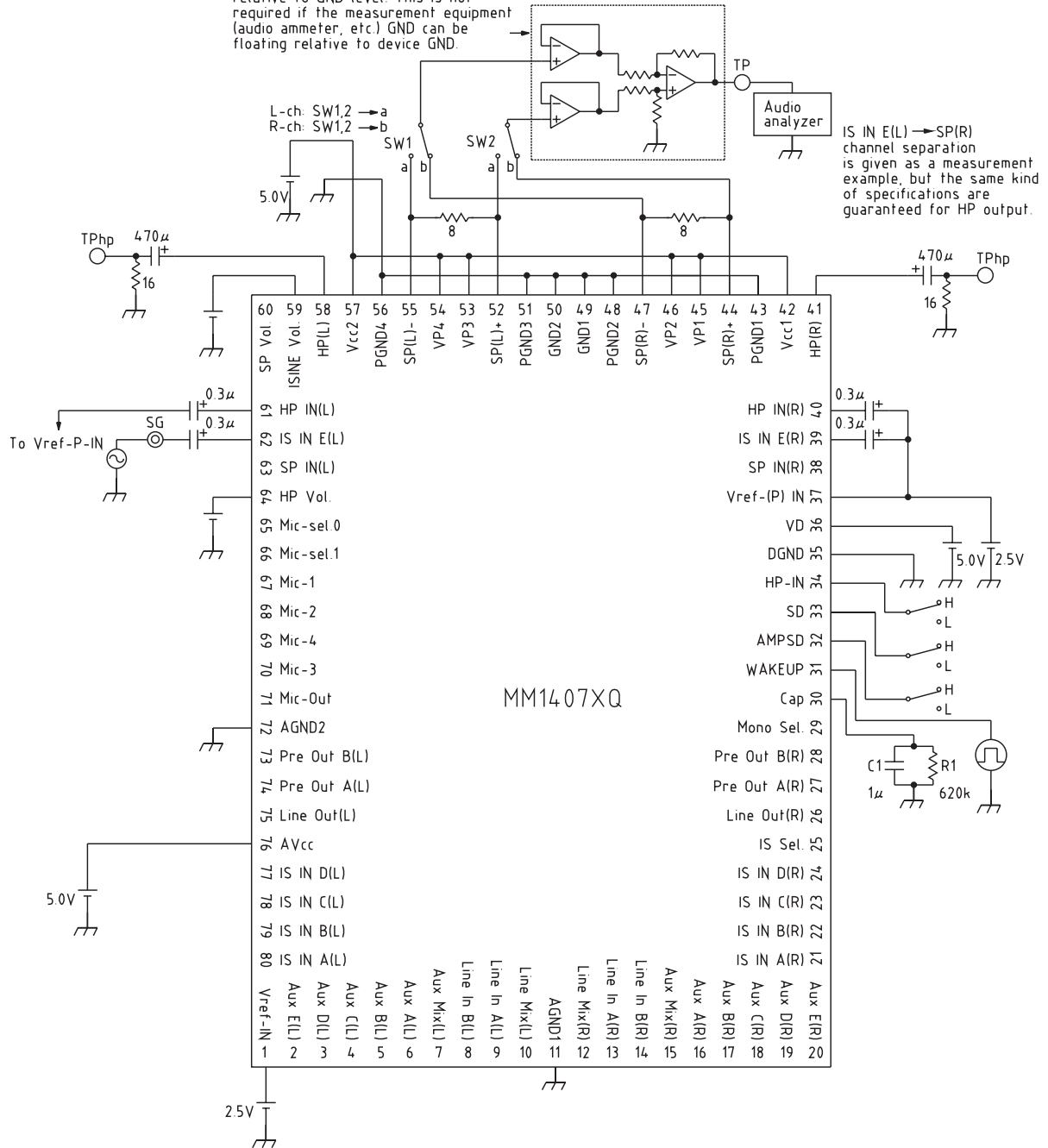


■ Voffsp



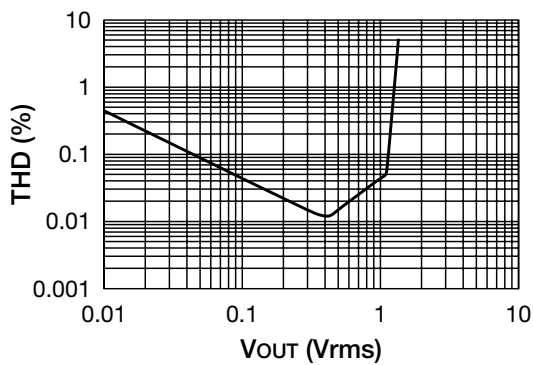
CSsp

This is an example of a measurement circuit with BTL output measured relative to GND level. This is not required if the measurement equipment (audio ammeter, etc.) GND can be floating relative to device GND.

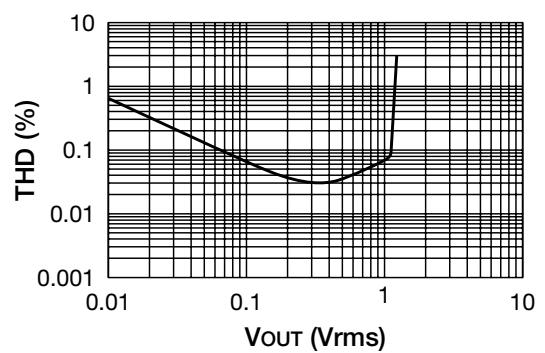


Measuring Circuit

THD Aux-A (L) → AuxMix (L)

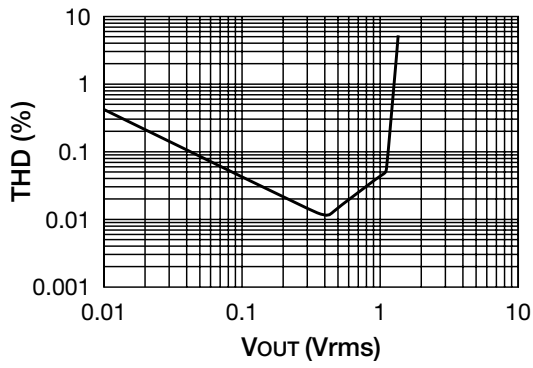


Mic-a → Micont

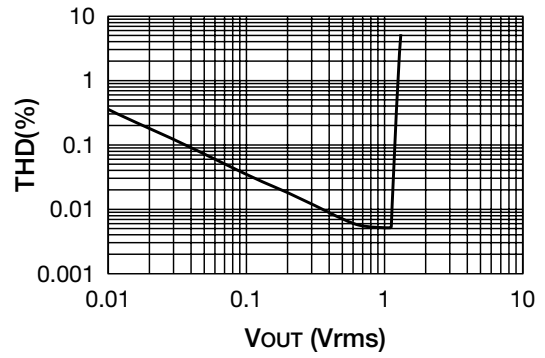




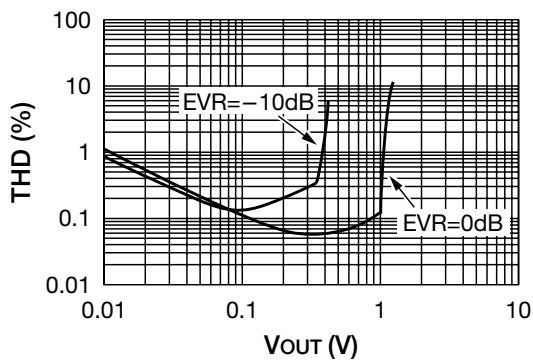
■ Line in A (L) →LineMix (L)



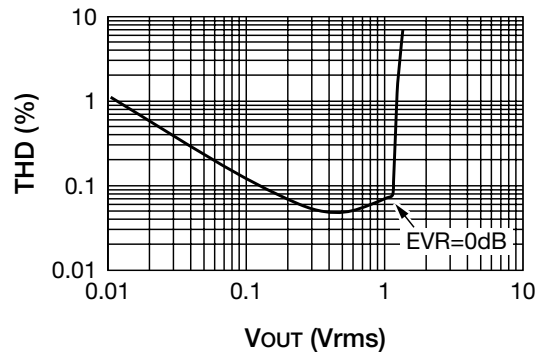
■ THD IS IN A (L) →LineOUT (L)



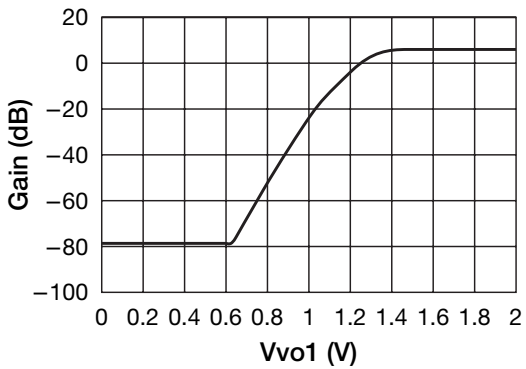
■ THD IS IN A (L) → Per Out A (L) →HP IN (L) →HP (L) RL=16Ω



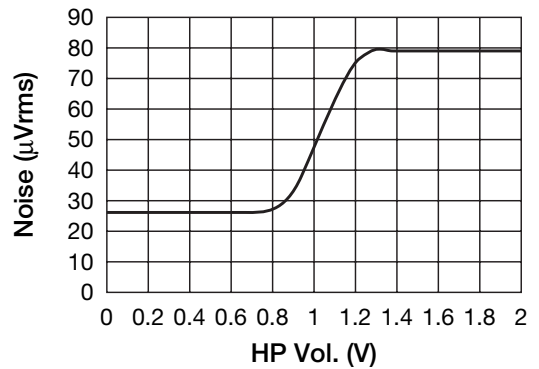
■ THD IS IN A (L) → Per Out A (L) →HP IN (L) →HP (L) RL=10kΩ



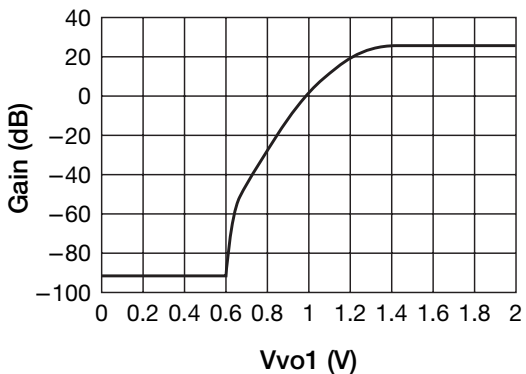
■ EVR-GAIN HP AMP



■ EVR-NOISE HP AMP



■ EVR-GAIN SP AMP



■ EVR-NOISE SP AMP (IS IN E Vol. = 1.25V, SP Vol. → Variable)

