Intel® StrongARM* SA-1110 Microprocessor

Brief Datasheet

Product Features

The Intel® StrongARM SA-1110 Microprocessor (SA-1110) is a device optimized for meeting portable and embedded application requirements. The SA-1110 incorporates a 32-bit StrongARM RISC processor capable of running at up to 206 MHz. The SA-1110 has a large instruction and data cache, memory-management unit (MMU), and read/write buffers. The SA-1110 memory bus interfaces to many device types including synchronous DRAM (SDRAM), synchronous mask ROM (SMROM), and SRAM-like variable latency I/O devices with a shared data ready signal. In addition, the SA-1110 provides system support logic, multiple serial communication channels, a color/gray scale LCD controller, PCMCIA support for up to two sockets, and general-purpose I/O ports.

- High performance
  - —150 Dhrystone 2.1 MIPS @ 133 MHz
  - —235 Dhrystone 2.1 MIPS @ 206 MHz
- Low power (normal mode) †
  - —<240 mW @1.55 V/133 MHz
  - —<400 mW @1.75 V/206 MHz
- Integrated clock generation
  - —Internal phase-locked loop (PLL)
  - —3.686-MHz oscillator
  - —32.768-kHz oscillator
- Power-management features
  - —Normal (full-on) mode
  - —Idle (power-down) mode
  - —Sleep (power-down) mode
- Big and little endian operating modes
- 3.3-V I/O interface
- Memory bus
  - —Interfaces to ROM, synchronous mask ROM (SMROM), Flash, SRAM, SRAM-like variable latency I/O, DRAM, and synchronous DRAM (SDRAM)
  - —Supports two PCMCIA sockets
- 32-way set-associative caches
  - —16 Kbyte instruction cache
  - —8 Kbyte write-back data cache
- 32-entry MMUs
  - —Maps 4 Kbyte, 8 Kbyte, or 1 Mbyte
- Write buffer
  - —8-entry, between 1 and 16 bytes each
- Read buffer
  - —4-entry, 1, 4, or 8 words
- 256 mini-ball grid array (mBGA)

† Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design

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Description

The SA-1110 is a general-purpose, 32-bit RISC microprocessor with a 16 Kbyte instruction cache (Icache), an 8 Kbyte write-back data cache (Dcache), a minicache, a write buffer, a read buffer, an MMU, an LCD controller, and serial I/O combined in a single component. The SA-1110 provides portable applications with high-end computing performance without requiring users to sacrifice available battery time. Its power-management functionality provides

further power savings. For embedded applications, the SA-1110 offers high-performance computing at consumer electronics pricing with MIPS-per-dollar and MIPS-per-watt advantages. The SA-1110 delivers in price/performance and power/performance, making it a chice for portable and embedded applications. The SA-1110 differs from the Intel® StrongARM SA-1100 Microprocessor (SA-1100) only in the features of its memory and PCMCIA controller.

Intel® StrongARM SA-1110 CPU

The SA-1110 CPU implements the ARM V4 architecture as defined in the *ARM Architecture Reference Manual*. Architectural enhancements beyond the ARM V4 are implemented through use of coprocessor 15. Control register reads and writes to coprocessor 15 provide access to MMU, cache, and write and read buffer control registers.

The SA-1110 MMUs provide separate 32-entry translation look-aside buffers (TLBs) for the instruction and data streams. Each of the 32 entries may map segments, large pages, or small pages in memory. The SA-1110 contains 16 Kbyte of instruction cache and 8 Kbyte of data cache. In addition to this, a minicache is provided to prevent periodic large data transfers from thrashing the main data cache. The data and instruction caches are implemented as 32-byte blocks, and provide 32-way associativity, with victim replacement performed in a round-robin fashion. The minicache is 16 entries and is 2-way set associative, implementing the least-recently-used (LRU) algorithm for victim replacement.

The SA-1110 also provides a write buffer and a read buffer. The read buffer allows critical data to be prefetched under software control, preventing pipeline stalls from occurring during external memory reads. The write buffer provides additional system efficiency by buffering between the CPU clock frequency and the actual bus speed when data is being written by the CPU to external memory. The write buffer is eight entries, and allows each entry to contain between 1 and 16 bytes. The read buffer is four entries, and allows each entry to contain 1, 4, or 8 words.

Intel® StrongARM SA-1110 System Control Functions

The SA-1110 provides timers, sophisticated power-management functions, interrupt control, reset control, and on-chip oscillators and PLLs for clock generation. There are 28 general-purpose I/Os, which can, in addition to being directly read or written by the CPU, be programmed to generate an interrupt.

The real-time clock and trim logic run off the 32.768-kHz crystal and provide accuracy of ±5 seconds/month.

The 32-bit OS timer runs off the 3.686-MHz oscillator and is used in companion with the four 32-bit timer match registers. One of the four match registers is used specifically as a watchdog timer interrupt, preventing system lockout from occurring when software or hardware is trapped in a loop state with no controlled exit. The remaining three registers are available for use as interval timers or other user-defined purposes.

The interrupt controller routes all interrupt sources to either an FIQ or IRQ request to the CPU. IRQ is a lower priority interrupt and may be interrupted by FIQ. FIQ is unique to the ARM architecture and allows fast servicing to occur on specific interrupt sources, as determined by the user. There are two levels in servicing interrupts. The first level alerts the user or operating system to what specific module on the SA-1110 experienced an interrupt condition. The second level provides information on what event within the specific module caused an interrupt to be flagged.

The reset controller manages the various reset sources within the SA-1110 and provides the ability to invoke a software reset. In addition, the reset controller tracks the cause of the last known reset, whether a hard reset, soft reset, watchdog timer expiration, or sleep mode reset.

The SA-1110 provides 28 general-purpose I/O pins, which may be programmed to generate interrupts on rising, falling, or both edges. The user is given the option of utilizing a subset of the GPIO pins to support extra functionality in either the serial channels or the LCD controller but may choose to use some, all, or none of the added functionality.

Power-Management Functions

Power management provides three modes of operation: normal, idle, and sleep. In normal mode, the CPU and peripherals are fully powered, but receive active clocks only when in use. In idle mode, clocks to the CPU are stopped, but the clocks to the peripheral functions are active. Power dissipation during idle mode is strongly dependent on the details of the system design. The SA-1110 returns to normal mode from idle mode upon receipt of any enabled interrupt, including interrupts resulting from timers expiring.

In sleep mode, once DRAM is placed in self-refresh, all functions are disabled except for the real-time clock. Wake-up from sleep occurs upon a preprogrammed interrupt and takes 10 ms if the 3.686-MHz clock is enabled or 160 ms if the 3.686-MHz clock is disabled.

Intel® StrongARM SA-1110 Memory and PCMCIA Control Module

The memory and PCMCIA control module (MPCM) supports four banks of fast-page-mode (FPM), extended-data-out (EDO), and/or synchronous DRAM (SDRAM). It also supports up to six banks of static memory; all six banks allow ROM or Flash memory, each with non-burst or burst read timings. Additionally, the lower three static banks support SRAM, the upper three static banks support variable latency I/O devices (with the variable data latency controlled by a shared data ready input), and the lower four static banks support synchronous mask ROM (SMROM). SMROM is supported only on 32-bit data busses. All other dynamic and static memory types and variable latency I/O devices are supported on either 16-bit or 32-bit data busses. Expansion devices are supported through PCMCIA control signals that share the memory bus data and address lines to complete the card interface. Some external glue logic (buffers and transceivers) is necessary to implement the interface. Control is provided to permit two card slots with hot-swap capability.

Intel® StrongARM SA-1110 Peripheral Control Module

The SA-1110 contains a six-channel DMA controller to support the high-speed data movement inherent in serial communications. Note that the LCD controller contains its own independent DMA channels, and that the six DMA channels are available for use by the other peripheral I/O functions. The DMA controller is dedicated to data movement between the serial channels and external memory, whether DRAM, SRAM, Flash, or ROM.

The LCD controller on the SA-1110 supports up to 256 colors and 16 gray-scale levels, on a single or split-screen display with resolution up to 1024 X 1024. The LCD controller is implemented using a patented dithering algorithm controlling the intensity of the information displayed. In the case of color, the dithering algorithm controls which 256 of the 4096 available colors are displayed during any given frame. Frame buffer data is used by the LCD controller as an address value, which is then decoded as an index into a 256-entry by 12-bit wide palette RAM. If 12-bit data is

required, the palette RAM may be bypassed and frame buffer data passes directly to the dither logic. If 16-bit data is required, both the palette RAM and the dither logic are bypassed, and data is sent directly to the LCD controller pins. The LCD controller supports both TFT and STN panels.

Serial port 0 on the SA-1110 implements the universal serial bus (USB) slave protocol, supporting three endpoints operating at 12 Mbps, half duplex.

Serial port 1 on the SA-1110 implements universal asynchronous receiver-transmitter (UART) at a baud rate up to 230 Kbps.

Serial port 2 on the SA-1110 provides logic to support infrared data (IrDA) at either 115 Kbps or 4 Mbps. The low-speed IrDA utilizes the HP-SIR* standard, and the high-speed IrDA implements the 4 PPM standard.

Serial port 3 on the SA-1110 is a UART channel operating from 56.24 bps to 230 Kbps. Modem control signals may be implemented via the GPIO pins if required, but for maximum flexibility these signals are not predefined.

Serial port 4 on the SA-1110 also implements a multimedia communications port or synchronous serial port (MCP/SSP). These ports are traditionally used for interfacing to specific digital/analog I/O devices such as codecs, keyboards, touchpads, audio and record/playback. If required, the SA-1110 provides the user with an option to support both the MCP as well as SSP by dedicating two GPIO pins to the SSP.

The MCP gluelessly interfaces to the Phillips UCB1200*, which provides support for both audio and telecom codecs as well as a touchpad interface and 10 general-purpose I/O pins. The SA-1110 contains two pairs of transmit and receive FIFOs to support the telecom and audio data. The SA-1110 also provides two 21-bit data registers, one each for receive and transmit codec data. The SSP logic interfaces to devices that support the National MicroWire* protocol, the

Texas Instruments* synchronous serial protocols, as well as a subset of the Motorola SPI* protocol. All of these protocols provide methods to interface to keyboard drivers, serial EPROMs, ADC/DAC, as well as special-purpose devices such as voice record/playback. The SSP functions as a master only, communicating to off-chip devices by driving a serial bit-rate clock ranging from 7.2 kHz to 1.8432 MHz, and supports data formats from 4 to 16 bits in length.

Intel® StrongARM SA-1110 Test and Debug Support

The SA-1110 provides debug support via instruction and data breakpoints. These are user-programmable and are implemented through the coprocessor instructions. In the case of an instruction breakpoint, the user may halt the processor after execution of an instruction at a specific address. The data breakpoint allows a user to halt on a specific data pattern as well as on the reference address to that data pattern. There is a data breakpoint mask register that provides further qualification on specific data.

The SA-1110 also provides a JTAG interface, which has been specifically targeted to provide continuity checking for system designs. Supported instructions include EXTEST, SAMPLE/PRELOAD, CLAMP, BYPASS, HIGH-Z, and IDCODE.

Intel® StrongARM SA-1110 Power/Performance Benefits

The SA-1110 continues the StrongARM family of low-power performance. The SA-1110 takes advantage of a 2.0-V nominal process technology. For processors running at 133 MHz, the SA-1110 allows the core voltage to run at 1.55 V. Processors running at 206 MHz run at a core voltage of 1.75 V. The I/O ring runs at 3.3 V to allow simple system interconnections. Another key element in the SA-1110 power strategy is the use of independent conditional clocking trees, which ensure that only currently required units are clocked and other units remain static. The SA-1110 may be run at a variety of frequencies, ranging from 39 MHz up to 206 MHz.

Table 1. SA-1110 Additional Features

	133 MHz	206 MHz
Unit Performance	150 MIPS	235 MIPS
Supply	1.55 V	1.75 V
USB	12 Mbps	12 Mbps
IrDA	115 Kbps, 4 Mbps	115 Kbps, 4 Mbps
UART	230 Kbps	230 Kbps
Codec	UCB1100, UCB1200, SPI, TI, µWire	UCB1100, UCB1200, SPI, TI, µWire
LCD	1-, 2-, 4-, 8-, 12-, 16-bits/pixel	1-, 2-, 4-, 8-, 12-, 16-bits/pixel
Memory	EDO, DRAM, ROM, Flash, SRAM, SMROM, and SDRAM	EDO, DRAM, ROM, Flash, SRAM, SMROM, and SDRAM
Interrupt	FIQ, IRQ, Wake-up	FIQ, IRQ, Wake-up

Figure 1. Block Diagram of the SA-1110

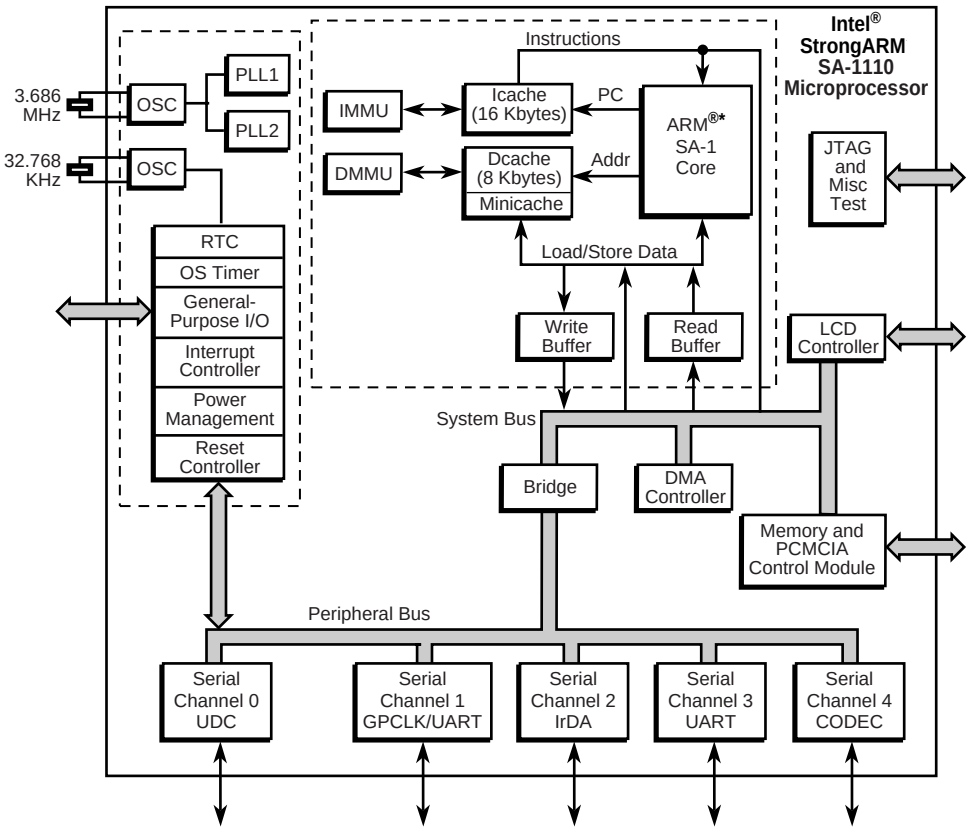

Table 2. SA-1110 Characteristics

Performance	133 MHz	206MHz
Voltage, Power, Temperature, Process, Packaging	150 Dhrystone 2.1 MIPS	235 Dhrystone 2.1 MIPS
VDD Minimum internal power supply voltage Nominal internal power supply voltage Maximum internal power supply voltage	 1.47 V 1.55 V 1.63 V	 1.65 V 1.75 V 2.10 V
VDDX Minimum external power supply voltage Nominal external power supply voltage Maximum external power supply voltage	 3.00 V 3.30 V 3.60 V	 3.00 V 3.30 V 3.60 V
Typical power dissipation †	Normal mode = <240 mW Idle mode = <75 mW Sleep mode = <50 µA	Normal mode = <400 mW Idle mode = <100 mW Sleep mode = <50 µA
Ambient operating temperature	0°C (32°F) min 70°C (158°F) max.	0°C (32°F) min 70°C (158°F) max.
Storage temperature	–20°C to +125°C (–4°F to +257°F)	–20°C to +125°C (–4°F to +257°F)
Packaging	256 mBGA	256 mBGA
Process technology	.35 µm, 3-layer metal	.35 µm, 3-layer metal
Transistor count	2.5 million	2.5 million
Order number	GDS1110AB	GDS1110BB

† Power dissipation, particularly in idle mode, is strongly dependent on the details of the system design.


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