QL5432 QuickPCI Data Sheet

33 MHz/32-Bit PCI Master/Target with Embedded Programmable Logic and Dual Port SRAM

Device Highlights

High Performance PCI Controller

QL5432 supports new enhanced features added to QL5232:

- All PCI commands (including configuration and MWI)
- Fully-customizable byte enables as a master
- Zero-wait-state write and one-wait-state read Target interface
- Target interface supports retry, disconnect with/without data transfer, and target abort
- Target aborts
- Has 125 more logic cells in FPGA section, but 2 less RAM blocks
- Pin compatible with QL5232

QL5432 also supports the original features of QL5232:

- 32-bit/33 MHz PCI Master/Target
- Zero-wait state PCI Master provides 132 MBps transfer rates
- Programmable back-end interface to optional local processor
- Independent PCI bus (33 MHz) and local bus (up to 160 MHz) clocks
- Fully customizable PCI configuration space
- Configurable FIFOs with depths up to 256
- Reference design with driver code (Win 95/98/2000/NT4.0) available
- PCI v2.2 compliant
- Supports Type 0 configuration cycles in Target mode
- 3.3 V, 5 V tolerant PCI signaling supports universal PCI adapter designs
- 3.3 V CMOS in 208-pin PQFP and 456-pin PBGA
- Supports endian conversions
- Unlimited/continuous burst transfers supported

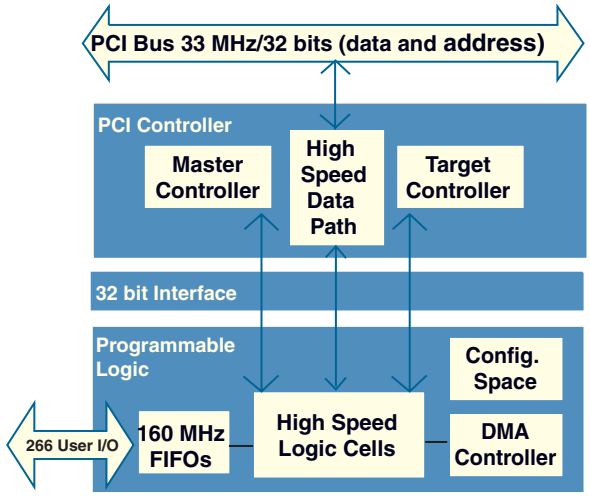
Extendable PCI Functionality

- Support for configuration space from 0x40 to 0x3FF
- Multi-function, expanded capabilities, and expansion ROM capable
- Power management, compact PCI, hot-swap/hot-plug compatible
- PCI v2.2 Power Management Spec compatible
- PCI v2.2 Vital Product Data (VPD) configuration support

Programmable logic

- 1,417 logic cells
- 23,040 RAM bits, up to 266 I/O pins
- 250 MHz 16-bit counters, 275 MHz Datapaths, 160 MHz FIFOs
- All back-end interface and glue-logic can be implemented on chip
- Any combination of FIFOs that require 20 or less QuickLogic RAM modules
- Six 32-bit busses interface between the PCI Controller and the Programmable Logic

Figure 1: QL5432 Block Diagram



Architecture Overview

The QL5432 device in the QuickLogic QuickPCI Embedded Standard Product (ESP) family provides a complete and customizable PCI interface solution combined with programmable logic. This device eliminates any need for the designer to worry about PCI bus compliance, yet allows for the maximum 32-bit PCI bus bandwidth (132 MBps).

The programmable logic portion of the device contains 1,417 QuickLogic logic cells and 12 QuickLogic dual-port RAM blocks. These configurable RAM blocks can be configured in many width/depth combinations. They can also be combined with logic cells to form FIFOs, or be initialized via Serial EEPROM on power-up and used as ROMs. See **RAM Module Features** on page 9 for more information.

The QL5432 device meets PCI v2.2 electrical and timing specifications and has been fully hardware-tested. The QL5432 device features 3.3 V operation with multi-volt compatible I/Os. Therefore, it can easily operate in 3 V systems and is fully compatible with 3.3 V, 5 V or Universal PCI card applications.

PCI Controller

The PCI Controller is a 32-bit/33 MHz PCI v2.2 compliant Master/Target Controller. It is capable of infinite length Master Write and Read transactions at zero-wait-states (132 MBps). The Master will never insert wait-states during transfers, so data must be supplied or received by FIFOs, which can be configured in the programmable region of the device. The Master is capable of initiating any type of PCI command, including configuration cycles and Memory Write and Invalidate (MWI). This enables the QL5432 device to act as a PCI host. The Master Controller is most often operated by a DMA Controller in the programmable region of the device. A DMA Controller reference design is available.

The Target interface offers full PCI Configuration Space and flexible target addressing. It supports zero-wait-state Target write and one-wait-state Target read operations. It also supports retry, disconnect with/without data transfer, and target abort requested by the backend. Any number of 32-bit BARs may be configured as memory or I/O space. All required and optional PCI v2.2 Configuration Space registers can be implemented within the programmable region of the device. A reference design of a Target Configuration and Addressing module is provided.

The interface ports are divided into a set of ports for Master transactions and a set for Target transactions. The Master DMA controller and Target Configuration Space and Address Decoding are done in the programmable logic region of the device. Since these functions are not timing critical, leaving these elements in the programmable region allows the greatest degree of flexibility to the designer. Reference DMA controller, Configuration Space, and Address Decoding blocks are included so that the design cycle can be minimized.

PCI Configuration Space and Address Decode

The configuration space is completely customizable in the programmable region of the device.

PCI address and command decoding is performed by logic in the programmable section of the device. This allows support for any size of memory or I/O space for backend logic. It also allows the user to implement any subset of the PCI commands supported by the QL5432. QuickLogic provides a reference Address Register/Counter and Command Decode block.

DMA Master/Target Control

The customizable DMA controller included with the QuickWorks design software contains the following features:

- Configurable DMA count size for Reads and Writes (up to 30-bits)
- Configurable DMA burst size for PCI (including unlimited/continuous burst)
- Customizable PCI command to use by core
- Customizable Byte Enable signal
- Programmable Arbitration between DMA Read & Write transactions
- DMA Registers may be mapped to any area of Target Memory Space
  - Read Address (32-bit register)
  - Write Address (32-bit register)
  - Read Length (16-bit register) / Write Length (16-bit register)
  - Control and Status (32-bit register, includes 8 bit Burst Length)
- DMA Registers are available to the local design or the PCI bus
- Programmable Interrupt Control to signal end of transfer or other event

Configurable FIFOs

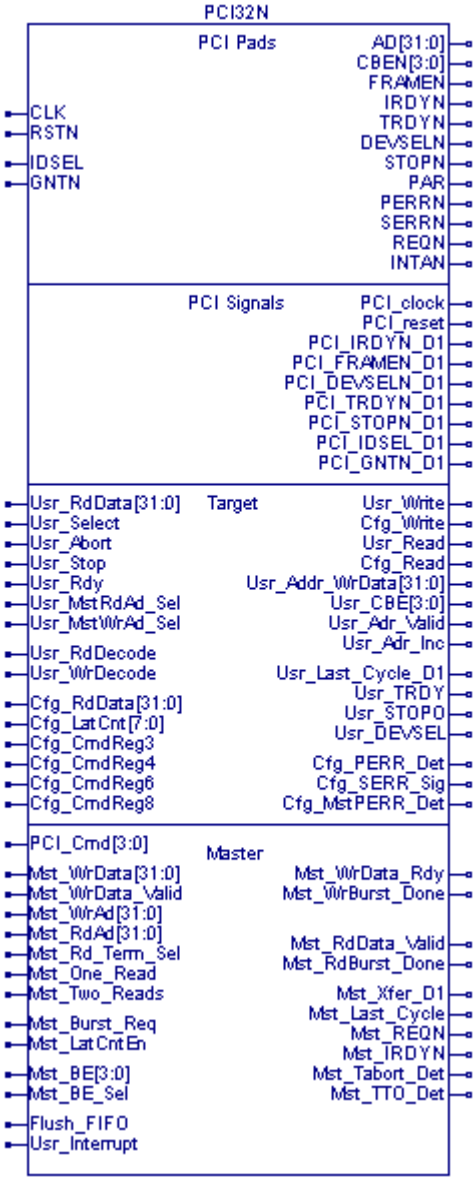
QuickWorks SpDE has a Creation Wizard that is used to create FIFOs. FIFOs may be designed up to 256 deep. Using the 20 QuickLogic RAM modules, the combinations include:

- 10 FIFOs at 64 deep (36 wide)
- 5 FIFOs at 128 deep (36 wide)
- 2 FIFO at 256 deep (40 wide)
- 1 FIFO at 215 deep (40 wide)

PCI Interface Symbol

Figure 2 shows the interface symbol to use in the schematic design to attach the local interface programmable logic design to the PCI core. This symbol is used in schematic or mixed schematic/HDL design flows in the QuickWorks software. If designing with a top-level Verilog or VHDL file, use a structural instantiation of this PCI32N block, instead of a graphical symbol.

Figure 2: PCI Interface Symbol



Internal Port Descriptions

Signals that end with the character 'N' should be considered active-low (for example, Mst_IRDYN). 'I' indicates that it is an input to the core, 'O' indicates it is an output of the core, and 'B' indicates it is a bi-directional signal (only on PCI pins).

Master Interface Signals

The master interface signals for QL5432 PCI32N are shown in **Table 1**.

Table 1: QL5432 PCI32N Master Interface Signals

Signal	Type	Description
PCI_Cmd[3:0]	I	PCI command to be used for the master transaction. This signal must remain unchanged throughout the period when Mst_Burst_Req is active. PCI commands considered as reads include: '0000' Interrupt Acknowledge '0010' I/O Read '0110' Memory Read '1010' Configuration Read '1100' Memory Read Multiple '1110' Memory Read Line PCI commands considered as writes include: '0001' Special Cycle '0011' I/O Write '0111' Memory Write '1011' Configuration Write '1111' Memory Write and Invalidate Users should make sure that only valid PCI commands are supplied.
Mst_Burst_Req	I	Request use of the PCI bus. When it is active, the core requests the PCI bus and once granted, it generates a master transaction using the command specified by PCI_Cmd[3:0]. This signal should be held active until all requested data are transferred on the PCI bus, and should be deactivated in the second clock cycle following the last data transfer on PCI (otherwise it is considered as requesting a new transaction).
Mst_WrAd[31:0]	I	Address for master DMA writes. This address must always be valid from the beginning of a DMA write until the DMA write operation is completed. It should be incremented (by 4 bytes) each time data is transferred on PCI (Mst_Xfer_D1 is active).
Mst_RdAd[31:0]	I	Address for master DMA reads. This address must always be valid from the beginning of a DMA read until the DMA read operation is completed. It should be incremented (by 4 bytes) each time data is transferred between the PCI core and the backend (Mst_RdData_Valid is active).
Mst_WrData[31:0]	I	Data for master DMA writes (to PCI bus).
Mst_BE[3:0]	I	Byte enables for master DMA reads and writes. Active-low.
Mst_WrData_Valid	I	When this signal is asserted, the core is notified that Mst_WrData[31:0] is valid in master write requests. If Mst_BE_Sel is active (high), it also means Mst_BE[3:0] is valid in both master write/read requests.
Mst_WrData_Rdy	O	Data receives acknowledge from the core for Mst_WrData[31:0] in master write requests, and Mst_BE[3:0] in both write/read requests if Mst_BE_Sel is active (high). This serves as the PUSH control for the internal FIFO and normally the POP control for the external FIFO in the backend which provides data and byte enables to the core.

Table 1: QL5432 PCI32N Master Interface Signals (Continued)

Signal	Type	Description
Mst_BE_Sel	I	Byte enable select for master transactions. When low, Mst_BE[3:0] should remain unchanged throughout the entire transfer (when Mst_Burst_Req is active) and it is used for every data phase of the master transaction. When high, Mst_BE[3:0] pushed into internal FIFO using Mst_WrData_Valid (along with data in case of a master write) is used. Should be held unchanged throughout the transaction.
Mst_WrBurst_Done	O	Requested master write transaction is completed. Active for only one clock cycle.
Mst_Rd_Term_Sel	I	Master read termination mode select when Mst_BE_Sel is high. When both Mst_BE_Sel and Mst_Rd_Term_Sel are high, master read termination happens when the internal FIFO is empty (out of byte enables). Mst_Two_Reads and Mst_One_Read (from backend) are ignored in this case. When either Mst_BE_Sel or Mst_Rd_Term_Sel is low, Mst_Two_Reads and Mst_One_Read are used to signal end of master read. Should be held unchanged throughout the transaction.
Mst_One_Read	I	This signals to the core that only one data transfer remains to be read in the burst read. Should be asserted after the backend receives the second last piece of data from the core. In the case of a single-data-phase master read request, it should be asserted at the time it makes the request.
Mst_Two_Reads	I	This signals to the core that only two data transfers remain to be read in the burst read. Should be asserted after the backend receives the third last piece of data from the core. It has no effect on single-data-phase master read requests.
Mst_RdData_Valid	O	Master read data valid on Usr_Addr_WrData[31:0] from the core to the backend. This serves as the PUSH control for the external FIFO in the backend that receives data from the core.
Mst_RdBurst_Done	O	Requested master read transaction is completed. Active for only one clock cycle.
Flush_FIFO	I	Internal FIFO flush. The internal FIFO is flushed immediately after it is sampled active on the rising edge of a PCI clock. Not usually used.
Mst_LatCntEn	I	Enable Latency Counter. Set to 0 to ignore the Latency Timer in the PCI configuration space (offset 0Ch). For full PCI compliance, this port should be always set to 1.
Mst_Xfer_D1	O	Data was transferred on the PCI bus in the previous clock cycle in PCI32_25N-initiated master transactions. Useful for updating DMA transfer counts on DMA Read operations and for updating master write address on DMA Write operations.
Mst_Last_Cycle	O	Active during the last data transfer of a master transaction.
Mst_REQN	O	Copy of the PCI REQN signal generated by QL5432 as a PCI master. Not usually used in the backend design.
Mst_IRDYN	O	Copy of the PCI IRDYN signal generated by QL5432 as a PCI master. Valid only when QL5432 is the PCI master. Kept high otherwise. Not usually used in the backend design.
Mst_Tabort_Det	O	Target abort detected during master transaction. This is normally an error condition to be handled in the DMA controller.
Mst_TTO_Det	O	Target timeout detected (master abort, no response from target). This is normally an error condition to be handled in the DMA controller.

Target Interface Signals

The target interface signals for QL5432 PCI32N are shown in **Table 2**.

Table 2: QL5432 PCI32N Target Interface Signals

Signal	Type	Description
Usr_Addr_WrData[31:0]	O	Target address and target write data. During all target accesses, the address is presented on Usr_Addr_WrData[31:0] at the same time Usr_Adr_Valid is active. During target write transactions, this port also presents valid write data to the PCI configuration space or user logic when Usr_Adr_Inc is active. During master read transactions, this port also presents valid data read from PCI to the backend. This is the registered version of the PCI AD[31:0] signal.
Usr_CBE[3:0]	O	PCI command and byte enables. During target accesses, the PCI command is presented on Usr_CBE[3:0] at the same time Usr_Adr_Valid is active. This port also presents active-low byte enables to the PCI configuration space or user logic. This is the registered version of the PCI CBEN[3:0] signal.
Usr_Adr_Valid	O	Indicates the beginning of a PCI transaction, and that a target address is valid on Usr_Addr_WrData[31:0] and the PCI command is valid on Usr_CBE[3:0]. When this signal is active, the target address must be latched and decoded to determine if this address belongs to the device memory or I/O space. Also, the PCI command must be decoded to determine the type of PCI transaction. On subsequent clocks of a target access, this signal is low, indicating that the address is no longer on Usr_Addr_WrData[31:0].
Usr_Adr_Inc	O	This signal, when asserted, indicates that the target address should be incremented, because the previous data transfer has completed. During burst target accesses, the target address is only presented to the backend at the beginning of the transaction when Usr_Adr_Valid is active, and must therefore be latched and incremented (by 4) for subsequent data transfers. For target write transactions, Usr_Adr_Inc indicates valid data on Usr_Addr_WrData[31:0] that must be accepted by the backend logic (regardless of the state of Usr_Rdy). For read transactions, Usr_Adr_Inc signals to the backend that the core has presented the read data onto the PCI bus (has asserted TRDYN).
Usr_RdDecode	I	This signal must be asserted by the backend when a user read command (e.g., Memory Read, Memory Read Line, Memory Read Multiple, I/O Read, etc.) has been decoded from Usr_CBE[3:0]. It is acknowledged by the core only when Usr_Adr_Valid is active.
Usr_WrDecode	I	This signal must be asserted by the backend when a user write command (e.g., Memory Write, Memory Write and Invalidate, I/O Write, etc.) has been decoded from Usr_CBE[3:0]. It is acknowledged by the core only when Usr_Adr_Valid is active.
Usr_Select	I	This signal must be driven active when the address on Usr_Addr_WrData[31:0] has been decoded and determined to be within the address space of the device. Usr_Addr_WrData[31:0] must be compared to each of the valid Base Address Registers in the PCI configuration space. Also, this signal must be gated by the Memory Access Enable or I/O Access Enable registers in the PCI configuration space (Command Register bits 1 or 0 at offset 04h). This signal is acknowledged by the core only when Usr_Adr_Valid is active.
Usr_Write	O	This signal is active throughout a “user write” transaction, which has been decoded by Usr_WrDecode at the beginning of the transaction. The write strobe for individual DWORDs of data (on Usr_Addr_WrData[31:0]) during a user write transaction should be generated by logically ANDing this signal with Usr_Adr_Inc.

Table 2: QL5432 PCI32N Target Interface Signals (Continued)

Signal	Type	Description
Cfg_Write	O	This signal is active throughout a “configuration write” transaction. The write strobe for individual DWORDs of data (on Usr_Addr_WrData[31:0]) during a configuration write transaction should be generated by logically ANDing this signal with Usr_Adr_Inc.
Usr_Read	O	This signal is active throughout a “user read” transaction, which has been decoded by Usr_RdDecode at the beginning of the transaction.
Cfg_Read	O	This signal is active throughout a “configuration read” transaction.
Cfg_RdData[31:0]	I	Data from the PCI configuration registers, required to be presented during PCI configuration reads.
Usr_RdData[31:0]	I	Data from the backend, required to be presented during user reads.
Cfg_CmdReg3	I	Bits 3 from the Command Register in the PCI configuration space (offset 04h). Enable Special Cycle monitoring. If high, the core reports data parity error in Special Cycles through SERRN if Cfg_CmdReg8 is active.
Cfg_CmdReg4	I	Bits 4 from the Command Register in the PCI configuration space (offset 04h). Memory Write and Invalidate (MWI) Enable. If high, the core can generate MWI transactions as requested by the backend. Otherwise it uses Memory Write instead even if MWI is requested. Note that there are also other conditions that limit whether MWI can be generated by the core.
Cfg_CmdReg6	I	Bits 6 from the Command Register in the PCI configuration space (offset 04h). Parity Error Response. If high, the core uses PERRN to report data parity errors. Otherwise the core always tristates PERRN.
Cfg_CmdReg8	I	Bits 8 from the Command Register in the PCI configuration space (offset 04h). SERRN Enable. If high, the core uses SERRN to report address parity errors if Cfg_CmdReg6 is high. Otherwise the core always tristates SERRN.
Cfg_LatCnt[7:0]	I	8-bit value of the Latency Timer in the PCI configuration space (offset 0Ch).
Cfg_CacheLineSize[7:2]	I	Upper 6 bits of the Cache Line Size register in the configuration space (offset 0Ch). The core always assumes that the lower two bits ([1:0]) of the Cache Line Size register to be “00”.
Usr_MstRdAd_Sel	I	Used when a target read operation should return the value set on Mst_RdAd[31:0] instead of Usr_RdData[31:0]. This select pin saves on logic which would otherwise need to be used to multiplex Mst_RdAd[31:0] into the Usr_RdData[31:0] bus. When this signal is asserted, the data on Usr_RdData[31:0] is ignored.
Usr_MstWrAd_Sel	I	Used when a target read operation should return the value set on Mst_WrAd[31:0] instead of Usr_RdData[31:0]. This select pin saves on logic which would otherwise need to be used to multiplex Mst_WrAd[31:0] into the Usr_RdData[31:0] bus. When this signal is asserted, the data on Usr_RdData[31:0] is ignored.
Cfg_PERR_Det	O	Parity error detected on the PCI bus. When this signal is active, bit 15 of the Status Register must be set in the PCI configuration space (offset 04h).
Cfg_SERR_Sig	O	System error asserted on the PCI bus. When this signal is active, the Signaled System Error bit, bit 14 of the Status Register, must be set in the PCI configuration space (offset 04h).
Cfg_MstPERR_Det	O	Data parity error detected on the PCI bus by the master. When this signal is active, bit 8 of the Status Register must be set in the PCI configuration space (offset 04h).
Usr_TRDY	O	Inverted copy of the TRDYN signal as driven by the PCI target interface. Valid only within target accesses to the core.

Table 2: QL5432 PCI32N Target Interface Signals (Continued)

Signal	Type	Description
Usr_STOP	O	Inverted copy of the STOPN signal as driven by the PCI target interface. Valid only within target accesses to the core.
Usr_DEVSEL	O	Inverted copy of the DEVSELN signal as driven by the PCI target interface. Valid only within target accesses to the core.
Usr_Last_Cycle_D1	O	Active one clock cycle after the last data phase occurs on PCI. Active only for one clock cycle.
Usr_Rdy	I	Used to delay (add wait states to) a target PCI transaction when the backend needs additional time to provide data (read) or accept data (write). Subject to PCI latency restrictions if PCI compliance is needed.
Usr_Stop	I	Used to prematurely stop a PCI target access.
Usr_Abort	I	Used to signal Target Abort on PCI when the backend is unable to complete a transaction and does not want the master to retry. Rarely used.

Internal PCI Signals

The internal PCI signals for QL5432 PCI32N are shown in **Table 3**.

Table 3: QL5432 PCI32N Internal PCI Signals

Signal	Type	Description
PCI_clock	O	PCI clock. On a global clock network.
PCI_reset	O	Inverted and synchronized PCI reset signal. Active high. When the PCI reset is removed, this signal also goes from high to low but synchronized to the PCI clock. On a global clock network.
PCI_IRDYN_D1	O	Copy of the IRDYN signal from the PCI bus, delayed by one clock.
PCI_FRAMEN_D1	O	Copy of the FRAMEN signal from the PCI bus, delayed by one clock.
PCI_DEVSELN_D1	O	Copy of the DEVSELN signal from the PCI bus, delayed by one clock.
PCI_TRDYN_D1	O	Copy of the TRDYN signal from the PCI bus, delayed by one clock.
PCI_STOPN_D1	O	Copy of the STOPN signal from the PCI bus, delayed by one clock.
PCI_IDSEL_D1	O	Copy of the IDSEL signal from the PCI bus, delayed by one clock.
PCI_GNTN_D1	O	Copy of the GNTN signal from the PCI bus, delayed by one clock.

RAM Module Features

The QL5432 device has twenty 1,152-bit RAM modules, for a total of 23,040 RAM bits. Using two "mode" pins, designers can configure each module into 64 (deep) x18 (wide), 128x9, 256x4, or 512x2 blocks (see **Figure 3**). The blocks are also easily cascadable to increase their effective width or depth. See **Table 4** for RAM mode configurations.

Figure 3: RAM Module

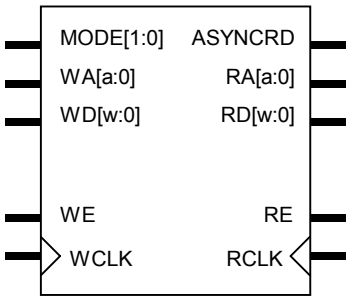


Table 4: RAM Configurations

Mode	Address Buses [a:0]	Data Buses [w:0]
64x18	[5:0]	[17:0]
128x9	[6:0]	[8:0]
256x4	[7:0]	[3:0]
512x2	[8:0]	[1:0]

The RAM modules are dual-ported, with completely independent READ and WRITE ports and separate READ and WRITE clocks. The READ ports support asynchronous and synchronous operation, while the WRITE ports support synchronous operation. Each port has 18 data lines and 9 address lines, allowing word lengths of up to 18 bits and address spaces of up to 512 words. Depending on the mode selected, however, some higher order data or address lines may not be used.

The Write Enable (WE) line acts as a clock enable for synchronous write operation. The Read Enable (RE) acts as a clock enable for synchronous READ operation (ASYNCRD input low), or as a flow-through enable for asynchronous READ operation (ASYNCRD input high).

Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules. This approach allows up to 512-deep configurations as large as 40 bits wide in the QL5432 device.

A similar technique can be used to create depths greater than 512 words. In this case address signals higher than the eighth bit are encoded onto the write enable (WE) input for WRITE operations. The READ data outputs are multiplexed together using encoded higher READ address bits for the multiplexer SELECT signals.

JTAG Support

JTAG pins support IEEE standard 1149.1a to provide boundary scan capability for the QL5432 device. Six pins are dedicated to JTAG and programming functions on each QL5432 device, and are unavailable for general design input and output signals. TDI, TDO, TCK, TMS, and TRSTB are JTAG pins. A sixth pin, STM, is used only for programming.

Development Tools

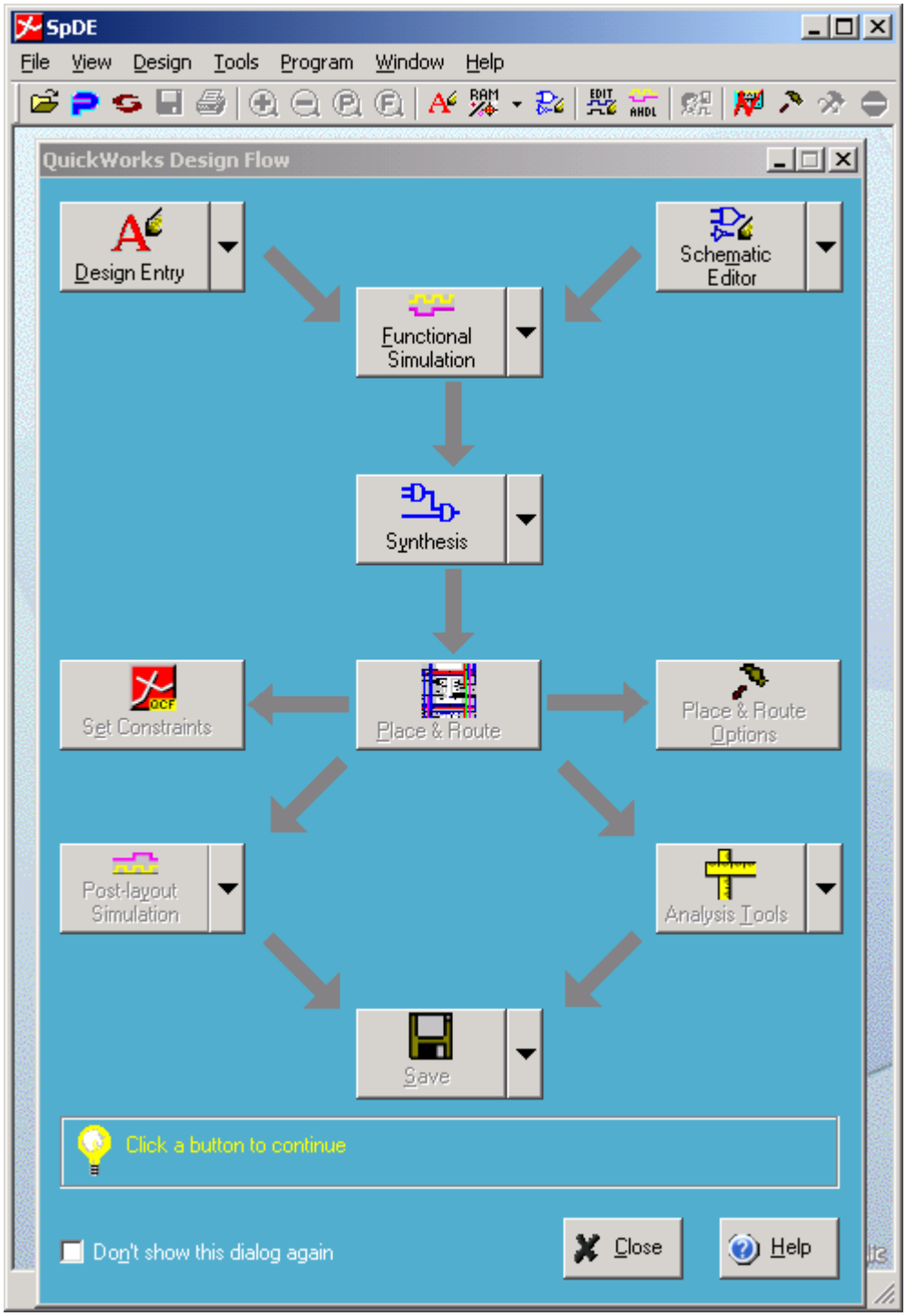
Software support for the QL5432 device is available through the QuickWorks® development package. QuickWorks is fully integrated into the Windows 98, 2000, NT, ME and XP operating systems. It provides design, layout, pre- and post-layout simulation and external stimulus design tools as shown in **Figure 4**. The program that links all these applications together and acts as the design flow manager is called Seamless pASIC Design Environment (SpDE). The term "pASIC" is a registered trademark of QuickLogic Corporation and refers to a QuickLogic FPGA, or "programmable ASIC."

QuickWorks can be used to perform the following functions in the design process:

- Design
- Pre-layout Simulation
- Synthesis
- Placement and Optimization
- Post-layout Simulation

The UNIX-based QuickTools™ package is a subset of QuickWorks and provides a solution for designers who use schematic-only design flow third-party tools for design entry, synthesis, or simulation. QuickTools reads EDIF netlists and provides support for all QuickLogic devices. QuickTools also supports a wide range of third-party modeling and simulation tools.

Figure 4: QuickWorks Design Flow



QL5432 External Device Pins

Table 5 describes the different types of devices pins. **Table 6** describes the external pins on the QL5432 device, some of which connect to the PCI bus, and others that are programmable as user IO.

Table 5: Pin Types

Type	Description
IN	Input. A standard input-only signal
OUT	Totem pole output. A standard active output driver
T/S	Tri-state. A bi-directional, tri-state input/output pin
S/T/S	Sustained Tri-state. An active low tri-state signal driven by one PCI agent at a time. It must be driven high for at least one clock before being disabled (set to Hi-Z). A pull-up needs to be provided by the PCI system central resource to sustain the inactive state once the active driver has released the signal.
O/D	Open Drain. Allows multiple devices to share this pin as a wired-or.

Table 6: QL5432 External Device Pins

Pin/Bus Name	Type	Function
VCC	IN	Supply Pin. Tie to 3.3V supply.
VCCIO	IN	Supply Pin for I/O. Set to 3.3V for 3.3V I/O, 5V for 5.0V compliant I/O.
GND	IN	Ground Pin. Tie to GND on the PCB.
I/O	T/S	Programmable Input/Output/Tri-State/Bi-directional Pin.
GLCK/I	IN	Programmable Global Network or Input-Only Pin. Tie to VCC or GND if unused.
ACLK/I	IN	Programmable Array Network or Input-Only Pin. Tie to VCC or GND if unused.
TDI/RSI[a]	IN	JTAG Data In/RAM Init. Serial Data In. Tie to VCC if unused. Connect to Serial EPROM data for RAM init.
TDO/RCO[a]	OUT	JTAG Data Out/RAM Init. Clock. Leave unconnected if unused. Connect to Serial EPROM clock for RAM init.
TCK	IN	JTAG Clock. Tie to GND if unused.
TMS	IN	JTAG Test Mode Select. Tie to VCC if unused.
TRSTB/RRO[a]	IN	JTAG Reset/RAM Init. Reset Out. Tie to GND if unused. Connect to Serial EPROM reset for RAM init.
STM	IN	QuickLogic Reserved Pin. Tie to GND on the PCB.
AD[31:0]	T/S	PCI Address and Data. 32 bit multiplexed address/data bus.
CBEN[3:0]	T/S	PCI Bus Command and Byte Enables. Multiplexed bus which contains byte enables for AD[31:0] or the Bus Command during the address phase of a PCI transaction.
PAR	T/S	PCI Parity. Even Parity across AD[31:0] and C/BEN[3:0] busses. Driven one clock after address or data phases. Master drives PAR on address cycles and PCI writes. The Target drives PAR on PCI reads.
FRAMEN	S/T/S	PCI Cycle Frame. Driven active by current PCI Master during a PCI transaction. Driven low to indicate the address cycle, driven high at the end of the transaction.
DEVSELN	S/T/S	PCI Device Select. Driven by a Target that has decoded a valid base address.
CLK	IN	PCI System Clock Input.
RSTN	IN	PCI System Reset Input.

Table 6: QL5432 External Device Pins (Continued)

Pin/Bus Name	Type	Function
REQN	T/S	PCI Request. Indicates to the Arbiter that this PCI Agent (Initiator) needs to use the bus. A point-to-point signal between the PCI device and the System Arbiter.
GNTN	IN	PCI Grant. Indicates to a PCI Agent (Initiator) that it has been granted access to the PCI bus by the Arbiter. A point-to-point signal between the PCI device and the System Arbiter.
PERRN	S/T/S	PCI Data Parity Error. Driven active by the initiator or target two clock cycles after a data parity error is detected on the AD and C/BEN busses.
SERRN	O/D	PCI System Error. Driven active when an address cycle parity error, data parity error during a special cycle, or other catastrophic error is detected.
IDSEL	IN	PCI Initialization Device Select. Use to select a specific PCI Agent during System Initialization.
IRDYN	S/T/S	PCI Initiator Ready. Indicates the Initiator's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
TRDYN	S/T/S	PCI Target Ready. Indicates the Target's ability to complete a read or write transaction. Data transfer occurs only on clock cycles where both IRDYN and TRDYN are active.
STOPN	S/T/S	PCI Stop. Used by a PCI Target to end a burst transaction.
INTAN	O/D	Interrupt A. Asynchronous Active-Low Interrupt Request.

a. See Quick Note 65 at http://quicklogic.com/images/quicknote65.pdf for information on RAM initialization.

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 7** through **Table 9**.

Table 7: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
VCCIO Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to VCCIO + 0.5 V	Storage Temperature	-65°C to + 150°C
Latch-up Immunity	±200 mA	Lead Temperature	300° C

Table 8: Operating Range

Symbol	Parameter		Industrial		Commercial		Unit
			Min	Max	Min	Max	
VCC	Supply Voltage		3.0	3.6	3.0	3.6	V
VCCIO	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-40	85	0	70	°C
K	Delay Factor	-A Speed Grade	0.43	0.95	0.46	0.93	n/a

Table 9: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
VIH	Input HIGH Voltage		0.5 VCC	VCCIO+ 0.5	V
VIL	Input LOW Voltage		-0.5	0.3 VCC	V
VOH	Output HIGH Voltage	IOH = -12 mA	2.4	-	V
		IOH = -500 µA	0.9 VCC	-	V
VOL	Output LOW Voltage	IOL = 16 mA	-	0.45	V
		IOL = 1.5 mA	-	0.1 VCC	V
II	I or I/O Input Leakage Current	VI = VCCIO or GND	-10	10	µA
IOZ	3-State Output Leakage Current	VI = VCCIO or GND	-10	10	µA
CI	I/O Input Capacitance[a]	-	-	10	pF
IOS	Output Short Circuit Current[b]	VO = GND VO = VCC	-15 40	-180 210	mA mA
ICC	D.C. Supply Current[c]	VI, VIO = VCCIO or GND	0.50 typ.	2	mA
ICCIO	D.C. Supply Current on VCCIO		0	100	µA

a. Capacitance is sample tested only. Clock pins are 12 pF maximum.
b. Only one output at a time. Duration should not exceed 30 seconds.
c. For -A commercial grade device only. Maximum ICC is 3 mA for all industrial grade devices. For AC conditions, contact QuickLogic Customer Engineering.

AC Characteristics

The AC Specifications (at VCC = 3.3 V, TA = 25° C (K = 1.00)) are provided in **Table 10** through **Table 17**.

(To calculate delays, multiply the appropriate K factor in **Table 8** operating ranges by the following numbers.)

Table 10: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{PD}	Combinatorial Delay of the longest path: time taken by the combinatorial circuit to output[b]	1.4	1.7	2.0	2.3	3.5
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge[b]	1.8	1.8	1.8	1.8	1.8
t_{H}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock-to-Q delay: the amount of time taken by the flip-flop to output after the active clock edge.	0.8	1.1	1.4	1.7	2.9
t_{CWHI}	Clock High Time: required minimum time the clock stays high	1.6	1.6	1.6	1.6	1.6
t_{CWLO}	Clock Low Time: required minimum time that the clock stays low	1.6	1.6	1.6	1.6	1.6
t_{SET}	Set Delay: time between when the flip-flop is ”set” (high) and when the output is consequently “set” (high)	1.4	1.7	2.0	2.3	3.5
t_{RESET}	Reset Delay: time between when the flip-flop is ”reset” (low) and when the output is consequently “reset” (low)	1.2	1.5	1.8	2.1	3.3
t_{SW}	Set Width: time that the SET signal must remain high/low	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width: time that the RESET signal must remain high/low	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at VCC=3.3 V and TA=25×C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

b. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 11: RAM Cell Synchronous Write Timing

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0.0	0.0	0.0	0.0	0.0
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0.0	0.0	0.0	0.0	0.0
t_{SWE}	WE setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HWE}	WE hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0.0	0.0	0.0	0.0	0.0
t_{WCRD}	WCLK to RD (WA = RA): time between the active WRITE CLOCK edge and the time when the data is available at RD	5.0	5.3	5.6	5.9	7.1

a. Stated timing for worst case Propagation Delay over process variation at VCC=3.3 V and TA=25×C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage and temperature settings as specified in the Operating Range.

Table 12: RAM Cell Synchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	8
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0.0	0.0	0.0	0.0	0.0
t_{SRE}	RE setup time to RCLK: time the READ ENABLE must be stable before the active edge of the READ CLOCK	1.0	1.0	1.0	1.0	1.0
t_{HRE}	RE hold time to RCLK: time the READ ENABLE must be stable after the active edge of the READ CLOCK	0.0	0.0	0.0	0.0	0.0
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD[a]	4.0	4.3	4.6	4.9	6.1

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 13: RAM Cell Synchronous Read Timing

Symbol	Parameter	Propagation Delays (ns) Fanout				
		1	2	3	4	8
r_{PDRD}	RA to RD: time between when the READ ADDRESS is input and when the DATA is output[a]	3.0	3.3	3.6	3.9	5.1

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 14: Input-Only Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]						
		1	2	3	4	8	12	24
t_{IN}	High drive input delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High drive input, inverting delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input register clock-to-Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input register reset delay: time between when the flip-flop is “reset”(low) and when the output is consequently “reset” (low)	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input register clock enable setup time: time “enable” must be stable before the active clock edge	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input register clock enable hold time: time “enable” must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 15: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]							
		1	2	3	4	8	10	12	15
t_{ACK}	Array clock delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7	1.8
t_{GCKP}	Global clock pin delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global clock buffer delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3	1.4

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to 8 loads per half column. The global clock has up to 11 loads per half column.

Table 16: I/O Cell Input Delays

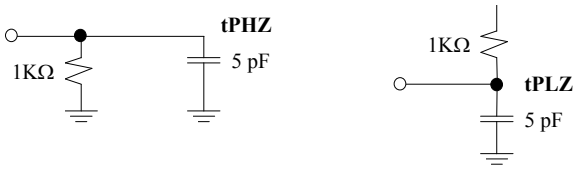
Symbol	Parameter	Propagation Delays (ns) Fanout[a]					
		1	2	3	4	8	10
$t_{I/O}$	Input delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input register clock-to-Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input register reset delay: time between when the flip-flop is “reset”(low) and when the output is consequently “reset” (low)	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input register clock enable setup time: time “enable” must be stable before the active clock edge	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input register clock enable hold time: time “enable” must be stable after the active clock edge	0.0	0.0	0.0	0.0	0.0	0.0

a. These limits are derived from a representative selection of the slowest paths through the QuickRAM logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of a particular design.

Table 17: I/O Cell Output Delays

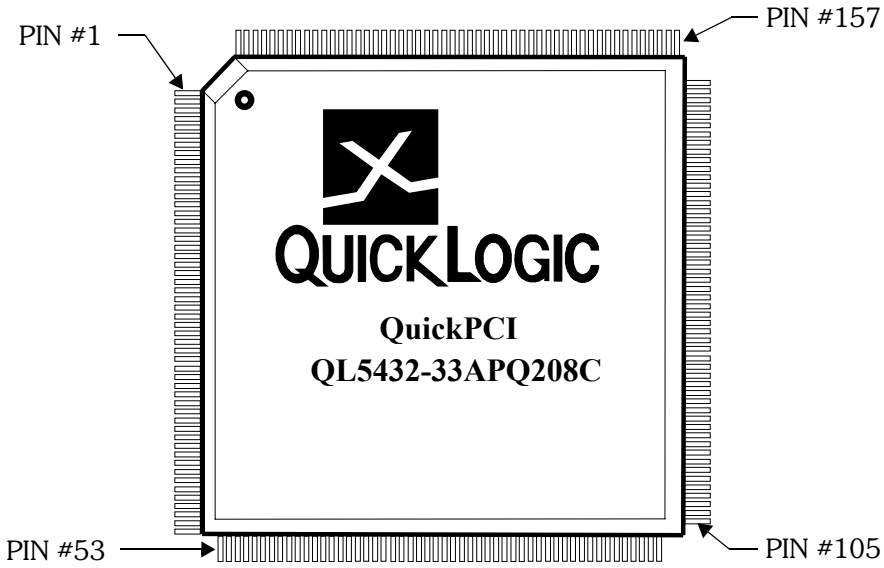
Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay low to high (90% of H)	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay high to low (10% of L)	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay tri-state to high (90% of H)	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay tri-state to low (10% of L)	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay high to tri-State[a]	2.0				
t_{PLZ}	Output Delay low to tri-State[a]	1.2				

a. The following loads are used for t_{PXZ}:



QL5432 - 208 PQFP Pinout Diagram

Figure 5: 208-pin PQFP



QL5432 - 208 PQFP Pinout Table

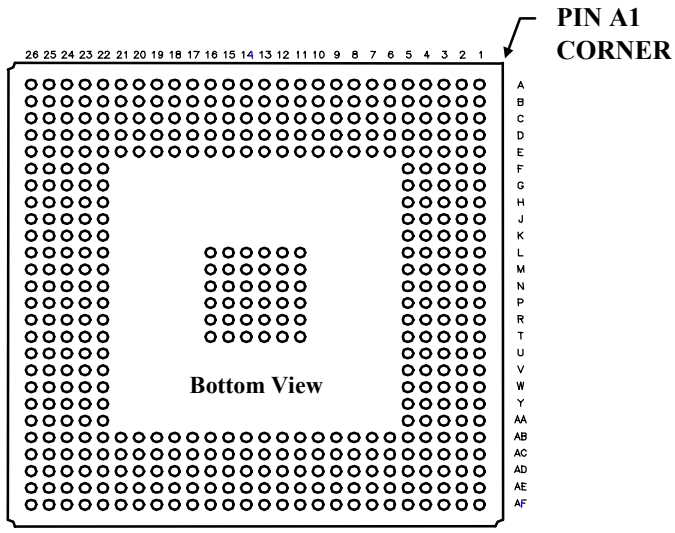
Table 18: QL5432 - 208 PQFP Pinout Table

PQ208	FUNCTION	PQ208	FUNCTION	PQ208	FUNCTION	PQ208	FUNCTION	PQ208	FUNCTION
1	I/O	43	GND	85	AD[3]	127	GND	169	I/O
2	I/O	44	IDSEL	86	AD[2]	128	I/O	170	I/O
3	I/O	45	AD[23]	87	AD[1]	129	GCLK/I	171	I/O
4	I/O	46	AD[22]	88	AD[0]	130	ACLK/I	172	I/O
5	I/O	47	AD[21]	89	I/O	131	VCC	173	I/O
6	I/O	48	AD[20]	90	I/O	132	GCLK/I	174	I/O
7	I/O	49	AD[19]	91	I/O	133	GCLK/I	175	I/O
8	I/O	50	AD[18]	92	I/O	134	VCC	176	I/O
9	I/O	51	AD[17]	93	I/O	135	I/O	177	GND
10	VCC	52	AD[16]	94	I/O	136	I/O	178	I/O
11	I/O	53	CBEN[2]	95	GND	137	I/O	179	I/O
12	GND	54	TDI	96	I/O	138	I/O	180	I/O
13	I/O	55	FRAMEN	97	VCC	139	I/O	181	I/O
14	I/O	56	IRDYN	98	I/O	140	I/O	182	GND
15	I/O	57	TRDYN	99	I/O	141	I/O	183	I/O
16	I/O	58	DEVSELN	100	I/O	142	I/O	184	I/O
17	I/O	59	GND	101	I/O	143	I/O	185	I/O
18	I/O	60	STOPN	102	I/O	144	I/O	186	I/O
19	I/O	61	VCC	103	TRSTB	145	VCC	187	VCCIO
20	I/O	62	I/O	104	TMS	146	I/O	188	I/O
21	I/O	63	I/O	105	I/O	147	GND	189	I/O
22	I/O	64	PERRN	106	I/O	148	I/O	190	I/O
23	GND	65	I/O	107	I/O	149	I/O	191	I/O
24	INTAN	66	SERRN	108	I/O	150	I/O	192	I/O
25	RSTN	67	PAR	109	I/O	151	I/O	193	I/O
26	ACLK/I	68	CBEN[1]	110	I/O	152	I/O	194	I/O
27	VCC	69	AD[15]	111	I/O	153	I/O	195	I/O
28	GCLK/I	70	AD[14]	112	I/O	154	I/O	196	I/O
29	CLK	71	AD[13]	113	I/O	155	I/O	197	I/O
30	VCC	72	AD[12]	114	VCC	156	I/O	198	I/O
31	GNTN	73	GND	115	I/O	157	TCK	199	GND
32	REQN	74	AD[11]	116	GND	158	STM	200	I/O
33	AD[31]	75	AD[10]	117	I/O	159	I/O	201	VCC
34	AD[30]	76	AD[9]	118	I/O	160	I/O	202	I/O
35	AD[29]	77	AD[8]	119	I/O	161	I/O	203	I/O
36	AD[28]	78	GND	120	I/O	162	I/O	204	I/O
37	AD[27]	79	CBEN[0]	121	I/O	163	GND	205	I/O
38	AD[26]	80	AD[7]	122	I/O	164	I/O	206	I/O
39	AD[25]	81	AD[6]	123	I/O	165	VCC	207	TDO
40	AD[24]	82	AD[5]	124	I/O	166	I/O	208	I/O
41	VCC	83	VCCIO	125	I/O	167	I/O		
42	CBEN[3]	84	AD[4]	126	I/O	168	I/O		

Summary: 50 PCI pins, 118 user I/O, 4 GCLK, and 2 ACLK.

QL5432 - 456 PBGA Pinout Diagram

Figure 6: 456-pin PBGA



QL5432 - 456 PBGA Pinout Table

Table 19: QL5432 - 456 PBGA Pinout Table

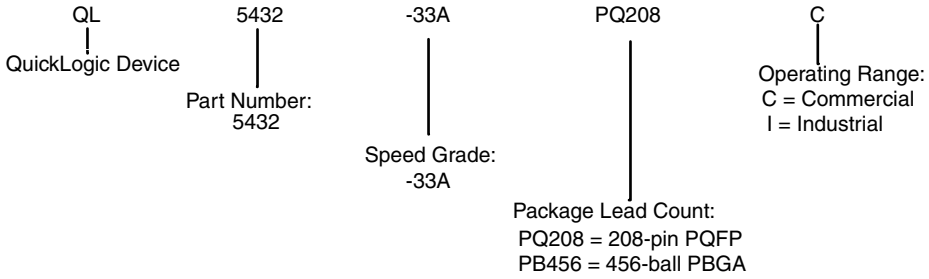
PB456	Function	PB456	Function	PB456	Function	PB456	Function	PB456	Function	PB456	Function
A1	I/O	B23	I/O	D19	I/O	G5	NC	L23	I/O	P23	GCLK / I
A2	I/O	B24	I/O	D20	I/O	G22	GND	L24	I/O	P24	GCLK / I
A3	I/O	B25	I/O	D21	NC	G23	I/O	L25	I/O	P25	I/O
A4	I/O	B26	STM	D22	I/O	G24	I/O	L26	I/O	P26	ACLK / I
A5	I/O	C1	I/O	D23	GND	G25	I/O	M1	ACLK / I	R1	I/O
A6	I/O	C2	I/O	D24	I/O	G26	I/O	M2	GCLK/I	R2	I/O
A7	I/O	C3	I/O	D25	I/O	H1	I/O	M3	I/O	R3	I/O
A8	I/O	C4	TDO	D26	I/O	H2	I/O	M4	NC	R4	NC
A9	I/O	C5	I/O	E1	I/O	H3	I/O	M5	GND	R5	NC
A10	I/O	C6	I/O	E2	I/O	H4	I/O	M11	GND/THERM	R11	GND/THERM
A11	I/O	C7	I/O	E3	I/O	H5	NC	M12	GND/THERM	R12	GND/THERM
A12	VCCIO	C8	I/O	E4	I/O	H22	NC	M13	GND/THERM	R13	GND/THERM
A13	I/O	C9	I/O	E5	GND	H23	I/O	M14	GND/THERM	R14	GND/THERM
A14	I/O	C10	I/O	E6	VCC	H24	I/O	M15	GND/THERM	R15	GND/THERM
A15	I/O	C11	I/O	E7	GND	H25	I/O	M16	GND/THERM	R16	GND/THERM
A16	I/O	C12	I/O	E8	NC	H26	I/O	M22	NC	R22	VCC
A17	I/O	C13	I/O	E9	GND	J1	I/O	M23	NC	R23	NC
A18	I/O	C14	I/O	E10	I/O	J2	I/O	M24	I/O	R24	I/O
A19	I/O	C15	I/O	E11	GND	J3	I/O	M25	I/O	R25	I/O
A20	I/O	C16	I/O	E12	GND	J4	NC	M26	I/O	R26	GCLK / I
A21	I/O	C17	I/O	E13	VCC	J5	GND	N1	CLK	T1	I/O
A22	I/O	C18	I/O	E14	GND	J22	NC	N2	I/O	T2	I/O
A23	I/O	C19	I/O	E15	GND	J23	NC	N3	I/O	T3	I/O
A24	I/O	C20	I/O	E16	GND	J24	I/O	N4	RSTN	T4	I/O
A25	I/O	C21	I/O	E17	NC	J25	I/O	N5	VCC	T5	VCC
A26	I/O	C22	I/O	E18	GND	J26	I/O	N11	GND/THERM	T11	GND/THERMAL
B1	I/O	C23	I/O	E19	NC	K1	I/O	N12	GND/THERM	T12	GND/THERMAL
B2	I/O	C24	I/O	E20	GND	K2	I/O	N13	GND/THERM	T13	GND/THERMAL
B3	I/O	C25	TCK	E21	VCC	K3	I/O	N14	GND/THERM	T14	GND/THERMAL
B4	I/O	C26	I/O	E22	GND	K4	I/O	N15	GND/THERM	T15	GND/THERMAL
B5	I/O	D1	I/O	E23	I/O	K5	VCC	N16	GND/THERM	T16	GND/THERMAL
B6	I/O	D2	I/O	E24	I/O	K22	GND	N22	GND	T22	GND
B7	I/O	D3	I/O	E25	I/O	K23	I/O	N23	I/O	T23	I/O
B8	I/O	D4	GND	E26	I/O	K24	I/O	N24	I/O	T24	I/O
B9	I/O	D5	I/O	F1	I/O	K25	I/O	N25	I/O	T25	I/O
B10	I/O	D6	NC	F2	I/O	K26	I/O	N26	I/O	T26	I/O
B11	I/O	D7	I/O	F3	I/O	L1	I/O	P1	I/O	U1	I/O
B12	I/O	D8	I/O	F4	NC	L2	I/O	P2	I/O	U2	I/O
B13	I/O	D9	GND	F5	VCC	L3	I/O	P3	I/O	U3	I/O
B14	I/O	D10	I/O	F22	VCC	L4	I/O	P4	I/O	U4	I/O
B15	I/O	D11	I/O	F23	NC	L5	NC	P5	NC	U5	GND
B16	I/O	D12	GND	F24	I/O	L11	GND/THERM	P11	GND/THERM	U22	NC
B17	I/O	D13	I/O	F25	I/O	L12	GND/THERM	P12	GND/THERM	U23	I/O
B18	I/O	D14	I/O	F26	I/O	L13	GND/THERM	P13	GND/THERM	U24	I/O
B19	I/O	D15	GND	G1	I/O	L14	GND/THERM	P14	GND/THERM	U25	I/O
B20	I/O	D16	I/O	G2	I/O	L15	GND/THERM	P15	GND/THERM	U26	I/O
B21	I/O	D17	I/O	G3	I/O	L16	GND/THERM	P16	GND/THERM	V1	I/O
B22	I/O	D18	GND	G4	I/O	L22	NC	P22	NC	V2	I/O

Table 19: QL5432 - 456 PBGA Pinout Table (Continued)

PB456	Function	PB456	Function	PB456	Function	PB456	Function	PB456	Function	PB456	Function
V3	I/O	AA1	I/O	AB19	GND	AC21	I/O	AD23	TRSTB	AE25	I/O
V4	NC	AA2	I/O	AB20	NC	AC22	NC	AD24	I/O	AE26	I/O
V5	NC	AA3	NC	AB21	VCC	AC23	GND	AD25	I/O	AF1	I/O
V22	GND	AA4	NC	AB22	GND	AC24	I/O	AD26	I/O	AF2	I/O
V23	NC	AA5	VCC	AB23	I/O	AC25	I/O	AE1	TDI	AF3	REQN
V24	I/O	AA22	VCC	AB24	I/O	AC26	I/O	AE2	INTAN	AF4	AD[31]
V25	I/O	AA23	NC	AB25	I/O	AD1	I/O	AE3	GNTN	AF5	AD[29]
V26	I/O	AA24	I/O	AB26	I/O	AD2	NC	AE4	AD[30]	AF6	AD[25]
W1	I/O	AA25	I/O	AC1	I/O	AD3	I/O	AE5	AD[27]	AF7	AD[23]
W2	I/O	AA26	I/O	AC2	I/O	AD4	I/O	AE6	CBEN[3]	AF8	AD[19]
W3	I/O	AB1	I/O	AC3	NC	AD5	AD[28]	AE7	AD[21]	AF9	CBEN[2]
W4	I/O	AB2	I/O	AC4	GND	AD6	AD[24]	AE8	AD[17]	AF10	IRDYN
W5	NC	AB3	I/O	AC5	AD[26]	AD7	IDSEL	AE9	AD[16]	AF11	I/O
W22	NC	AB4	I/O	AC6	NC	AD8	AD[20]	AE10	DEVSELN	AF12	SERRN
W23	I/O	AB5	GND	AC7	AD[22]	AD9	FRAMEN	AE11	PERRN	AF13	AD[14]
W24	I/O	AB6	VCC	AC8	AD[18]	AD10	TRDYN	AE12	CBEN[1]	AF14	AD[10]
W25	I/O	AB7	NC	AC9	NC	AD11	I/O	AE13	AD[12]	AF15	AD[7]
W26	I/O	AB8	NC	AC10	STOPN	AD12	PAR	AE14	AD[8]	AF16	AD[3]
Y1	I/O	AB9	NC	AC11	I/O	AD13	AD[13]	AE15	AD[5]	AF17	AD[0]
Y2	I/O	AB10	VCC	AC12	NC	AD14	AD[9]	AE16	AD[1]	AF18	I/O
Y3	I/O	AB11	GND	AC13	AD[11]	AD15	CBEN[0]	AE17	I/O	AF19	I/O
Y4	I/O	AB12	NC	AC14	VCCIO	AD16	AD[4]	AE18	I/O	AF20	I/O
Y5	I/O	AB13	AD[15]	AC15	NC	AD17	I/O	AE19	I/O	AF21	I/O
Y22	GND	AB14	GND	AC16	AD[2]	AD18	I/O	AE20	I/O	AF22	I/O
Y23	I/O	AB15	VCC	AC17	I/O	AD19	I/O	AE21	I/O	AF23	I/O
Y24	I/O	AB16	AD[6]	AC18	NC	AD20	I/O	AE22	I/O	AF24	I/O
Y25	I/O	AB17	NC	AC19	I/O	AD21	I/O	AE23	NC	AF25	I/O
Y26	I/O	AB18	VCC	AC20	I/O	AD22	I/O	AE24	TMS	AF26	I/O

Summary: 50 PCI pins, 260 user I/O, 4 GCLK, and 2 ACLK.

Ordering Information



Contact Information

Phone: (408) 990-4000 (US)
(416) 497-8884 (Canada)
+(44) 1932 57 9011 (Europe – except Germany/Benelux)
+(49) 89 930 86 170 (Germany/Benelux)
+(86) 21 6867 0273 (Asia – except Japan)
+(81) 45 470 5525 (Japan)
E-mail: info@quicklogic.com
Sales: www.quicklogic.com/sales
Support: www.quicklogic.com/support
Internet: www.quicklogic.com

Revision History

Revision	Date	Originator and Comments
Rev. A	December 2000	First Release
Rev. B	September 2003	Bernhard Andretzky and Kathleen Murchek
Rev. C	July 2004	Bernhard Andretzky and Kathleen Murchek Converted to new format. Added Summary to pinout tables.

Copyright and Trademark Information