

# AV Switch for I<sup>2</sup>C BUS Control, 4-input, 3-output and Canal Plus Compatible

# Monolithic IC MM1422, 1423, 1442, 1443

## Outline

These ICs are four-input, three-output AV switches under I<sup>2</sup>C BUS control with Canal Plus support, intended for use in VCRs and DVD for the European market. There are four models, described below. Audio subsystems are either stereo or monaural; video subsystems either do or do not have a clamping circuit.

## Features

1. I<sup>2</sup>C BUS serial control.
2. Internal two-output 75Ω video driver, internal two-output 600Ω audio driver.
3. Audio mute function through an external pin.
4. Operating power supply voltage 11 to 13 V
5. Models both with and without video subsystem clamp.
6. Models with monaural and stereo audio subsystems.

## Package

- SSOP-34A (MM1443XJ)
- SDIP-32A (MM1443XD)

## Applications

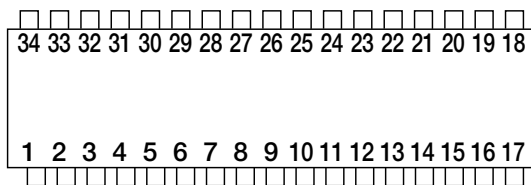
- (1)VCRs with Canal Plus Support for the European Market.
- (2)DVD

## Series Table

	Video input clamp	Stereo	Monaural	Package	
				SDIP-32A	SSOP-34A
MM1422			○	○	○
MM1423		○		○	○
MM1442	○		○	○	○
MM1443	○	○		○	○

## Pin Assignment

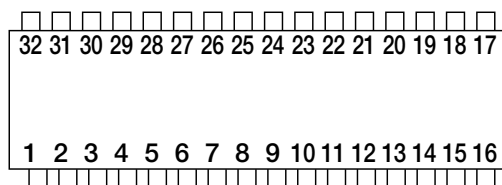
### MM1443XJ



SSOP-34A

1	E1-V	10	E1-L	19	GND1	28	TUN-V
2	Vcc2	11	FS	20	TUN-R(N.C.)	29	Vout3
3	E2-V	12	EXT-R(N.C.)	21	Rout3(N.C.)	30	Vout2
4	Vcc1	13	Port1	22	Rout2(N.C.)	31	Vout1
5	EXT-V	14	E2-R(N.C.)	23	Rout1(N.C.)	32	SDA
6	EXT-L	15	Port2	24	TUN-L	33	SCL
7	BIAS	16	E1-R(N.C.)	25	Lout3	34	GND2
8	E2-L	17	NC	26	Lout2		
9	Mute	18	NC	27	Lout1		

### MM1443XD

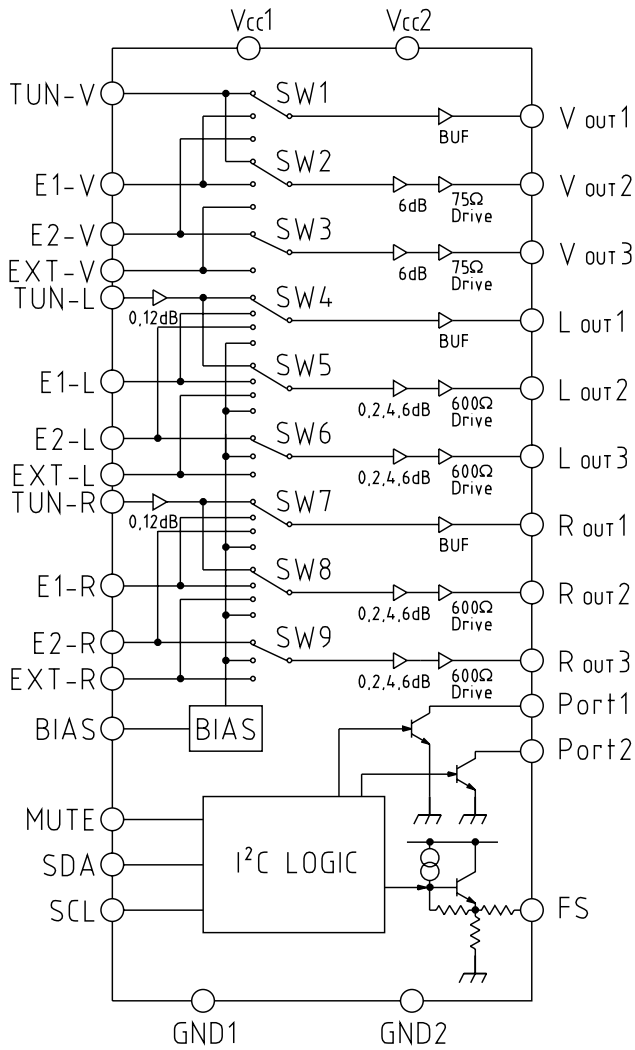


SDIP-32A

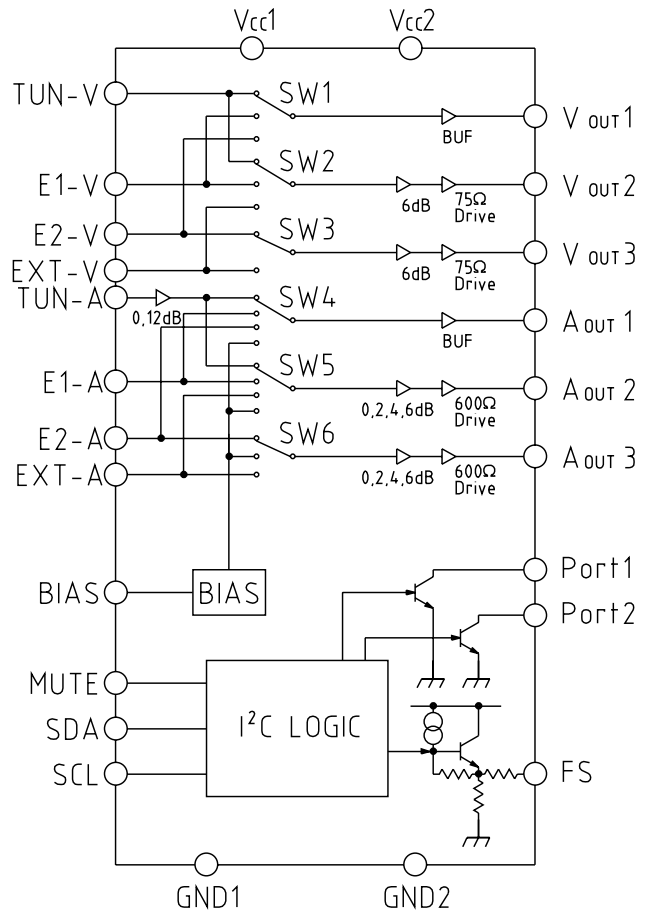
1	E1-V	9	Mute	17	GND1	25	Lout1
2	Vcc2	10	E1-L	18	TUN-R(N.C.)	26	TUN-V
3	E2-V	11	FS	19	Rout3(N.C.)	27	Vout3
4	Vcc1	12	EXT-R(N.C.)	20	Rout2(N.C.)	28	Vout2
5	EXT-V	13	Port1	21	Rout1(N.C.)	29	Vout1
6	EXT-L	14	E2-R(N.C.)	22	TUN-L	30	SDA
7	BIAS	15	Port2	23	Lout3	31	SCL
8	E2-L	16	E1-R(N.C.)	24	Lout2	32	GND2

Block Diagram

Stereo type (MM1423, MM1443)



Monaural type (MM1422, MM1442)



Introduction of Main Model

AV Switch for I<sup>2</sup>C BUS Control, 4-input, 3-output and Canal Plus Compatible  
**Monolithic IC MM1443**

Pin Description

Pin No.	Pin name	Functions	Equivalent circuit diagram
1 3 5 28	E1-V E2-V EXT-V TUN-V	Video input pin	
2 4	Vcc2 Vcc1	Vcc2 is power supply voltage pin for 75Ω driver	
13 15	Port1 Port2	Port output pin	
6 8 10 12 14 16 20 24	EXT-L E2-L E1-L EXT-R E2-R E1-R TUN-R TUN-L	Audio input pin	
7	BIAS	Bias pin	

Pin No.	Pin name	Functions	Equivalent circuit diagram
9	Mute	Mute pin	
19 34	GND1 GND2	GND2 is a GND pin for 75Ω driver	
11	FS	FS output pin	
21 22 25 26	ROUT3 ROUT2 LOUT3 LOUT2	Audio driver output pin	
23 27	ROUT1 LOUT1	Audio buffer output pin	

Pin No.	Pin name	Functions	Equivalent circuit diagram
29 30	V <sub>out3</sub> V <sub>out2</sub>	Video driver output pin	
31	V <sub>out1</sub>	Video buffer output pin	
32	SDA	SDA pin	
33	SCL	SCL pin	
17 18	NC		

**Absolute Maximum Ratings** (Ta=25°C)

Item	Symbol	Ratings	Unit
Storage temperature	T <sub>STG</sub>	-40~+125	°C
Operating temperature	T <sub>OPR</sub>	-25~+75	°C
Power supply voltage	V <sub>CC max.</sub>	15	V
Allowable loss	P <sub>d</sub>	700	mW

**Recommend Operating Conditions**

Item	Symbol	Ratings	Unit
Operating temperature	T <sub>OPR</sub>	-25~+75	°C
Operating voltage	V <sub>OP</sub>	11~13	V

**Electrical Characteristics** (Except where noted otherwise, Ta=25°C, V<sub>CC</sub>=12V)

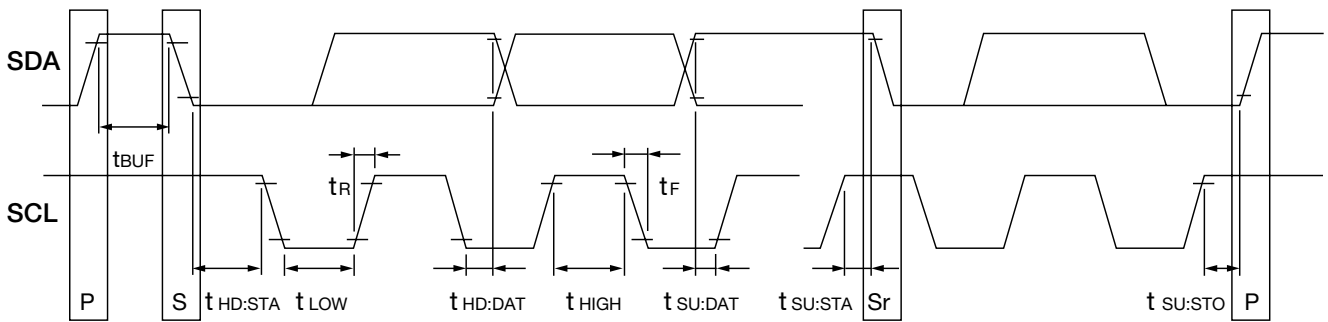
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Consumption current	I <sub>CC</sub>	No-signal, no-load		33.5	40.0	mA
[FS pin output level]						
High voltage	V <sub>FSH</sub>	FS pin control High selected	9.5	11.0	12.0	V
Middle voltage	V <sub>FSM</sub>	FS pin control Mid selected	4.5	6.0	7.0	V
Low voltage	V <sub>FSL</sub>	FS pin control Low selected		0.2	1.0	V
[Crosstalk]						
V <sub>OUT1</sub>	CT <sub>V1</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> f=4.43MHz		-70	-50	dB
V <sub>OUT2</sub>	CT <sub>V2</sub>					
V <sub>OUT3</sub>	CT <sub>V3</sub>					
L <sub>OUT1</sub>	CT <sub>L1</sub>	V <sub>IN</sub> =1V <sub>rms</sub> f=1kHz		-90	-70	dB
L <sub>OUT2</sub>	CT <sub>L2</sub>					
L <sub>OUT3</sub>	CT <sub>L3</sub>					
R <sub>OUT1</sub>	CT <sub>R1</sub>	V <sub>IN</sub> =1V <sub>rms</sub> f=1kHz		-90	-70	dB
R <sub>OUT2</sub>	CT <sub>R2</sub>					
R <sub>OUT3</sub>	CT <sub>R3</sub>					
[V <sub>OUT1</sub> ]						
Voltage gain	G <sub>V1</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> f=100kHz	-0.5	0	+0.5	dB
Frequency characteristic	F <sub>V1</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> 10MHz/100kHz	-1.0	0	+1.0	dB
Differential gain	DG <sub>1</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> : staircase APL = 10~90%	-3	0	+3	%
Differential phase	DP <sub>1</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> : staircase APL = 10~90%	-3	0	+3	deg
Maximam output level	V <sub>OV1</sub>	f = 100kHz, Maximum output at THD < 1.0%	2.1			V <sub>P-P</sub>
Input pin voltage	V <sub>IV1</sub>	No-signal, no-load	2.3	2.8	3.3	V
Output pin voltage	V <sub>OV1</sub>	No-signal, no-load	1.0	1.5	2.0	V
[V <sub>OUT2</sub> , V <sub>OUT3</sub> ]						
Voltage gain	G <sub>V2</sub> G <sub>V3</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> f=100kHz	5.5	6.0	6.5	dB
Frequency characteristic	F <sub>V2</sub> F <sub>V3</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> 10MHz/100kHz	-1.0	0	+1.0	dB
Differential gain	DG <sub>2</sub> DG <sub>3</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> : staircase APL = 10~ 90%	-3	0	+3	%

Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Differential phase	DP <sub>2</sub> DP <sub>3</sub>	V <sub>IN</sub> =1V <sub>P-P</sub> : staircase APL = 10~90%	-3	0	+3	deg
Maximam output level	V <sub>OV2</sub> V <sub>OV3</sub>	f = 100kHz, Maximum output at THD < 1.0%	4.2			V <sub>P-P</sub>
Input pin voltage	V <sub>IV2</sub> V <sub>IV3</sub>	No-signal, no-load	2.3	2.8	3.3	V
Output pin voltage	V <sub>OV2</sub> V <sub>OV3</sub>	No-signal, no-load	1.0	1.5	2.0	V
<b>[Lout1, Rout1]</b>						
Voltage gain	G <sub>1L1</sub>	V <sub>IN</sub> =1V <sub>rms</sub> f=1kHz TUN-L GAIN adjustment at 0dB	-0.5	0	+0.5	dB
	G <sub>2L1</sub>	V <sub>IN</sub> =0.25V <sub>rms</sub> f=1kHz TUN-L GAIN adjustment at 12dB	11.5	12	12.5	dB
Maximam output level	DL <sub>1</sub>	V <sub>CC</sub> = 12V, f = 1kHz Maximum output at THD < 0.5%	3.0			V <sub>rms</sub>
Total harmonic distortion	THD <sub>L1</sub>	V <sub>IN</sub> such that V <sub>OUT</sub> = 1V <sub>rms</sub> , f = 1kHz		0.03	0.1	%
Output noise voltage	V <sub>NL1</sub>	A curve band 20kHz		3	50	μV <sub>rms</sub>
Output offset voltage	V <sub>OFL1</sub>	DC step for switching	-15	0	15	mV
Input impedance	Z <sub>INL1</sub>		100	150	200	kΩ
Input pin voltage	V <sub>IL1</sub>	No-signal, no-load	5.30	5.65	6.00	V
Output pin voltage	V <sub>OL1</sub>	No-signal, no-load	5.30	5.65	6.00	V
<b>[Lout2, Lout3, Rout2, Rout3]</b>						
Voltage gain	G <sub>0L2</sub> G <sub>0L3</sub>	V <sub>IN</sub> =1V <sub>rms</sub> TUN-L=0dB Output GAIN adjustment at 0dB	-0.5	0	+0.5	dB
	G <sub>2L2</sub> G <sub>2L3</sub>	V <sub>IN</sub> =1V <sub>rms</sub> TUN-L=0dB Output GAIN adjustment at 2dB	1.5	2	2.5	dB
	G <sub>4L2</sub> G <sub>4L3</sub>	V <sub>IN</sub> =1V <sub>rms</sub> TUN-L=0dB Output GAIN adjustment at 4dB	3.5	4	4.5	dB
	G <sub>6L2</sub> G <sub>6L3</sub>	V <sub>IN</sub> =1V <sub>rms</sub> TUN-L=0dB Output GAIN adjustment at 6dB	5.5	6	6.5	dB
Maximam output level	V <sub>L2</sub> V <sub>L3</sub>	V <sub>CC</sub> =12V f=1kHz Maximum output when THD < 0.5%	3.0			V <sub>rms</sub>
Total harmonic distortion	THD <sub>L2</sub> THD <sub>L3</sub>	V <sub>IN</sub> such that V <sub>OUT</sub> = 1V <sub>rms</sub> f=1kHz G=0, 2, 4, 6dB		0.03	0.1	%
Output noise voltage	V <sub>NL2</sub> V <sub>NL3</sub>	A curve band 20kHz		20	50	μV <sub>rms</sub>
Output offset voltage	V <sub>OFL2</sub> V <sub>OFL3</sub>	DC step for switching	-15	0	15	mV
Input impedance	Z <sub>INL2</sub> Z <sub>INL3</sub>		100	150	200	kΩ
Input terminal voltage	V <sub>IL2</sub> V <sub>IL3</sub>	No-signal, no-load	5.30	5.65	6.00	V
Output terminal voltage	V <sub>OL2</sub> V <sub>OL3</sub>	No-signal, no-load	5.30	5.65	6.00	V
<b>[Logic] (refer to next page)</b>						
Input voltage L	V <sub>IL</sub>	I <sup>2</sup> C logic L level judgment value	0.0		1.5	V
Input voltage H	V <sub>IH</sub>	I <sup>2</sup> C logic H level judgment value	3.0		5.0	V
Low level output voltage	V <sub>OL</sub>	for SDA 3mA inflow	0.0		0.4	V
High level input current	I <sub>IH</sub>	for SDA, SCL = 4.5V impressed	-10		+10	μA
Low level input current	I <sub>IL</sub>	for SDA, SCL = 0.4V impressed	-10		+10	μA
Clock frequency	f <sub>SCL</sub>				100	kHz

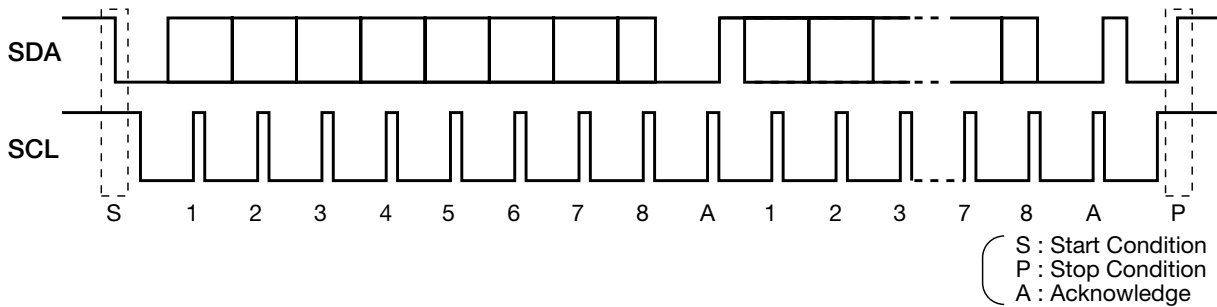


Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Unit
Data transfer waiting time	t <sub>BUF</sub>		4.7			μS
SCL start hold time	t <sub>HD : STA</sub>		4.0			μS
SCL low level hold time	t <sub>LOW</sub>		4.7			μS
SCL high level hold time	t <sub>HIGH</sub>		4.0			μS
SCL start setup time	t <sub>SU : STA</sub>		4.7			μS
SDA data hold time	t <sub>HD : DAT</sub>		200			nS
SDA data setup time	t <sub>SU : DAT</sub>		250			nS
SCL rise time	t <sub>R</sub>				1000	nS
SCL fall time	t <sub>F</sub>				300	nS
SCL stop setup time	t <sub>SU : STO</sub>		4.0			μS

**I<sup>2</sup>C BUS control signal**



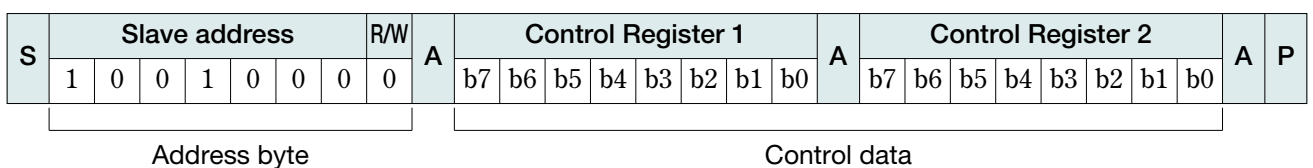
**I<sup>2</sup>C BUS**



I<sup>2</sup>C BUS (Inter IC BUS) is an inter bus system developed by Philips Co. It transmits and receives data through 2 (SDA, SCL) lines. Data are transmitted and received in the units of bytes by MSB first from the start condition.

**[Control registers]**

Control registers are data sent from the master for determining the switch condition of the MM1422 series.



The data format of the MM1422 series is set as shown in the above figure. Out of the address bytes, first 7 bits are assigned to the slave addresses, while the residual 1 bit is assigned to the R/W bit. Set the R/W bit to 0 when data are used as control registers. Slave address of the MM1422 series is 90H. Each bit of control registers is reset to 0. MM1422 series consists of one address byte and two control data bytes(3 bytes in total). For details of the control contents of control register 1 and 2, refer to the separate table.

**[Control Register 1]**

b7	b6	b5	b4	b3	b2	b1	b0
OUT 1 select		OUT 2 select		OUT 3 select		FS CTRL	

**[Control Register 2]**

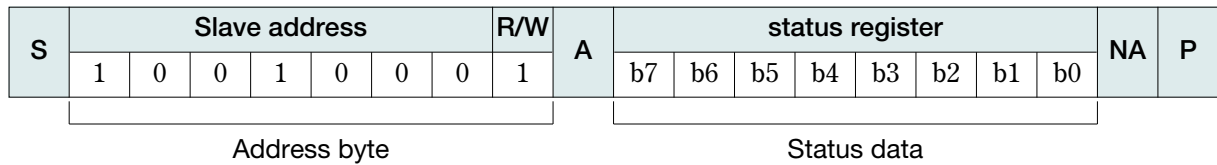
b7	b6	b5	b4	b3	b2	b1	b0
0, 12dB select	Port 1 CTRL	Port 2 CTRL	Audio OUT2 gain select	Audio OUT3 gain select	Mute		

All data over the limited length (4th and subsequent bytes) are fully neglected. Because of this, the faulty operation that switch changes by the data after the 4th byte doesn't occur.

Each audio output can be set to mute by setting MUTE terminal to high.

**[Status registers]**

There is no preparation of the status register in MM1422 series. A status register returns all the 1 when is set in the R/W bit.



## Switch Control Table

[Control register 1] (2nd byte)

b7	b6	b5	b4	b3	b2	b1	b0	V OUT1	A OUT1	V OUT2	A OUT2	V OUT3	A OUT3	FS
0	0							*1	MUTE					
0	1							TUNER	TUNER					
1	0							SCART E1	SCART E1					
1	1							SCART E2	SCART E2					
		0	0							*1	MUTE			
		0	1							TUNER	TUNER			
		1	0							SCART E1	SCART E1			
		1	1							EXT IN	EXT IN			
				0	0							*2	MUTE	
				0	1							EXT IN	EXT IN	
				1	0							SCART E2	SCART E2	
				1	1							SCART E2	SCART E2	
						0	0							Low
						0	1							Middle
						1	0							High
						1	1							High

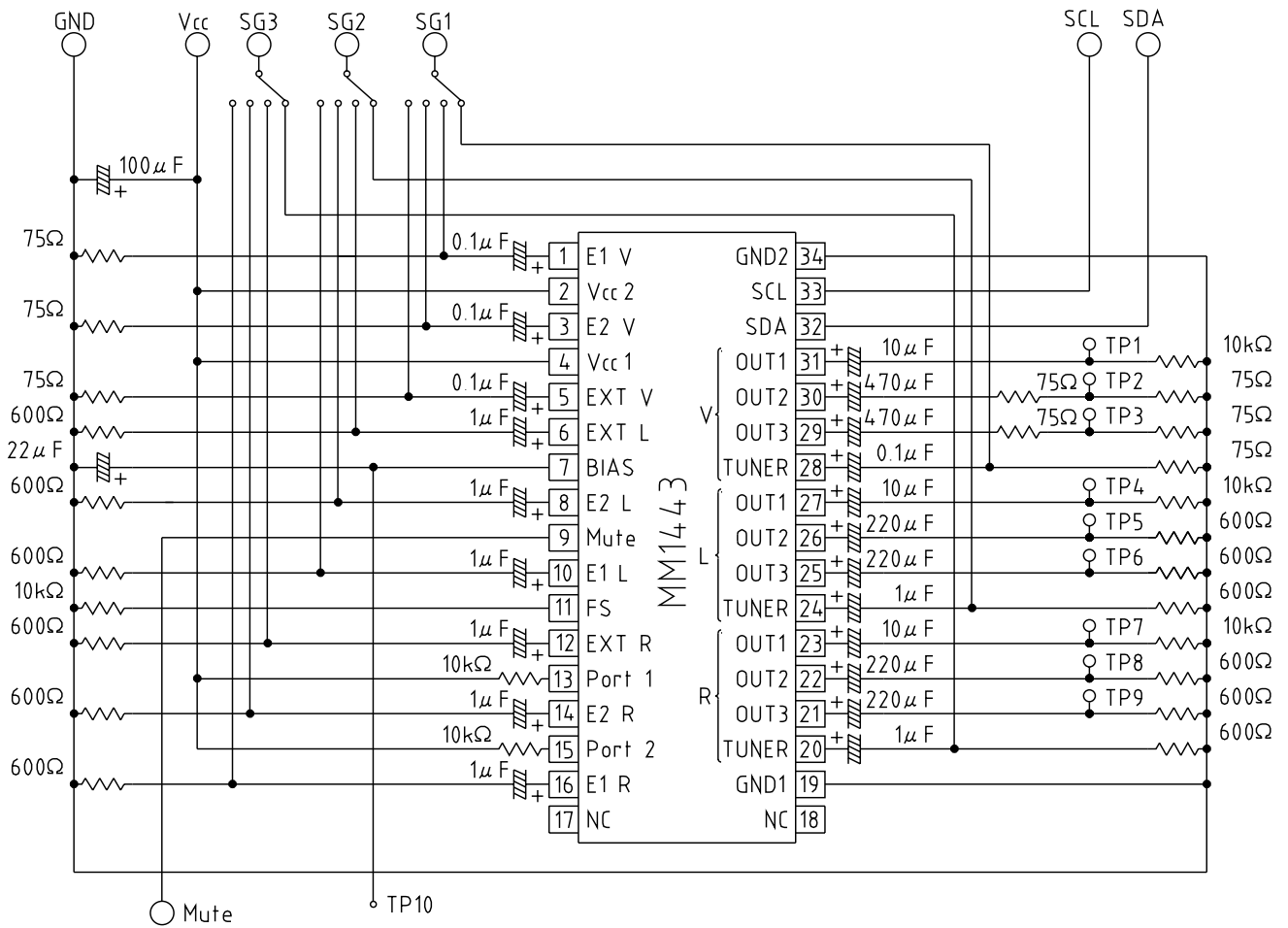
Note 1 : Previous choice condition is held. TUNER is chosen at power on.

Note 2 : Previous choice condition is held. EXT IN is chosen at power on.

[Control register 2] (3rd byte)

b7	b6	b5	b4	b3	b2	b1	b0	0, 12dB	Port 1	Port 2	GainOUT2	GainOUT3	MUTE
0								0dB					
1								12dB					
	0								Low				
	1								High				
		0								Low			
		1								High			
			0	0							0dB		
			0	1							2dB		
			1	0							4dB		
			1	1							6dB		
					0	0						0dB	
					0	1						2dB	
					1	0						4dB	
					1	1						6dB	
							0						OFF
							1						ON

Measuring Circuit



Application Circuit

