Wolfson Microelectronics

WM5615

Production Data
January 1997 Rev 2

10-Bit Digital-to-Analogue Converter

Description

The WM5615 is a 10-bit voltage output digital-to-analogue converter (DAC) with a buffered reference input (high impedance). The DAC produces a maximum output voltage that is twice the reference voltage and the DAC is monotonic. The device is simple to use, running from a single supply of 5V. A power-on reset function is incorporated to ensure repeatable start-up conditions.

Digital control of the WM5615 is over a 3-wire serial bus that is CMOS compatible and easily interfaced to industry standard microprocessor and microcontroller devices. The device receives a 16-bit data word to produce the analogue output. The digital inputs feature Schmitt triggers for high noise immunity. Digital communication protocols include the SPI™, QSPI™ and Microwire™ standards.

The 8-terminal small-outline D package allows digital control of analogue functions in space-critical applications. The WM5615C is characterised for operation from 0°C to 70°C. The WM5615I is for operation from -40°C to 85°C.

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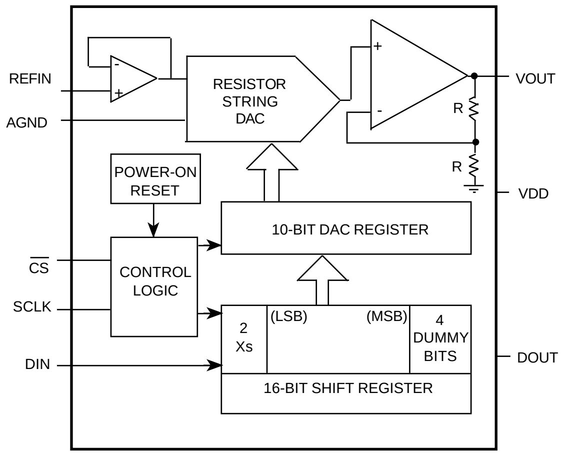
Features

- **10-bit CMOS voltage output DAC in an 8-terminal package**
- **5V single supply operation**
- **3-wire serial interface**
- **High-impedance reference input**
- **Maximum voltage output twice reference input voltage**
- **Internal power-on reset**
- **Low power consumption ... 1.75mW max**
- **877kHz update rate**
- **Setting time to 0.5 LSB ... 12.5µs typical**
- **Monotonic over temperature**
- **Pin compatible with the Maxim MAX515**

Applications

- **Battery-powered test Instruments**
- **Digital offset and gain adjustment**
- **Battery-operated/remote industrial controls**
- **Machine and motion control devices**
- **Cellular telephones**

Block Diagram



Production Data data sheets contain final specifications current on publication date. Supply of products conforms to Wolfson Microelectronics standard terms and conditions.

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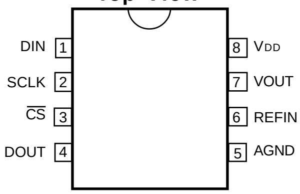
Pin Configuration

D or P package
Top View



Ordering Information

DEVICE	TEMP RANGE	PACKAGE
WM5615CD	**0°C to +70°C**	**8 pin SO**
WM5615CP	**0°C to +70°C**	**8 pin DIP**
WM5615ID	**-40°C to +85°C**	**8 pin SO**
WM5615IP	**-40°C to +85°C**	**8 pin DIP**

Absolute Maximum Ratings

Supply voltage (V_{DD} to AGND) 7V
Digital input voltage range to AGND . .-0.3V to V_{DD} +0.3V
Ref. input voltage range to AGND . . .-0.3V to V_{DD} + 0.3V
Output voltage at OUT from external source . .V_{DD} + 0.3V
Continuous current, any terminal . . . . ±20mA

Operating free-air temperature range T_A:
WM5615C . . . . 0°C to +70°C
WM5615I . . . . -40°C to +85°C
Storage temperature range T_{stg} . . . . . -65°C to +150°C
Lead temperature 1.6mm (1/16 inch)
from case for 10 seconds . . . . .260°C

Note: Stresses beyond those listed under 'Absolute Maximum Ratings' may cause damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 'Recommended Operating Conditions' is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Supply voltage		V_{DD}	4.5	5	5.5	V
High-level digital input voltage		V_{IH}	2.4			V
Low-level digital input voltage		V_{IL}			0.8	V
Reference voltage to REFIN terminal		V_{ref}	0	2.048	V_{DD}-2	V
Load resistance		R_L	2			kΩ
Operating free air temperature	WM5615C	T_A	0		70	°C
	WM5615I	T_A	-40		85	°C

Electrical Characteristics (over recommended operating free-air temperature range)

V_{DD} = 5.0V ±5%, V_{ref} = 2.048V unless otherwise stated.

Static DAC Specifications

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Resolution				10			bits
Integral nonlinearity	INL	(see note 1)				±1	LSB
Differential nonlinearity	DNL	(see note 2)			+0.1	±0.5	LSB
Zero scale error (offset error)	E_{ZS}	(see note 3)				±3	LSB
Zero scale error (offset error) temperature coefficient		(see note 4)			3		ppm/°C
Gain error	E_G	(see note 5)				±3	LSB
Gain error temperature coefficient		(see note 6)			1		ppm/°C
Power-supply rejection ratio	PSRR	Offset	(see notes 7 and 8)		0.1		LSB/V
		Gain			0.1		
Analogue full scale output		R_L = 100kΩ		2Vref(1023/1024)			V

Notes:

1. The relative accuracy or integral nonlinearity (INL), sometimes referred to as linearity error, is the maximum deviation ot the output from the line between zero and full scale, excluding the effect of zero code and full scale errors (see text).
2. The differential nonlinearity (DNL), sometimes referred to as differential error, is the difference between the measured and ideal LSB amplitude change of any two adjacent codes. Monotonic means the output voltage changes in the same direction (or remains constant) as a change in the digital input code.
3. Zero-scale error is the deviation from zero voltage output when the digital input is zero (see text)
4. Zero-scale error temperature coefficient is given by E_{ZS} TC = [E_{ZS} (T_{max}) - E_{ZS} (T_{min})] /V_{ref} x 10^6/ (T_{max}-T_{min})
5. Gain error is the deviation from the ideal output (Vref - 1LSB) with an output load of 10kΩ, excluding the effects of zero error.
6. Gain temperature coefficient is given by EG TC = [E_G (T_{max}) - E_G (T_{min})] /V_{ref} x 10^6/(T_{max}-T_{min}).
7. Zero-scale offset error rejection ratio (E_{ZS}-RR) is measured by varying the V_{DD} from 4.5V to 5.5V DC and measuring the proportion of this signal imposed on the zero-code output voltage.
8. Gain error rejection ratio (E_G-RR) is measured by varying the V_{DD} from 4.5 to 5.5 V DC and measuring the proportion of this signal imposed on the full-scale output voltage after subtracting the zero scale change.

Voltage Output (OUT)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Voltage output range	V_O	R_L = 10kΩ	0		V_{DD}-0.4	V
Output load regulation accuracy		V_O(OUT) = 2V RL=2kΩ			0.5	LSB
Output short circuit current	I_{OSC}	OUT to V_{DD} or AGND		20		mA
Output voltage, low level	$V_{OL(low)}$	I_O (OUT) <= 5mA			0.25	V
Output voltage, high level	$V_{OH(high)}$	I_O (OUT) <= -5mA	4.75			V

Electrical Characteristics (continued)

V_{DD} = 5.0V ±5%, V_{ref} = 2.048V unless otherwise stated.

Reference Input (REFIN)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range	V_I		0		V_{DD}-2	V
Input resistance			10			MΩ
Input capacitance	C_I			5		pF

Digital Inputs (DIN, SCLK, $\overline{CS}$)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
High level digital input voltage	V_{IH}		2.4			V
Low level digital input voltage	V_{IL}				0.8	V
High level digital input current	I_{IH}	V_I = V_{DD}			±1	µA
Low level digital input current	I_{IL}	V_I = 0V			±1	µA
Input capacitance	C_I			8		pF

Digital Output (DOUT)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage high	V_{OH}	I_O = -2mA	V_{DD}-1			V
Output voltage low	V_{OL}	I_O = 2mA			0.4	V

Power Supply

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNIT
Supply voltage	V_{DD}			4.5	5	5.5	V
Power supply current	I_{DD}	V_{DD} = 5.5V, no load. All inputs = 0V or V_{DD}	V_{ref} = 0V		150	250	µA
		V_{DD} = 5.5V, no load. All inputs = 0V or V_{DD}	V_{ref} = 2.048V		230	350	µA

Electrical Characteristics (continued)

V_{DD} = 5.0V ±5%, V_{ref} = 2.048V unless otherwise stated.

Analogue Output Dynamic Performance

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output slew rate	SR	C_L = 100pF R_L = 10 kΩ T_A = 25°C	0.3	0.5		V/µs
Output settling time	ts	T_O 0.5 LSB C_L = 100pF R_L = 2kΩ (see note 9)		12.5		µs
Glitch energy		DIN = All 0s to all 1s		5		nV▪ s
Signal to noise + distortion	S/(N+D)	V_{ref} = $2V_{pp}$ at 1kHz + 2.048 V DC, code 512		60		dB

Note 9: Settling time is the time for the output signal to remain within 0.5 LSB of the final measured value for a digital input code change from code zero to 1023 rising and 1023 to 64 falling.

Digital Input Timing Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup time, DIN before SCLK high	t_{su} (DS)	45			ns
Hold time, DIN valid after SCLK high	t_h (DH)	0			ns
Setup time, $\overline{CS}$ low to SCLK high	t_{su} (CSS)	1			ns
Setup time $\overline{CS}$ high to SCLK high	t_{su} (CS1)	50			ns
Hold time, SCLK low to $\overline{CS}$ low	t_h (CSHO)	1			ns
Hold time, SCLK low to $\overline{CS}$ high	t_h (CSHI)	0			ns
Pulse duration, min. chip select pulse width height	t_w(CS)	20			ns
Pulse duration, SCLK low	t_w (CL)	18			ns
Pulse duration, SCLK high	tw (CH)	18			ns

Output Switching Specification

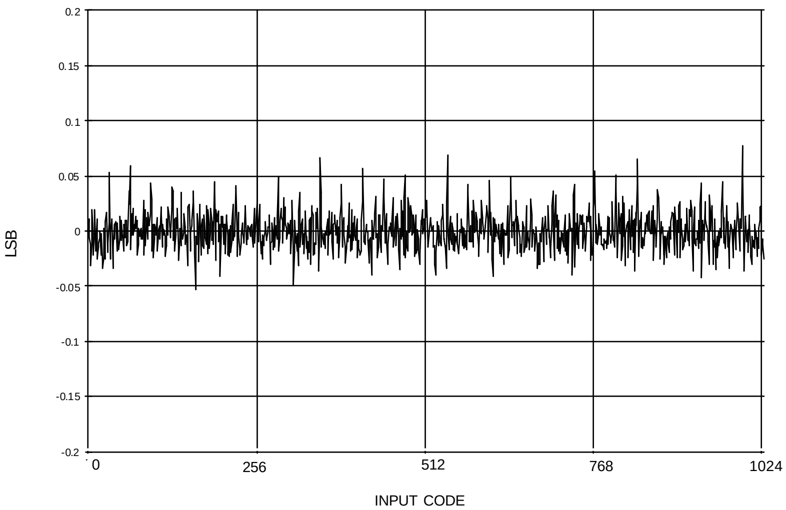
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Propagation delay time	t_{pd}(DOUT)	C_L = 50pF			50	ns

reference input (REFIN)

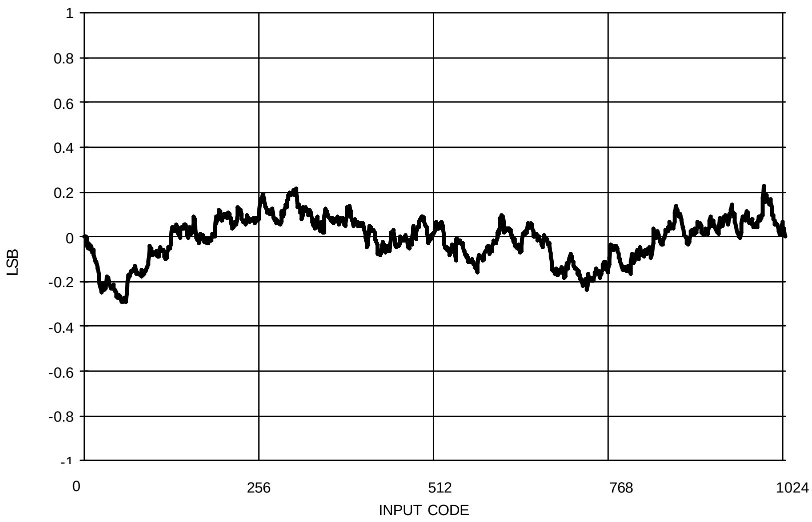
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
Reference feedthrough		Input code = 00 (see note 10)		-80		dB
Reference input bandwidth		Input code = 512 (see note 10)		100		kHz

Note 10: Reference feedthrough and bandwidth are measured at the DAC output with Vref input = 2Vpp at 1kHz + 2.048V DC

Typical Performance Characteristics



WM5615 DNL Linearity Error

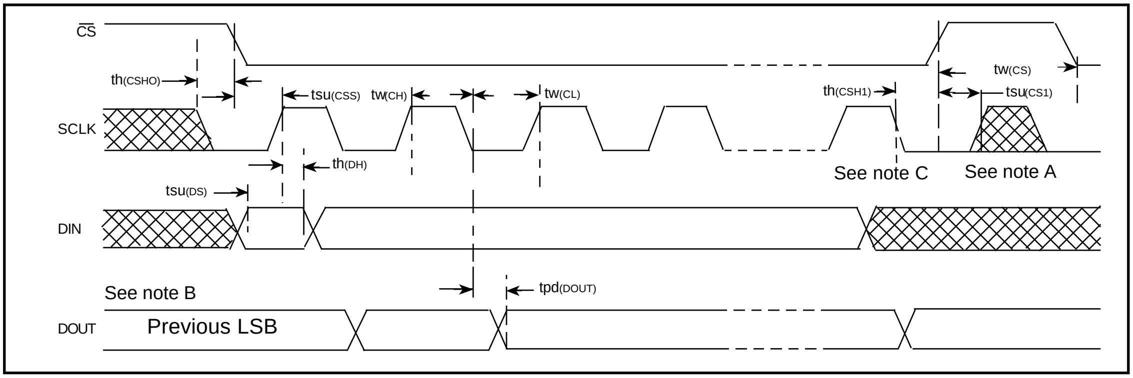


WM5615 INL Linearity Error

Pin Description

PIN	NAME	FUNCTION
1	DIN	Serial data input.
2	SCLK	Serial clock input.
3	$\overline{CS}$	Chip select, active low.
4	DOUT	Serial data output for daisy-chaining.
5	AGND	Analogue ground.
6	REFIN	Reference input.
7	VOUT	DAC output.
8	VDD	Positive power supply.

Timing Diagram



NOTES: A. The input clock, applied at the SCLK terminal, should be inhibited low when CS is high to minimise clock feedthrough.
B. Data input from preceeding conversion cycle.
C. Sixteenth SCLK falling edge.

Detailed Description

General Function

The WM5615 uses a resistor string network buffered with a single-supply CMOS op amp in a fixed gain of x2 to convert 10-bit digital data to analogue voltage levels (see Block Diagram). The topology of the WM5615 makes the output the same polarity as the reference input (see Table 1).

An internal reset circuit forces the DAC register to reset to all 0s on power-up.

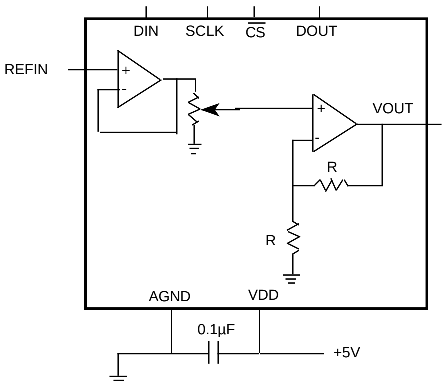


Figure 1 - Typical Operating Circuit

Detailed Description (Continued)

Table 1 - Binary Code Table
(0V to 2VREFIN Output), Gain = 2

INPUT*	OUTPUT
1111 1111 11 (xx)	$+2(V_{REFIN})\frac{1023}{1024}$
1000 0000 01 (xx)	$+2(V_{REFIN})\frac{513}{1024}$
1000 0000 00 (xx)	$+2(V_{REFIN})\frac{512}{1024} = V_{REFIN}$
0111 1111 11 (xx)	$+2(V_{REFIN})\frac{511}{1024}$
0000 0000 01 (xx)	$+2(V_{REFIN})\frac{1}{1024}$
0000 0000 00 (xx)	0V

* A 10-bit data word with two sub-LSB Xs must be written since the DAC input latch is 12-bits wide.

Buffer Amplifier
The output buffer is a rail-to-rail output CMOS op amp. Max. setting time is 12.5µs to +/-0.5 LSB of final value. The output is short-circuit protected and can drive a 2kΩ load with a 100pF load capacitance.

External Reference
The external voltage input is buffered and must be positive but less than V_{DD} - 2V. The reference voltage determines the DAC full-scale output. Since the reference terminal is buffered, the DAC input resistance is not code dependent and is 10MΩ minimum. The REFIN input capacitance is typically 5pF.

Digital Interface
The digital inputs are designed to be compatible with TTL or CMOS logic levels. However, to achieve the lowest power dissipation, the digital inputs should be driven with rail-to-rail CMOS logic. With TTL logic levels, the power requirement increases by a factor of approximately two.

Serial Interface
The WM5615 uses a three-wire serial interface which is compatible with SPI, QSPI (CPOL = CPHA = 0) and Microwire standards as shown in figures 2 and 3. The DAC is programmed by writing two 8-bit words, MSB first (see Block Diagram and Timing Diagram). 16 bits of serial data are clocked into the DAC in the following order, 4 fill (dummy) bits, 10 data bits and 2 sub-LSB Xs. The 4 dummy bits are not normally needed and are required only when DACs are daisy chained. The 2 sub-LSB Xs, however, are always needed because the input register is 12 bits wide. Transitions at $\overline{CS}$ should occur while SCLK is low. Data is clocked in on the SCLK rising edge while $\overline{CS}$ is low. The serial input data is held in a 16-bit serial shift register. On the $\overline{CS}$ rising edge, the ten data-bits are transferred to the DAC register and update the DAC. With $\overline{CS}$ high, data cannot be clocked into the DIN terminal.

The WM5615 receives data in 16-bit blocks. The SPI and Microwire interfaces output data in 8-bit blocks requiring two write cycles to input data to the DAC. The QSPI interface allows variable data output from 8 to 16 bits so can load into the DAC in one write cycle.

Detailed Description (Continued)

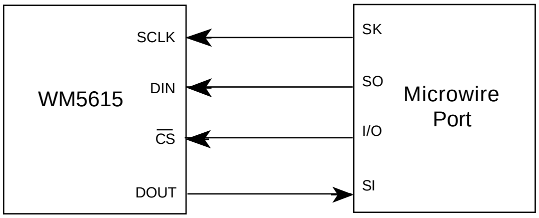


Figure 2 - Microwire Connection

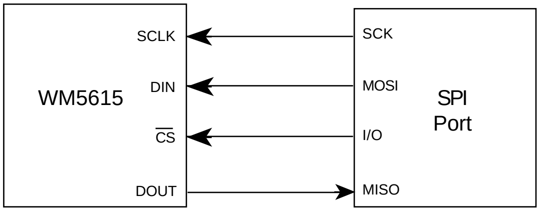


Figure 3 - SPI/QSPI Connection

Note: The DOUT-MISI connection is not required for writing to the WM5615, but may be used for verifying data transfer.

Daisy-Chaining Devices

The serial output, DOUT, allows cascading of two or more DACs. The data at DIN appears at DOUT, delayed by 16 clock cycles plus one clock width. For low power, DOUT does not require an external pull-up resistor. DOUT does not go into a high-impedance state when $\overline{CS}$ is high. DOUT changes on SCLK's falling edge when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT remains in the state of the last data bit.

Any number of DACs can be daisy-chained by connecting the DOUT of one device to the DIN of the next device in the chain.

Linearity, Offset and Gain Error using Single End Supplies

When an amplifier is operated from a single supply, the voltage offset can still be either positive or negative. With a positive offset, the output voltage changes on the first code change. With a negative offset, the output voltage may not change with the first code depending on the magnitude of the offset voltage.

The output amplifier, with a negative voltage offset, attempts to drive the output to a negative voltage. However, because the most negative supply rail is ground, the output cannot drive to a negative voltage. So when the output offset voltage is negative, the output voltage remains at zero volts until the input code value produces a sufficient output voltage to overcome the inherent negative offset voltage, resulting in the transfer function shown in figure 4.

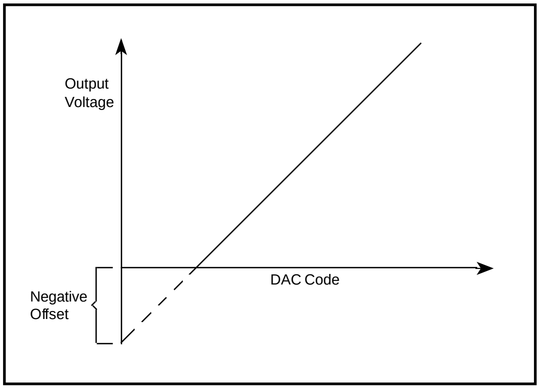


Figure 4 - Effect of Negative Offset (Single Supply)

This negative offset, not the linearity error, produces this breakpoint. The transfer function would have followed the dotted line if the output buffer could drive to a negative voltage.

For a DAC, linearity is measured between zero input code (all inputs 0) after offset and full-scale are adjusted out or accounted for in some way. However, single supply operation does not allow for adjustment when the output is negative due to the breakpoint in the transfer function. So the linearity is measured between the full-scale and the lowest code which produces a positive output voltage. For the WM5615, the zero scale (offset) is plus or minus 3LSB maximum. The code is calculated from the maximum specification for the negative offset.

Detailed Description (Continued)

Power-Supply Bypassing and Ground Management

Best system performance is obtained with printed-circuit boards that use separate analog and digital ground planes. Wire-wrap boards are not recommended. The two ground planes should be connected together at the low-impedance power-supply source. The best ground connection may be achieved by connecting the DAC AGND terminal to the system analogue ground plane.

V_{DD} should be bypassed with a 0.1µF ceramic capacitor connected between V_{DD} and AGND. It should be mounted with short leads close to the device. Ferrite beads may be used to further isolate the system analogue and digital power supplies.

Figure 5 illustrates the grounding and bypassing scheme described.

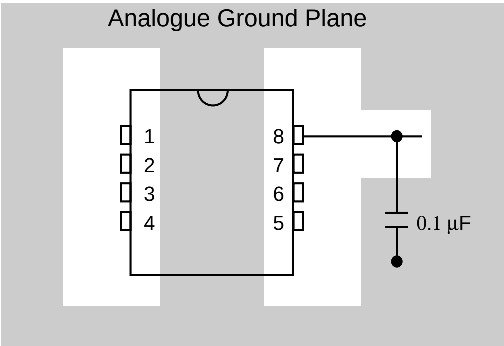


Figure 5 - Power-Supply Bypassing

Saving Power

When the DAC is not being used by the system, minimize power consumption by setting the appropriate code to minimize load. For example, with a resistive load to ground, set the DAC code to 0 (see Table 1). In addition, the REFIN buffer has to drive current into the DAC resistor string and so setting REFIN to 0 further reduces power consumption.

Analogue Feedthrough

Because of internal stray capacitance, higher frequency analog input signals may couple to the output. this is tested by holding $\overline{CS}$ high, setting the DAC code to all 0s and sweeping REFIN.

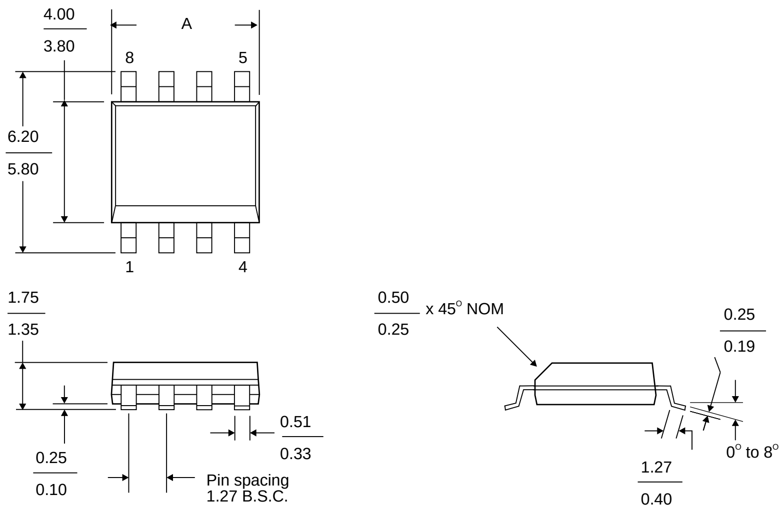
Digital Feedthrough

High-speed serial data at any of the digital input or output pins may couple through the DAC package internal stray capacitance to appear at the DAC output as noise, even though $\overline{CS}$ is held high. This digital feedthrough is tested by holding $\overline{CS}$ high while transmitting 1010... from DIN to DOUT.

Package Descriptions

Plastic Small-Outline Package

D - 8 pins shown



Dimension 'A' Variations

N	Min	Max
8	4.80	5.00
14	8.55	8.75
16	9.80	10.00

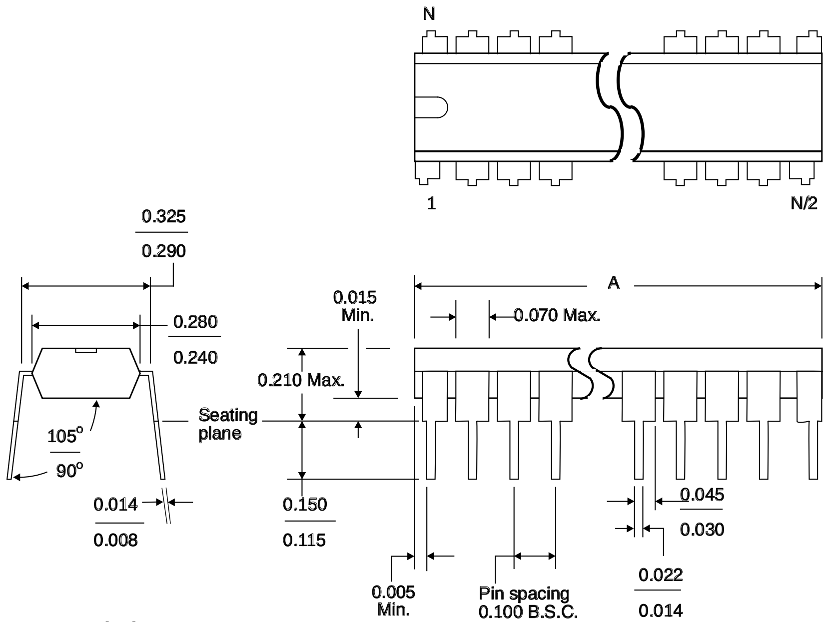
Notes:

A. Dimensions in millimeters.
B. Complies with Jedec standard MS-012.
C. This drawing is subject to change without notice.
D. Body dimensions do not include mold flash or protrusion.
E. Dimension A, mould flash or protrusion shall not exceed 0.15mm. Body width, interlead flash or protrusions shall not exceed 0.25mm.

Package Descriptions

Dual-In-Line Package

N or P



Dimension 'A' Variations

N	Min	Max
8	0.355	0.400
14	0.735	0.775
16	0.735	0.775
20	0.940	0.975

Notes:

A. Dimensions are in inches
B. Falls within JEDEC MS-001(20 pin package is shorter than MS-001)
C. N is the maximum number of terminals
D. All end pins are partial width pins as shown, except the 14 pin package which is full width.