SYNCHRONOUS CACHE TAG SRAM PIPELINED OUTPUT

64K x 18 SRAM

+3.3V SUPPLY WITH CLOCKED REGISTERED INPUTS

FEATURES

- Fast match times: 4.5, 5.0, 6.0, and 7.0ns
- Fast clock speed: 133, 100, 83, and 75 MHz
- Fast OE# access times: 4.5ns and 5.0ns
- Pipelined data comparator
- Data input register load control by DEN#
- 3.3V -5% and +10% power supply
- 5V tolerant inputs except I/O's
- Clamp diodes to VSS at all inputs and outputs
- Common data inputs and data outputs
- Two chip enables for depth expansion
- Address, data and control registers
- Internally self-timed WRITE CYCLE
- Automatic power-down for portable applications
- Low profile 119 lead, 14mm x 22mm BGA (Ball Grid Array) and 100 pin TQFP packages

OPTIONS MARKING

- Timing

4.5ns access/7.5ns cycle	-4
5.0ns access/10ns cycle	-5
6.0ns access/12ns cycle	-6
7.0ns access/13.3ns cycle	-7

- Packages

119-lead BGA	B
100-pin TQFP	T

GENERAL DESCRIPTION

The Galvantech Synchronous SRAM family employs high-speed, low power CMOS designs using advanced triple-layer polysilicon, double-layer metal technology. Each memory cell consists of four transistors and two high valued resistors.

The GVT7164T18 SRAM integrates 65,536 x 18 SRAM cells with advanced synchronous peripheral circuitry and a 18-bit comparator for tag compare operation. All synchronous inputs are gated by registers controlled by a positive-edge-triggered clock input (CLK). The synchronous inputs include all addresses, all data inputs, depth-expansion chip enables (CE# and CE1), write enable (WE#), and data input enable (DEN#).

Asynchronous inputs include the output enable (OE#) and the match output enable (MOE#). The data outputs (Q) and match output (MATCH), enabled by OE# and MOE# respectively, are also asynchronous.

Data inputs are registered with data input enable (DEN#) and chip enable pins (CE#, CE1). The outputs of the data input registers are compared with data in the memory array and a match signal is generated. The match output is gated into a pipeline register and released to the match output pin at the next rising edge of clock (CLK).

The GVT7164T18 operates from a +3.3V power supply. All inputs and outputs are LVTTL compatible. The device is ideally suited for address tag RAM for up to 2 MB secondary cache.

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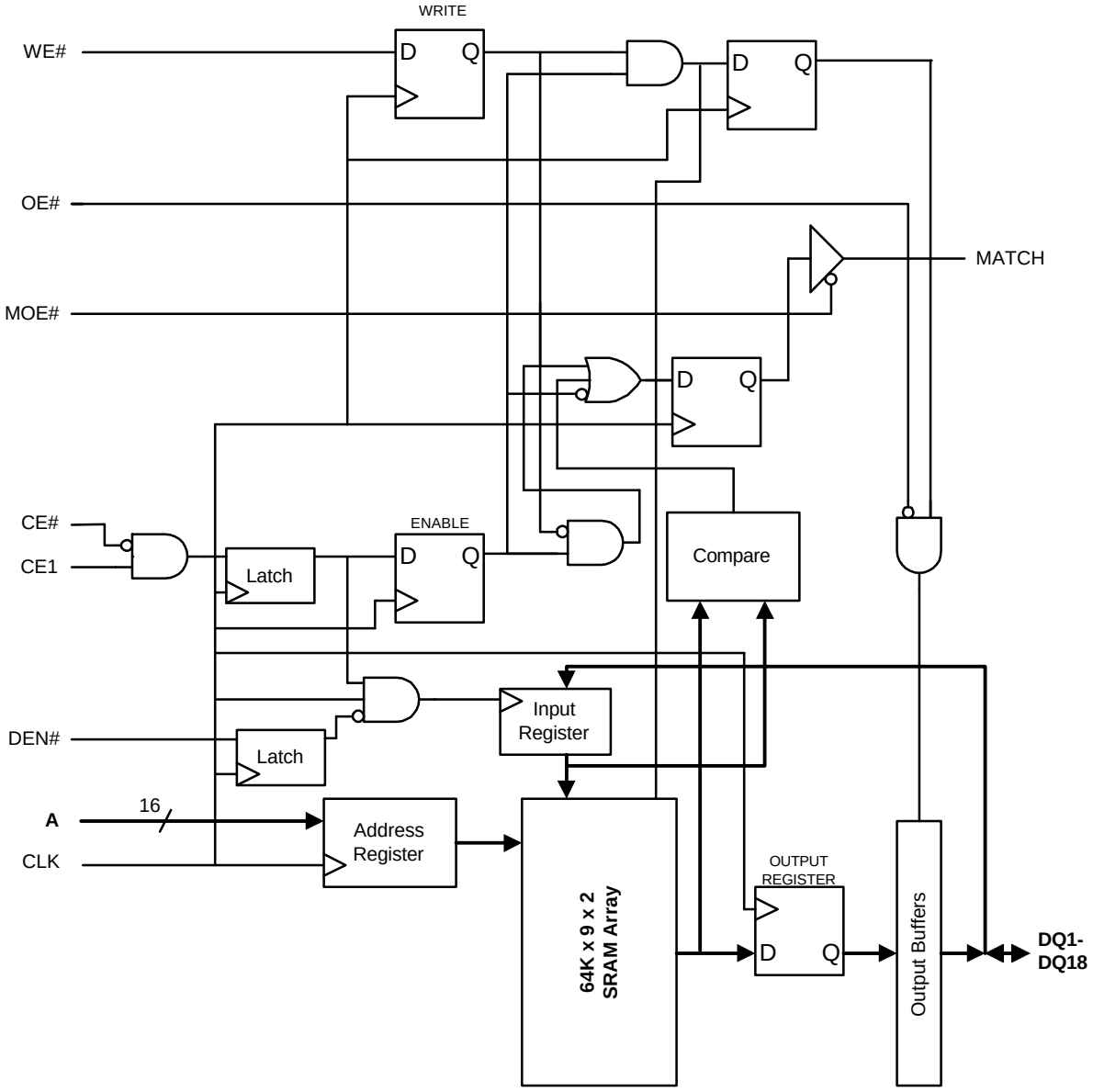
Rev. 11/97

FUNCTIONAL BLOCK DIAGRAM

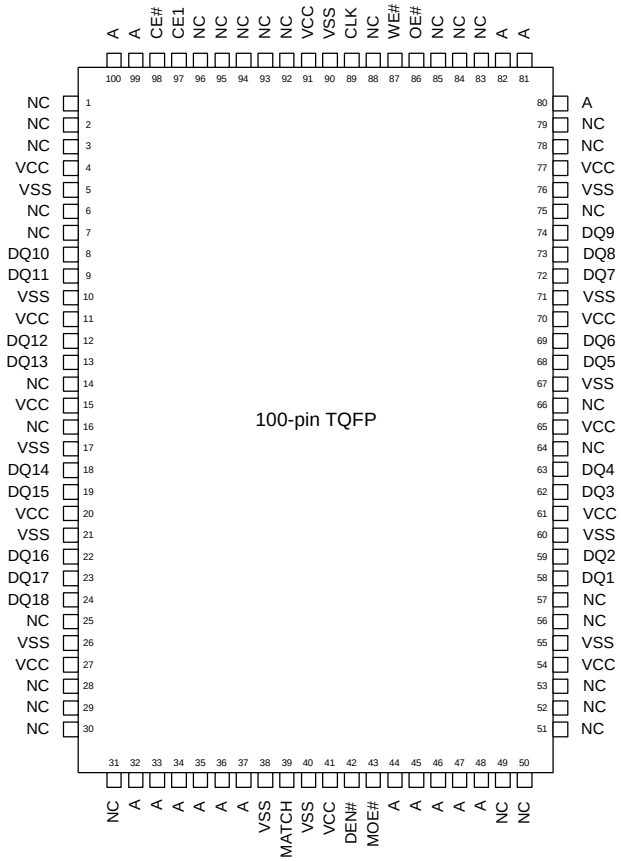


NOTE: The Functional Block Diagram illustrates simplified device operation. See Truth Table, pin descriptions and timing diagrams for detailed information.

PIN ASSIGNMENTS (TOP VIEW)

	1	2	3	4	5	6	7
A	VCC	A	A	NC	A	NC	VCC
B	NC	CE1	NC	NC	NC	CE#	NC
C	NC	NC	NC	VCC	A	A	NC
D	DQ10	NC	VSS	NC	VSS	DQ9	NC
E	NC	DQ11	VSS	NC	VSS	NC	DQ8
F	VCC	NC	VSS	OE#	VSS	DQ7	VCC
G	NC	DQ12	NC	NC	VSS	NC	DQ6
H	DQ13	NC	VSS	WE#	VSS	DQ5	NC
J	VCC	VCC	NC	VCC	NC	VCC	VCC
K	NC	DQ14	VSS	CLK	VSS	NC	DQ4
L	DQ15	NC	VSS	NC	NC	DQ3	NC
M	VCC	DQ16	VSS	NC	VSS	NC	VCC
N	DQ17	NC	VSS	A	VSS	DQ2	NC
P	NC	DQ18	VSS	A	VSS	NC	DQ1
R	NC	A	A	VCC	A	A	NC
T	NC	A	A	MATCH	A	A	NC
U	VCC	DEN#	NC	A	MOE#	NC	VCC

TOP VIEW 119 LEAD BGA



PIN DESCRIPTIONS

BGA PINS	TQFP PINS	SYMBOL	TYPE	DESCRIPTION
2A, 3A, 5A, 5C, 6C, 4N, 4P, 2R, 3R, 5R, 6R, 2T, 3T, 5T, 6T, 4U	37, 36, 35, 34, 33, 32, 100, 99, 82, 81, 80, 48, 47, 46, 45, 44	A	Input-Synchronous	Addresses: These inputs are registered and must meet the setup and hold times around the rising edge of CLK.
4H	87	WE#	Input-Synchronous	Write Enable: this write enable is LOW for a WRITE cycle and HIGH for a READ cycle. Data I/O are high impedance one cycle after WE#=LOW is gated into register.
4K	89	CLK	Input-Synchronous	Clock: This signal registers the addresses, data, chip enables, write control and data input enable control input on its rising edge. All synchronous inputs must meet setup and hold times around the clock's rising edge.
6B	98	CE#	Input-Synchronous	Chip Enable: This active LOW input is used to enable the device.
2B	97	CE1	input-Synchronous	Chip enable: This active HIGH input is used to enable the device.
4F	86	OE#	Input	Output Enable: This active LOW asynchronous input enables the data output drivers.
2U	42	DEN#	Input-Synchronous	Data Input Enable: This active LOW input is used to control the update of data input registers.
4T	39	MATCH	Output	Match Output: MATCH will be HIGH if data in the data input registers match the data stored in the memory array, assuming MOE# being LOW. MATCH will be LOW if data do not match.
5U	43	MOE#	Input	Match Output Enable: This active LOW asynchronous input enables the MATCH output drivers.
7P, 6N, 6L, 7K, 6H, 7G, 6F, 7E, 6D, 1D, 2E, 2G, 1H, 2K, 1L, 2M, 1N, 2P	58, 59, 62, 63, 68, 69, 72, 73, 74, 8, 9, 12, 13, 18, 19, 22, 23, 24	DQ1-DQ18	Input/ Output	Data Inputs/Outputs: Input data must meet setup and hold times around the rising edge of CLK.
1A, 7A, 4C, 1F, 7F, 1J, 2J, 4J, 6J, 7J, 1M, 7M, 4R, 1U, 7U	4, 11, 15, 20, 27, 41, 54, 61, 65, 70, 77, 91	VCC	Supply	Power Supply: +3.3V -5% and +10%
3D, 5D, 3E, 5E, 3F, 5F, 5G, 3H, 5H, 3K, 5K, 3L, 3M, 5M, 3N, 5N, 3P, 5P	5, 10, 17, 21, 26, 38, 40, 55, 60, 67, 71, 76, 90	VSS	Ground	Ground: GND.
4A, 6A, 1B, 3B, 4B, 5B, 7B, 1C, 2C, 3C, 7C, 2D, 4D, 7D, 1E, 4E, 6E, 2F, 1G, 3G, 4G, 6G, 2H, 7H, 3J, 5J, 1K, 6K, 2L, 4L, 5L, 7L, 4M, 6M, 2N, 7N, 1P, 6P, 1R, 7R, 1T, 7T, 3U, 6U	1-3, 6, 7, 14, 16, 25, 28-31, 49-53, 56, 57, 64, 66, 75, 78, 79, 83-85, 88, 92-96	NC	-	No Connect: These signals are not internally connected.

TRUTH TABLE

OPERATION	E#	WE#	DEN#	MOE##	OE#	MATCH	DQ
READ Cycle	L	H	X	X	L	-	Q
WRITE Cycle	L	L	L	X	H	-	D
Fill WRITE Cycle	L	L	H	X	H	-	High-Z
COMPARE Cycle	L	H	L	L	H	Output	D
Deselected Cycle (MATCH Out)	H	X	X	L	X	H	High-Z
Deselected Cycle	H	X	X	H	X	High-Z	High-Z

Note:
1. X means “don’t care.” H means logic HIGH. L means logic LOW.
2. E# =L is defined as CE#=LOW and CE1=HIGH. E# =H is defined as CE#=HIGH or CE1=LOW.
3. All inputs except OE# and MOE# must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
4. For a write operation following a read operation, OE# must be HIGH before the input data required setup time plus High-Z time for OE# and staying HIGH throughout the input data hold time.
5. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

THERMAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	BGA TYP	TQFP TYP	UNITS	NOTES
Thermal Resistance - Junction to Ambient	Still air, soldered on 4.25 x 1.125 inch 4-layer PCB	Θ_{JA}	19	25	^{o}C/W	
Thermal Resistance - Junction to Case		Θ_{JC}	9	9	^{o}C/W	

ABSOLUTE MAXIMUM RATINGS*

Voltage on VCC Supply Relative to VSS.....-0.5V to +4.6V
V_{IN} .....-0.5V to VCC+0.5V
Storage Temperature (plastic) .....-55°C to +150°
Junction Temperature .....+150°
Power Dissipation 1.0W
Short Circuit Output Current 50mA

*Stresses greater than those listed uunder "Absolute Maximum Ratings" may cause permanent damage to the device.This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED OPERATING CONDITIONS

(0°C ≤ T_a ≤ 70°C; VCC = 3.3V -5% and +10% unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) voltage	Data Inputs (DQxx)	V_{IHD}	2.0	VCC+0.5	V	1,2
	All Other Inputs	V_{IH}	2.0	4.6	V	1,2
Input Low (Logic 0) Voltage		V_{II}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ VCC	IL_I	-1	1	uA	14
Output Leakage Current	Output(s) disabled, 0V ≤ V_{OUT} ≤ VCC	IL_O	-1	1	uA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1, 11
Output Low Voltage	I_{OL} =8.0mA	V_{OL}		0.4	V	1, 11
Supply Voltage		VCC	3.135	3.6	V	1

DESCRIPTION	CONDITIONS	SYM	TYP	-4	-5	-6	-7	UNITS	NOTES
Power Supply Current: Operating	Device selected; all inputs ≤ V_{IL} or ≥ V_{IH};cycle time ≥ ^tKC MIN; VCC =MAX; outputs open	Icc	150	300	240	220	200	mA	3, 12, 13
CMOS Standby	Device deselected; VCC = MAX; all inputs ≤ VSS +0.2 or ≥VCC -0.2; all inputs static; CLK frequency = 0	I_{SB2}	5	10	10	10	10	mA	12,13
TTL Standby	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; all inputs static; VCC = MAX; CLK frequency = 0	I_{SB3}	10	20	20	20	20	mA	12,13
Clock Running	Device deselected; all inputs ≤ V_{IL} or ≥ V_{IH}; VCC = MAX; CLK cycle time ≥ ^tKC MIN	I_{SB4}	40	80	70	60	50	mA	12,13

AC ELECTRICAL CHARACTERISTICS

(Note 5) ($0^oC \leq T_A \leq 70^oC$; VCC = 3.3V -5% and +10%)

DESCRIPTION		- 4 133MHz		- 5 100MHz		- 6 83MHz		- 7 75MHz			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Clock											
Clock cycle time	^tKC	7.5		10		12		13.3		ns	
Clock HIGH time	^tKH	3.0		3.5		4.0		4.5		ns	
Clock LOW time	^tKL	3.0		3.5		4.0		4.5		ns	
Output Times											
Clock to output valid	^tKQ		4.5		5.0		6.0		7.0	ns	
Clock to MATCH valid	^tKM		4.5		5.0		6.0		7.0	ns	
Clock to output invalid	^tKQX	1.5		1.5		1.5		1.5		ns	
Clock to MATCH invalid	^tKMX	1.5		1.5		1.5		1.5		ns	
Clock to output in Low-Z	^tKQLZ	0		0		0		0		ns	4, 6,7
Clock to output in High-Z	^tKQHZ	1.5	5.0	1.5	5.0	1.5	5.0	1.5	5.0	ns	4, 6,7
OE to output valid	^tOEQ		4.5		5.0		5.0		5.0	ns	9
MOE to MATCH valid	^tMOEM		4.5		5.0		5.0		5.0	ns	9
OE to output in Low-Z	^tOELZ	0		0		0		0		ns	4, 6,7
MOE to MATCH in Low-Z	^tMOELZ	0		0		0		0		ns	4, 6,7
OE to output in High-Z	^tOEHZ		4.5		5.0		5.0		5.0	ns	4, 6,7
MOE to MATCH in High-Z	^tMOEHZ		4.5		5.0		5.0		5.0	ns	4, 6,7
Setup Times											
Address, Controls and Data In	^tS	2.0		2.5		2.5		2.5		ns	10
Hold Times											
Address, Controls and Data In	^tH	0.5		0.5		0.5		0.5		ns	10

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25^oC$; f = 1 MHz VCC = 3.3V	C_I	4	5	pF	4
Input/Output Capacitance (DQ)		C_O	7	8	pF	4

TYPICAL OUTPUT BUFFER CHARACTERISTICS

OUTPUT HIGH VOLTAGE	PULL-UP CURRENT			OUTPUT LOW VOLTAGE	PULL-DOWN CURRENT	
VOH (V)	IOH(mA) Min	IOH(mA) Max		VOL (V)	IOL(mA) Min	IOL(mA) Max
-0.5	-38	-105		-0.5	0	0
0	-38	-105		0	0	0
0.8	-38	-105		0.4	10	20
1.25	-26	-83		0.8	20	40
1.5	-20	-70		1.25	31	63
2.3	0	-30		1.6	40	80
2.7	0	-10		2.8	40	80
2.9	0	0		3.2	40	80
3.4	0	0		3.4	40	80

AC TEST CONDITIONS

Input pulse levels	0V to 3.0V
Input rise/fall time	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V

OUTPUT LOADS

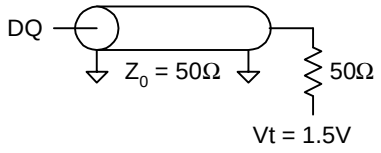


Fig. 1 OUTPUT LOAD EQUIVALENT

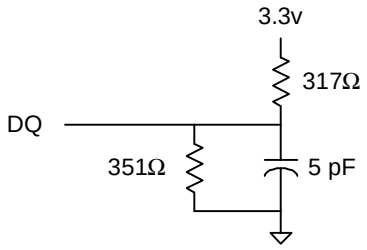
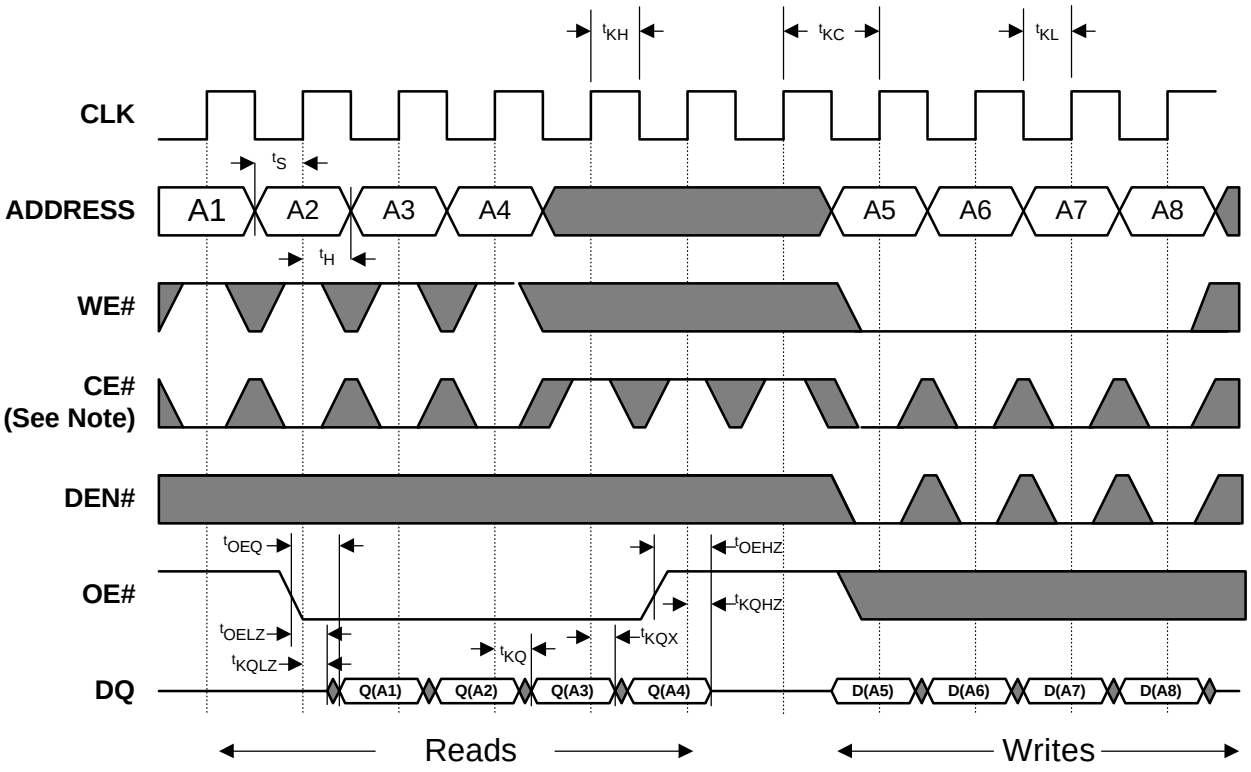


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

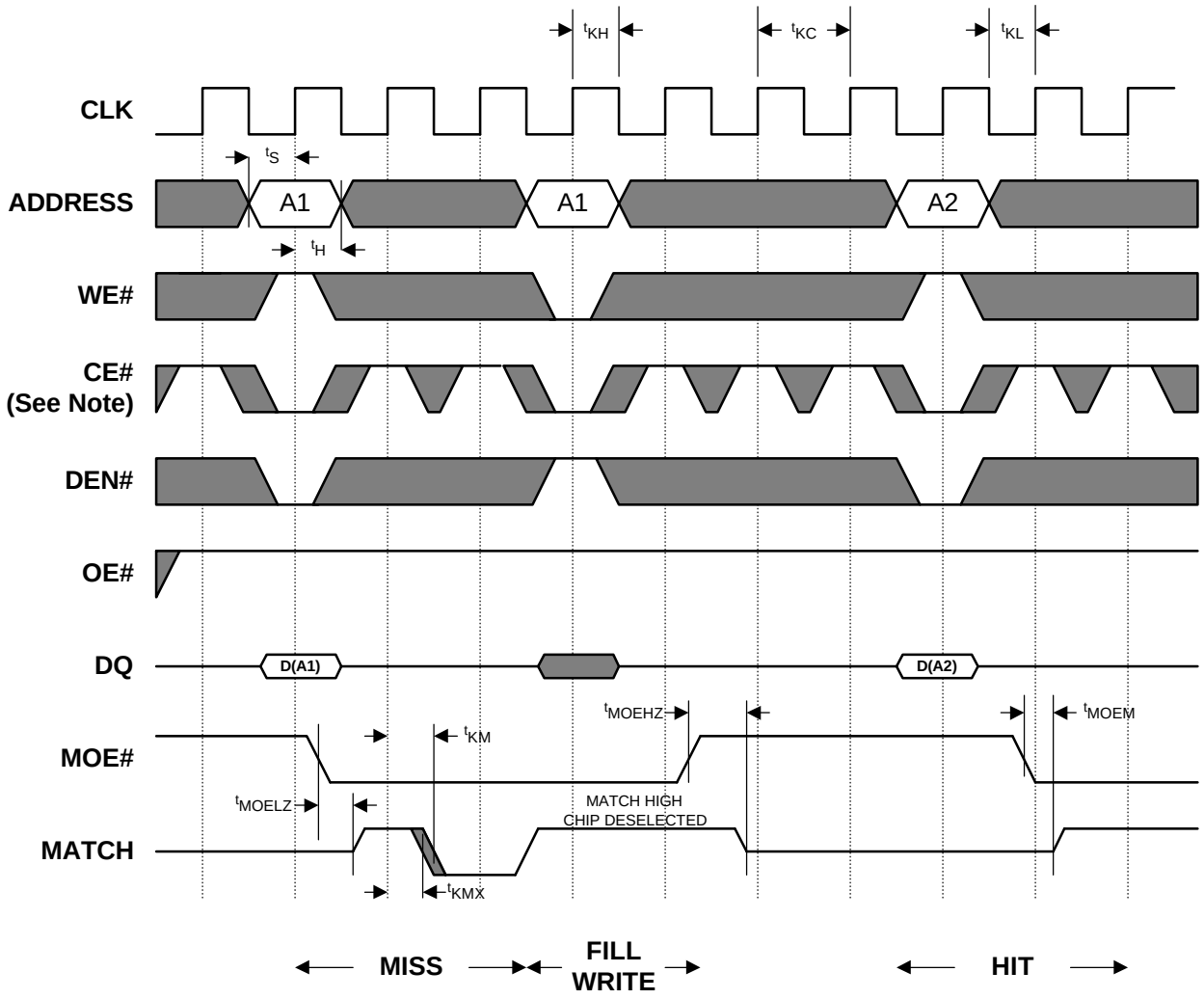
1. All voltages referenced to VSS (GND).
2. Overshoot: $V_{IH} \leq +6.0V$ for $t \leq {}^tKC/2$.
   Undershoot: $V_{IL} \leq -2.0V$ for $t \leq {}^tKC/2$
3. I_{cc} is given with no output current. I_{cc} increases with greater output loading and faster cycle times.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL=5pF as in Fig. 2.
7. At any given temperature and voltage condition, ${}^tKQHZ$ is less than ${}^tKQLZ$, ${}^tOEHZ$ is less than ${}^tOELZ$ and ${}^tMOEHZ$ is less than ${}^tMOELZ$.
8. A READ cycle is defined by write enable (WE#) HIGH along with chip enables being active for the required setup and hold times. A WRITE cycle is defined by write enable (WE#) LOW along with chip enables being active for the required setup and hold times.
9. OE# is a “don’t care” when a write enable (WE#) is sampled LOW.
10. This is a synchronous device. All synchronous inputs must meet specified setup and hold time, except for “don’t care” as defined in the truth table.
11. AC I/O curves are available upon request.
12. “Device Deselected” means the device is in POWER -DOWN mode as defined in the truth table. “Device Selected” means the device is active.
13. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
14. Capacitance derating applies to capacitance different from the load capacitance shown in Fig. 1.

READ/WRITE TIMING



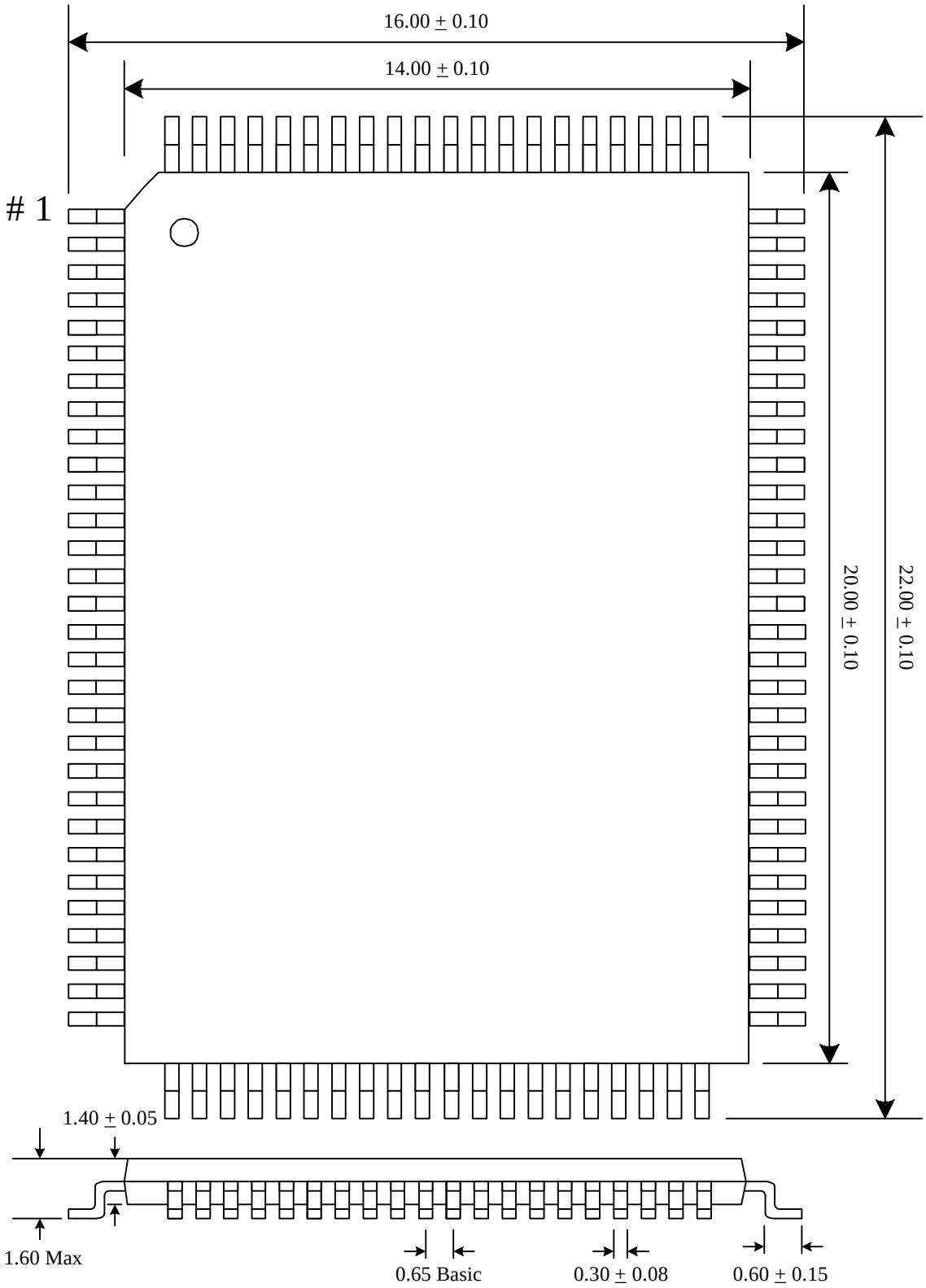
Note: CE# active in this timing diagram means that all chip enables CE# and CE1 are active.

COMPARE/FILL WRITE TIMING



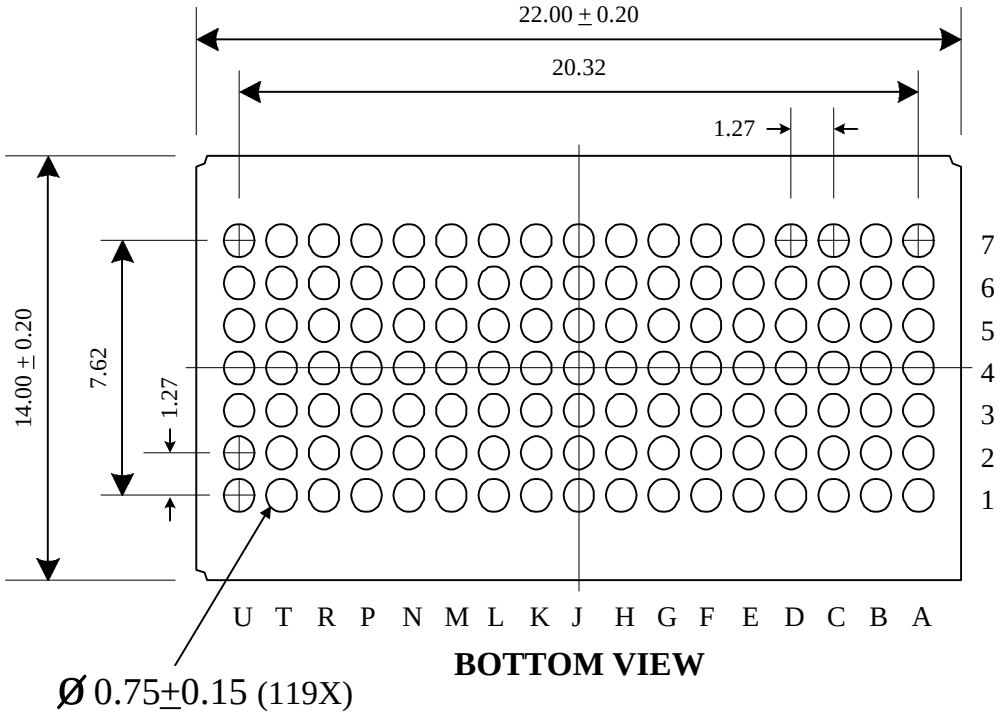
Note: CE# active in this timing diagram means that all chip enables CE# and CE1 are active.

100 Pin TQFP Package Dimensions

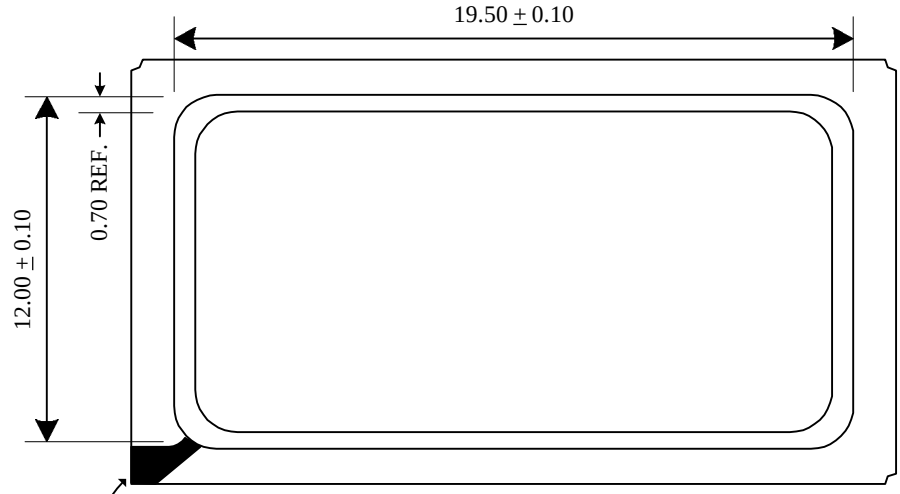


Note: All dimensions in Millimeters

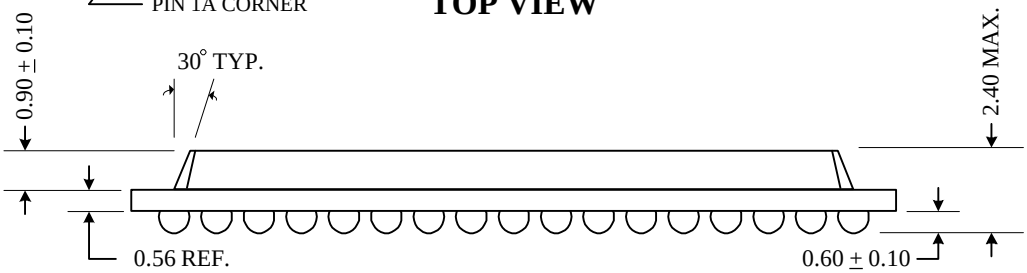
7 x 17 (119-lead) BGA Dimensions



BOTTOM VIEW



TOP VIEW



SIDE VIEW

Note: All dimensions in Millimeters

Ordering Information