8925

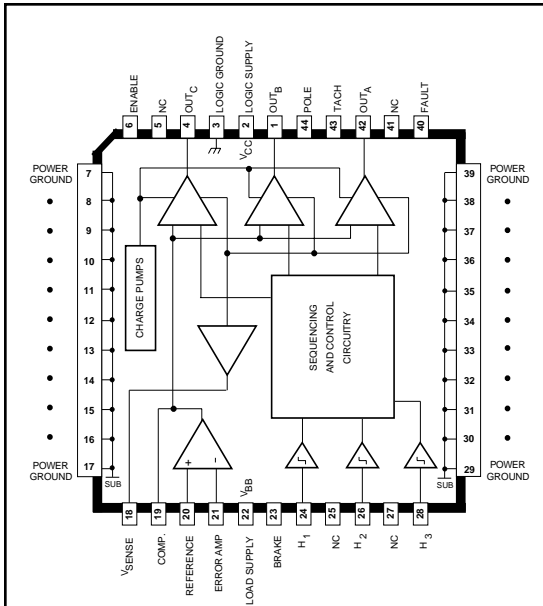# 3-PHASE BRUSHLESS DC MOTOR CONTROLLER/DRIVER WITH LINEAR CURRENT CONTROL AND POWER DMOS OUTPUTS

Dwg. PP-034

The A8925CEB is a DMOS three-phase brushless dc motor controller/driver designed for use in Winchester disk drives and other data storage applications. The power output stages are capable of ±4 A output currents and have DMOS power outputs with less than 0.25 Ω $r_{DS(on)}$ for low power dissipation. Intrinsic ground clamp and flyback diodes protect the output drivers when switching inductive loads. Thermal shutdown circuitry is provided to protect the device from excessive junction temperature.

A transconductance amplifier is used to linearly regulate the load current and control motor speed. Internal current-sensing circuitry eliminates the need for external sense resistors. Analog and digital control circuitry provide complete sequencing of the output drivers as well as providing brake, disable, and tachometer functions. A FAULT output flag indicates the presence of an under-voltage condition on the 12 V supply, excessive junction temperature, or an invalid Hall input combination. The A8925CEB's commutation logic is compatible with motors that have digital Hall-effect sensors with 120° of electrical separation. Internal charge pump circuitry is provided to drive the N-channel DMOS source drivers to their required gate voltages.

The A8925CEB is provided in a 44-lead PLCC power package for surface-mount applications. The copper batwing provides for maximum allowable package power dissipation in the smallest possible construction.

ABSOLUTE MAXIMUM RATINGS
AT T_A = +25°C

Load Supply Voltage, V_{BB} .... **14 V**
Output Current, I_{OUT} .... **±4.0 A**
Logic Supply Voltage, V_{CC} .... **14 V**
Logic Input Voltage Range,
 V_{IN} .... **-0.3 V to +6.0 V**
Package Power Dissipation,
 P_D .... **See Graph**
Operating Temperature Range,
 T_A .... **0°C to +70°C**
Junction Temperature, T_J .... **+150°C†**
Storage Temperature Range,
 T_S .... **-55°C to +150°C**

† Fault conditions that produce excessive junction temperature will activate device thermal shutdown circuitry. These conditions can be tolerated, but should be avoided.

Output current rating may be restricted to a value determined by system concerns and factors. These include: system duty cycle and timing, ambient temperature, and use of any heatsinking and/or forced cooling. For reliable operation, the specified maximum junction temperature should not be exceeded.

FEATURES

■ DMOS Outputs
■ Low $r_{DS(on)}$ - 0.25 Ω Maximum
■ Linear Current Control
■ Internal Commutation Circuitry
■ Internal Current Sensing
■ Thermal Shutdown Circuitry
■ Under Voltage Detection Circuitry
■ Fault Output Flag
■ Power Surface-Mount Package

Always order by complete part number: **A8925CEB** .

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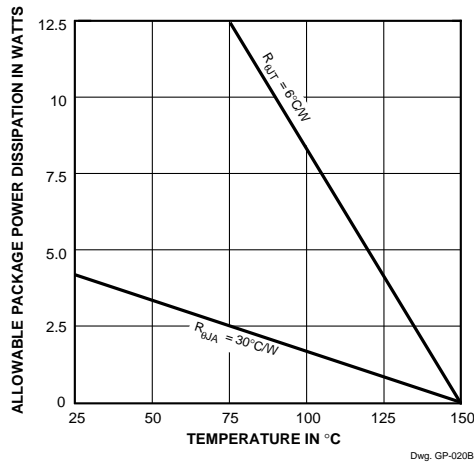
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ELECTRICAL CHARACTERISTICS AT T_A = +25°C, V_{CC} = V_{BB} = 12 V

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Logic Supply Voltage	V_{CC}	Operating	10	12	14	V
Load Supply Voltage	V_{BB}	Operating	10	12	14	V
Supply Current	I_{CC}	Operating	—	30	50	mA
		V_{ENABLE} = 0 V	—	2.0	4.0	mA
Thermal Shutdown	T_J		—	165	—	°C
Output Drivers						
Output ON Resistance	$r_{DS(on)}$	I_{OUT} = ±4.0 A, Pulse Test	—	0.20	0.25	Ω
Output Sustaining Voltage	$V_{DS(sus)}$	I_{OUT} = 4.0 A, L = 2 mH	14	—	—	V
Clamp Diode Forward Voltage	V_F	I_F = ±4.0 A	—	1.5	2.0	V
Output Leakage Current	I_{DSX}	V_{OUT} = 14 V	—	10	300	μA
		V_{OUT} = 0 V	—	-10	-300	μA
Control Logic						
Logic Input Voltage	$V_{IN(0)}$	ENABLE, POLE	—	—	0.8	V
	$V_{IN(1)}$		2.4	—	—	V
Logic Input Voltage	$V_{IN(0)}$	BRAKE	—	—	0.8	V
	$V_{IN(1)}$		3.0	—	—	V
Logic Input Current	$I_{IN(0)}$	V_{IN} = 0.8 V	—	—	-1.0	μA
	$I_{IN(1)}$	V_{IN} = 2.4 V	—	—	1.0	μA

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

ELECTRICAL CHARACTERISTICS CONTINUED

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Logic Output Voltage (FAULT, TACH)	$V_{OUT(0)}$	I_{OUT} = 3 mA	—	—	0.8	V
	$V_{OUT(1)}$	I_{OUT} = -50 µA	2.0	—	—	V
Error Amplifier						
Input Bias Current	I_{IB}	V_{CM} = 0.01 V	—	5.0	10	µA
Input Offset Voltage	V_{OS}	V_{CM} = 1.0 V	—	3.0	5.0	mV
Input Common-Mode Voltage Range	V_{IC}		0.01	—	6.0	V
Error Voltage Gain	A_{VD}	$V_{S\ OUT}$ / $V_{S\ IN}$, V_{CM} = 1.0 V	—	80	—	dB
Unity Gain Bandwidth	BW		—	1.0	—	MHz
Common-Mode Rejection Ratio	CMRR		—	80	—	dB
Power Supply Rejection Ratio	PSRR		—	50	—	dB
Miscellaneous						
Current Sense Gain	A_{iCS}	I_{OUT} = -1.0 A	1/1k	1/1.2k	1/1.4k	—
Current-Sense Matching	—	I_{OUT} = -1.0 A	—	±3.0	±5.0	%
Under-Voltage Trip Point	V_{CC}		8.0	—	9.5	V
Hall Input Current	$I_{IN(0)}$	V_{IN} = 0 V	—	-500	-1000	µA
	$I_{IN(1)}$	V_{IN} = 5.0 V	—	-250	-500	µA
Hall Input Threshold	V_{IN}		—	3.8	—	V
Hall Input Pull-Up Resistance	R_{PU}		—	25	—	kΩ

NOTE: Negative current is defined as coming out of (sourcing) the specified device terminal.

COMMUTATION TRUTH TABLE

Hall Sensor Inputs						Outputs		
H_1	H_2	H_3	ENABLE	BRAKE	FAULT	OUT_A	OUT_B	OUT_C
High	Low	High	High	High	High	High	Low	Z
High	Low	Low	High	High	High	High	Z	Low
High	High	Low	High	High	High	Z	High	Low
Low	High	Low	High	High	High	Low	High	Z
Low	High	High	High	High	High	Low	Z	High
Low	Low	High	High	High	High	Z	Low	High
High	High	High	High	High	Low	Z	Z	Z
Low	Low	Low	High	High	Low	Z	Z	Z
X	X	X	Low	High	X	Z	Z	Z
X	X	X	X	Low	X	Low	Low	Low

X = Irrelevant
Z = High Impedance

TERMINAL FUNCTIONS

Term.	Terminal Name	Function
1	OUT_B	Power DMOS output.
2	LOGIC SUPPLY	V_{CC}; low-current 12 V supply for the logic.
3	LOGIC GROUND	Low-level logic ground.
4	OUT_C	Power DMOS output.
6	ENABLE	Active high chip enable.
7–17	POWER GROUND	Power ground and thermal heat sink.
18	V_{SENSE}	External precision resistor for sense-FET current.
19	COMP.	Compensation; error amplifier output.
20	REFERENCE	V_{REF}; voltage input that sets the power output current.
21	ERROR AMP.	Input that controls the current in the load.
22	LOAD SUPPLY	V_{BB}; high-current 12 V supply for the voice-coil motor.
23	$\overline{BRAKE}$	A logic low turns OFF all source drivers and turns ON all sink drivers (shorts the windings to ground).
24	H_1	High-level input from a Hall sensor.
26	H_2	High-level input from a Hall sensor.
28	H_3	High-level input from a Hall sensor.
29–39	POWER GROUND	Power ground and thermal heat sink.
40	FAULT	A logic low at this output indicates a thermal shutdown, under -voltage fault, or an invalid Hall input combination.
42	OUT_A	Power DMOS output.
43	TACH	Speed reference output; the H_1 Hall input divided by the number of motor poles.
44	POLE	Designates four- or eight-pole motor; Low = 4 pole, High = 8 pole.

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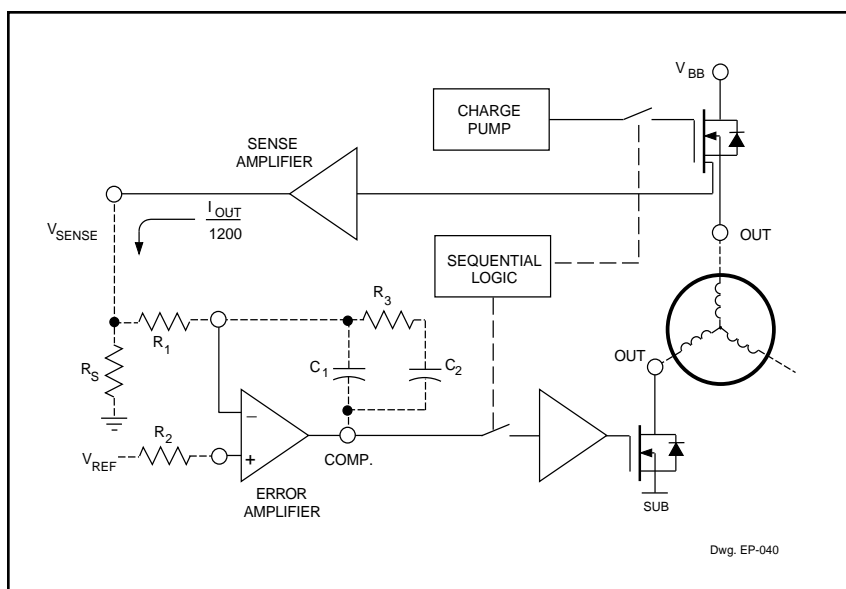
FUNCTIONAL DESCRIPTION

Power Outputs (OUT$_A$, OUT$_B$, and OUT$_C$). The power outputs of the A8925CEB are DMOS transistors with a maximum $r_{DS(on)}$ of 0.25 Ω. Intrinsic ground clamp and flyback diodes clamp transient voltage spikes when switching inductive loads. Internal charge pump circuitry is used to drive the gates of the N-channel source drivers to their required gate voltages.

Current Control. Current in the load is monitored by an internal sense amplifier that produces an output current that is approximately one twelve hundredth that of the load current (see Figure). This current is output to the V_{SENSE} terminal and develops a voltage

across R_S that equals $R_S \cdot I_{LOAD}/1200$. This sense voltage (V_{SENSE}) is compared to a reference voltage (V_{REF}) and an error voltage is developed that is gated in by the sequential control logic to drive the gate of the appropriate output sink transistor. A transconductance control function is thus realized where $I_{OUT} = V_{REF} \cdot 1200/R_S$. External components C_1, C_2, R_1, R_2, and R_3 are compensation components used to obtain optimal response and settling of the current control loop. Information on how to select these components is available.

FAULT. The FAULT terminal when low indicates the presence of one of three fault conditions:

A) An under-voltage condition on the logic supply. The trip point for this function is between 8 and 9.5 volts.

B) An invalid Hall input combination … all inputs High or all inputs Low.

C) An excessive device junction temperature. The thermal shutdown circuitry disables the output drivers in addition to forcing the FAULT output signal low.

TACH and POLE. In order to develop a low-jitter tachometer signal (TACH) for use in controlling motor speed, the A8925CEB divides the frequency of the H_1 input by the number of poles in the motor. This eliminates the jitter caused by variations in Hall-effect device placement , sensitivity, and magnet strengths by always changing state when looking at the same magnet/sensor pair. The resulting TACH signal changes state every mechanical revolution of the motor. The POLE input sets the TACH signal for four-pole motors when Low or eight-pole motors when High.

HALL INPUTS (H$_1$, H$_2$, H$_3$). The A8925CEB is configured for use with open-collector Hall-effect devices. Internal 25 kΩ pull up resistors to 10 volts are connected to these inputs.

ENABLE. The ENABLE terminal when Low puts the device in a low current consumption, power-down mode. When ENABLE is High the device is active.

BRAKE. When the BRAKE input goes Low the output source drivers are disabled and the gates of the sink drivers are pulled high and left floating. This achieves optimum passive braking performance since the sink power DMOS output drivers are ON until the motor has fully completed braking. The braking control circuitry operates off the load supply (V_{BB}) to allow it to remain operational during power loss by using the back-EMF voltage of the motor as it's supply.

LOAD SUPPLY (V$_{BB}$). This terminal is the power supply connection for the power output drivers and braking control circuitry. This terminal should be decoupled with a large-value capacitor to absorb load currents dumped back into the supply during the de-energization of motor windings. These currents can cause the supply voltage to exceed the maximum voltage rating of the device if not properly decoupled. The intrinsic ground clamp and flyback diodes will rectify the motor's back-EMF voltage during power loss.   In applications were use of the motor's back-EMF voltage is desired a series diode should be used to isolate this terminal from the logic supply (V_{CC}). This is to avoid dumping the charge back into the supply and therefor clamping the voltage available from rectification of the motor's back-EMF voltage.

LOGIC SUPPLY (V$_{CC}$). This is the 12 volt supply terminal for the A8925CEB and powers all circuitry except the power outputs and brake control circuitry.

LOGIC GROUND. This must be connected to the power ground terminals in systems that do not use separate power and logic grounds.

POWER GROUND. Terminals 7 through 17 and 29 through 39 are webbed together and attach to the die mounting area to form a low thermal resistance path to allow heat to be conducted out of the device. The power dissipation of the package can be further enhanced by soldering these terminals to a large area of copper foil on the printed wiring board.

DIMENSIONS IN INCHES
(for reference only)

28   18

29

0.032
0.026

17

0.319
0.291

0.021
0.013

0.695
0.685

0.656
0.650

INDEX AREA

0.319
0.291

0.050
BSC

39

7

40   44 1 2   6

0.020
MIN

0.180
0.165

0.656
0.650

0.695
0.685

Dwg. MA-005-44A in

DIMENSIONS IN MILLIMETERS
(controlling dimensions)

28   18

29

0.812
0.661

17

8.10
7.39

0.533
0.331

17.65
17.40

16.662
16.510

INDEX AREA

8.10
7.39

1.27
BSC

39

7

40   44 1 2   6

0.51
MIN

4.57
4.20

16.662
16.510

17.65
17.40

Dwg. MA-005-44A mm

NOTES: 1. Webbed lead frame. Leads 7 through 17 and 29 through 39 are internally one piece.
2. Exact body and lead configuration at vendor's option within limits shown.
3. Lead spacing tolerance is non-cumulative.