FAIRCHILD

SEMICONDUCTOR ™

May 2002
Revised May 2002

74LVXZ161284
Low Voltage IEEE 161284 Translating Transceiver with Power-Up Protection

General Description

The LVXZ161284 contains eight bidirectional data buffers and eleven control/status buffers to implement a full IEEE 1284 compliant interface. The device supports the IEEE 1284 standard and is intended to be used in an Extended Capabilities Port mode (ECP). The pinout allows for easy connection from the Peripheral (A-side) to the Host (cable side).

Outputs on the cable side can be configured to be either open drain or high drive ($\pm$ 14 mA) and are connected to a separate power supply pin ($V_{CC\text{-}Cable}$) that allows these outputs to be driven by a higher supply voltage than the A-side. The pull-up and pull-down series termination resistance of these outputs on the cable side is optimized to drive an external cable. In addition, the C inputs and the B and Y outputs on the cable side contain internal pull-up resistors connected to the $V_{CC\text{-}Cable}$ supply to provide proper input termination and pull-ups for open drain output mode.

Outputs on the Peripheral side are standard low-drive CMOS outputs designed to interface with 3V logic. The DIR input controls data flow on the A_1–A_8/B_1–B_8 transceiver pins.

This device also has an added power-up protection feature which forces the Y outputs (Y_9 - Y_{13}) to a high state after power-on until one of the associated inputs (A_9 - A_{13}) goes HIGH. When an associated input (A_9 - A_{13}) goes HIGH, all Y outputs (Y_9 - Y_{13}) are activated.

Features

■ Supports IEEE 1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals

■ Translation capability allows outputs on the cable side to interface with 5V signals

■ All inputs have hysteresis to provide noise margin

■ B and Y output resistance optimized to drive external cable

■ B and Y outputs in high impedance mode during power down

■ C inputs and B, Y outputs on cable side have internal 1.4 kΩ pull-up resistors

■ Flow-through pin configuration allows easy interface between the "Peripheral and Host"

■ Replaces the function of two (2) 74ACT1284 devices

■ Power-up protection prevents errors when the printer is powered on but no valid signal is at the input pins (A_9 - A_{13}).

Ordering Code

Order Number	Package Number	Package Description
74LVXZ161284MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [RAIL]
74LVXZ161284MEX	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide [TAPE and REEL]
74LVXZ161284MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [RAIL]
74LVXZ161284MTX	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

www.fairchildsemi.com

Logic Symbol
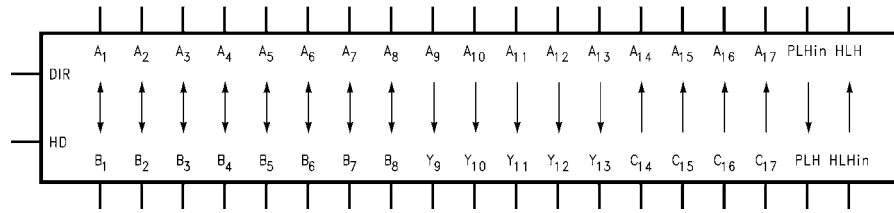
Connection Diagram
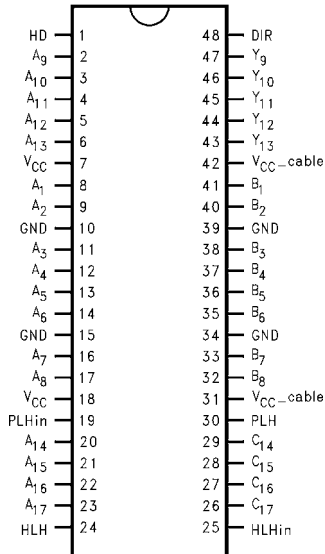
Pin Descriptions

Pin Names	Description
HD	High Drive Enable Input (Active HIGH)
DIR	Direction Control Input
A_1–A_8	Inputs or Outputs
B_1–B_8	Inputs or Outputs
A_9–A_{13}	Inputs
Y_9–Y_{13}	Outputs
A_{14}–A_{17}	Outputs
C_{14}–C_{17}	Inputs
PLH_{IN}	Peripheral Logic HIGH Input
PLH	Peripheral Logic HIGH Output
HLH_{IN}	Host Logic HIGH Input
HLH	Host Logic HIGH Output

Truth Table

| Inputs		Outputs
DIR	HD	
L	L	B_1–B_8 Data to A_1–A_8, and
		A_9–A_{13} Data to Y_9–Y_{13} (Note 1)
		C_{14}–C_{17} Data to A_{14}–A_{17}
		PLH Open Drain Mode
L	H	B_1–B_8 Data to A_1–A_8, and
		A_9–A_{13} Data to Y_9–Y_{13}
		C_{14}–C_{17} Data to A_{14}–A_{17}
H	L	A_1–A_8 Data to B_1–B_8 (Note 2)
		A_9–A_{13} Data to Y_9–Y_{13} (Note 1)
		C_{14}–C_{17} Data to A_{14}–A_{17}
		PLH Open Drain Mode
H	H	A_1–A_8 Data to B_1–B_8
		A_9–A_{13} Data to Y_9–Y_{13}
		C_{14}–C_{17} Data to A_{14}–A_{17}

Note 1: Y_9–Y_{13} Open Drain Outputs with 1.4 kΩ pullups

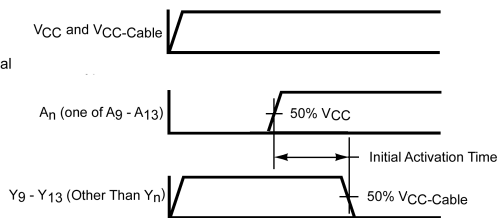**Note 2:** B_1–B_8 Open Drain Outputs with 1.4 kΩ pullups

Logic Diagrams
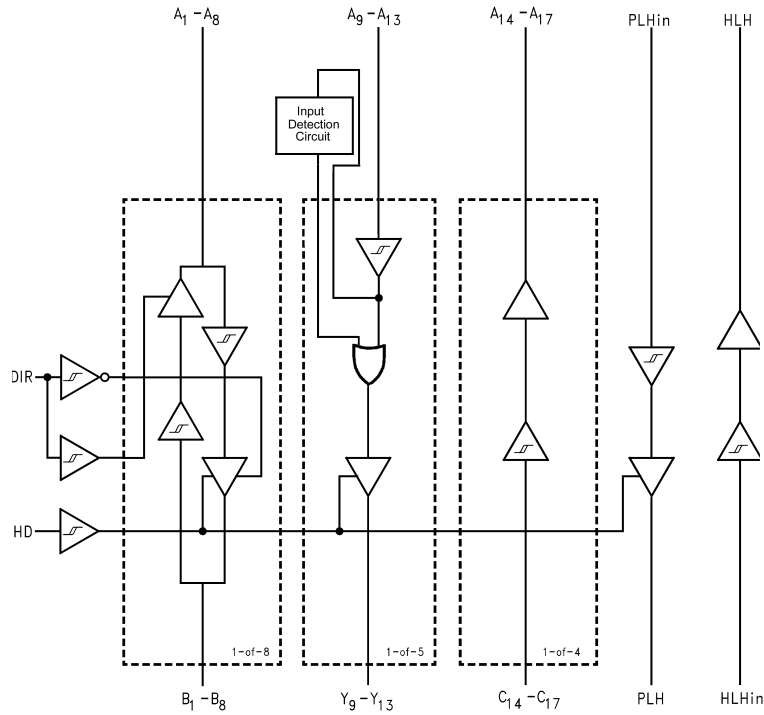
Input Detection Circuit
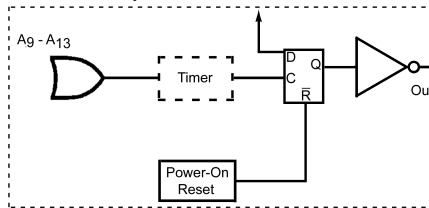
V_{CC} = 3.3V
V_{CC}-Cable = 5V
T_A = 25° C
Initial Activation Time = 140ns typical

A_n (One of A_9 - A_{13}) is Switched as Shown Above and
Other Four Inputs are Forced at Low State

FIGURE 1. Input Detection Circuit Timing

Absolute Maximum Ratings(Note 3)

Supply Voltage

  V_{CC} −0.5V to +4.6V

  $V_{CC-Cable}$ −0.5V to +7.0V

  $V_{CC-Cable}$ Must Be ≥ V_{CC}

Input Voltage (V_I)—(Note 4)

  A_1–A_{13}, PLH$_{IN}$, DIR, HD   −0.5V to V_{CC} + 0.5V

  B_1–B_8, C_{14}–C_{17}, HLH$_{IN}$ −0.5V to +5.5V (DC)

  B_1–B_8, C_{14}–C_{17}, HLH$_{IN}$ −2.0V to +7.0V*

                                      *40 ns Transient

Output Voltage (V_O)

  A_1–A_8, A_{14}–A_{17}, HLH   −0.5V to V_{CC} +0.5V

  B_1–B_8, Y_9–Y_{13}, PLH   −0.5V to +5.5V (DC)

  B_1–B_8, Y_9–Y_{13}, PLH   −2.0V to +7.0V*

                                      *40 ns Transient

DC Output Current (I_O)

  A_1–A_8, HLH   ±25 mA

  B_1–B_8, Y_9–Y_{13} ±50 mA

  PLH (Output LOW)   84 mA

  PLH (Output HIGH)   −50 mA

Input Diode Current (I_{IK})—(Note 4)

  DIR, HD, A_9–A_{13}, PLH, HLH, C_{14}–C_{17} −20 mA

Output Diode Current (I_{OK})

  A_1–A_8, A_{14}–A_{17}, HLH   ±50 mA

  B_1–B_8, Y_9–Y_{13}, PLH   −50 mA

DC Continuous V_{CC} or Ground

  Current   ±200 mA

Storage Temperature   −65°C to +150°C

ESD

  Human Body Model   4000V

  Machine Model   200V

  Charged Device Model   2000V

Recommended Operating Conditions

Supply Voltage

  V_{CC} 3.0V to 3.6V

  $V_{CC-Cable}$ 3.0V to 5.5V

DC Input Voltage (V_I)   0V to V_{CC}

Open Drain Voltage (V_O)   0V to 5.5V

Operating Temperature (T_A)   −40°C to +85°C

Note 3: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Fairchild does not recommend operation outside the databook specifications.

Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		V_{CC} (V)	$V_{CC-Cable}$ (V)	$T_A = 0°C$ to +70°C	$T_A = −40°C$ to +85°C	Units	Conditions
					Guaranteed Limits			
V_{IK}	Input Clamp Diode Voltage		3.0	3.0	−1.2	−1.2	V	$I_i = −18$ mA
V_{IH}	Minimum HIGH Level Input Voltage	A_n, B_n, PLH$_{IN}$, DIR, HD	3.0–3.6	3.0–5.5	2.0	2.0	V	
		C_n	3.0–3.6	3.0–5.5	2.3	2.3		
		HLH$_{IN}$	3.0–3.6	3.0–5.5	2.6	2.6		
V_{IL}	Maximum LOW Level Input Voltage	A_n, B_n, PLH$_{IN}$, DIR, HD	3.0–3.6	3.0–5.5	0.8	0.8	V	
		C_n	3.0–3.6	3.0–5.5	0.8	0.8		
		HLH$_{IN}$	3.0–3.6	3.0–5.5	1.6	1.6		
ΔV_T	Minimum Input Hysteresis	A_n, B_n, PLH$_{IN}$, DIR, HD	3.3	5.0	0.4	0.4	V	$V_T^+ - V_T^-$
		C_n	3.3	5.0	0.8	0.8		$V_T^+ - V_T^-$
		HLH$_{IN}$	3.3	5.0	0.2	0.2		$V_T^+ - V_T^-$
V_{OH}	Minimum HIGH Level Output Voltage	A_n, HLH	3.0	3.0	2.8	2.8	V	$I_{OH} = −50$ μA
			3.0	3.0	2.4	2.4		$I_{OH} = −4$ mA
		B_n, Y_n	3.0	3.0	2.0	2.0		$I_{OH} = −14$ mA
		B_n, Y_n	3.0	4.5	2.23	2.23		$I_{OH} = −14$ mA
		PLH	3.15	3.15	3.1	3.1		$I_{OH} = −500$ μA

DC Electrical Characteristics (Continued)

Symbol	Parameter		V_{CC} (V)	$V_{CC-Cable}$ (V)	$T_A = 0°C$ to +70°C	$T_A = -40°C$ to +85°C	Units	Conditions
					Guaranteed Limits			
V_{OL}	Maximum LOW Level Output Voltage	A_n, HLH	3.0	3.0	0.2	0.2	V	$I_{OL} = 50\ \mu A$
			3.0	3.0	0.4	0.4		$I_{OL} = 4\ mA$
		B_n, Y_n	3.0	3.0	0.8	0.8		$I_{OL} = 14\ mA$
		B_n, Y_n	3.0	4.5	0.77	0.77		$I_{OL} = 14\ mA$
		PLH	3.0	3.0	0.85	0.95		$I_{OL} = 84\ mA$
		PLH	3.0	4.5	0.8	0.9		$I_{OL} = 84\ mA$
R_D	Maximum Output Impedance	B_1 - B_8, Y_9 - Y_{13}	3.3	3.3	60	60	Ω	(Note 5)(Note 7)
			3.3	5.0	55	55		
	Minimum Output Impedance	B_1 - B_8, Y_9 - Y_{13}	3.3	3.3	30	30		(Note 5)(Note 7)
			3.3	5.0	35	35		
R_P	Maximum Pull-Up Resistance	B_1 - B_8, Y_9 - Y_{13}, C_{14} - C_{17}	3.3	3.3	1650	1650	Ω	
			3.3	5.0	1650	1650		
	Minimum Pull-Up Resistance	B_1 - B_8, Y_9 - Y_{13}, C_{14} - C_{17}	3.3	3.3	1150	1150	Ω	
			3.3	5.0	1150	1150		
I_{IH}	Maximum Input Current in HIGH State	A_9 - A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	3.6	3.6	1.0	1.0	μA	$V_I = 3.6V$
		C_{14} - C_{17}	3.6	3.6	50.0	50.0		$V_I = 3.6V$
		C_{14} - C_{17}	3.6	5.5	100	100		$V_I = 5.5V$
I_{IL}	Maximum Input Current in LOW State	A_9 - A_{13}, PLH_{IN}, HD, DIR, HLH_{IN}	3.6	3.6	−1.0	−1.0	μA	$V_I = 0.0V$
		C_{14} - C_{17}	3.6	3.6	−3.5	−3.5	mA	$V_I = 0.0V$
		C_{14} - C_{17}	3.6	5.5	−5.0	−5.0		
I_{OZH}	Maximum Output Disable Current (HIGH)	A_1 - A_8	3.6	3.6	20	20	μA	$V_O = 3.6V$
		B_1 - B_8	3.6	3.6	50	50		$V_O = 3.6V$
		B_1 - B_8	3.6	5.5	100	100		$V_O = 5.5V$
I_{OZL}	Maximum Output Disable Current (LOW)	A_1 - A_8	3.6	3.6	−20	−20	μA	$V_O = 0.0V$
		B_1 - B_8	3.6	3.6	−3.5	−3.5	mA	
		B_1 - B_8	3.6	5.5	−5.0	−5.0		
I_{OZPU}	Maximum Power-Up Disable Current	Y_9 - Y_{13}	0 to 1.5	0 to 1.5	350	350	μA	$V_O = 5.5V$
		B_1 - B_8	(Note 8)	(Note 8)	−5	−5	mA	$V_O = 0.0V$
I_{OZPD}	Maximum Power-Down Disable Current	Y_9 - Y_{13}	0 to 1.5	0 to 1.5	350	350	μA	$V_O = 5.5V$
		B_1 - B_8	(Note 8)	(Note 8)	−5	−5	mA	$V_O = 0.0V$
I_{OFF}	Power Down Output Leakage	B_1 - B_8, Y_9 - Y_{13}, PLH	0.0	0.0	100	100	μA	$V_O = 5.5V$
I_{OFF}	Power Down Input Leakage	C_{14}–C_{17}, HLH_{IN}	0.0	0.0	100	100	μA	$V_I = 5.5V$
$I_{OFF-ICC}$	Power Down Leakage to V_{CC}		0.0	0.0	250	250	μA	(Note 6)
$I_{OFF-ICC2}$	Power Down Leakage to $V_{CC-Cable}$		0.0	0.0	250	250	μA	(Note 6)
I_{CC}	Maximum Supply Current		3.6	3.6	45	45	mA	$V_I = V_{CC}$ or GND
			3.6	5.5	70	70	mA	$V_I = V_{CC}$ or GND

Note 5: Output impedance is measured with the output active LOW and active HIGH (HD = HIGH).

Note 6: Power-down leakage to V_{CC} or $V_{CC-Cable}$ is tested by simultaneously forcing all pins on the cable-side (B_1–B_8, Y_9–Y_{13}, PLH, C_{14}–C_{17} and HLH_{IN}) to 5.5V and measuring the resulting I_{CC} or $I_{CC-Cable}$.

Note 7: This parameter is guaranteed but not tested, characterized only.

Note 8: Connect all V_{CC} pins and $V_{CC-Cable}$ pins when forcing voltage applied, DIR = HD = 0V.

AC Electrical Characteristics

Symbol	Parameter	$T_A = 0°C$ to $+70°C$ $V_{CC} = 3.0V–3.6V$ $V_{CC—Cable} = 3.0V–5.5V$		$T_A = -40°C$ to $+85°C$ $V_{CC} = 3.0V–3.6V$ $V_{CC—Cable} = 3.0V–5.5V$		Units	Figure Number
		Min	Max	Min	Max		
t_{PHL}	$A_1–A_8$ to $B_1–B_8$	2.0	40.0	2.0	44.0	ns	Figure 2
t_{PLH}	$A_1–A_8$ to $B_1–B_8$	2.0	40.0	2.0	44.0	ns	Figure 3
t_{PHL}	$B_1–B_8$ to $A_1–A_8$	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PLH}	$B_1–B_8$ to $A_1–A_8$	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PHL}	$A_9–A_{13}$ to $Y_9–Y_{13}$	2.0	40.0	2.0	44.0	ns	Figure 2
t_{PLH}	$A_9–A_{13}$ to $Y_9–Y_{13}$	2.0	40.0	2.0	44.0	ns	Figure 3
t_{PHL}	$C_{14}–C_{17}$ to $A_{14}–A_{17}$	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PLH}	$C_{14}–C_{17}$ to $A_{14}–A_{17}$	2.0	40.0	2.0	44.0	ns	Figure 4
t_{SKEW}	LH-LH or HL-HL		10.0		12.0	ns	(Note 10)
t_{PHL}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	Figure 2
t_{PLH}	PLH_{IN} to PLH	2.0	40.0	2.0	44.0	ns	Figure 3
t_{PHL}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PLH}	HLH_{IN} to HLH	2.0	40.0	2.0	44.0	ns	Figure 4
t_{PHZ}	Output Disable Time	2.0	15.0	2.0	18.0	ns	Figure 8
t_{PLZ}	DIR to $A_1–A_8$	2.0	15.0	2.0	18.0		
t_{PZH}	Output Enable Time	2.0	50.0	2.0	50.0	ns	Figure 9
t_{PZL}	DIR to $A_1–A_8$	2.0	50.0	2.0	50.0		
t_{PHZ}	Output Disable Time	2.0	50.0	2.0	50.0	ns	Figure 10
t_{PLZ}	DIR to $B_1–B_8$	2.0	50.0	2.0	50.0		
t_{pEN}	Output Enable Time	2.0	25.0	2.0	28.0	ns	Figure 3
	HD to $B_1–B_8$, $Y_9–Y_{13}$	2.0	25.0	2.0	28.0		
t_{pDIS}	Output Disable Time	2.0	25.0	2.0	28.0	ns	Figure 3
	HD to $B_1–B_8$, $Y_9–Y_{13}$	2.0	25.0	2.0	28.0		
$t_{pEN}–t_{pDIS}$	Output Enable-Output Disable		10.0		12.0	ns	
t_{SLEW}	Output Slew Rate					V/ns	
t_{PLH}	$B_1–B_8$, $Y_9–Y_{13}$	0.05	0.40	0.05	0.40		Figure 6
t_{PHL}		0.05	0.40	0.05	0.40		Figure 5
t_r, t_f	t_{RISE} and t_{FALL}		120		120	ns	Figure 7
	$B_1–B_8$ (Note 9),		120		120		(Note 11)
	$Y_9–Y_{13}$ (Note 9)						

Note 9: Open Drain

Note 10: t_{SKEW} is measured for common edge output transitions and compares the measured propagation delay for a given path type:

(i) $A_1–A_8$ to $B_1–B_8$, $A_9–A_{13}$ to $Y_9–Y_{13}$

(ii) $B_1–B_8$ to $A_1–A_8$

(iii) $C_{14}–C_{17}$ to $A_{14}–A_{17}$

Note 11: This parameter is guaranteed but not tested, characterized only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	3	pF	$V_{CC} = 0.0V$ (HD, DIR, $A_9–A_{13}$, $C_{14}–C_{17}$, PLH_{IN} and HLH_{IN})
$C_{I/O}$ (Note 12)	I/O Pin Capacitance	5	pF	$V_{CC} = 3.3V$

Note 12: $C_{I/O}$ is measured at frequency = 1 MHz, per MIL-STD-883B, Method 3012

AC Loading and Waveforms

Pulse Generator for all pulses: Rate ≤ 1.0 MHz; $Z_O \leq 50\Omega$; $t_f \leq 2.5$ ns, $t_r \leq 2.5$ ns.
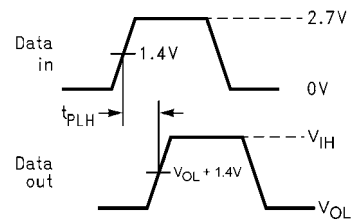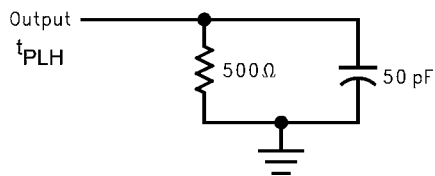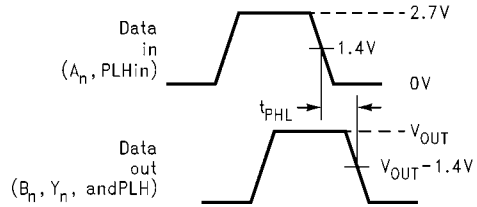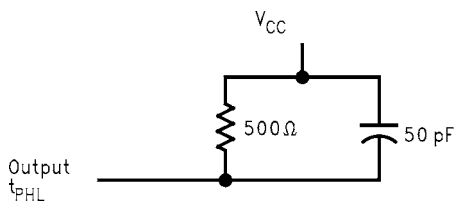

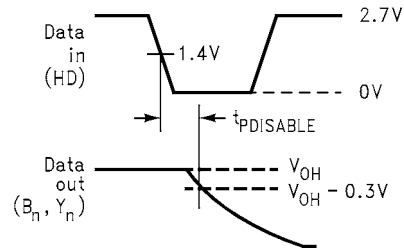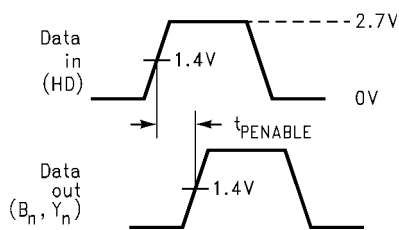**FIGURE 2. Port A to B and A to Y Propagation Delay Waveforms**

FIGURE 3. Port A to B and A to Y Output Waveforms
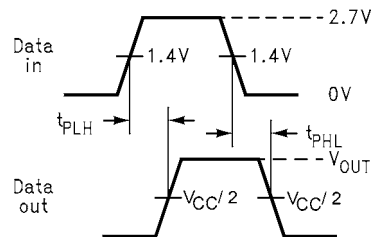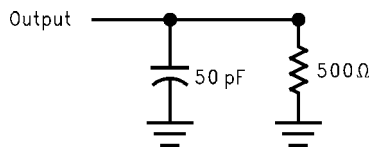

FIGURE 4. Port B to A, C to A and HLHin to HLH Propagation Delay Waveforms

74LVXZ161284

AC Loading and Waveforms (Continued)

FIGURE 5. Port A to B and A to Y HL Slew Test Load and Waveforms
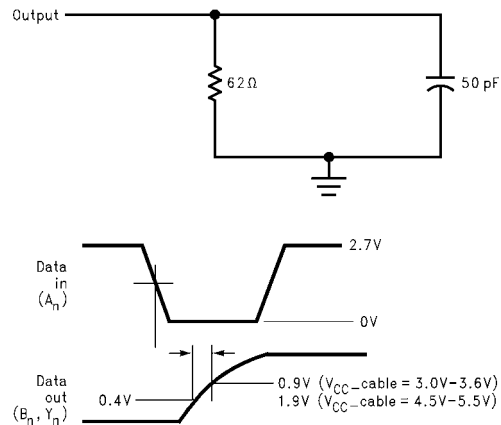
FIGURE 6. Port A to B and A to Y LH Slew Test Load and Waveforms

AC Loading and Waveforms (Continued)
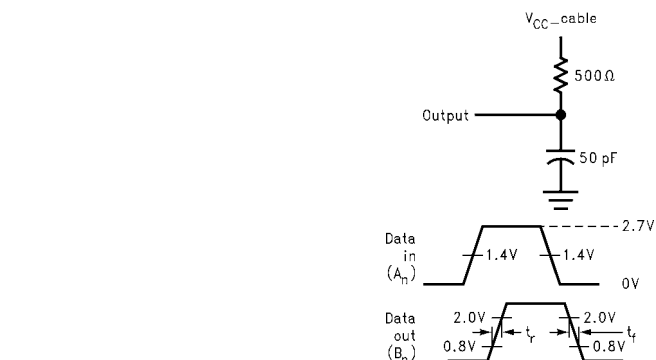
t_r = Output Rise Time, Open Drain

t_f = Output Fall Time, Open Drain

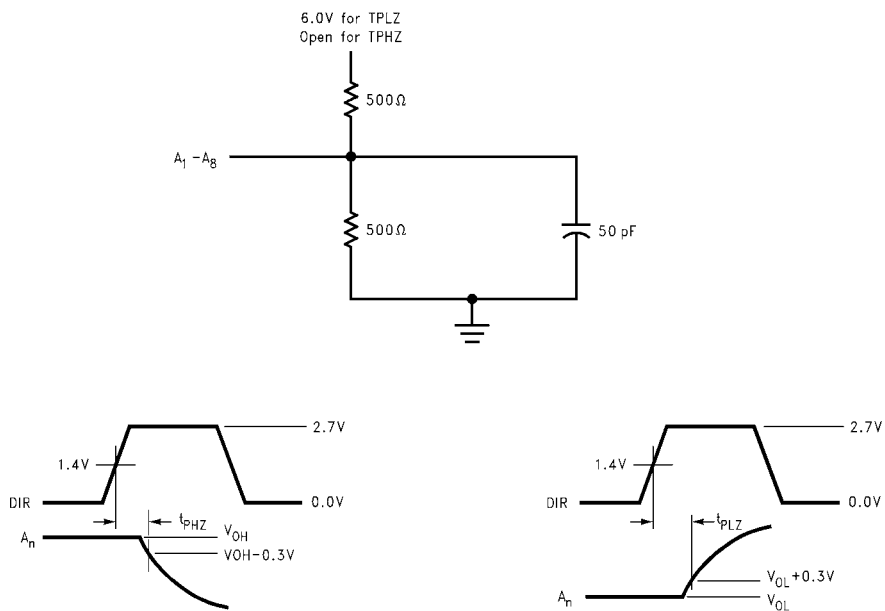**FIGURE 7. Ports A to B and A to Y Rise and Fall Test Load and Waveforms for Open Drain Outputs**

FIGURE 8. t_{PHZ} and t_{PLZ} Test Load and Waveforms, DIR to A_1–A_8
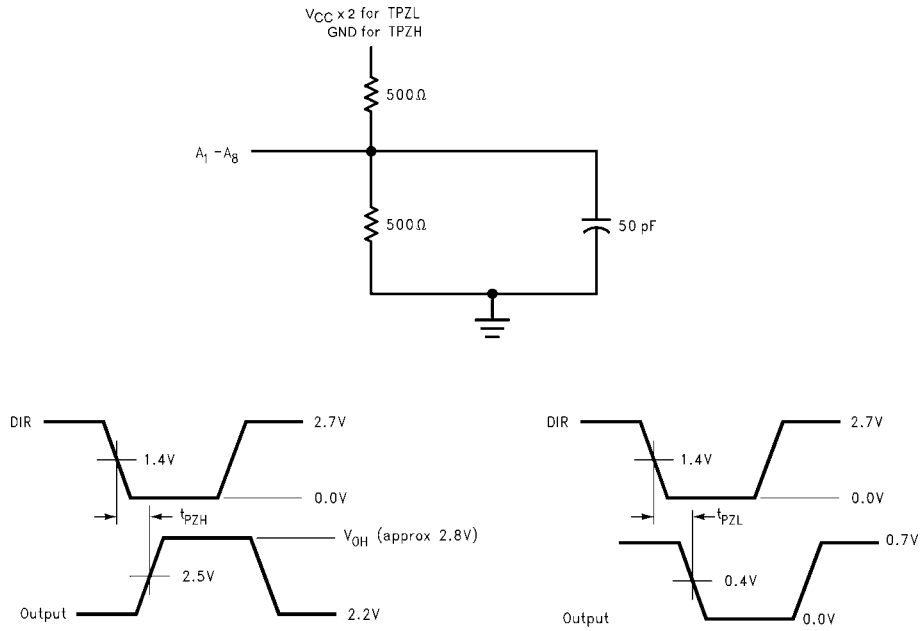
AC Loading and Waveforms (Continued)

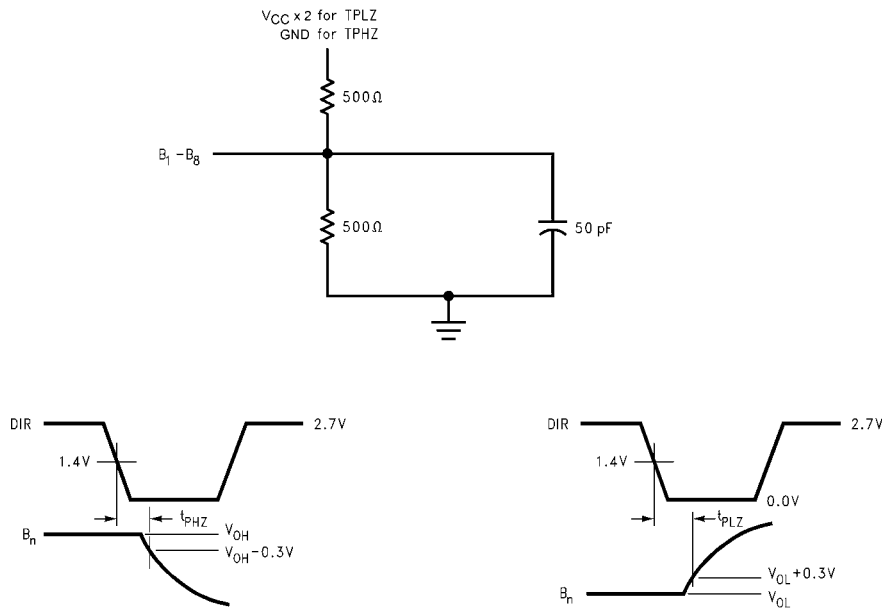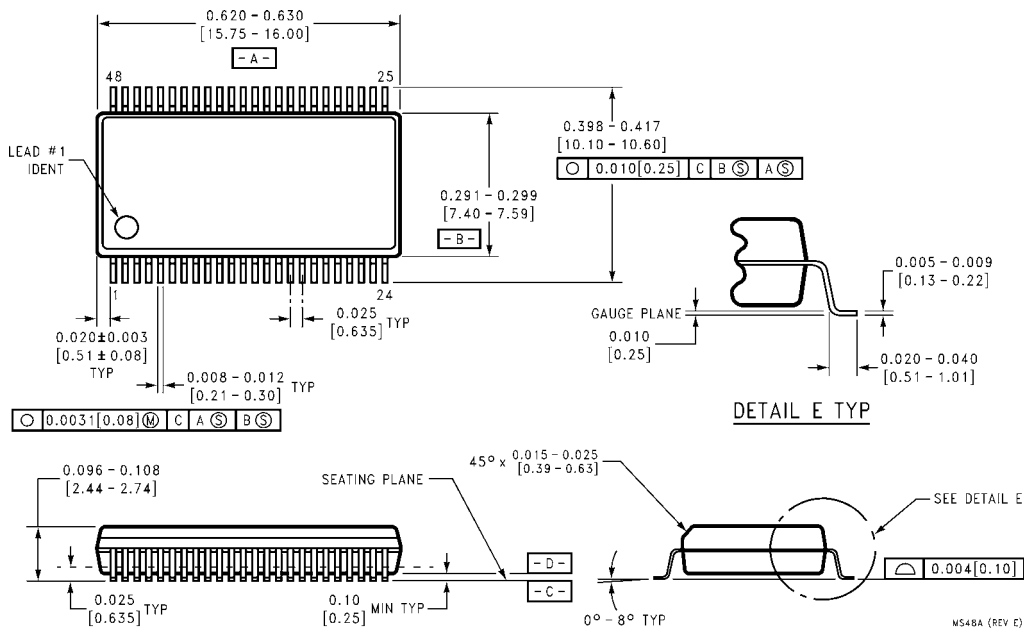FIGURE 9. t_{PZH} and t_{PZL} Test Load and Waveforms, DIR to A_1–A_8

FIGURE 10. t_{PHZ} and t_{PLZ} Test Load and Waveforms
DIR to B_1–B_8

Physical Dimensions inches (millimeters) unless otherwise noted

0.620 − 0.630
[15.75 − 16.00]
− A −

48   25

LEAD #1
IDENT

0.398 − 0.417
[10.10 − 10.60]

⌀ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 − 0.299
[7.40 − 7.59]
− B −

1   24

0.020±0.003
[0.51 ± 0.08]
TYP

0.025
[0.635] TYP

0.008 − 0.012
[0.21 − 0.30] TYP

⌀ 0.0031[0.08]Ⓜ C A Ⓢ B Ⓢ

0.005 − 0.009
[0.13 − 0.22]

GAUGE PLANE

0.010
[0.25]

0.020 − 0.040
[0.51 − 1.01]

DETAIL E TYP

0.096 − 0.108
[2.44 − 2.74]

SEATING PLANE

45° x 0.015 − 0.025
[0.39 − 0.63]

SEE DETAIL E

− D −
− C −

0.025
[0.635] TYP

0.10
[0.25] MIN TYP

0° − 8° TYP

△ 0.004[0.10]

MS48A (REV E)

48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.50±0.10
-A-

0.40 TYP

48   43   30   25

8.10

4.05

6.10±0.10
-B-

PIN #1 IDENT.

1   6   19   24

⌓ 0.2 C B A
ALL LEAD TIPS

48   43   30   25

4.60   9.20

2.30

1   6   19   24

0.30

0.50

LAND PATTERN RECOMMENDATION

⌓ 0.1 C
ALL LEAD TIPS

1.2 MAX

-C-

0.50   0.17-0.27

⊕ 0.13 Ⓜ A BⓈ CⓈ

$0.90^{+0.15}_{-0.10}$

0.10±0.05

SEE DETAIL A

0.09-0.20

DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB,
   REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND
   TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

12.00° TOP & BOTTOM

R0.16

R0.31

GAGE PLANE

1.25

0°-8°

SEATING PLANE

0.60±0.10

1.00

DETAIL A

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.