



## Wireless Components

2 Band TV Tuner Mixer-Oscillator-PLL with balanced IF-Amplifier  
TUA6020 Version 1.2

Specification April 2000

preliminary

<b>Revision History: Current Version: 04.00</b>		
Previous Version: Target Data Sheet		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
5-8, 5-9	5-8, 5-9	oscillator phase noise data
all	all	status: target to preliminary
5-27		Input impedance of VHF mixer
5-29		Output impedance of IF output

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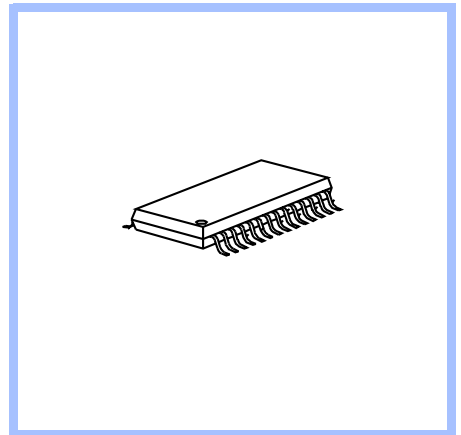
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## Product Info

**General Description** The **TUA6020** is a 5 V mixer/oscillator and synthesizer for analog and digital TV and VCR tuners.

### Package



### Features **General**

- Suitable for analog and digital terrestrial TV tuner
- Full ESD protection

### Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

### IF-Amplifier

- balanced SAW preamplifier
- Low output impedance

### PLL

- PLL with short lock-in time
- High voltage VCO tuning output

- Fast I<sup>2</sup>C bus
- 3 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch
- Lock-in flag
- Power-down reset
- Programmable reference divider ratios: 24, 64, 80, 128
- Programmable charge pump current

**Application** ■ The IC is suitable for PAL tuner in TV- and VCR-sets or set-top receivers for analog TV and **D**igital **V**ideo **B**roadcasting.

### Ordering Information

Type	Ordering Code	Package
TUA6020	Q67037-A1127-A701 (tape and reel)	P-TSSOP-28-1

# 1

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# 2 Product Description

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## 2.1 General Description

The **TUA6020** device combines a digitally programmable phase locked loop (PLL), with a mixer-oscillator block including two balanced mixers and oscillators for use in TV and VCR tuners.

The PLL block with four selectable chip addresses forms a digitally programmable phase locked loop. With a 4 MHz quartz crystal, the PLL permits precise setting of the frequency of the tuner oscillator up to 1024 MHz in increments of 31.25, 50, 62.5 or 166.7 kHz. The tuning process is controlled by a microprocessor via an I<sup>2</sup>C bus. The device has three output ports. A flag is set when the loop is locked. It can be read by the processor via the I<sup>2</sup>C bus.

The mixer-oscillator block includes two balanced mixers (one mixer with high-impedance input and one mixer with a balanced low-impedance input), two frequency and amplitude-stable balanced oscillators for LOW/MID and HIGH, an IF amplifier, a low-noise reference voltage source, and a band switch.

## 2.2 Features

### General

- Suitable for analog and digital terrestrial TV tuner
- Full ESD protection

### Mixer/Oscillator

- High impedance mixer input for LOW/MID band
- Low impedance mixer input for HIGH band
- 4 pin oscillator for LOW/MID band
- 4 pin oscillator for HIGH band

### IF-Amplifier

- balanced SAW preamplifier
- Low output impedance

### PLL

- PLL with short lock-in time
- High voltage VCO tuning output
- Fast I<sup>2</sup>C bus
- 3 NPN bandswitch buffers
- Internal LOW-MID/HIGH switch
- Lock-in flag
- Power-down reset

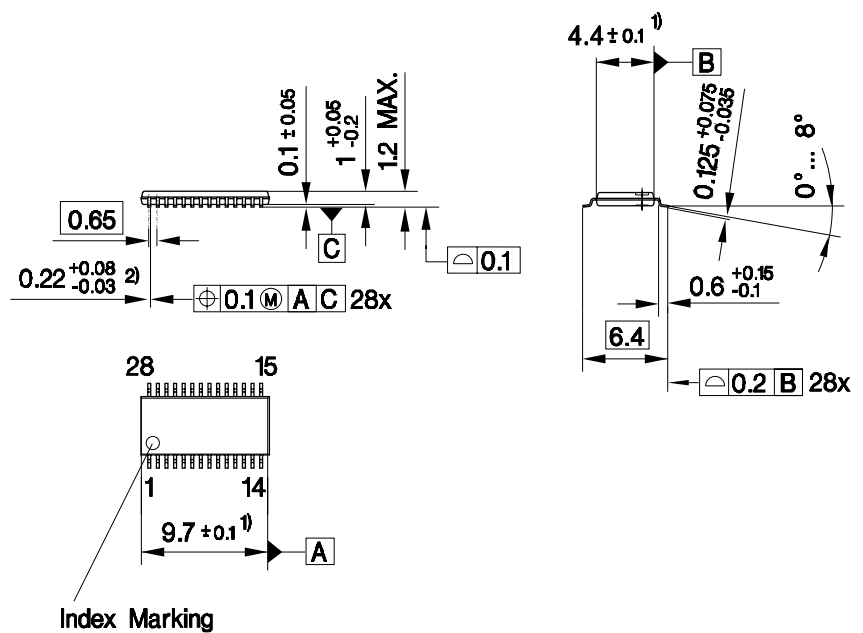
- Programmable reference divider ratios: 24, 64, 80, 128
- Programmable charge pump current

## 2.3 Application

- The IC is suitable for PAL tuners in TV- and VCR-sets or set-top receivers for analog TV and Digital Video Broadcasting.

## 2.4 Package Outlines

P-TSSOP-28-1



Index Marking

- 1) Does not include plastic or metal protrusion of 0.15 max. per side
- 2) Does not include dambar protrusion

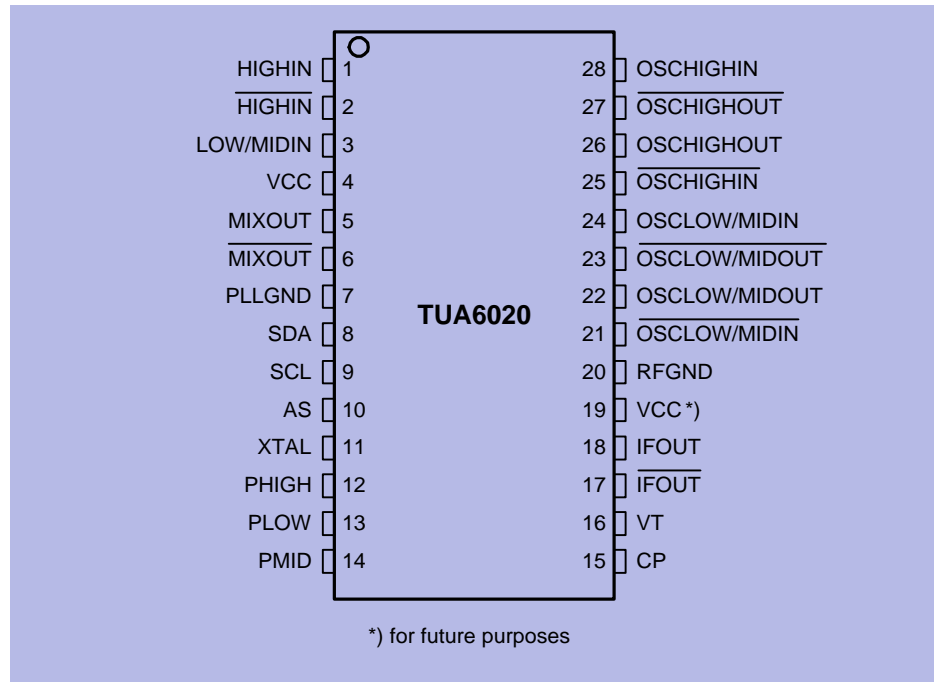


# 3 Functional Description

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### 3.1 Pin Configuration



Pin\_config

Figure 3-1 Pin Configuration

### 3.2 Internal Pin Configuration

Table 3-1 Pin Definition and Function

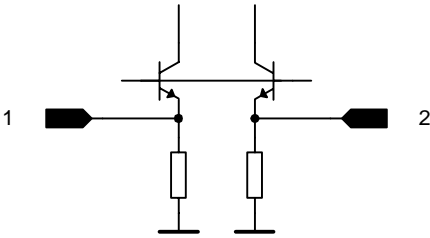
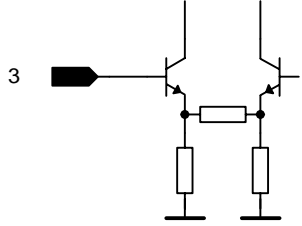
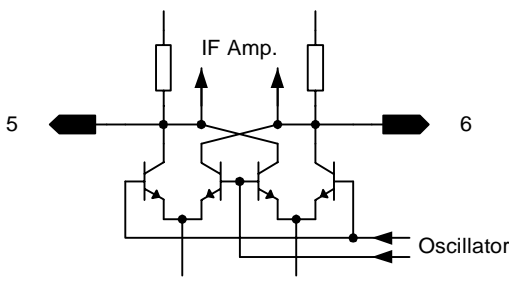
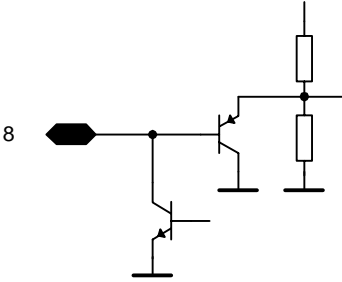
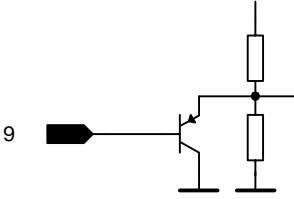
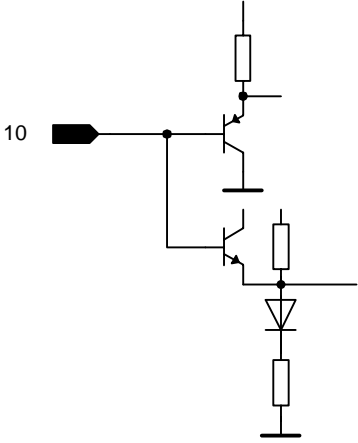
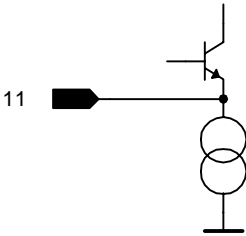
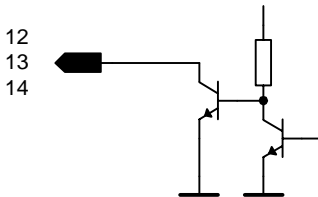
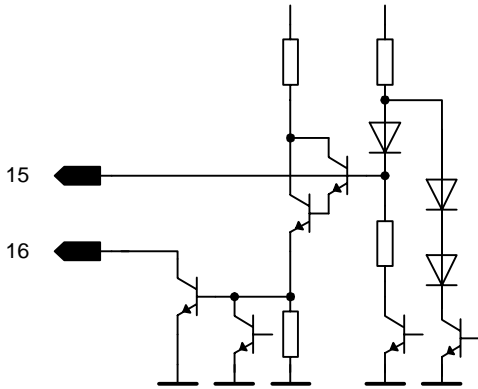
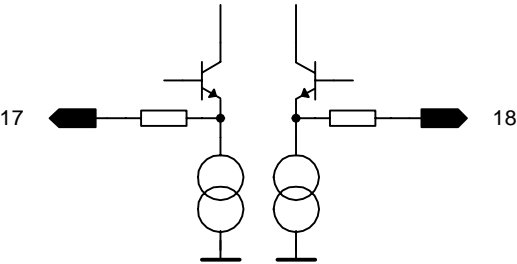
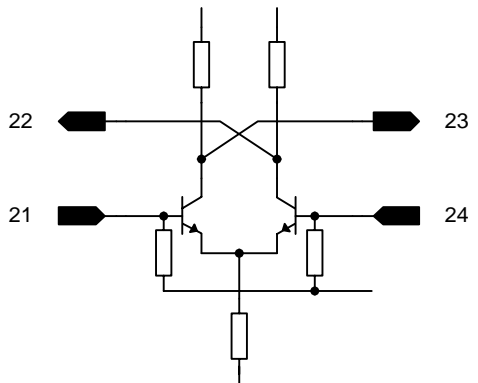
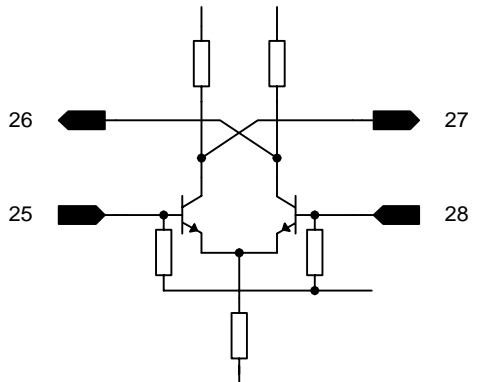
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
1	HIGHIN		0.0 V	0.9 V
2	HIGHIN		0.0 V	0.9 V
3	LOW/MIDIN		1.8 V	0.0 V
4	VCC	supply voltage	5.0 V	5.0 V
5	MIXOUT		3.8 V	3.8 V
6	MIXOUT		3.8 V	3.8 V
7	PLLGND	digital ground	0.0 V	0.0 V

Table 3-1 Pin Definition and Function (continued)				
Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
8	SDA		n.a.	n.a.
9	SCL		n.a.	n.a.
10	AS		$V_{AS}$	$V_{AS}$
11	XTAL		3.0 V	3.0 V

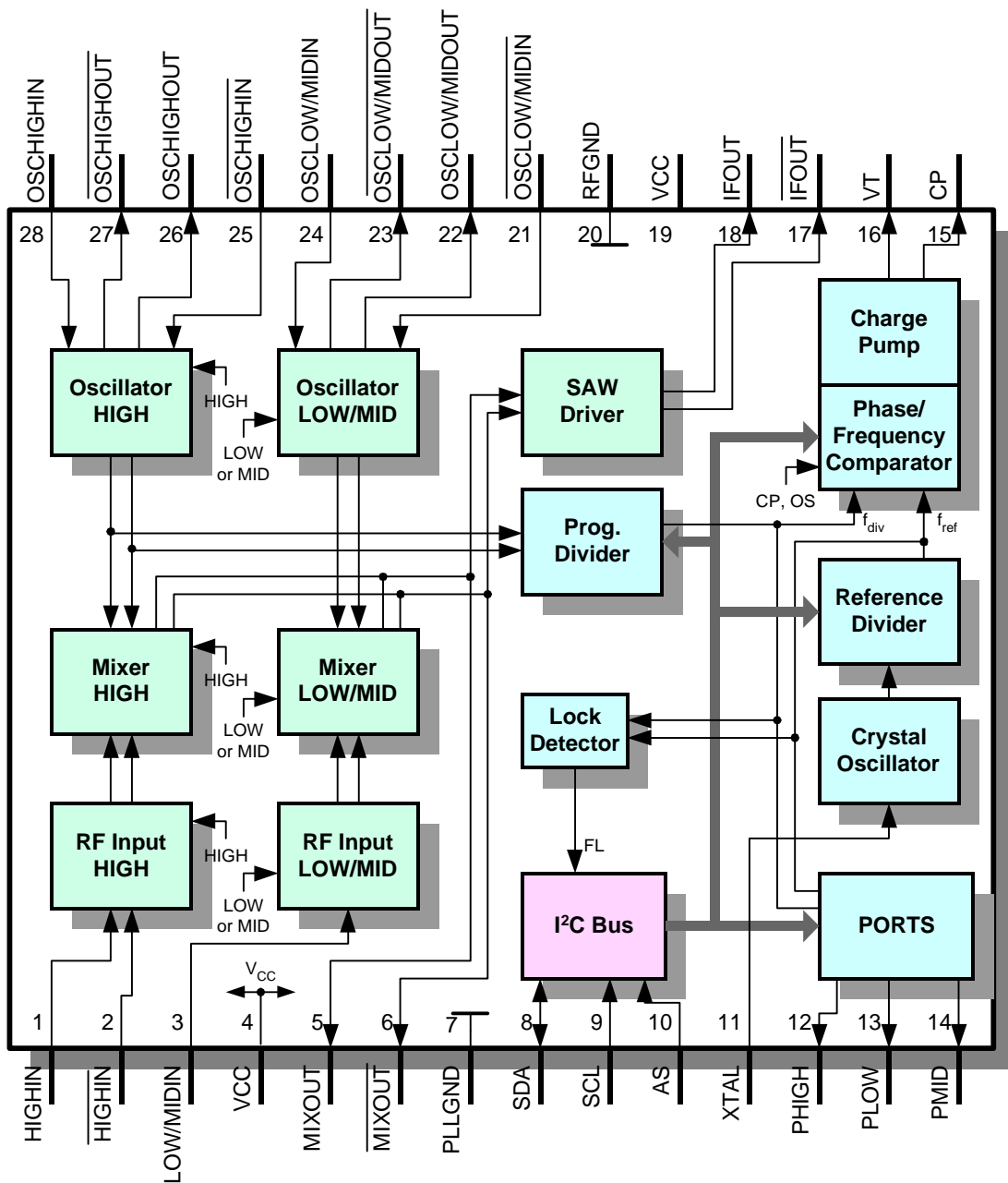
**Table 3-1 Pin Definition and Function (continued)**

Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
12	PHIGH		5 V	$V_{CE}$
13	PLow		5 V or $V_{CE}$	5 V
14	PMID		5 V or $V_{CE}$	5 V
15	CP		1.9 V	1.9 V
16	VT		$V_T$	$V_T$
17	$\overline{\text{IFOUT}}$		2.3 V	2.3 V
18	IFOUT		2.3 V	2.3 V
19	VCC	supply voltage	5.0 V	5.0 V
20	RFGND	analog ground	0.0 V	0.0 V

**Table 3-1 Pin Definition and Function (continued)**

Pin No.	Symbol	Equivalent I/O-Schematic	Average DC voltage	
			LOW/MID	HIGH
21	$\overline{\text{OSCLOW/MIDIN}}$		1.6 V	0.0 V
22	OSCLOW/MIDOUT		2.3 V	0.0 V
23	$\overline{\text{OSCLOW/MIDOUT}}$		2.3 V	0.0 V
24	OSCLOW/MIDIN		1.6 V	0.0 V
25	$\overline{\text{OSCHIGHIN}}$		0.0 V	1.6 V
26	OSCHIGHOUT		0.0 V	2.8 V
27	$\overline{\text{OSCHIGHOUT}}$		0.0 V	2.8 V
28	OSCHIGHIN		0.0 V	1.6 V

### 3.3 Block Diagram



Block\_diag

Figure 3-2 Block Diagram

## 3.4 Circuit Description

### 3.4.1 Mixer-Oscillator block

The mixer oscillator section includes two balanced mixers (double balanced mixer), two balanced oscillators for LOW/MID and HIGH, an IF amplifier, a reference voltage source and a band switch.

Filters between tuner input and IC separate the TV frequency signals into two bands. The band switching in the tuner front-end is done by using two or three port outputs. In the selected band the signal passes a tuner input stage with MOSFET amplifier, a double-tuned bandpass filter and is then fed to the balanced mixer input of the IC which has in case of LOW / MID a high-impedance input and in case of HIGH a low-impedance input. The input signal is mixed there with the signal from the activated on chip oscillator to the IF frequency which is filtered out at the balanced high-impedance output pair by means of a parallel tuned circuit. The following SAW preamplifier has a low output impedance to drive the SAW filter directly.

### 3.4.2 PLL block

The oscillator signal is internally DC-coupled as a differential signal to the programmable divider inputs. The signal subsequently passes through a programmable divider with ratio  $N = 256$  through 32767 and is then compared in a digital frequency / phase detector to a reference frequency  $f_{ref} = 31.25, 50, 62.5$  or  $166.7$  kHz. This frequency is derived from an unbalanced, low-impedance 4 MHz crystal oscillator (pin XTAL) divided by  $R = 128, 80, 64$  or  $24$ .

The phase detector has two outputs that drive two current sources of opposite polarity as charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the positive current source pulses for the duration of the phase difference. In the reverse case the I- current source pulses. If the two signals are in phase, the charge pump output (CP) goes into the high-impedance state (PLL is locked). An active low-pass filter integrates the current pulses to generate the tuning voltage for the VCO (internal amplifier, external pull-up resistor at TUNE and external RC circuitry). The charge pump output is also switched into the high-impedance state if the control bits  $T0 = 1$  and  $T1 = 0$ . Here it should be noted, however, that the tuning voltage can alter over a long period in the high-impedance state as a result of self-discharge in the peripheral circuitry. TUNE may be switched off by the control bit OS to allow external adjustments.

If the VCO is not oscillating the PLL locks to a tuning voltage of 33V ( $V_{TH}$ ).

By means of control bit CP the pump current can be switched between two values by software. This programmability permits alteration of the control response time of the PLL in the locked-in state. In this way different VCO gains can be compensated, for example.



The software-switched ports PLOW, PMID and PHIGH are general-purpose open-collector outputs. The test bits T0 = 0 and T1 = 1, switch the test signals  $f_{ref}$  (i.e.  $f_{XTAL} / 64$ ) and  $f_{div}$  (divided input signal) to PMID and PLOW respectively.

The lock detector resets the lock flag FL if the width of the charge pump current pulses is wider than the period of the crystal oscillator (i.e. 250 ns). Hence, if FL = 1, the maximum deviation of the input frequency from the programmed frequency is given by

$$\Delta f = \pm I_P * (K_{VCO} / f_{XTAL}) * (C1+C2) / (C1*C2)$$

where  $I_P$  is the charge pump current,  $K_{VCO}$  the VCO gain,  $f_{XTAL}$  the crystal oscillator frequency and C1, C2 the capacitances in the loop filter (see [Figure 4-1 Evaluation board, PAL application on page 2](#)). As the charge pump pulses at i.e. 62.5 kHz (=  $f_{ref}$ ), it takes a maximum of 16  $\mu$ s for FL to be reset after the loop has lost lock state.

Once FL has been reset, it is set only if the charge pump pulse width is less than 250 ns for eight consecutive  $f_{ref}$  periods. Therefore it takes between 128 and 144  $\mu$ s for FL to be set after the loop regains lock.

### 3.4.3 I<sup>2</sup>C-Bus Interface

Data is exchanged between the processor and the PLL via the I<sup>2</sup>C bus. The clock is generated by the processor (input SCL), while pin SDA functions as an input or output depending on the direction of the data (open collector, external pull-up resistor). Both inputs have hysteresis and a low-pass characteristic, which enhance the noise immunity of the I<sup>2</sup>C bus.

The data from the processor pass through an I<sup>2</sup>C bus controller. Depending on their function the data are subsequently stored in registers. If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each telegram begins with the start condition and ends with the stop condition. Start condition: SDA goes LOW, while SCL remains HIGH. Stop condition: SDA goes HIGH while SCL remains HIGH. All further information transfer takes place during SCL = LOW, and the data is forwarded to the control logic on the positive clock edge.

The table "Bit Allocation" (see [Table 5-4 Bit Allocation Read / Write on page 10](#)) should be referred to the following description. All telegrams are transmitted byte-by-byte, followed by a ninth clock pulse, during which the control logic returns the SDA line to LOW (acknowledge condition). The first byte is comprised of seven address bits. These are used by the processor to select the PLL from several peripheral components (chip select). The LSB bit (R/W) determines whether data are written into (R/W = 0) or read from (R/W = 1) the PLL.

In the data portion of the telegram during a WRITE operation, the MSB bit of the first or third data byte determines whether a divider ratio or control information is to follow. In each case the second byte of the same data type has to follow the first byte.

If the address byte indicates a READ operation, the PLL generates an acknowledge and then shifts out the status byte onto the SDA line. If the processor generates an acknowledge, a further status byte is output; otherwise the data line is released to allow the processor to generate a stop condition. The status word consists the lock flag and the power-on flag.

Four different chip addresses can be set by appropriate DC level at pin AS (see [Table 5-6 Address selection on page 11](#)).

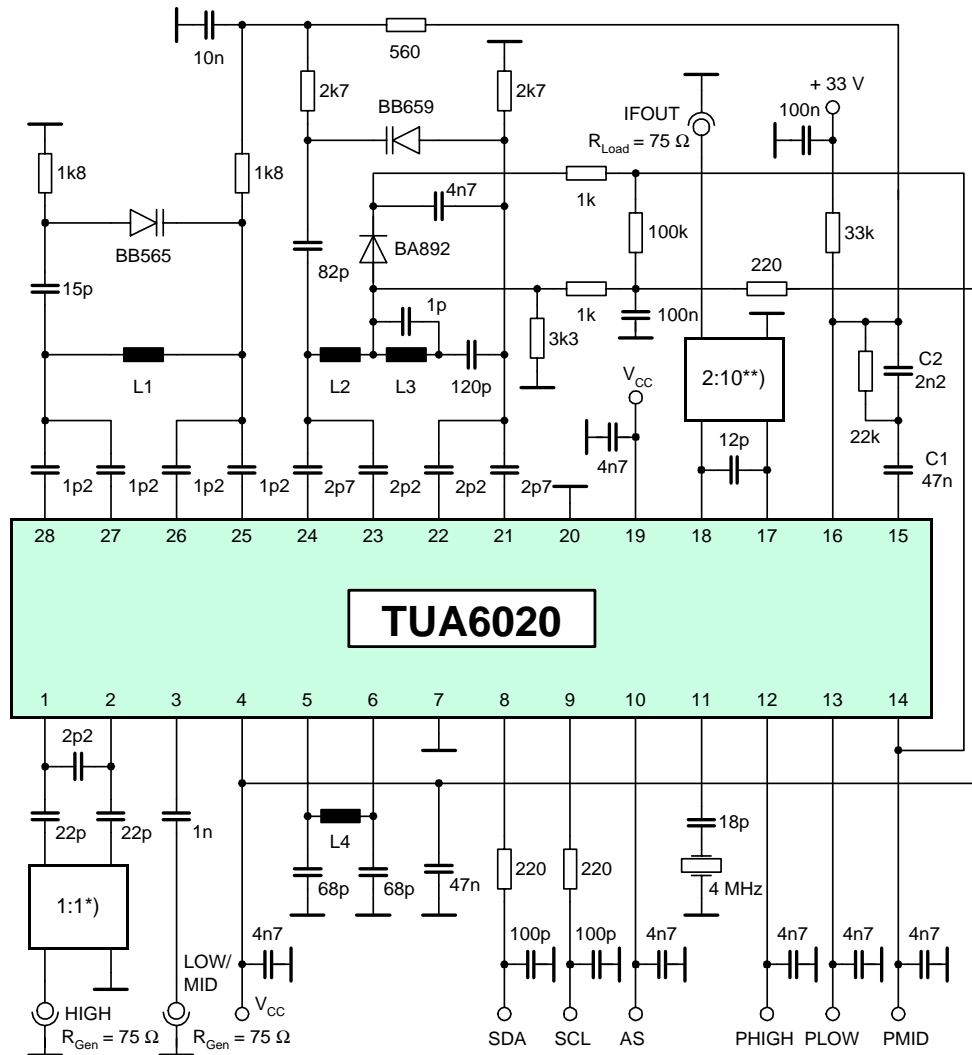
While applying the supply voltage, a power-on reset circuit prevents the PLL from setting the SDA line to LOW, which would block the bus. The power-on reset flag POR is set at power-on and when  $V_{CC}$  falls below 3.2 V. It will be reset at the end of a READ operation.

# 4 Applications

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### 4.1 Evaluation board, PAL application



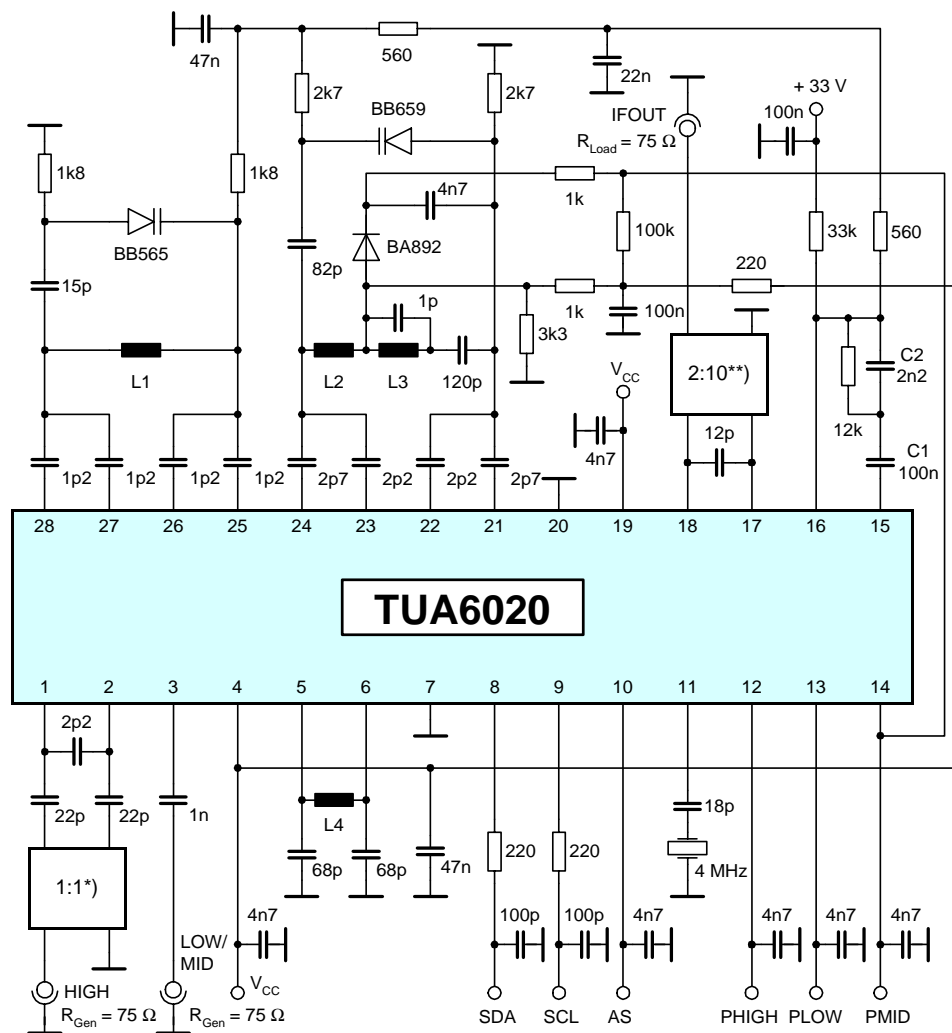
Application Circuit

Figure 4-1 Evaluation board, PAL application

	Table 4-1 Recommended band limits in MHz			
	RF input		Oscillator	
	min	max	min	max
LOW	48.25	140.25	87.15	179.15
MID	147.25	423.25	186.15	462.15
HIGH	431.25	855.25	470.15	894.15

	Table 4-1 Coils		
	turns	Ø	wire Ø
L1	1.5	2.4 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	8.5	3.2 mm	0.5 mm
L4	14.5	4 mm	0.3 mm
*)	TOKO B4F Type 617DB-1023		
**)	TOKO 7KL600 GCS-A1010DX		

## 4.2 Evaluation board, low phase noise application



Application Circuit digital

Figure 4-2 Evaluation board, low phase noise application

	Table 4-1 Recommended band limits in MHz			
	RF input		Oscillator	
	min	max	min	max
LOW	48.25	140.25	87.15	179.15
MID	147.25	423.25	186.15	462.15
HIGH	431.25	855.25	470.15	894.15

	Table 4-1 Coils		
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L1	1.5	2.4 mm	0.5 mm
L2	2.5	3 mm	0.5 mm
L3	8.5	3.2 mm	0.5 mm
L4	14.5	4 mm	0.3 mm
*)	TOKO B4F Type 617DB-1023		
**)	TOKO 7KL600 GCS-A1010DX		

# 5 Reference

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## 5.1 Electrical Data

### 5.1.1 Absolute Maximum Ratings



#### WARNING

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

**Table 5-1 Absolute Maximum Ratings, Ambient temperature  $T_{AMB} = -20^{\circ}\text{C} \dots +85^{\circ}\text{C}$**

Parameter <sup>1)</sup>	Symbol	Limit Values		Unit	Remarks
		min	max		
Supply voltage	$V_{CC}$	-0.3	6	V	
Junction temperature	$T_J$		+150	$^{\circ}\text{C}$	
Storage temperature	$T_{Stg}$	-40	+125	$^{\circ}\text{C}$	
Thermal resistance (junction to ambient)	$R_{thJA}$		120	K/W	
<b>PLL</b>					
CP	$V_{CP}$	-0.3	3	V	
	$I_{CP}$		1	mA	
Crystal oscillator pin XTAL	$V_{XTAL}$		$V_{CC}$	V	
	$I_{XTAL}$	-5		mA	
Bus input/output SDA	$V_{SDA}$	-0.3	$V_{CC}$	V	
Bus output current SDA	$I_{SDA(L)}$		5	mA	open collector
Bus input SCL	$V_{SCL}$	-0.3	$V_{CC}$	V	
Chip address switch AS	$V_{AS}$	-0.3	$V_{CC}$	V	
Tuning voltage output (loop filter)	$V_T$	-0.3	35	V	
Port outputs PLOW, PMID, PHIGH	$V_P$	-0.3	$V_{CC}$	V	
	$I_{P(L)}$	-1	25	mA	$t_{max} = 0.1 \text{ sec. at } 5.5 \text{ V}$
Total port output current	$\Sigma I_{P(L)}$		40	mA	$t_{max} = 0.1 \text{ sec. at } 5.5 \text{ V}$
<b>Mixer-Oscillator</b>					
Mixer inputs LOW/MID	$V_i$	-0.3	3	V	
Mixer inputs HIGH	$V_i$		2	V	
	$I_i$	-5	6	mA	

**Table 5-1 Absolute Maximum Ratings, Ambient temperature  $T_{AMB} = -20^{\circ}\text{C} \dots +85^{\circ}\text{C}$  (continued)**

Parameter <sup>1)</sup>	Symbol	Limit Values		Unit	Remarks
		min	max		
Oscillator base voltage	$V_B$	-0.3	3	V	
Oscillator collector voltage	$V_C$		$V_{CC}$	V	
<b>ESD-Protection <sup>2)</sup></b>					
all pins	$V_{ESD}$		2	kV	

- 1). All values are referred to ground (pin), unless stated otherwise.  
 Currents with a positive sign flow into the pin and currents with a negative sign flow out of pin.
- 2). According to MIL STD 883D, method 3015.7 and EOS/ESD assn. standard S5.1 - 1993



## 5.1.2 Operating Range

Within the operational range the IC operates as described in the circuit description. The AC / DC characteristic limits are not guaranteed.

Table 5-2 Operating Range							
Parameter	Symbol	Limit Values		Unit	Test Conditions	L	Item
		min	max				
Supply voltage	$V_{CC}$	+4.5	+5.5	V			
Programmable divider factor	N	256	32767				
LOW/MID Mixer input frequency range	$f_i$	30	500	MHz			
HIGH Mixer input frequency range	$f_i$	400	900	MHz			
LOW/MID Oscillator frequency range	$f_O$	65	560	MHz			
HIGH Oscillator frequency range	$f_O$	430	950	MHz			
Ambient temperature	$T_{AMB}$	-20	+85	°C			

### 5.1.3 AC/DC Characteristics

AC / DC characteristics involve the spread of values guaranteed in the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
<b>Supply</b>								
Supply voltage	$V_{CC}$	4.5	5	5.5	V			
Current consumption	$I_{CC}$	56	70	84	mA			
<b>Digital Unit</b>								
<b>PLL</b>								
<b>Crystal oscillator connections XTAL</b>								
Crystal frequency	$f_{XTAL}$	3.2	4.0	4.8	MHz	series resonance		
Crystal resistance	$R_{XTAL}$	10		100	$\Omega$	series resonance		
Oscillation frequency	$f_{XTAL}$	3,99975	4,000	4,00025	MHz	$f_{XTAL} = 4\text{ MHz}$		
Input impedance	$Z_{XTAL}$	-500	-700	-900	$\Omega$	$f_{XTAL} = 4\text{ MHz}$		
<b>Charge pump output CP</b>								
HIGH output current	$I_{CPH}$	$\pm 90$	$\pm 220$	$\pm 300$	$\mu\text{A}$	$CP = 1, V_{CP} = 2\text{ V}$		
LOW output current	$I_{CPL}$	$\pm 22$	$\pm 50$	$\pm 75$	$\mu\text{A}$	$CP = 0, V_{CP} = 2\text{ V}$		
Tristate current	$I_{CPZ}$		+1		nA	$T_0 = 1, T_1 = 0, V_{CP} = 2\text{ V}$		
Output voltage	$V_{CP}$	1.0		2.5	V	PLL locked		
<b>Drive output VT (open collector)</b>								
HIGH output current	$I_{TH}$			10	$\mu\text{A}$	$V_{TH} = 33\text{ V}, T_0 = 1, T_1 = 0$		
LOW output voltage	$V_{TL}$			0.4	V	$I_{TL} = 1.0\text{ mA}$		
<b>I<sup>2</sup>C-Bus</b>								
<b>Bus inputs SCL, SDA</b>								
HIGH input voltage	$V_{IH}$	3		5.5	V			
LOW input voltage	$V_{IL}$	0		1.5	V			
HIGH input current	$I_{IH}$			10	$\mu\text{A}$	$V_{IH} = V_{CC}$		
LOW input current	$I_{IL}$	-10			$\mu\text{A}$	$V_{IL} = 0\text{ V}$		
<b>Bus output SDA (open collector)</b>								
HIGH output current	$I_{OH}$			10	$\mu\text{A}$	$V_{OH} = 5.5\text{ V}$		

**Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$  (continued)**

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
LOW output voltage	$V_{OL}$			0.4	V	$I_{OL} = 3\text{ mA}$		
<b>Edge speed SCL,SDA</b>								
Rise time	$t_r$			300	ns			
Fall time	$t_f$			300	ns			
<b>Clock timing SCL</b>								
Frequency	$f_{SCL}$	0		400	kHz			
HIGH pulse width	$t_H$	0.6			$\mu\text{s}$			
LOW pulse width	$t_L$	1.3			$\mu\text{s}$			
<b>Start condition</b>								
Set-up time	$t_{susta}$	0.6			$\mu\text{s}$			
Hold time	$t_{hsta}$	0.6			$\mu\text{s}$			
<b>Stop condition</b>								
Set up time	$t_{susto}$	0.6			$\mu\text{s}$			
Bus free	$t_{buf}$	1.3			$\mu\text{s}$			
<b>Data transfer</b>								
Set-up time	$t_{sudat}$	0.1			$\mu\text{s}$			
Hold time	$t_{hdat}$	0			$\mu\text{s}$			
Input hysteresis SCL, SDA	$V_{hys}$		200		mV			
Pulse width of spikes which are suppressed	$t_{sp}$	0		50	ns			
Capacitive load for each bus line	$C_L$			400	pF			
<b>Port outputs PLOW, PMID, PHIGH (open collector)</b>								
HIGH output current	$I_{POH}$			1	$\mu\text{A}$	$V_{POH} = 5\text{ V}$		
LOW output voltage	$V_{POL}$			0.5	V	$I_{POL} = 25\text{ mA}$		
<b>Address selection input AS</b>								
HIGH input current	$I_{ASH}$			50	$\mu\text{A}$	$V_{ASH} = 5\text{ V}$		
LOW input current	$I_{ASL}$	-50			$\mu\text{A}$	$V_{ASL} = 0\text{ V}$		

**Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$  (continued)**

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
<b>Analog Unit</b>								
<b>LOW/MID Band Section (including IF amplifier)</b>								
Voltage gain	$G_V$	20	23	26	dB	$f_{RF} = 43.25$ to $463.25$ MHz, $f_{IF} = 33.4$ to $58.75$ MHz		
Mixer noise figure	NF		9	11	dB	$f_{RF} = 43.25$ to $463.25$ MHz		
Output voltage causing 0.8% of crossmodulation in channel, see 5.4.6 on page 15	$V_i$		118		dB $\mu$ V	$f_{RFw} = 48.25$ MHz		
	$V_i$		117		dB $\mu$ V	$f_{RFw} = 399.25$ MHz		
Input IP2	IIP2		137		dB $\mu$ V	$f_{RF1} = 48.25$ MHz $f_{RF2} = 98.50$ MHz, $P_{RF1} = P_{RF2}$		
	IIP2		137		dB $\mu$ V	$f_{RF1} = 415.25$ MHz $f_{RF2} = 832.50$ MHz, $P_{RF1} = P_{RF2}$		
Input IP3	IIP3		119		dB $\mu$ V	$f_{RF1} = 48.25$ MHz $f_{RF2} = 49.25$ MHz $P_{RF1} = P_{RF2}$		
	IIP3		119		dB $\mu$ V	$f_{RF1} = 252.25$ MHz $f_{RF2} = 253.25$ MHz, $P_{RF1} = P_{RF2}$		
Output voltage causing 1 dB compression	$V_o$		121		dB $\mu$ V	$f_{RF} = 48.25$ MHz		
	$V_o$		121		dB $\mu$ V	$f_{RF} = 252.25$ MHz		
Mixer input impedance	$R_i$	0.5	1	1.5	k $\Omega$	parallel equivalent circuit, $f_{RF} = 100$ MHz		
	$C_i$		2	3	pF	parallel equivalent circuit, $f_{RF} = 100$ MHz		
Oscillator frequency shift, PLL unlocked	$\Delta f_{Osc(V)}$			400	kHz	$V_S = 5\text{ V} \pm 10\%$		
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(T)}$			500	kHz	$\Delta T = 25\text{ }^{\circ}\text{C}$		
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(t)}$			100	kHz	$t = 5\text{ s}$ up to $15\text{ min}$ after switching on		
Oscillator pulling, PLL unlocked	$V_i$	100	108		dB $\mu$ V	$\Delta f = 10\text{ kHz}$ $f_{RF} = 48.25\text{ MHz}$		
	$V_i$	100	108		dB $\mu$ V	$\Delta f = 10\text{ kHz}$ $f_{RF} = 399.25\text{ MHz}$		

**Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$  (continued)**

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
N + 5 pulling, PLL unlocked	N+5	-50			dBc	$f_{RF} = 48.25\text{ MHz}$ , $f_{RF1} = 83.25\text{ MHz}$ , $P_{RF} = P_{RF1} = 80\text{ dB}\mu\text{V}$		
	N+5	-50			dBc	$f_{RF} = 399.25\text{ MHz}$ , $f_{RF1} = 439.25\text{ MHz}$ , $P_{RF} = P_{RF1} = 80\text{ dB}\mu\text{V}$		
Oscillator phase noise <sup>1)</sup>	$\Phi_{OSC}$	-58	-60		dBc/Hz	$f_m = 1\text{ kHz}$		
	$\Phi_{OSC}$	-88	-90		dBc/Hz	$f_m = 10\text{ kHz}$		
IF suppression	a	15	20		dB	$V_i = 80\text{ dB}\mu\text{V}$		
<b>HIGH Band Section (including IF amplifier)</b>								
Voltage gain	$G_V$	31	34	37	dB	$f_{RF} = 367.25\text{ MHz}$ to 863.25 MHz, $f_{IF} = 33.4\text{ MHz}$ to 58.75 MHz		
Mixer noise figure	NF		6	9	dB	$f_{RF} = 367.25$ to 615.25 MHz		
			7	10	dB	$f_{RF} = 623.25$ to 863.25 MHz		
Output voltage causing 0.8% of crossmodulation in channel, <a href="#">see 5.4.7 on page 16</a>	$V_i$		116		dB $\mu\text{V}$	$f_{RFw} = 503.25\text{ MHz}$		
	$V_i$		117		dB $\mu\text{V}$	$f_{RFw} = 799.25\text{ MHz}$		
Input IP2	IIP2		139		dB $\mu\text{V}$	$f_{RF1} = 423.25\text{ MHz}$ $f_{RF2} = 848.50\text{ MHz}$ , $P_{RF1} = P_{RF2}$		
Input IP3	IIP3		108		dB $\mu\text{V}$	$f_{RF1} = 503.25\text{ MHz}$ $f_{RF2} = 504.25\text{ MHz}$ $P_{RF1} = P_{RF2}$		
	IIP3		108		dB $\mu\text{V}$	$f_{RF1} = 799.25\text{ MHz}$ $f_{RF2} = 800.25\text{ MHz}$ $P_{RF1} = P_{RF2}$		
Output voltage caus- ing 1 dB compression	$V_o$		121		dB $\mu\text{V}$	$f_{RF} = 503.25\text{ MHz}$		
	$V_o$		121		dB $\mu\text{V}$	$f_{RF} = 799.25\text{ MHz}$		
Mixer input impedance	$R_i$	14	20	26	$\Omega$	serial equivalent cir- cuit, $f_{RF} = 600\text{ MHz}$		
	$L_i$	6	10	14	nH	serial equivalent cir- cuit, $f_{RF} = 600\text{ MHz}$		
Oscillator frequency shift, PLL unlocked	$\Delta f_{Osc(V)}$			400	kHz	$V_S = 5\text{ V} \pm 10\%$		

**Table 5-3 AC/DC Characteristics with  $T_{AMB} = 25\text{ }^{\circ}\text{C}$ ,  $V_{CC}$  (continued)**

	Symbol	Limit Values			Unit	Test Conditions	L	Item
		min	typ	max				
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(T)}$			800	kHz	$\Delta T = 25\text{ }^{\circ}\text{C}$		
Oscillator frequency drift, PLL unlocked	$\Delta f_{Osc(t)}$			100	kHz	$t = 5\text{ s}$ up to 15 min after switching on		
Oscillator pulling, PLL unlocked	$V_i$	100	108		dB $\mu$ V	$\Delta f = 10\text{ kHz}$ $f_{RF} = 375.25\text{ MHz}$		
	$V_i$	100	108		dB $\mu$ V	$\Delta f = 10\text{ kHz}$ $f_{RF} = 847.25\text{ MHz}$		
N + 5 pulling, PLL unlocked	$V_i$	-50			dBc	$f_{RF} = 471.25\text{ MHz}$ , $f_{RF1} = 511.25\text{ MHz}$ , $P_{RF} = P_{RF1} = 80\text{ dB}\mu\text{V}$		
	$V_i$	-50			dBc	$f_{RF} = 847.25\text{ MHz}$ , $f_{RF1} = 887.25\text{ MHz}$ , $P_{RF} = P_{RF1} = 80\text{ dB}\mu\text{V}$		
Oscillator phase noise <sup>1)</sup>	$\Phi_{OSC}$	-58	-60		dBc/Hz	$f_m = 1\text{ kHz}$		
	$\Phi_{OSC}$	-88	-90		dBc/Hz	$f_m = 10\text{ kHz}$		
IF suppression	a	15	20		dB	$V_i = 80\text{ dB}\mu\text{V}$		
<b>SAW preamplifier</b>								
IF output impedance, double ended	$R_{IF}$		125		$\Omega$	serial equivalent circuit, $f_{IF} = 38.9\text{ MHz}$		
	$L_{IF}$		10		nH			
IF output impedance, single ended	$R_{IF}$		75		$\Omega$	serial equivalent circuit, $f_{IF} = 38.9\text{ MHz}$		
	$L_{IF}$		5		nH			
<b>Rejection at the IF outputs</b>								
Divider interference level <sup>2)</sup> .	$V_o$			30	dB $\mu$ V			
Channel S02 beat rejection <sup>3)</sup> .	$INT_{S02}$	66			dBc	$f_{RF} = 76.25\text{ MHz}$ $P_{RF} = 80\text{ dB}\mu\text{V}$		

■ This value is only guaranteed in lab.

- 1). Measured in the evaluation board (see Chapter 4), worst case in band
- 2). This is the level of divider interferences close to the IF frequency. For example channel S3:  $f_{OSC} = 158.15\text{ MHz}$ ,  $1/4 f_{OSC} = 39.5375\text{ MHz}$ . Measured in the evaluation board (see Chapter 4).
- 3). Channel S02 beat is the interfering product of  $f_{RF}$ ,  $f_{IF}$  and  $f_{OSC}$  of channel S02,  $f_{beat} = 37.35\text{ MHz}$ . The possible mechanisms are  $f_{OSC} - 2 \times f_{IF}$  or  $2 \times f_{RFpix} - f_{OSC}$ . Measured in evaluation board (see Chapter 4).

## 5.2 Programming

**Table 5-4 Bit Allocation Read / Write**

Byte	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB	Ack
Write Data									
Address Byte	1	1	0	0	0	MA1	MA0	0	A
Progr. Divider Byte 1	0	N14	N13	N12	N11	N10	N9	N8	A
Progr. Divider Byte 2	N7	N6	N5	N4	N3	N2	N1	N0	A
Control Byte	1	CP	T1	T0	FP	RSA	RSB	OS	A
Bandswitch Byte	x	x	x	x	x	PHIGH 1).	PLOW 1).2).	PMID 1).2).	A
Read Data									
Address Byte	1	1	0	0	0	MA1	MA0	1	A
Status Byte	POR	FL	x	x	x	x	x	x	A

1). [see Table 5-9 IC frequency range selection on page 11](#)

2). In a tuner PLOW and PMID are interchangeable. Both bits switch the IC into LOW/MID (VHF) mode.

**Table 5-5 Description of symbols**

Symbol	Description
MA0, MA1	Address selection bits ( <a href="#">see Table 5-6 Address selection on page 11</a> )
N14 to N0	programmable divider bits: $N = 2^{14} \times N14 + 2^{13} \times N13 + \dots + 2^3 \times N3 + 2^2 \times N2 + 2^1 \times N1 + N0$
CP	Charge pump current:      bit = 0: charge pump current = 50 $\mu$ A bit = 1: charge pump current = 220 $\mu$ A
T1, T0	test bits ( <a href="#">see Table 5-7 Test modes on page 11</a> )
FP	reserved for future purposes, actually ignored, default: 1
RSA, RSB	reference divider bits ( <a href="#">see Table 5-8 Reference divider ratio on page 11</a> )
OS	Tuning amplifier control bit:    bit = 0: enable $V_T$ bit = 1: disable $V_T$
PLOW, PMID, PHIGH	NPN ports control bits:      bit = 0: NPN open-collector output is inactive bit = 1: NPN open-collector output is active ( <a href="#">see Table 5-9 IC frequency range selection on page 11</a> )
FL	PLL lock flag, bit = 1: loop is locked
POR	Power-on reset flag flag is set at power-on and reset at the end of READ operation
x	don't care

Table 5-6 Address selection		
Voltage at AS	MA1	MA0
$(0...0.1) * V_{CC}$	0	0
open circuit	0	1
$(0.4...0.6) * V_{CC}$	1	0
$(0.9...1) * V_{CC}$	1	1

Table 5-7 Test modes		
Test mode	T1	T0
Normal operation	0	0
Charge pump output, CP is in high-impedance state	0	1
PLOW = $f_{div}$ output, PMID = $f_{ref}$ output	1	0
not used	1	1

Table 5-8 Reference divider ratio			
Reference divider ratio	$f_{ref}^{1)}$	RSA	RSB
80	50 kHz	0	0
128	31.25 kHz	0	1
24	166.7 kHz	1	0
64	62.5 kHz	1	1

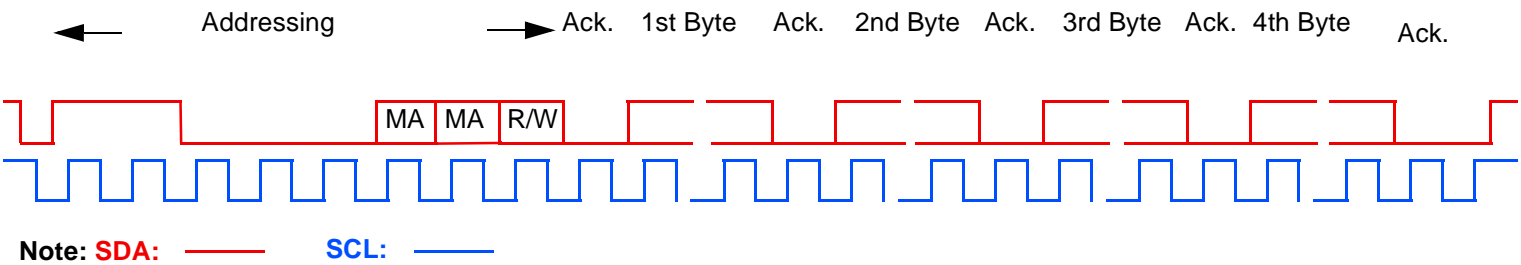
1). With a 4 MHz quartz.

Table 5-9 IC frequency range selection			
Frequency range	Bit 2 (PHIGH)	Bit 1 (PLOW) <sup>1)</sup>	Bit 0 (PMID) <sup>1)</sup>
LOW/MID (VHF)	0	1	0
LOW/MID (VHF)	0	0	1
HIGH (UHF)	1	0	0

1). In a tuner PLOW and PMID are interchangeable. Both bits switch the IC into LOW/MID (VHF) mode.



### 5.3 I<sup>2</sup>C Bus Timing Diagram



**Telegram examples:**

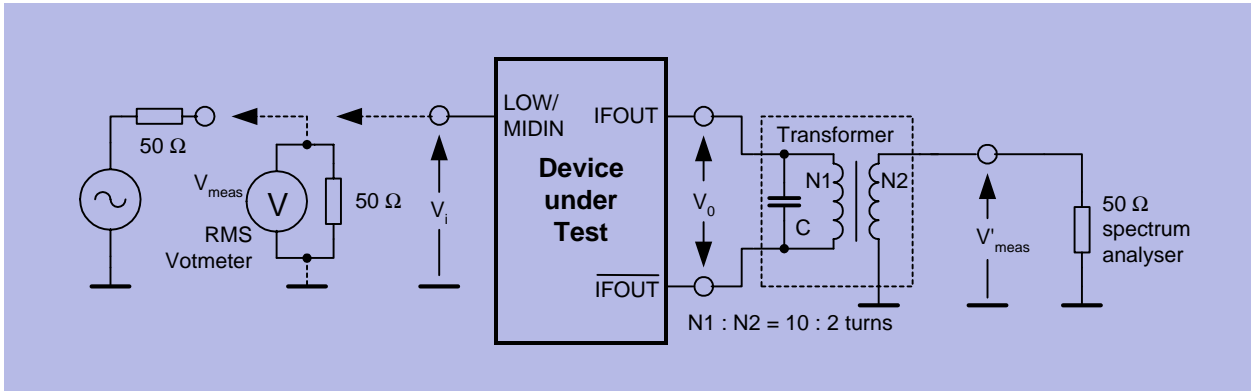
- Start-ADB-DB1-DB2-CB-BB-Stop
- Start-ADB-CB-BB-DB1-DB2-Stop
- Start-ADB-DB1-DB2-Stop
- Start-ADB-CB-BB-Stop

**Abbreviations:**

- Start= start condition
- ADB= address byte
- DB1= prog. divider byte 1
- DB2= prog. divider byte 2
- CB= Control byte
- BB= Bandswitch byte
- Stop= stop condition

## 5.4 Test Circuits

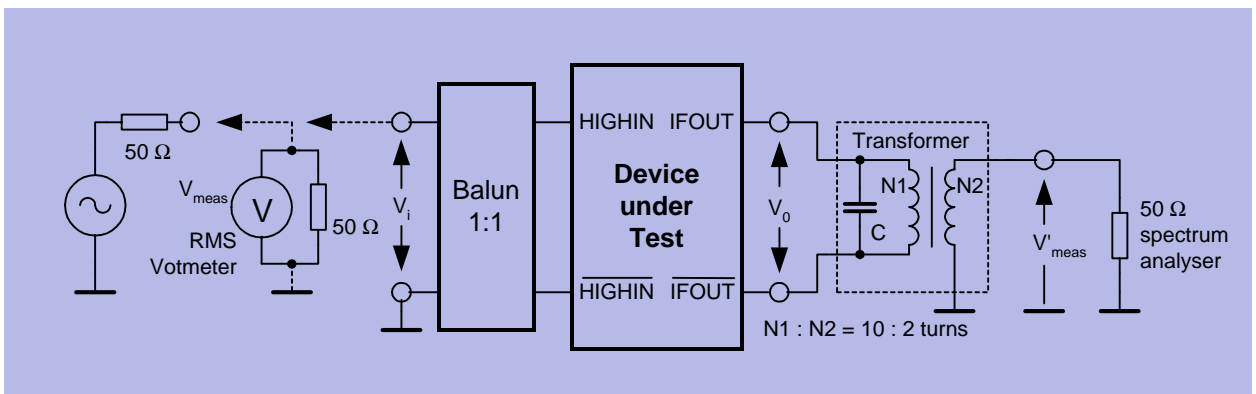
### 5.4.1 Gain ( $G_V$ ) test Set-up in LOW/MID band



GVHF2

- $Z_i \gg 50 \Omega \Rightarrow V_i = 2 \times V_{\text{meas}} = 80 \text{ dB}\mu\text{V}$
- $V_i = V_{\text{meas}} + 6\text{dB} = 80 \text{ dB}\mu\text{V}$
- $V_0 = V'_{\text{meas}} + 16 \text{ dB}$  (transformer ratio N1:N2 and transformer loss)
- $G_V = 20 \log(V_0 / V_i)$

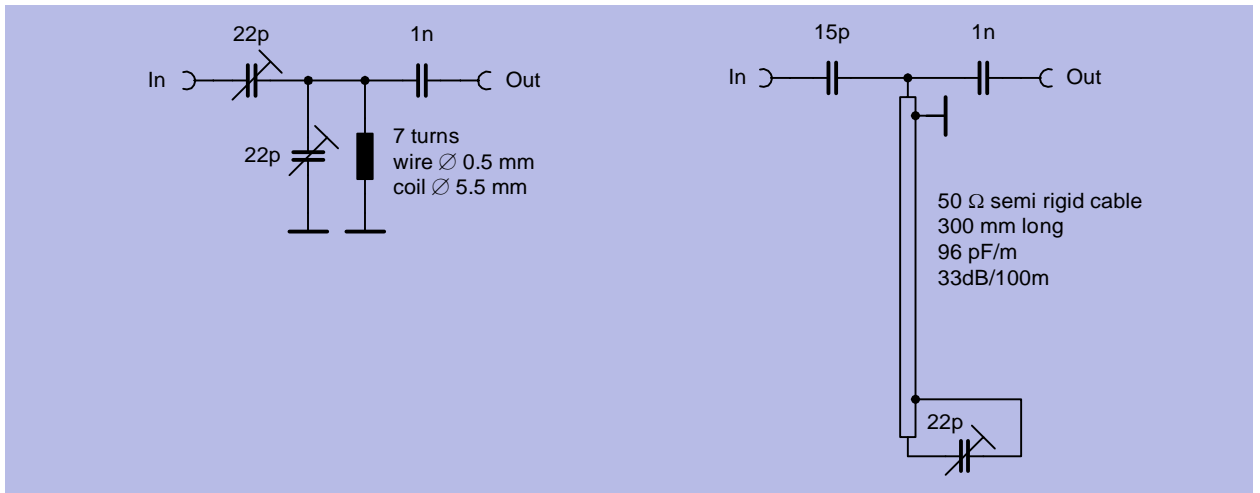
### 5.4.2 Gain ( $G_V$ ) test Set-up in HIGH band



GVHF2

- $V_i = V_{\text{meas}} = 70 \text{ dB}\mu\text{V}$
- $V_0 = V'_{\text{meas}} + 16 \text{ dB}$  (transformer ratio N1:N2 and transformer loss)
- $G_V = 20 \log(V_0 / V_i) + 1 \text{ dB}$  (1 dB = insertion loss of balun)

### 5.4.3 Matching circuit for optimum noise figure in LOW/MID band



Nfm

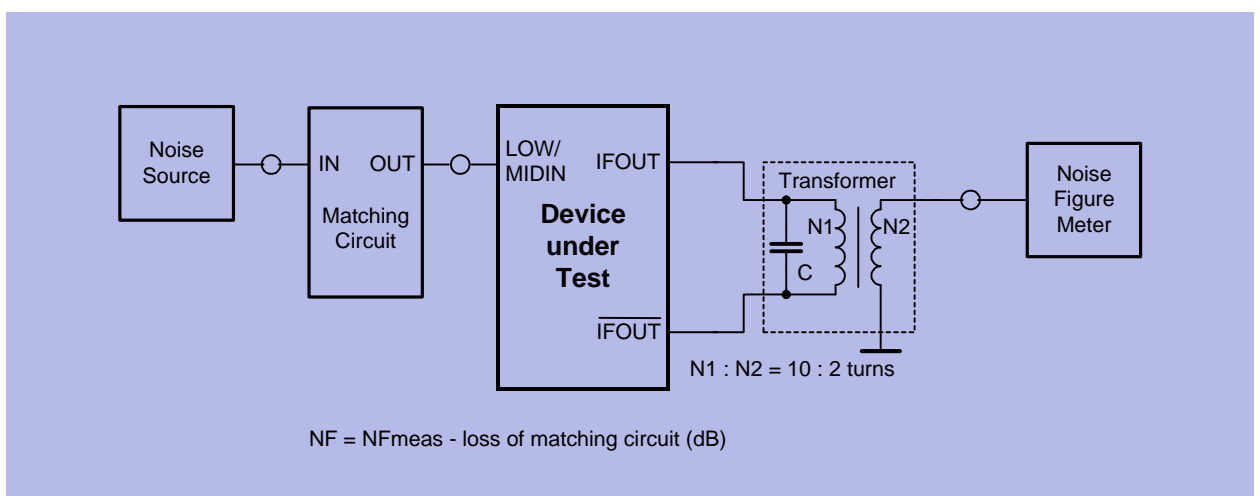
For  $f_{RF} = 50 \text{ MHz}$

- loss = 0 dB
- image suppression = 16 dB

For  $f_{RF} = 150 \text{ MHz}$

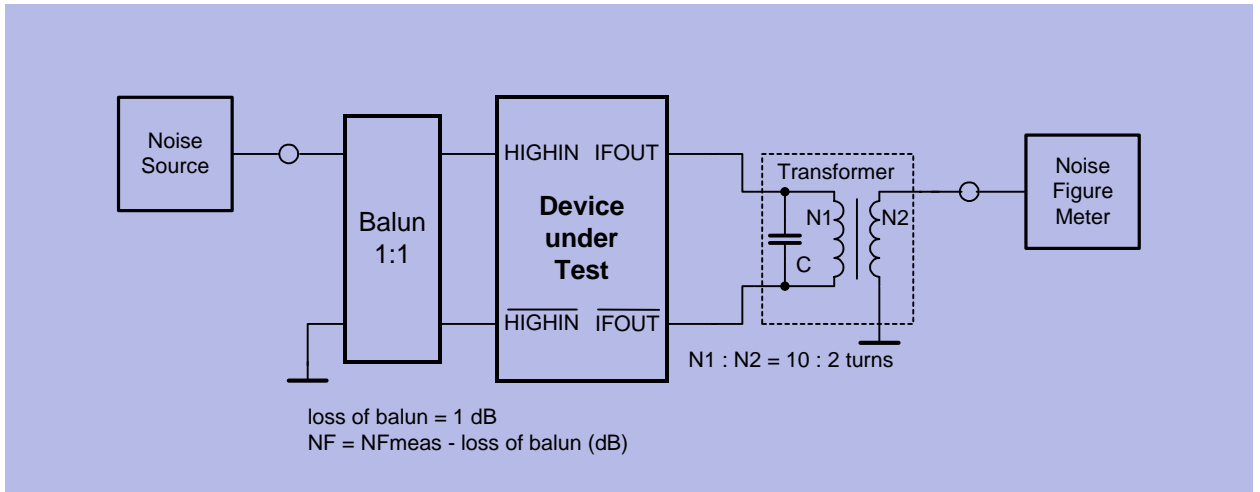
- loss = 1.3 dB
- image suppression = 13 dB

### 5.4.4 Noise Figure Test Set-up in LOW/MID band



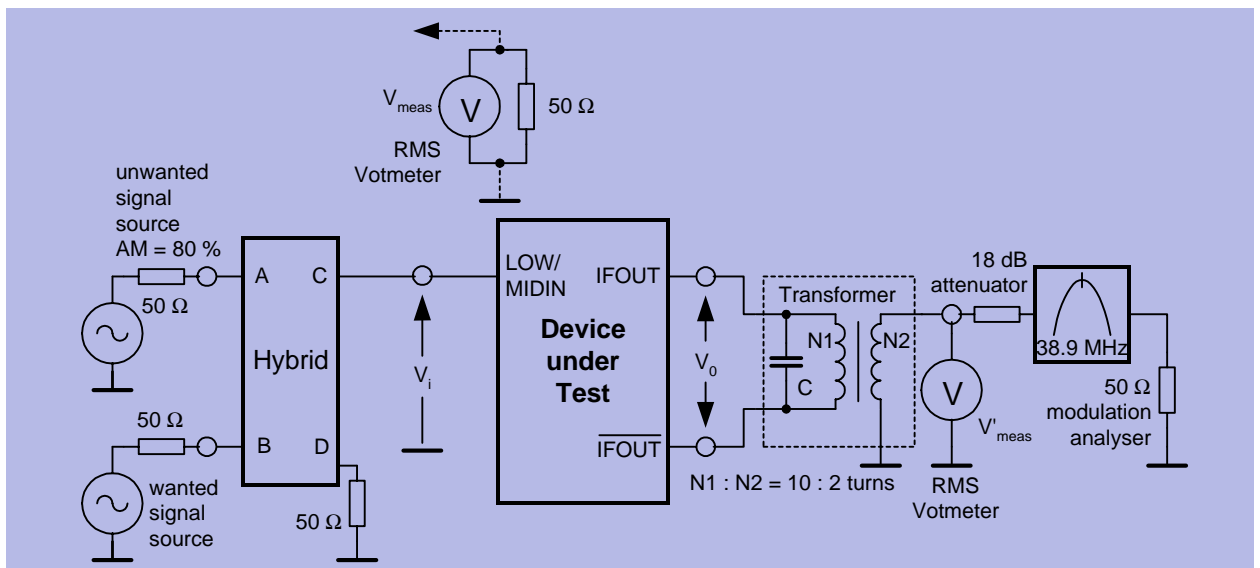
NFVHF2

### 5.4.5 Noise Figure Test Set-up in HIGH band



NFUHF2

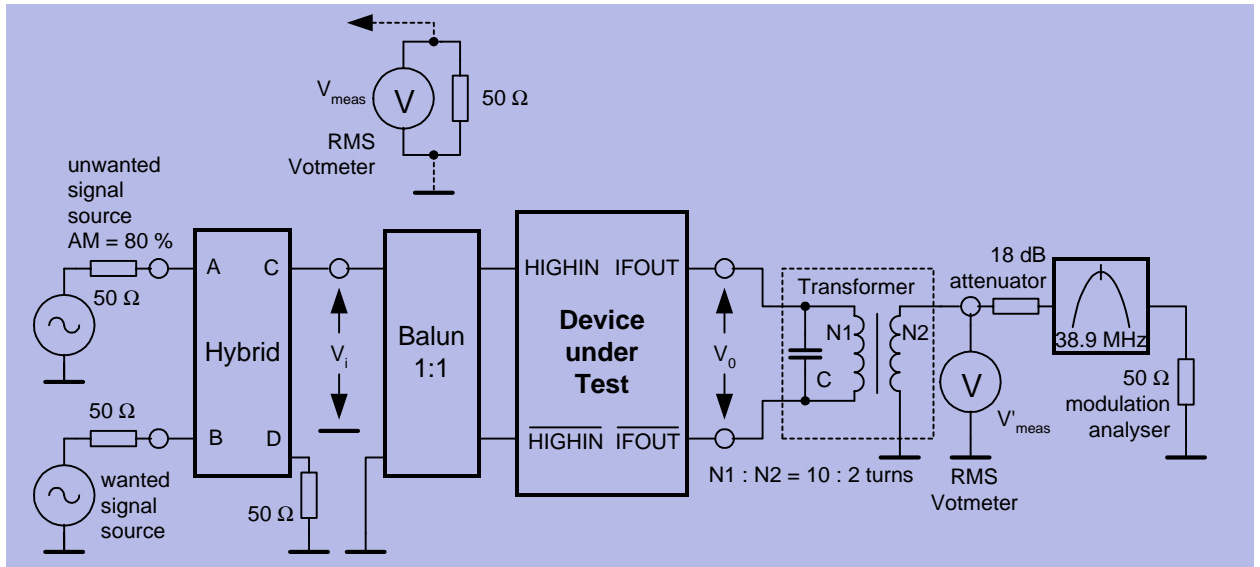
### 5.4.6 Cross modulation Test Set-up in LOW/MID band



XVHF2

- $Z_i \gg 50 \Omega \Rightarrow V_i = 2 \times V_{meas}$
- $V'_{meas} = V_o - 16 \text{ dB}$  (transformer ratio  $N1:N2$  and transformer loss)
- wanted output signal at  $f_{pix}$ ,  $V_o = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at  $f_{snd}$ , 80 % AM modulated with 1 kHz

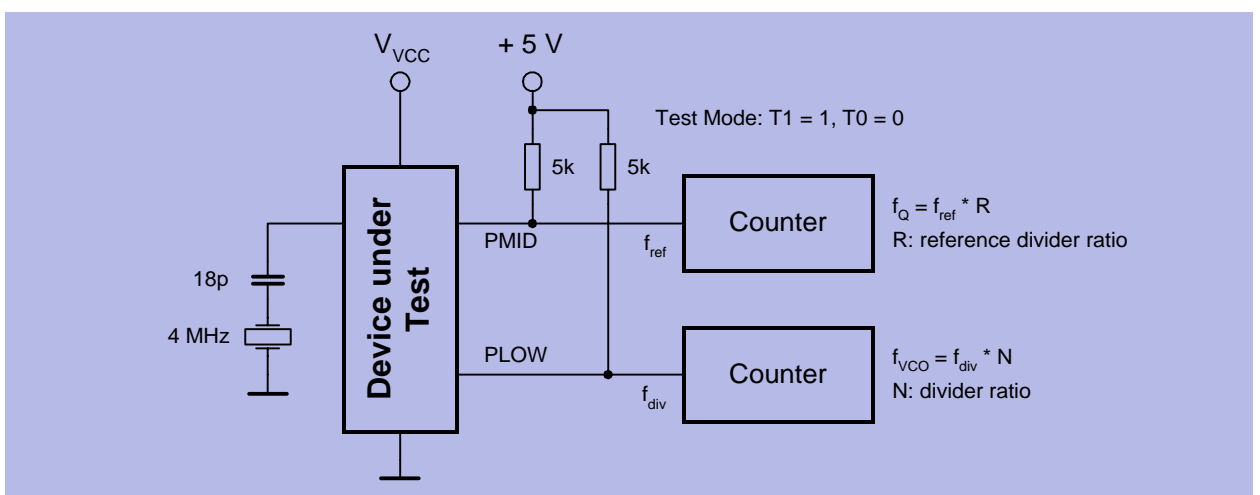
### 5.4.7 Cross modulation Test Set-up in HIGH band



XUHF2

- $V'_{meas} = V_o - 16 \text{ dB}$  (transformer ratio  $N1:N2$  and transformer loss)
- wanted output signal at  $f_{pix}$ ,  $V_o = 100 \text{ dB}\mu\text{V}$
- unwanted output signal at  $f_{snd}$ , 80 % AM modulated with 1 kHz

### 5.4.8 Measurement of $f_{ref}$ and $f_{div}$

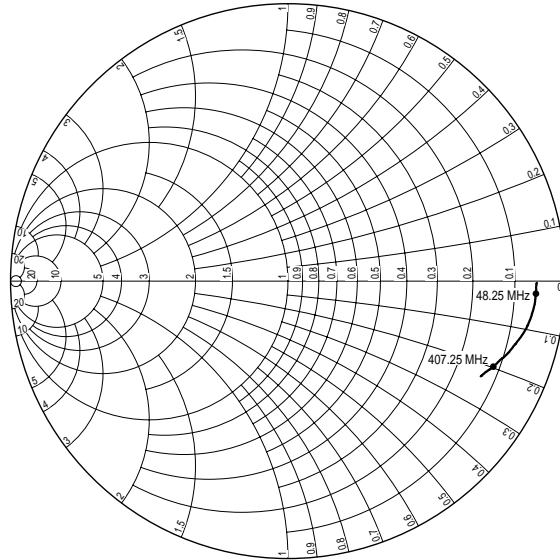


MEAS\_COF

## 5.5 Electrical Diagrams

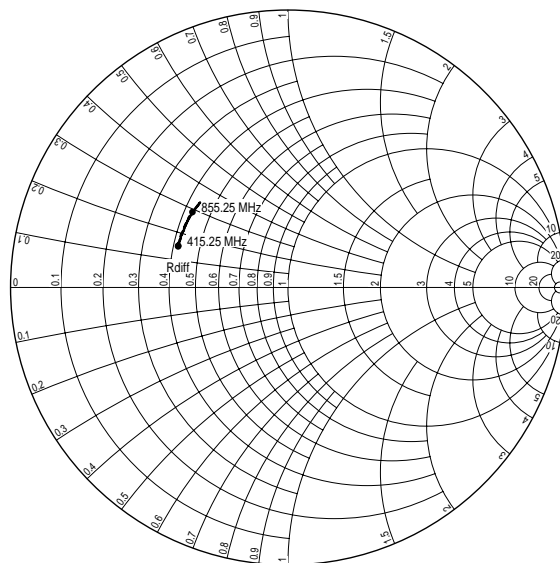
### 5.5.1 Input admittance (S11) of the LOW/MID band mixer input

$Y_0 = 20\text{mS}$  (single ended)



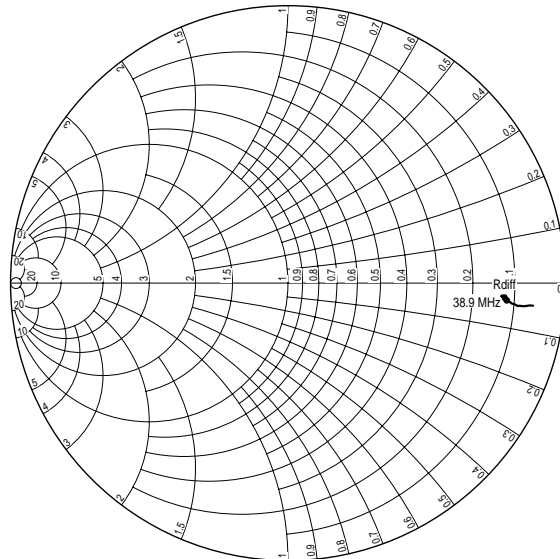
### 5.5.2 Input impedance (S11) of the HIGH band mixer input

$Z_0 = 50\ \Omega$  (balanced)



### 5.5.3 Output admittance (S22) of the Mixer output

$Y_0 = 20\text{mS}$  (balanced)



### 5.5.4 Output impedance (S22) of the IF output

$Z_0 = 50\ \Omega$  (single/ double ended)

