

# HD14553B

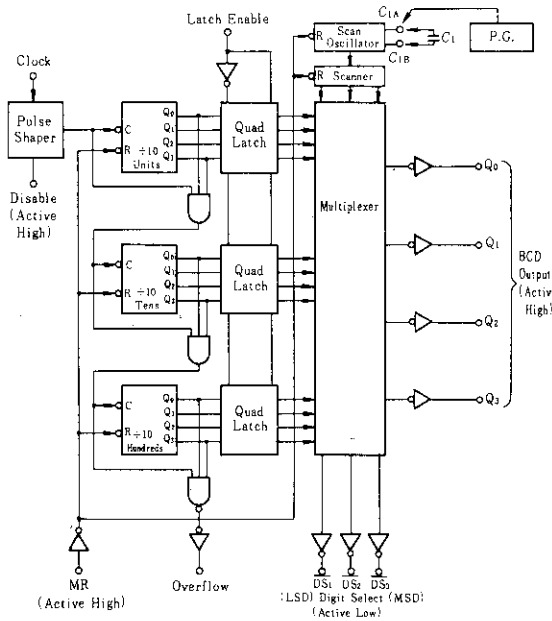
## Three-Digit BCD Counter

The HD14553B three-digit BCD counter consists of three negative-edge triggered BCD counters that are cascaded synchronously. A quad latch at the output of each counter permits storage of any given count. The information is then time division multiplexed, providing on BCD number or digit at a time. Digit select outputs provide display control. All outputs are TTL compatible. An on-chip oscillator provides the low-frequency scanning clock which drives the multiplexer output selector. This device is used in instrumentation counters, clock displays, digital panel meters, and as a building block for general logic applications.

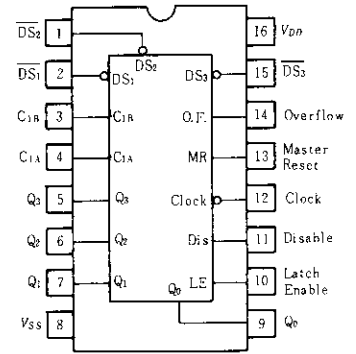
### FEATURES

- TTL Outputs
- On-Chip Oscillator
- Cascadable
- Clock Disable Input
- Pulse Shaping Permits Very Slow Rise Times on Input Clock
- Output Latches
- Master Reset

### BLOCK DIAGRAM



### PIN ARRANGEMENT



(Top View)

### TRUTH TABLE

Inputs				Outputs
MR	Clock	Disable	LE	
0		0	0	No Change
0		0	0	Advance
0	x	1	x	No Change
0	1		0	Advance
0	1		0	No Change
0	0	x	x	No Change
0	x	x		Latched
0	x	x	1	Latched
1	x	x	0	$Q_0 \sim Q_3 = 0$

x = Don't Care

### MAXIMUM RATINGS (Voltages refeeced to $V_{SS}$ )

Characteristic	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	-0.5 ~ +18	V
Input/Output Voltage	$V_{in}, V_{out}$	-0.5 ~ $V_{DD} + 0.5$	V
DC Current Drain per Input Pin	$I_{in}$	$\pm 10$	mA
DC Current per Pin, All Outputs	$I_{out}$	20	mA
Operating Temperature Range	$T_A$	-40 ~ +85	$^{\circ}C$
Storage Temperature Range	$T_{stg}$	-65 ~ +150	$^{\circ}C$
Power Dissipation	$P_D$	300	mW

■ ELECTRICAL CHARACTERISTICS

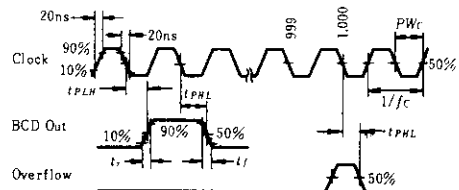
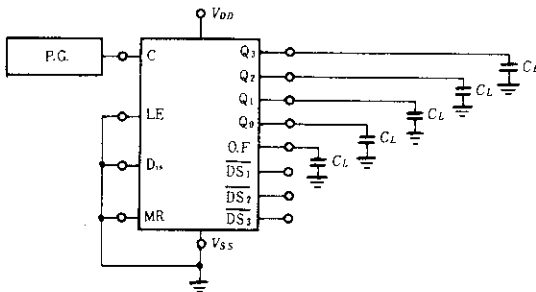
Characteristic	Symbol	Test Conditions	-40°C		25°C			85°C		Unit		
			min	max	min	typ	max	min	max			
Output Voltage	$V_{OL}$	5.0	$V_{in} = V_{DD}$ or 0	—	0.05	—	0	0.05	—	0.05	V	
		10		—	0.05	—	0	0.05	—	0.05		
		15		—	0.05	—	0	0.05	—	0.05		
	$V_{OH}$	5.0	$V_{in} = 0$ or $V_{DD}$	4.95	—	4.95	5.0	—	4.95	—	V	
		10		9.95	—	9.95	10	—	9.95	—		
		15		14.95	—	14.95	15	—	14.95	—		
Input Voltage	$V_{iL}$	5.0	$V_{out} = 4.5$ or $0.5V$	—	1.5	—	2.25	1.5	—	1.5	V	
		10	$V_{out} = 9.0$ or $1.0V$	—	3.0	—	4.50	3.0	—	3.0		
		15	$V_{out} = 13.5$ or $1.5V$	—	4.0	—	6.75	4.0	—	4.0		
	$V_{iH}$	5.0	$V_{out} = 0.5$ or $4.5V$	3.5	—	3.5	2.75	—	3.5	—	V	
		10	$V_{out} = 1.0$ or $9.0V$	7.0	—	7.0	5.50	—	7.0	—		
		15	$V_{out} = 1.5$ or $13.5V$	11.0	—	11.0	8.25	—	11.0	—		
Output Drive Current	$I_{OH}$	5.0	$V_{OH} = 4.6V$	-0.2	—	-0.16	-0.36	—	-0.12	—	mA	
		10	$V_{OH} = 9.5V$	-0.5	—	-0.4	-0.9	—	-0.3	—		
		15	$V_{OH} = 13.5V$	-1.4	—	-1.2	-3.5	—	-1.0	—		
	Pin 3	$I_{OL}$	5.0	$V_{OL} = 0.4V$	0.52	—	0.44	0.88	—	0.36	—	mA
			10	$V_{OL} = 0.5V$	1.3	—	1.1	2.25	—	0.9	—	
			15	$V_{OL} = 1.5V$	3.6	—	3.0	8.8	—	2.4	—	
		Other Outputs	5.0	$V_{OL} = 0.4V$	2.4	—	2.0	4.0	—	1.6	—	
			10	$V_{OL} = 0.5V$	3.8	—	3.0	8.0	—	2.5	—	
			15	$V_{OL} = 1.5V$	10	—	8.4	20	—	7.0	—	
	Input Current	$I_{in}$	15		—	$\pm 0.3$	—	$\pm 0.00001$	$\pm 0.3$	—	$\pm 1.0$	$\mu A$
	Input Capacitance	$C_{in}$		$V_{in} = 0$	—	—	—	5.0	7.5	—	—	pF
	Quiescent Current	$I_{DD}$	5.0	Zero Signal, per Package	—	50	—	0.010	50	—	375	$\mu A$
10			—		100	—	0.020	100	—	750		
15			—		200	—	0.030	200	—	1500		
Total Supply Current*	$I_T$	5.0	Dynamic + $I_{DD}$ ,	—	—	—	0.35	—	—	—	$\mu A$	
		10	per Gate	—	—	—	0.85	—	—	—		
		15	$C_L = 50pF, f = 1 kHz$	—	—	—	1.50	—	—	—		

\* To calculate total supply current at frequency other than 1kHz.

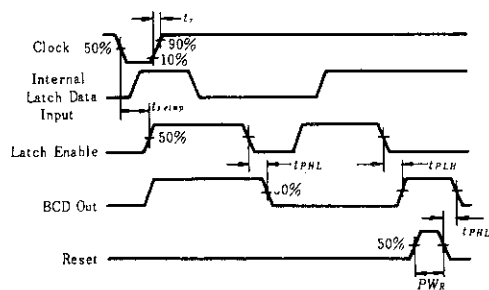
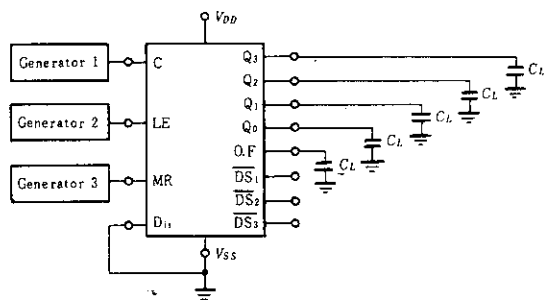
@ $V_{DD} = 5.0V$   $I_T = (0.35 \mu A/kHz)f + I_{DD}$ , @ $V_{DD} = 10V$   $I_T = (0.85 \mu A/kHz)f + I_{DD}$ , @ $V_{DD} = 15V$   $I_T = (1.50 \mu A/kHz)f + I_{DD}$

■ SWITCHING TIME TEST CIRCUIT

1.



2.

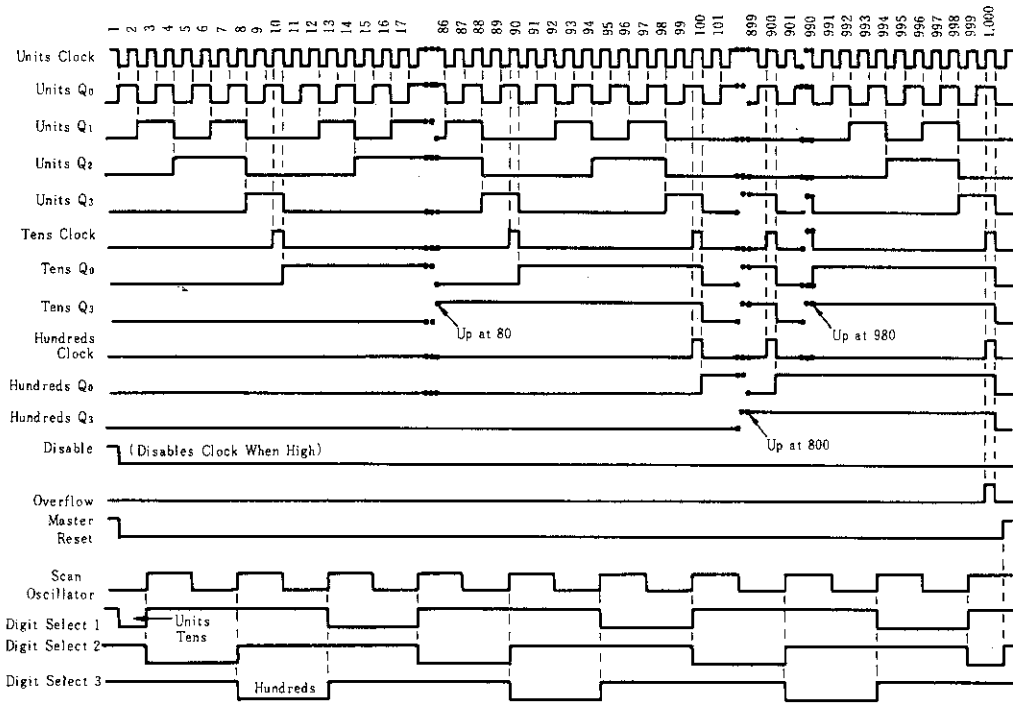


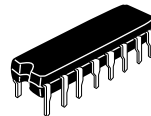
■ SWITCHING CHARACTERISTICS ( $C_L=50\text{pF}$ ,  $T_a=25^\circ\text{C}$ )

Characteristic		Symbol	Test Circuit	$V_{DD}(\text{V})$	min	typ	max	Unit
Output Rise Time		$t_r$	1	5.0	—	180	400	ns
				10	—	90	200	
				15	—	65	160	
Output Fall Time		$t_f$	1	5.0	—	120	250	ns
				10	—	60	125	
				15	—	40	100	
Propagation Delay Time	Clock to BCD Out	$t_{PLR}$ , $t_{PHL}$	1	5.0	—	900	2000	ns
				10	—	500	1000	
				15	—	300	750	
	Clock to Overflow	$t_{PHL}$	1	5.0	—	600	1300	ns
				10	—	400	800	
				15	—	200	600	
	Reset to BCD Out	$t_{PHL}$	2	5.0	—	900	2000	ns
				10	—	500	1000	
				15	—	300	750	
Setup Time		$t_{setup}$	2	5.0	900	300	—	ns
				10	500	200	—	
				15	375	100	—	
Clock Pulse Width		$PW_C$	1	5.0	550	275	—	ns
				10	200	100	—	
				15	150	75	—	
Reset Pulse Width		$PW_R$	2	5.0	1200	600	—	ns
				10	600	300	—	
				15	450	225	—	
Clock Frequency		$f_c$	1	5.0	—	1.5	0.7	MHz
				10	—	5.0	2.0	
				15	—	7.0	2.5	
Input Clock Rise Time		$t_r$	2	5.0	No Limit			
				10				
				15				
Scon Oscillator Frequency		$f_{osc}$		5.0	—	$0.4/C_1^*$	—	Hz
				10	—	$1.2/C_1^*$	—	
				15	—	$1.6/C_1^*$	—	

\*  $C_1 = \mu\text{F}$

● TIMING DIAGRAM





Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

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